

Commercialization Activities for Wafer Level Magnetics



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ENERGY
SAVINGS



SIZE
REDUCTION



PERFORMANCE
ENHANCEMENT



MANUFACTURING
SAVINGS



MISSING
LINK



Brief Intro



- ☞ Trifon Liakopoulos, PhD - CEO and Founder Enachip
 - Prior to Enachip: Altera, Enpirion (co-founder), Bell Labs
 - Integrated Magnetics, MEMS, Materials

- ☞ Matt Wilkowski, MS – VP Magnetics Engineering Enachip
 - Prior to Enachip: Intel, Altera, Enpirion, Tyco, Bell Labs
 - Magnetics Technology, Design & Commercialization

- ☞ Prof. Mark Allen, UPENN, Founder & Sci. Advisory Board Chair Enachip
 - Scientific Director, Singh Center for Nanotechnology,
Alfred Fitler Moore Professor
Electrical and Systems Engineering, Mechanical Engineering and Applied Mechanics

- ☞ Jun Beom Pyo
 - PhD Candidate, UPenn

EnaChip Inc. – Intro



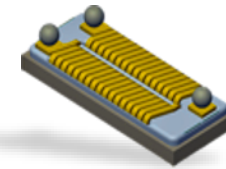
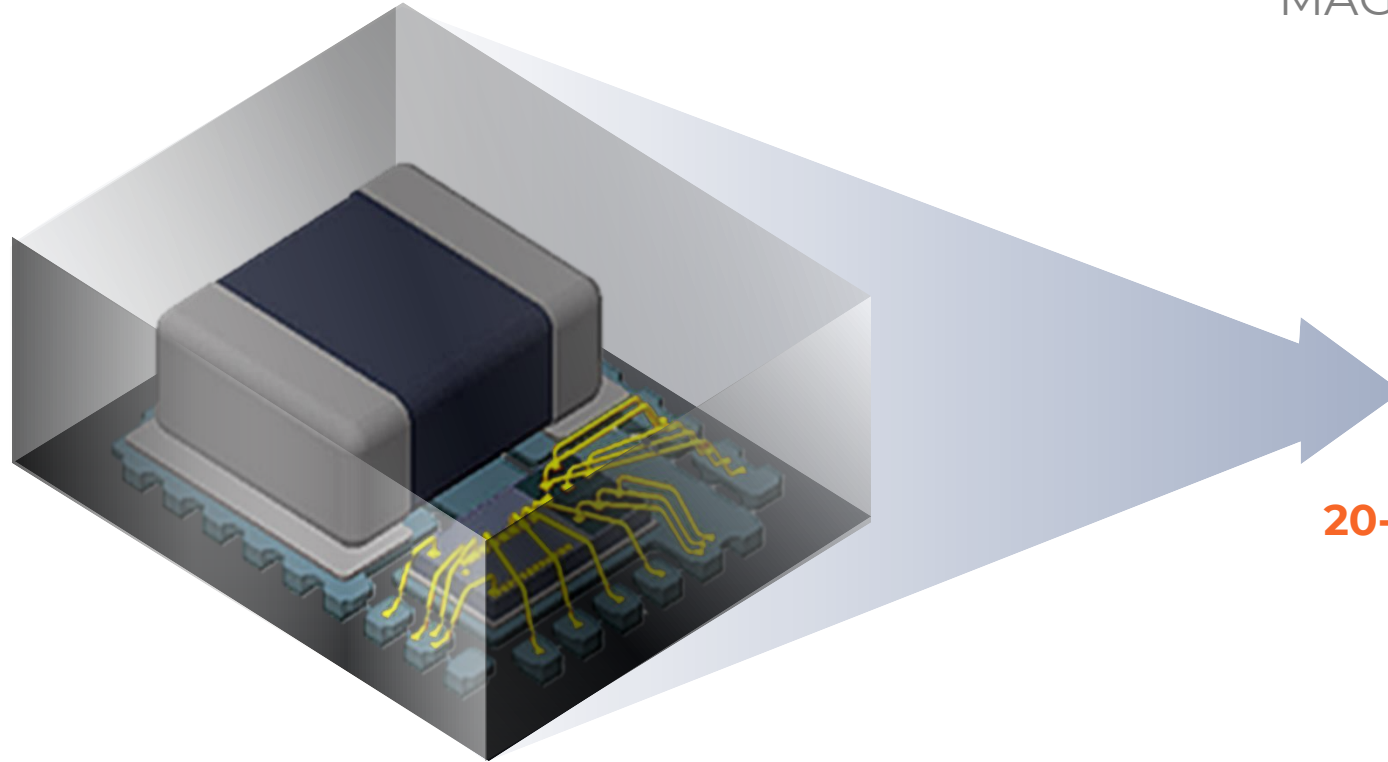
- Enachip (“One”-Chip) started operations in 2018 (early stage, VC funded startup)
- Mission: Re-invent Power Management by Commercializing Wafer Level Magnetics



HQ Located between NYC and Philadelphia (30min south of Newark Airport)

EnaChip – Breakthrough Innovation in Integration

COMMERCIALLY VIABLE TECHNOLOGY THAT INTEGRATES POWER MAGNETICS WITH SILICON IC



20-50% Energy Savings
30x Smaller Size
3x Lower Cost

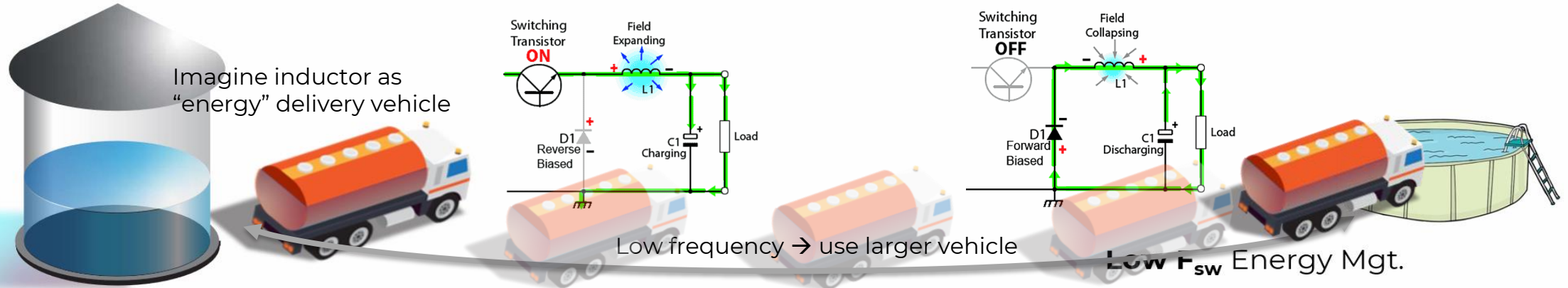
Power System in Package
State of the Art

Power System on Chip
EnaChip Enabled Solution

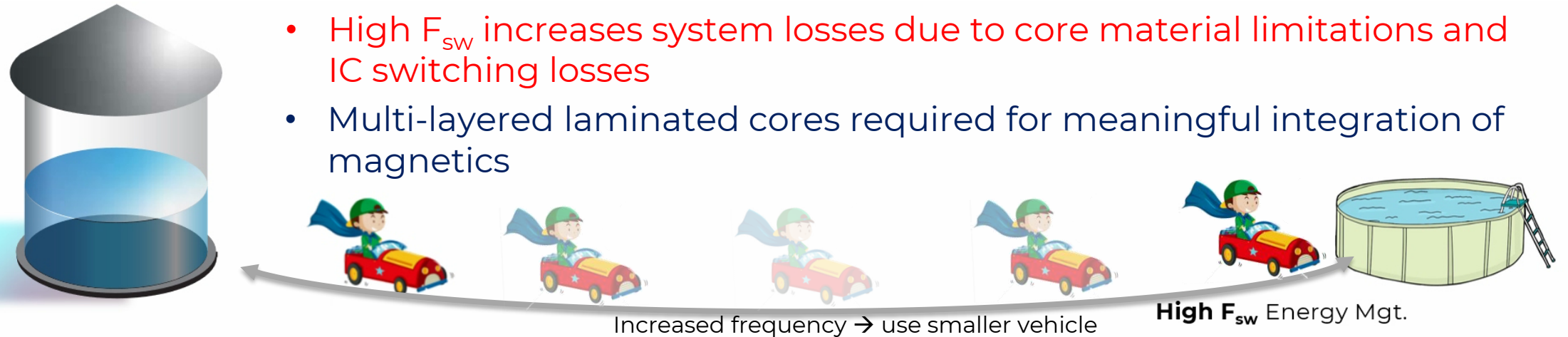
Wafer Level Magnetics

(Si & GaN trends to higher F_{sw} shift the PwrSoC's bottleneck to magnetics)

The inductor is acting as an energy storage element on a switching converter



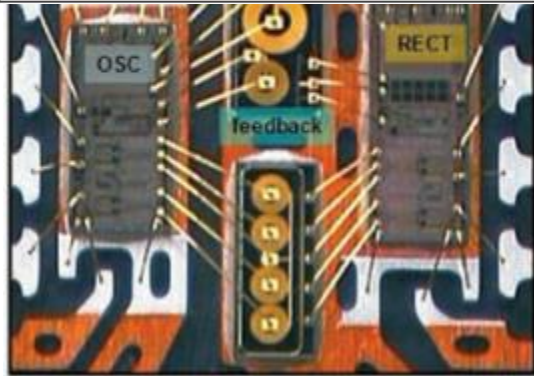
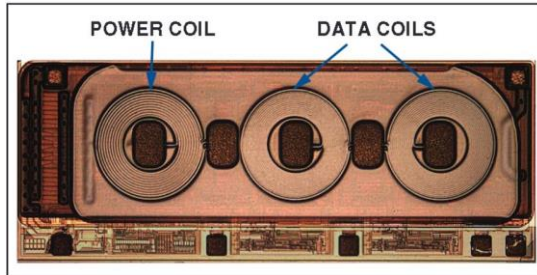
- Core Materials: High B_{sat} allows for size reduction
- Output Power: High F_{sw} allows for size reduction
- High F_{sw} increases system losses due to core material limitations and IC switching losses
- Multi-layered laminated cores required for meaningful integration of magnetics



Wafer Level Magnetics

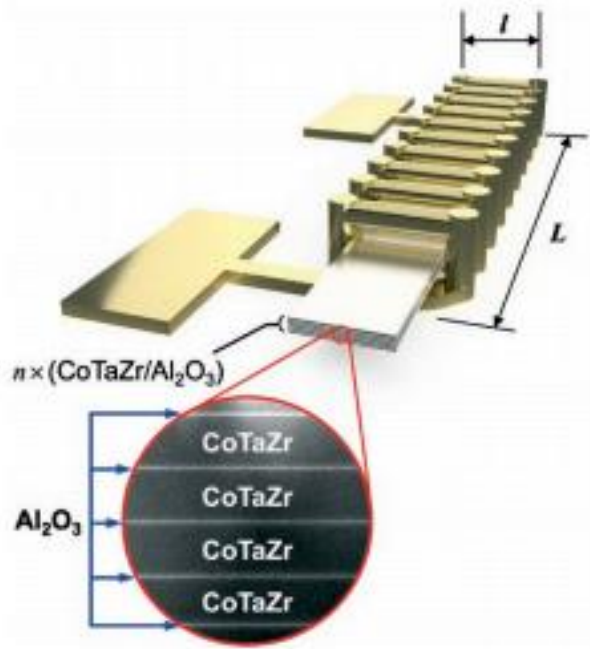
(Core technology options)

Aircore WLM



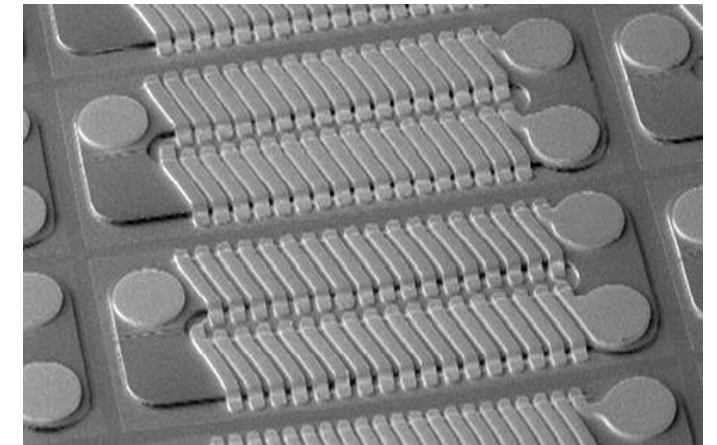
iCoupler, ADI

Multilayered thick film sputtered core



Evatec

Electroplated thick film core



Enpirion

Electroplating windings

Electroplating windings

Electroplating windings

Wafer Level Magnetics

(Core technology comparison)

Aircore WLM

- ↑ Easy to fabricate
- ↑ Low cost
- ↑ Low power loss
- ↓ High near magnetic fields
- ↓ Low inductance
- ↓ Requires high F_{sw}

Multilayered thick film sputtered core

- ↑ High performance
- ↑ Process/thickness control
- ↑ FEOL compatible
- ↓ Slow (.1um/min)
- ↓ High-cost process (~10-20x of the plating)
- ↓ High capital costs (>5X over electroplating)
- ↓ Limited alloy selection
- ↓ Thickness/Stress limitations (<20L, <3 um)
Power \approx core thickness

Electroplated thick film core

- ↑ Fast deposition (1um/min)
- ↑ Low cost process
- ↑ Intrinsically low stress → No. layers (>100)
- ↑ Low capital costs (BEOL-OSAT)
- ↑ Highly scalable
- ↓ Metallic high μ crystalline films have low ρ → small skin depth → higher loss
- ↓ Multi-layer laminations needed for high currents >1A
Complex multi-layer/multi-mask
cost prohibited process

Enachip's Technology Platform

Enachip addresses the electroplating core shortcomings to enable a high performance WLM cost competitive solution

Electroplated core

- ↑ Fast deposition process (1 μ m/min)
- ↑ Low cost process
- ↑ Intrinsically low stress → No. layers (>100)
- ↑ Low capital costs (BEOL-OSAT)
- ↑ Highly scalable



↓ Metallic high μ crystalline films have low ρ → small skin depth → higher loss



↓ Multi-layer laminations needed for high currents >1A
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EnaChip : Enabling Technology Platform

(Multiple Market Verticals)

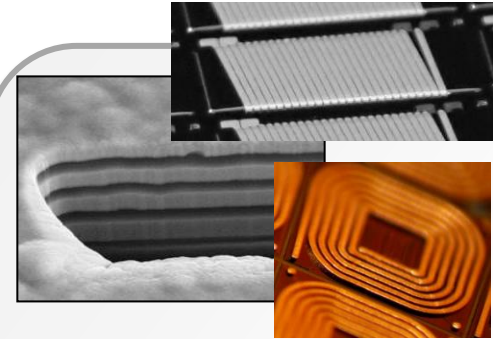
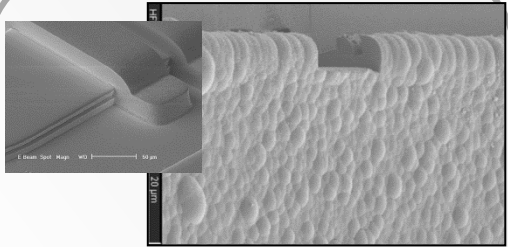


Post Process (BEOL-OSAT) compatible
INDEPENDENT of Si node!

Unique high-performance magnetic materials

Utilizes highest speed integrated electronic circuits

Innovative wafer fabrication processes



Unique Magnetic Alloys

- New Compositions of mater
- Unique formulations to meet performance
- Enachip Proprietary
- CMOS compatible

Miniaturization / Cost

Addressable Market Verticals

Voltage Regulation

- DC/DC Voltage Regulators
- Integrated Power Management IC
- LED Drivers

Magnetic Field Sensing

- Magnetic field -> Electric Signal

Power Harvesting

- RF → DC
- Solar -> DC/AC
- Mechanical -> DC/AC

Signal Conditioning

- Low Pass Filter
- Band Pass Filter
- Tuner
- RF Suppression (Beads)

Electromagnetic Actuation

- Moving Beams
(*Reed switches, Relays*)
- Electromagnetic Separation
(*Bio-medical devices POC Lab on Chip*)
- Moving membranes
(*micro Pumps, micro Valves*)

Innovative Mfg. Processes

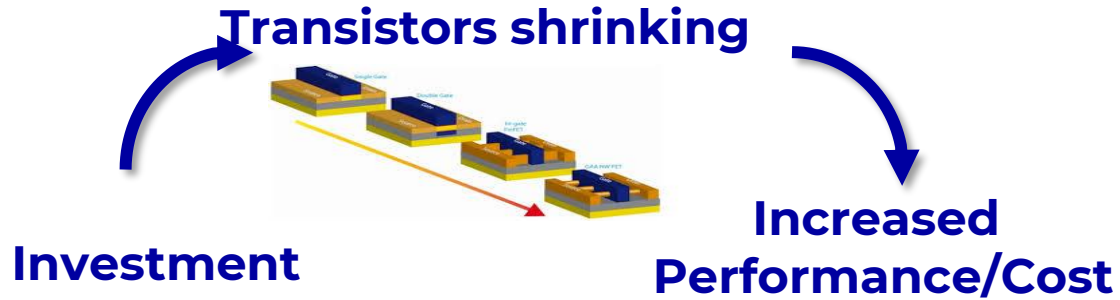
- Game changing low-cost magnetic core laminations
- Copper windings
- Integrated circuit compatible

Performance / Cost

More than Moore : Added Functionality at Chip Level

Moore's law reaching physical limitations

Added functionality on chip level



Technical progress & industry's confidence in **Moore's Law** feeds into a virtues cycle!



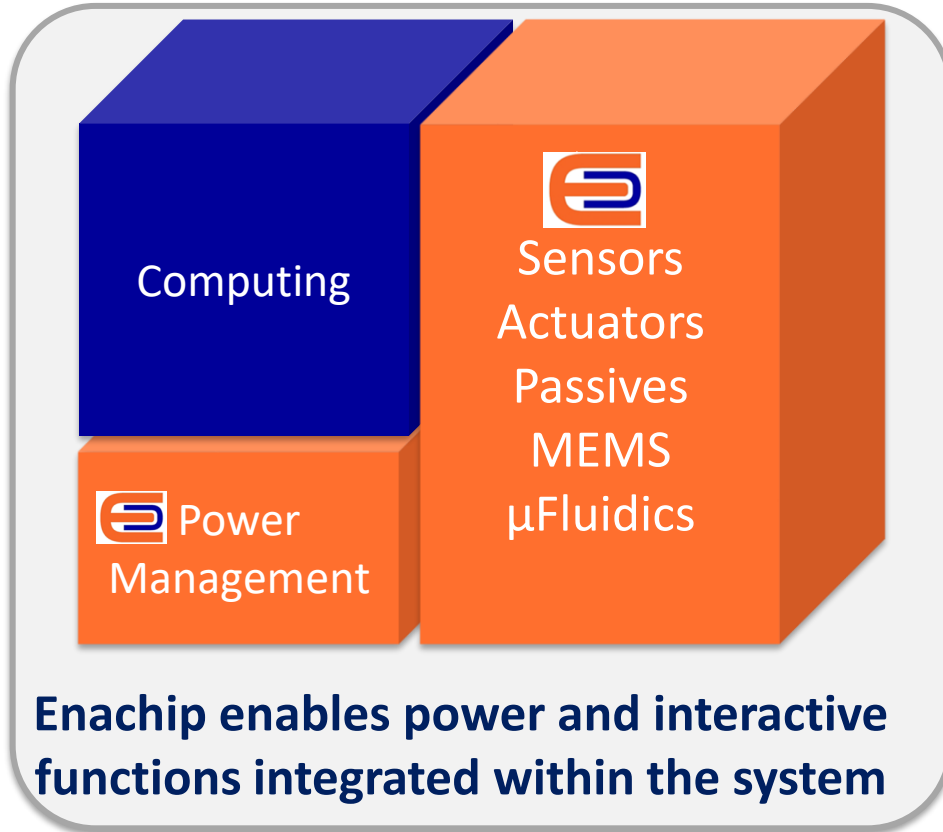
Increased functionality at chip level feeds into a **More than Moore** virtues cycle!



Smart Power Integration is needed in All Systems

ENACHIP WLM platform enables power and interactive functions in system

System Integration at chip level

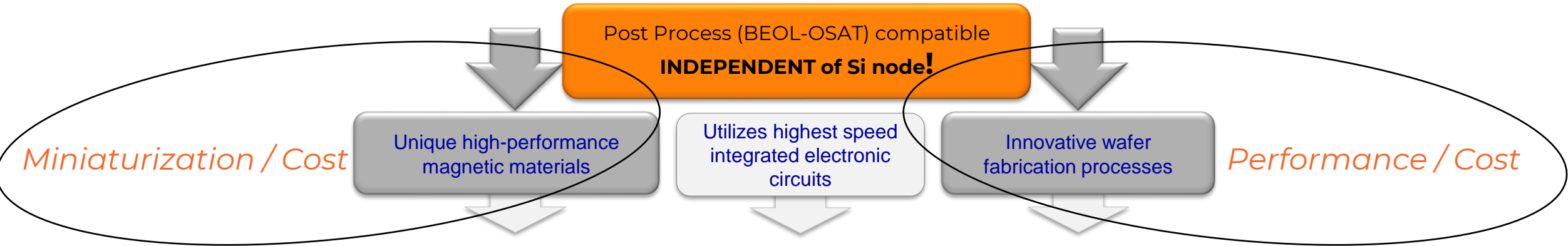


Devices are “talking” to environment and to the users



EnaChip : Enabling Technology Platform

(Multiple Market Verticals)



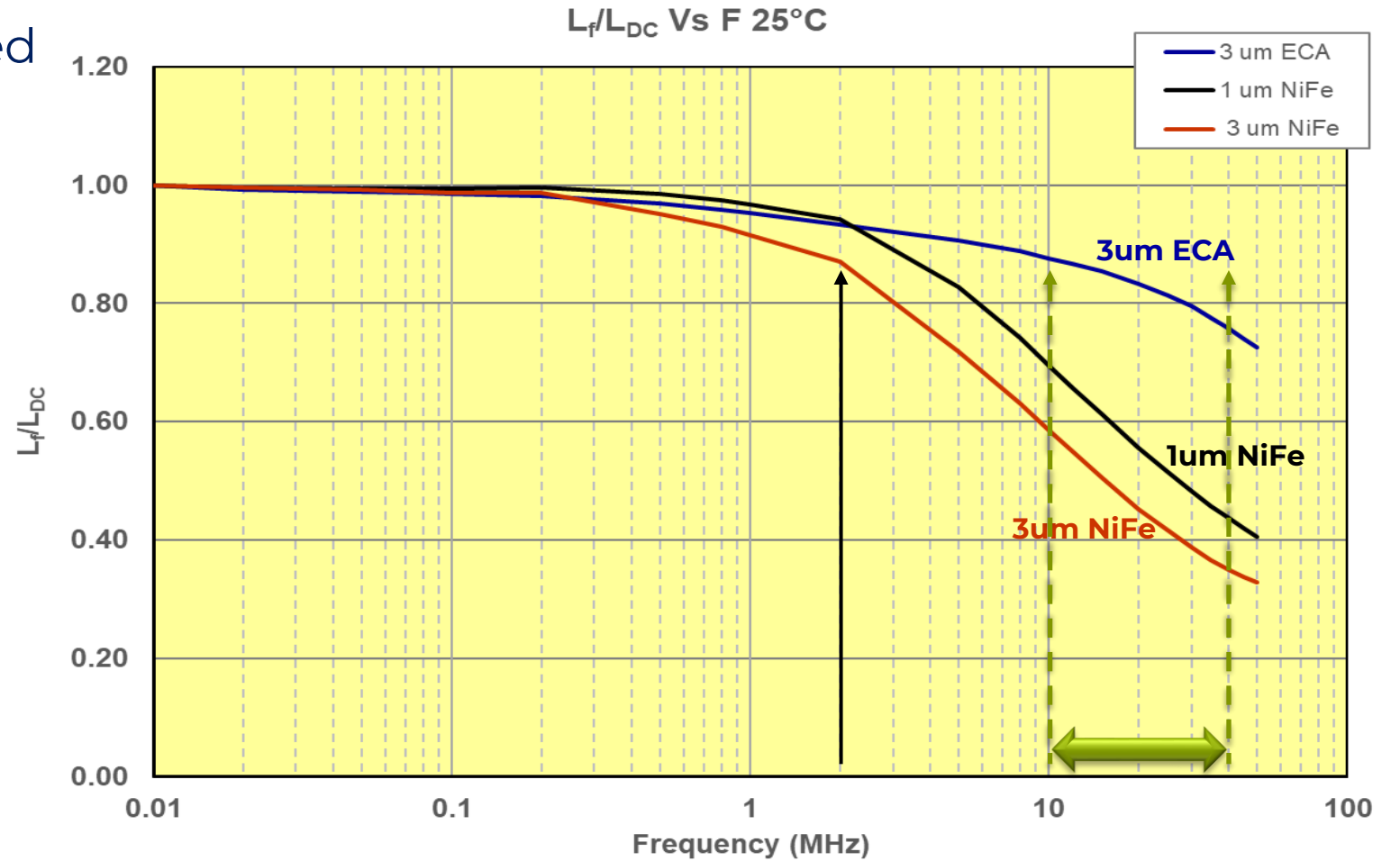
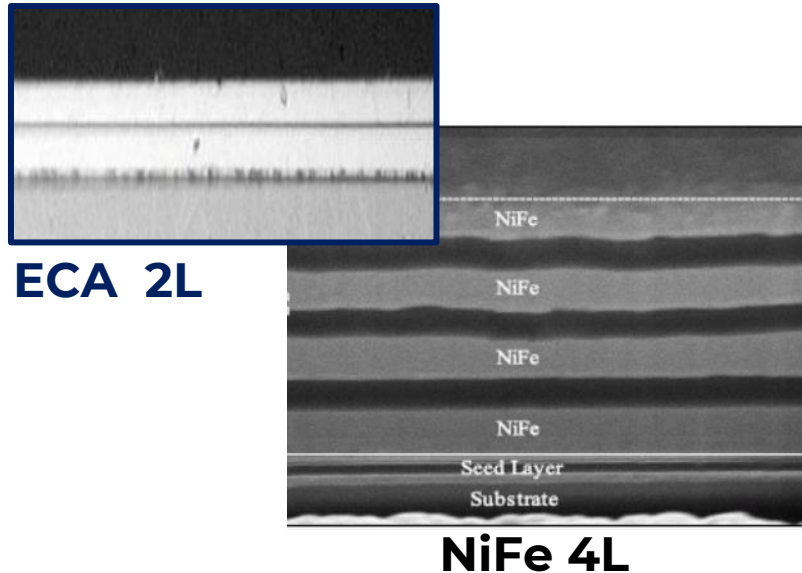
Addressable Market Verticals

- | | |
|---|--|
| <p><u>Voltage Regulation</u></p> <ul style="list-style-type: none"> • DC/DC Voltage Regulators • Integrated Power Management IC • LED Drivers | <p><u>Signal Conditioning</u></p> <ul style="list-style-type: none"> • Low Pass Filter • Band Pass Filter • Tuner • RF Suppression (Beads) |
| <p><u>Magnetic Field Sensing</u></p> <ul style="list-style-type: none"> • Magnetic field -> Electric Signal | <p><u>Electromagnetic Actuation</u></p> <ul style="list-style-type: none"> • Moving Beams
<i>(Reed switches, Relays)</i> • Electromagnetic Separation
<i>(Bio-medical devices POC Lab on Chip)</i> • Moving membranes
<i>(micro Pumps, micro Valves)</i> |
| <p><u>Power Harvesting</u></p> <ul style="list-style-type: none"> • RF → DC • Solar -> DC/AC • Mechanical -> DC/AC | |

High Performance proprietary Mag. Alloys

EnaChip Alloy (ECA)

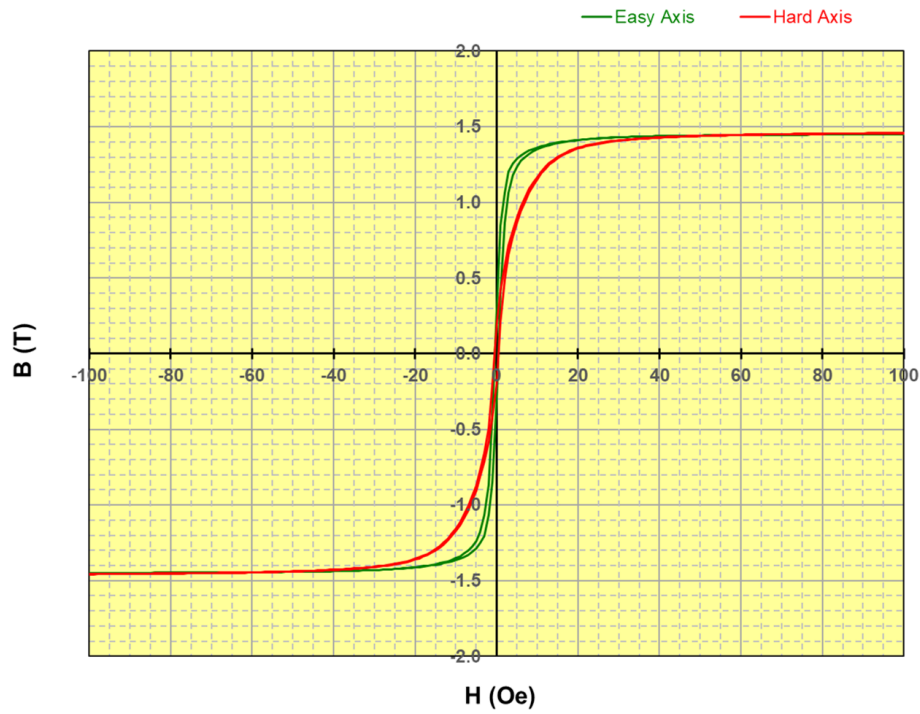
- Amorphous Electroplated
- 3x NiFe resistivity
- F_{sw} up to 30MHz



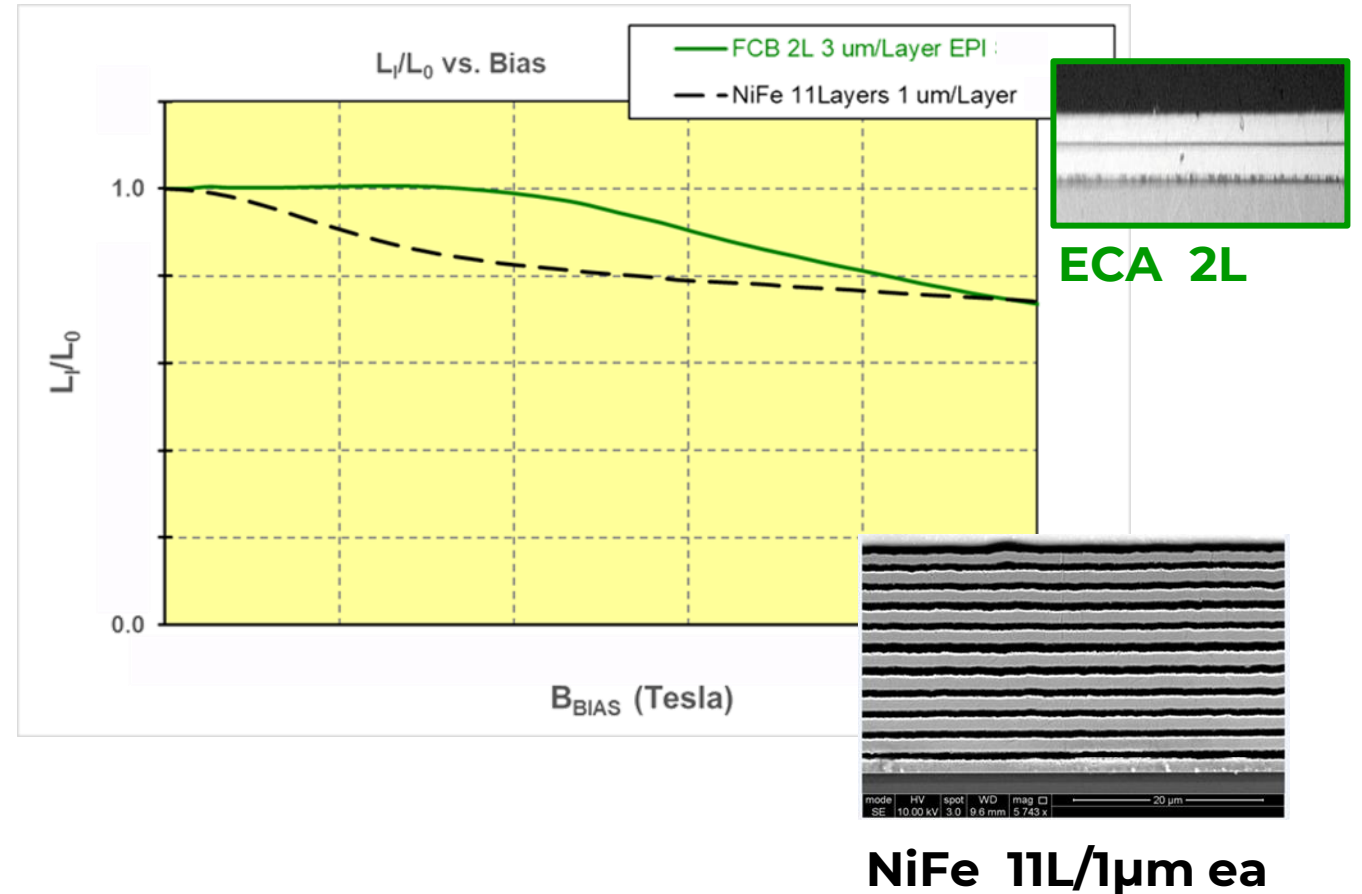
High Performance Proprietary Mag. Alloys

EnaChip Alloy (ECA)

- Permeability 900
- $B_{sat} \geq 1.5$ T

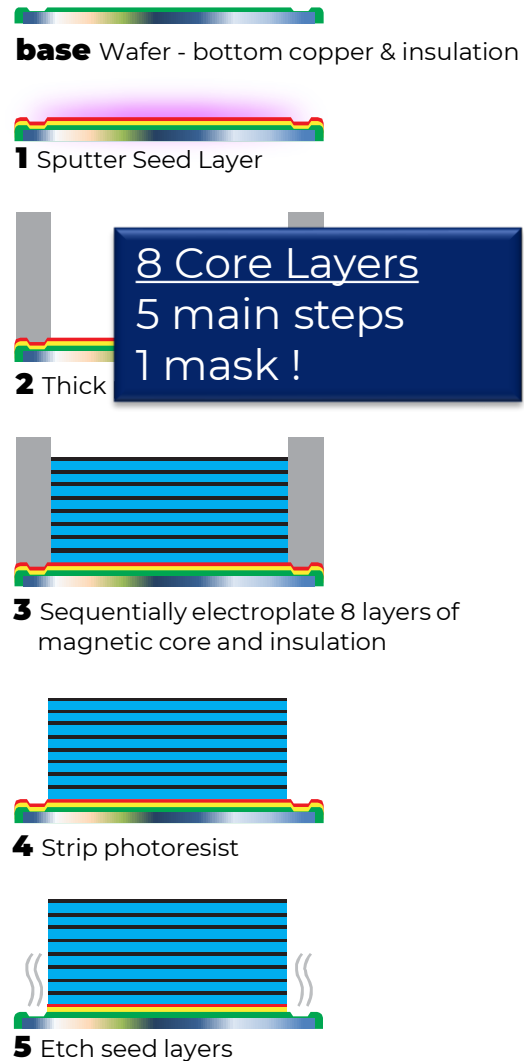


ECA Bias operational range \gg NiFe

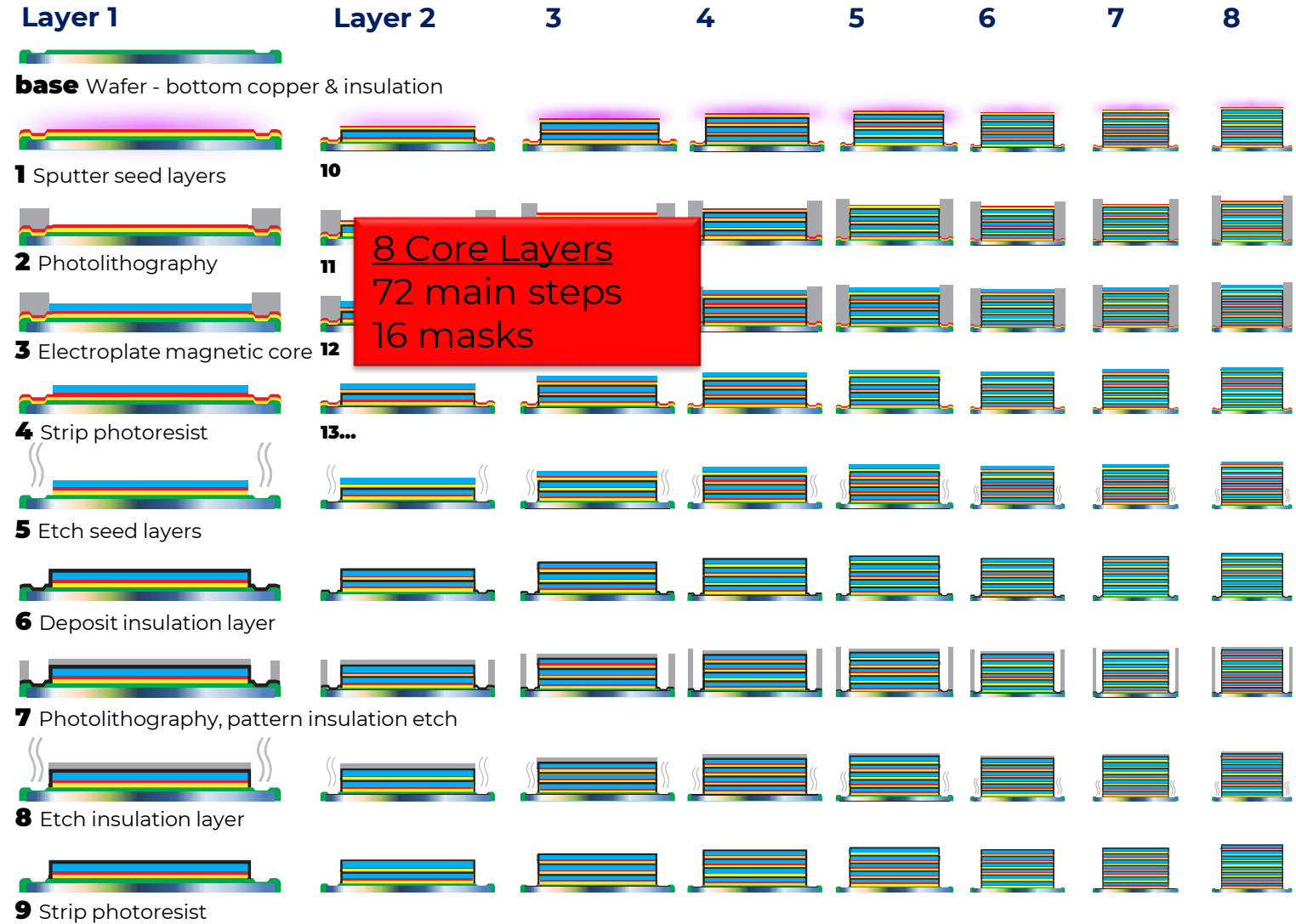


Game Changing Multilayer Cost Reduction !

EnaChip

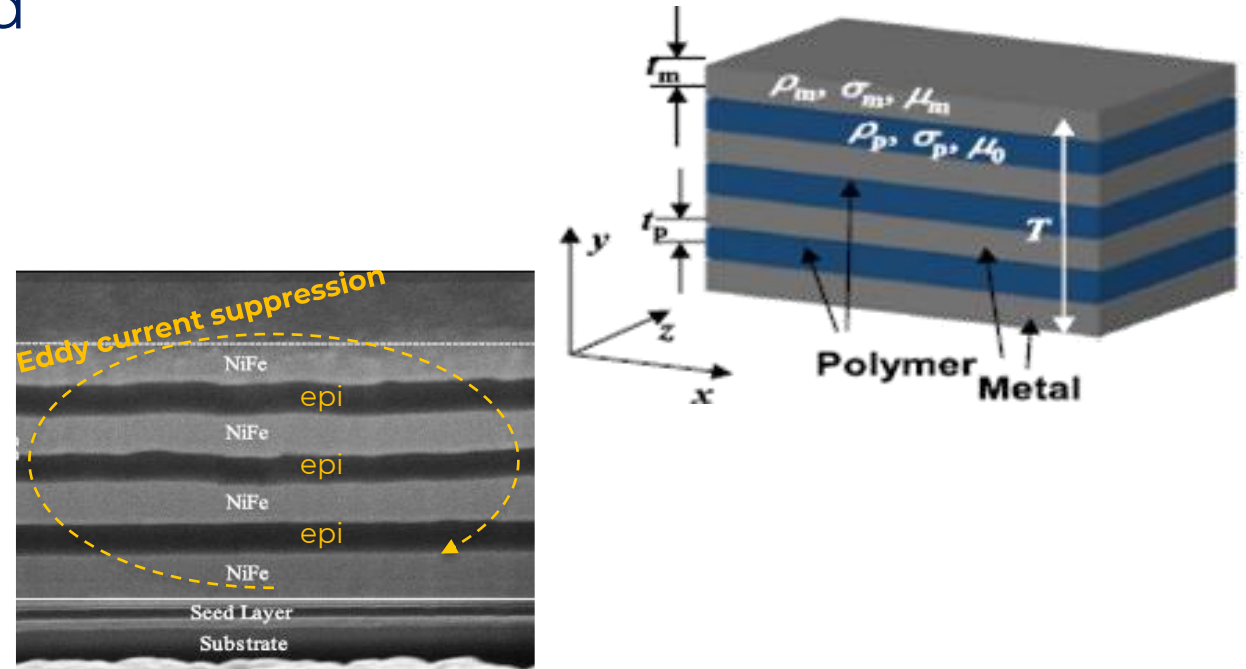
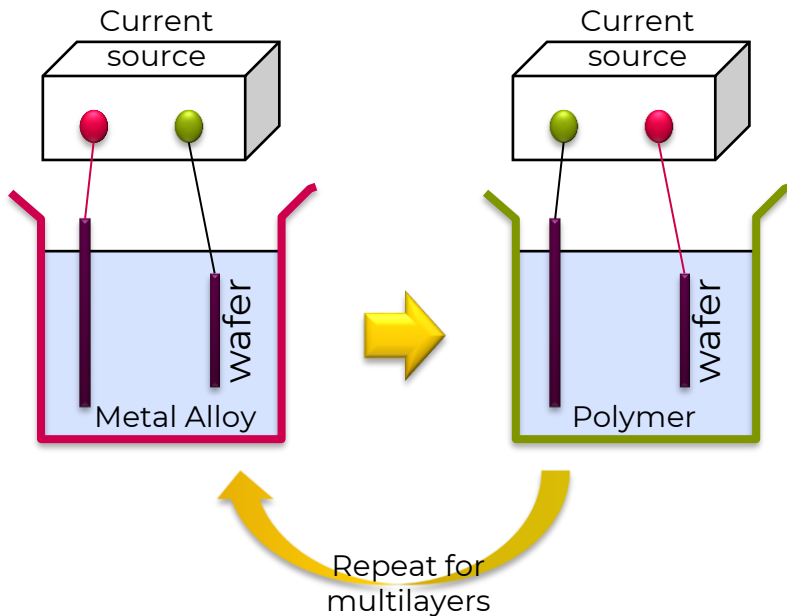


Standard



Multi Layer process incorporates electroplated insulator (epi)

- Electrochemically synthesized insulator
 - Conjugated polymer based
- Conductivity $< 1\text{S/m}$

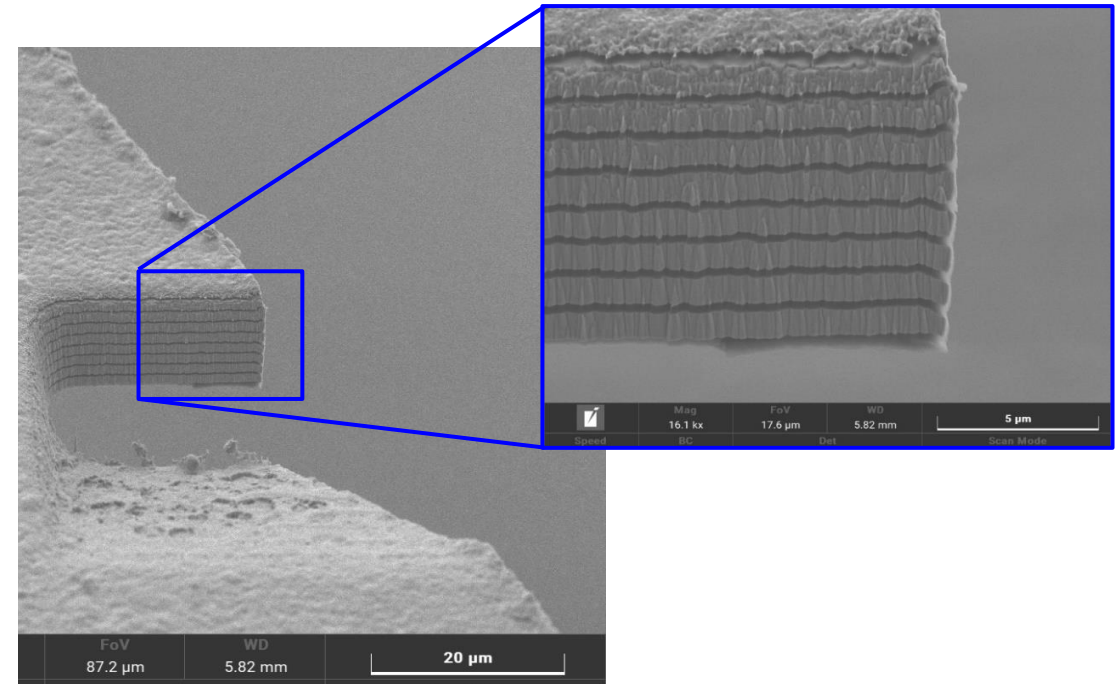
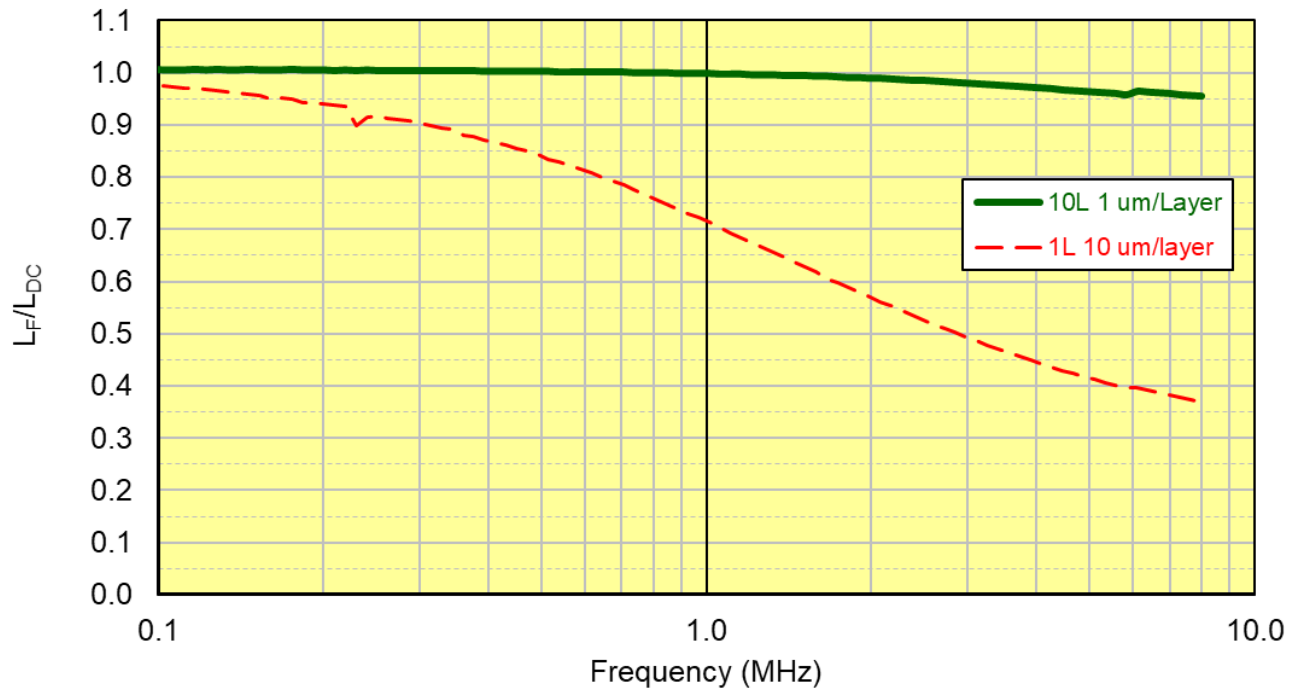


Vertical conductivity is important for Eddy current suppression

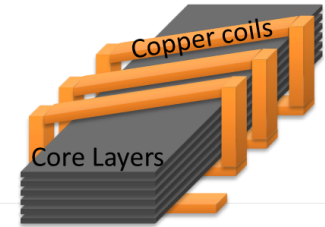
Multi Layer process Thin Insulator !

- Multiple layer with thin Insulator → Very high layer packing coefficient
→ Low profile cores
- EPI performance is comparable to ideal insulator with ability to suppress Eddy Current Loss

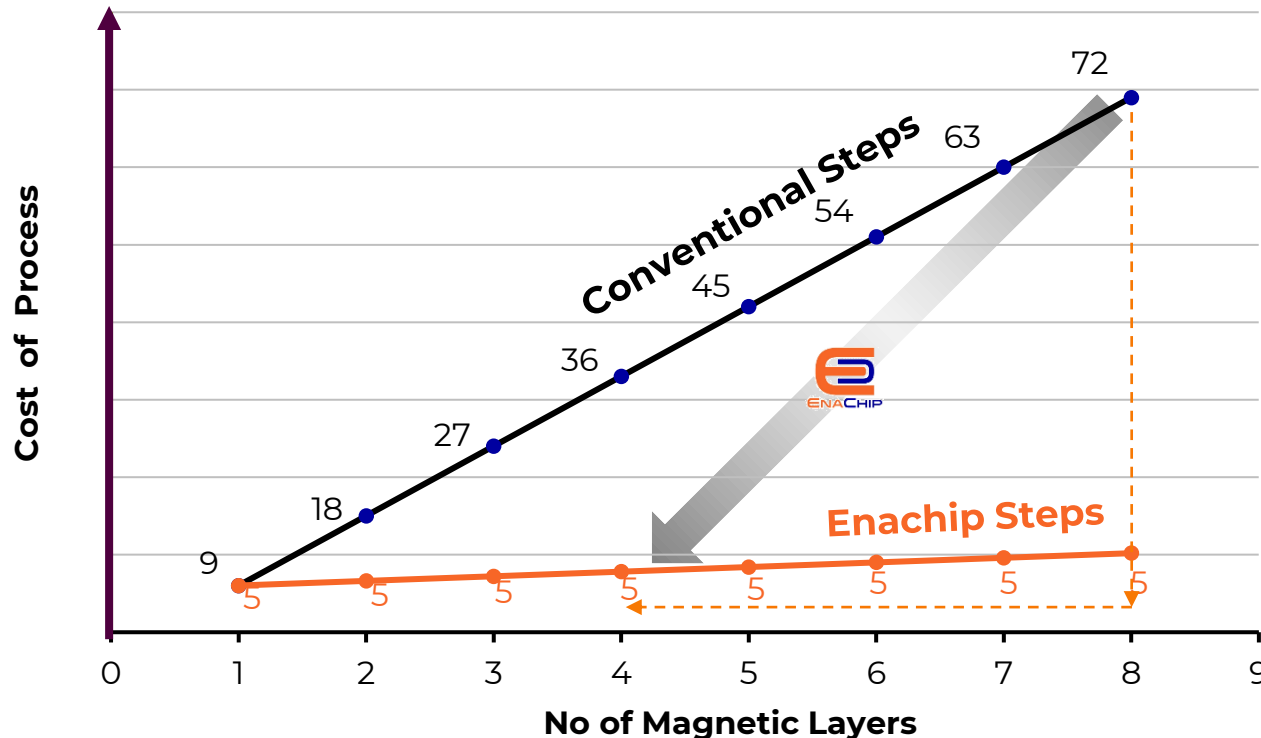
NiFe - L_F/L_{DC} Vs F 25°C



Combination of performance alloys and cost reduction manufacturing process → Competitive WLM commercialization



Number of Steps & Cost of Manufacturing Comparison

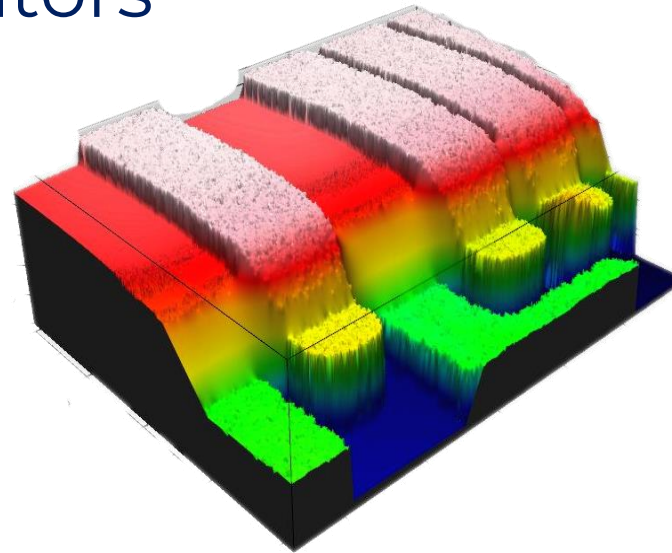


Example Multi Layer Process:
Build a high current MEMS inductor
e.g. requires 8 Core layers
 Conventional: **72 steps**
 Enachip: **5 steps**
 → **14x less steps**
 → **game changing cost reduction**

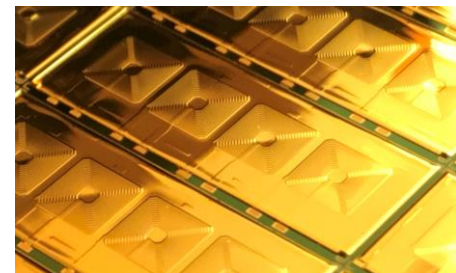
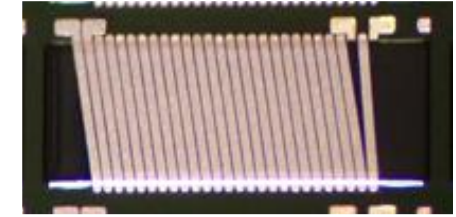
Enachip's Alloy:
Reduces the required layers by 2x
 → **Reduce process time by 50%**

Device Examples

- ☞ Thick Cu toroid micro-inductors
- ☞ Multi-core toroids
- ☞ Spiral coils
- ☞ Electromagnets/Actuators
- ☞ Transformers
- ☞ Sensors



High aspect ratio lithography and electroplating!

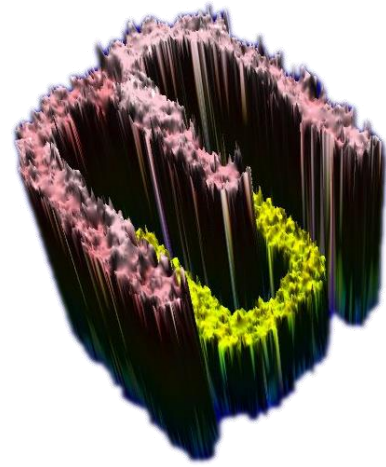


Summary

- New amorphous high resistivity magnetic alloys
- Single-mask multi-layer core electroplating laminations



- Potential game changing Wafer Level Magnetic integration for PwrSoC
- Post process technology platform – independent from Si nodes can address multiple PwrSoC applications
 - Low current ($I_{out} < 3A$), Low profile $< 0.3mm$
 - Moderate current ($3A < I_{out} < 6A$), DCR $< 30 m\Omega$, Low profile $< 0.5mm$
 - High current ($6A < I_{out} < 10A$), DCR $< 1 m\Omega$, Low profile $< 0.6mm$



Thank you

More to come at Live PwrSoc 2021 in Philadelphia !