Ferric

Efficient On-chip Power Conversion

POWER SOC 2020

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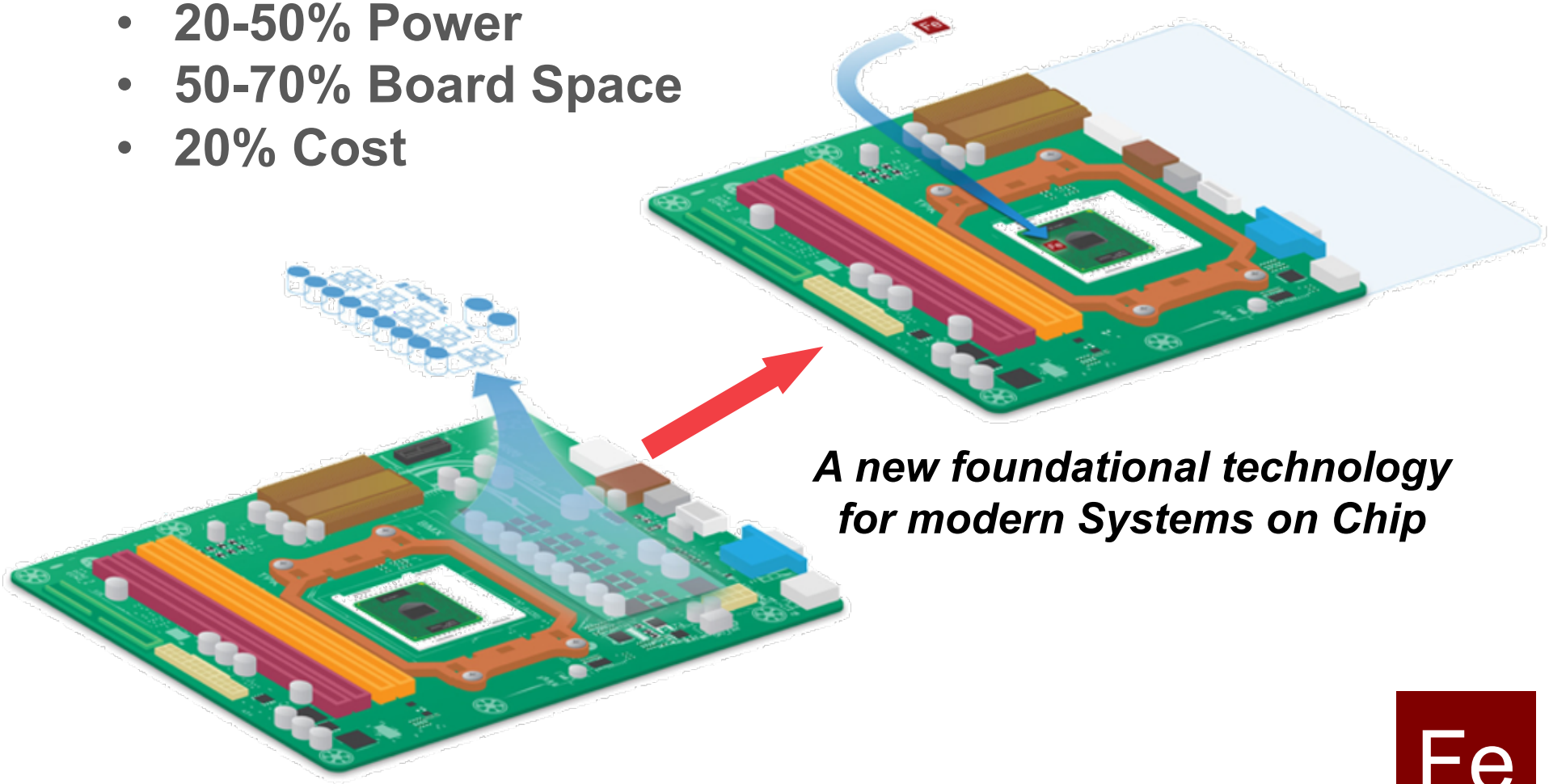
Ferric President & CEO

NEXT GEN ELECTRONICS REQUIRE NEXT GEN POWER SYSTEMS

Ferric's manufacturing and system technology enable integrated power management, saving…

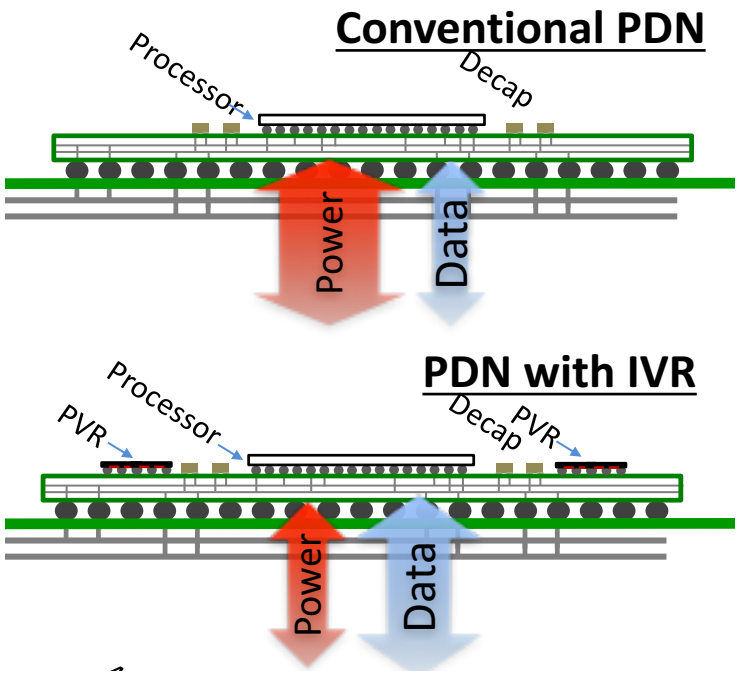
- **20-50% Power**
- **50-70% Board Space**
- **20% Cost**

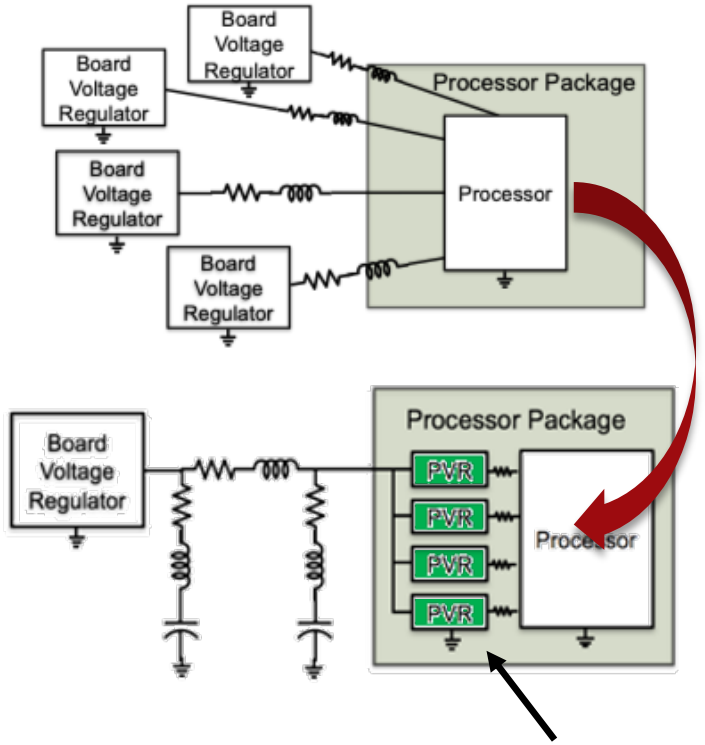


A new foundational technology for modern Systems on Chip

FERRIC PACKAGE VOLTAGE REGULATORS (PVRS)

- Shrink power converters to be co-packaged with processors
- Reduce losses associated with high currents passed through
  board → socket → package → processor
- Enable delivery of many independently scalable supplies





Save:
20% power
$20 BOM
20cm^2 area

US Pat. 16/129,305
PCT/US 18/48290
TW Pat. 107141297

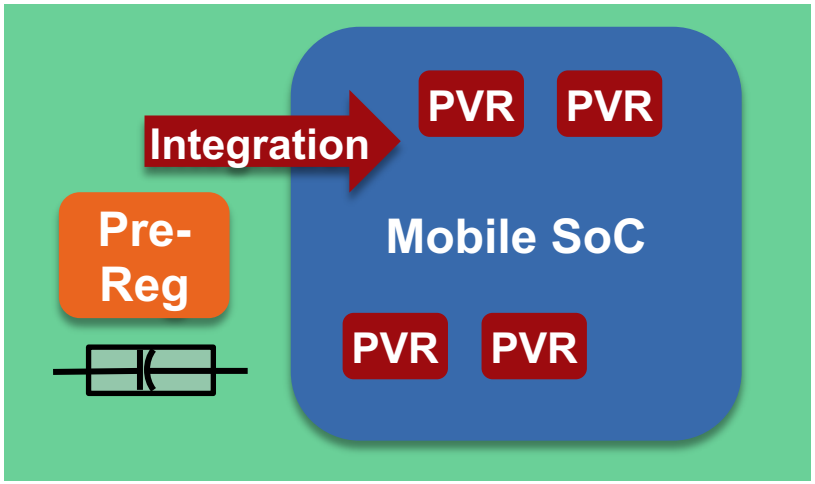
Ferric Single-Chip Power Converters

Fe

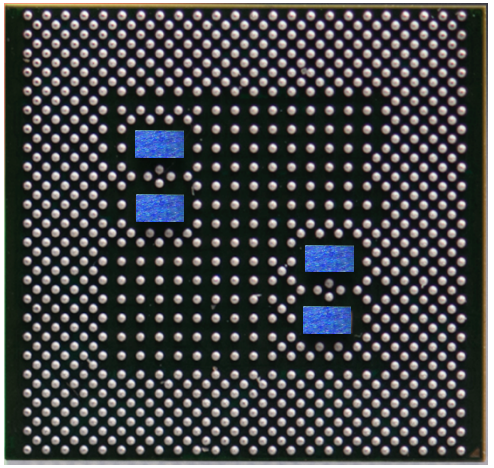
PACKAGE VR for Mobile Applications Processor

- Low-profile (150um) PVR chiplets can be attached to landside of chip-scale packages or be embedded into wafer-level packages
- Consolidate SOC power supplies to a single, loosely regulated 1.8V

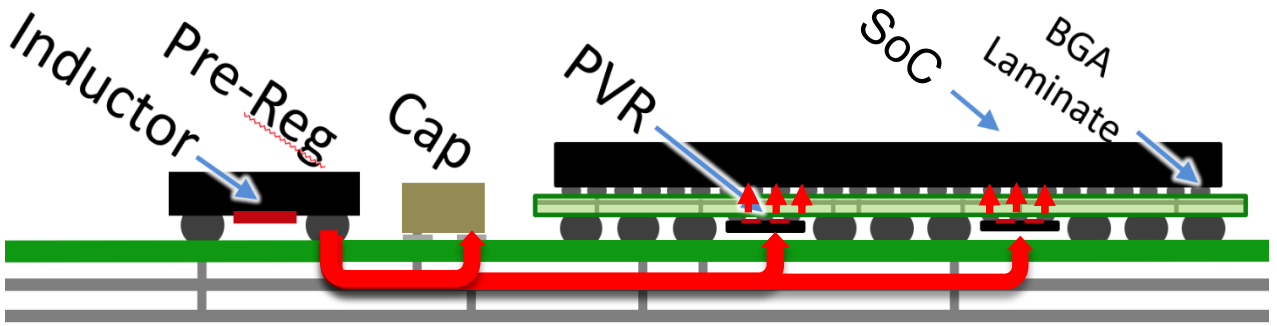
Top View



SoC Landside View



Cross-Section View



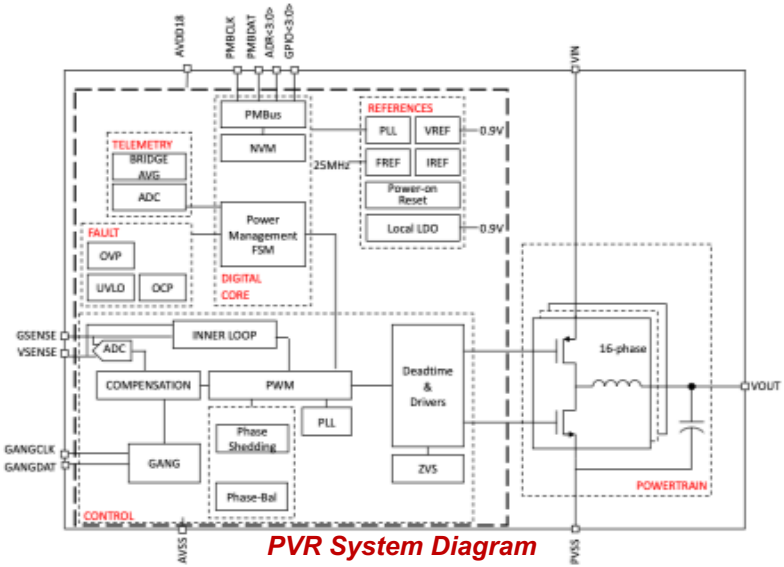
FERRIC Single Chip Power Converters

Package Voltage Regulator

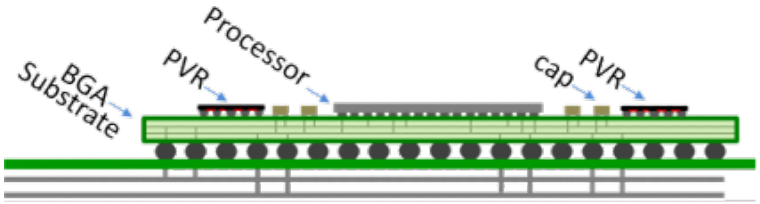
Complete many-phase Buck on a single CMOS chip

- Integrating switches, inductors, controller, telemetry and references
- Only missing bulk decoupling capacitance

- **V_{IN} 1.0V-2.0V :: V_{OUT} 0.3V-1.5V with I_{OUT} 0-20A**
- **Conversion efficiency 90% ~ 80%**
- **Digital Feedback Controller**
  - 50MHz+ feedback control bandwidth
  - 12-bit windowed flash ADC
  - Up-to 18-phase DPWM with < 3mV resolution and < 200ps latency
  - Fast-Phase-Shedding inner control loop
- **1MHz PMBus-Compliant Serial Interface**
  - Programmable V_{OUT}, F_{SW}, Compensation, Telemetry, Faults, etc.
  - Dynamic Voltage Scaling (DVS) bus for 200ns voltage transitions
  - Gang mode for 1-16 parallel chips



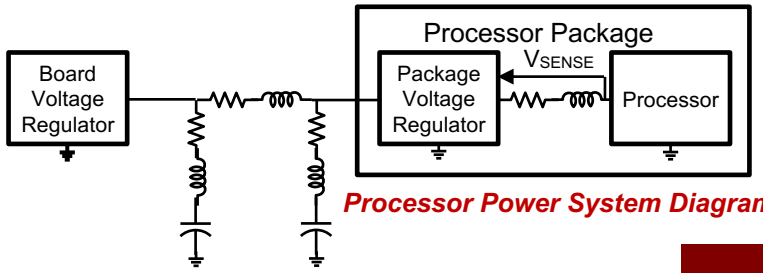
PVR System Diagram



Processor Package Illustration

Technology

- **TSMC N28 HPC+**
- **Ferric-2 power inductors**
- **TSMC Cu Pillar terminations on 160µm pitch**
- **Achieve ~2A/mm² chip current density (excluding cap)**
  - **~1.2A/mm² with ceramic decoupling on input and output**
- **Sold as Standard Product direct to SoC vendors**
- **Known-Good-Die (KGD) for package integration into FC-BGA/LGA or Si Interposer**



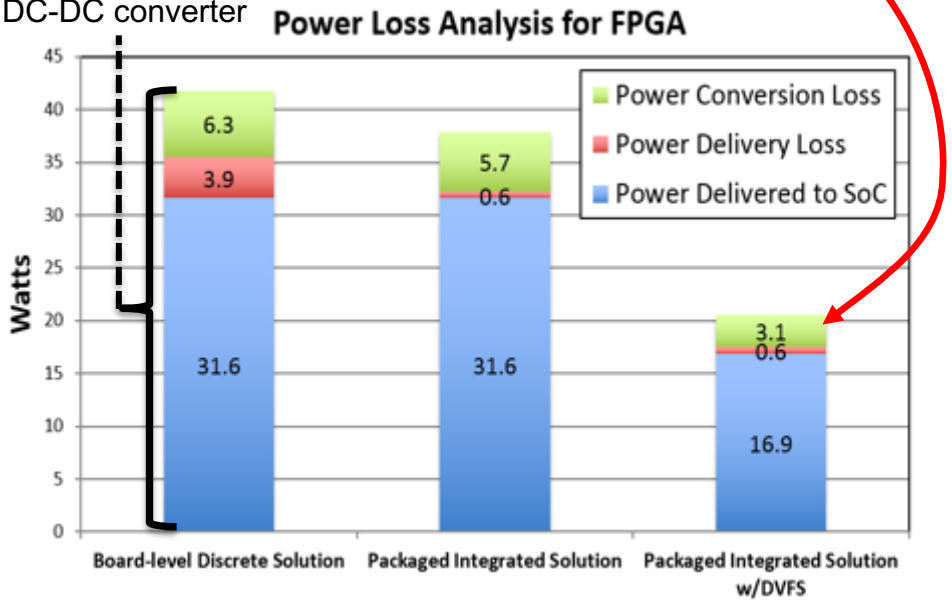
Processor Power System Diagram

PACKAGE VR Power Savings: 20-50%

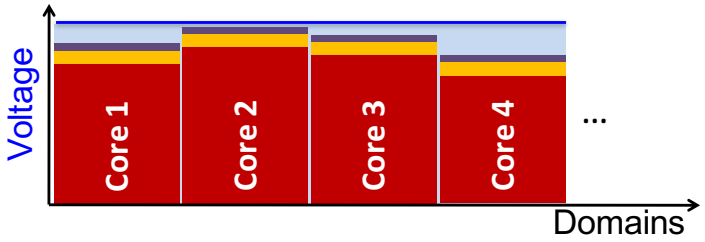
- **Lower Distribution Losses**: Package Voltage Regulators reduce losses in the power distribution network since they are small enough to be integrated at the true Point of Load
- **Improve Voltage Regulation:** Package Voltage Regulators offer ~100x higher regulation bandwidth than conventional solutions, allowing for improved performance and power savings from reduced voltage margins
- **Improve Power Management**: Ferric's integrated solution improves spatial and temporal granularity for power management by 100x which enables more than 50% power savings depending on workload

More than 50% reduction
in overall power consumption
from power management

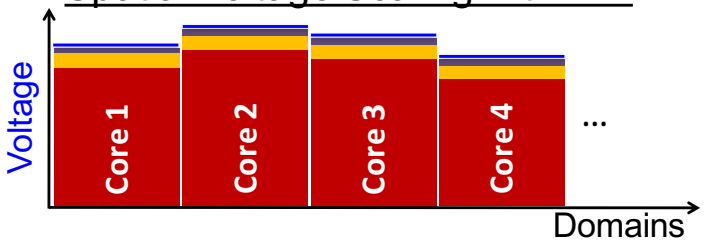
Total power delivered
to DC-DC converter



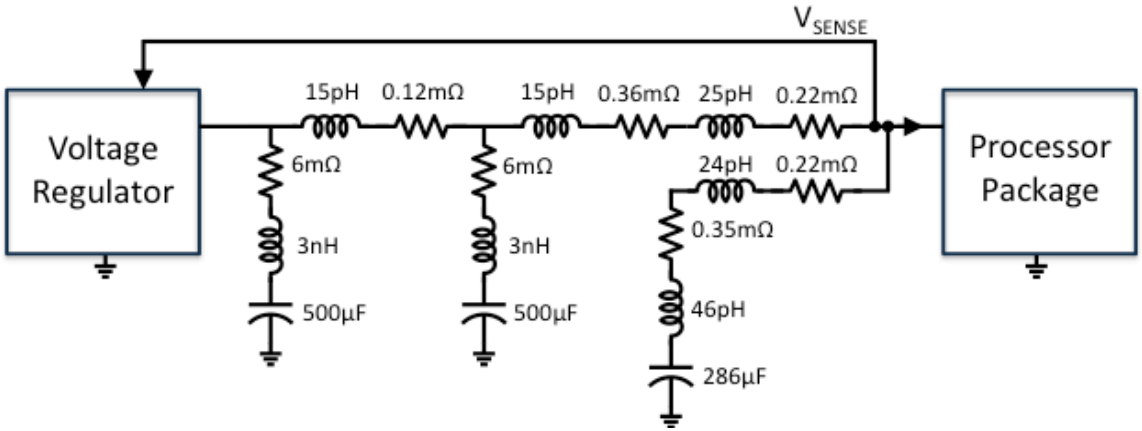
Spatial Voltage Scaling with Discrete VR



Spatial Voltage Scaling with IVR

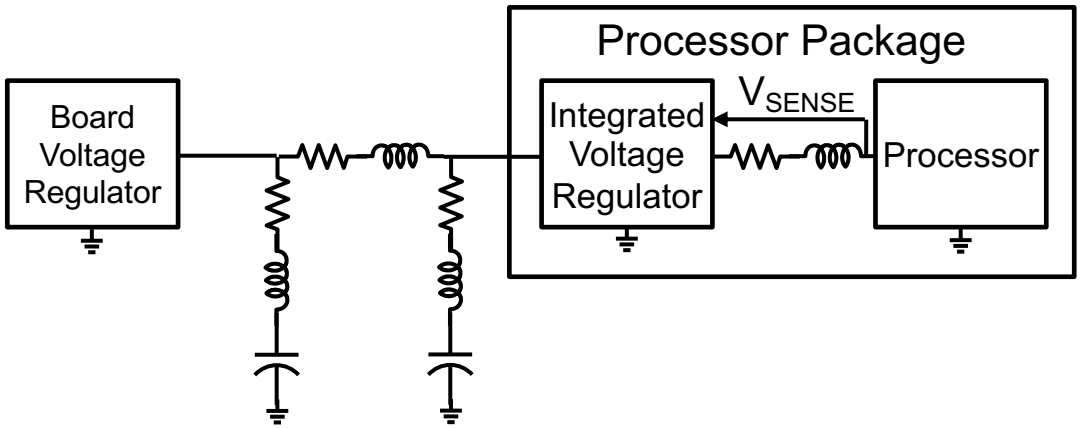


PACKAGE VR Improved Power Integrity



Conventional Power Delivery Network (PDN)

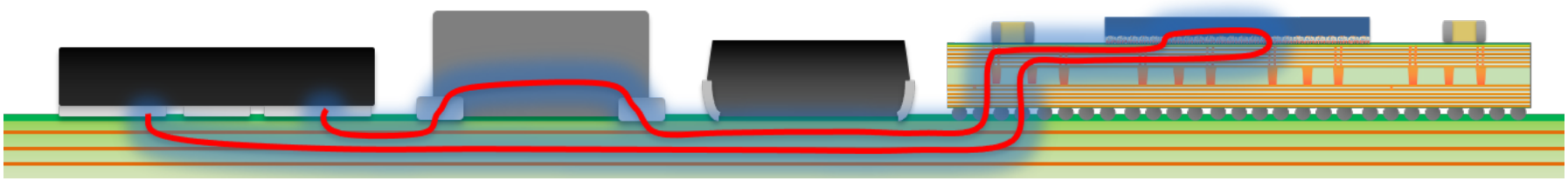
Integrated Power Delivery Network (PDN)



High bandwidth (>50MHz) feedback in immediate proximity to the load:

- *Reduce maximum broadband supply impedance to << 1mΩ*
- *Reduce processor supply voltage margins for improved efficiency*
- *Regulate resonant impedance peaks from upstream PDN*

PACKAGE VR Improved Power Integrity



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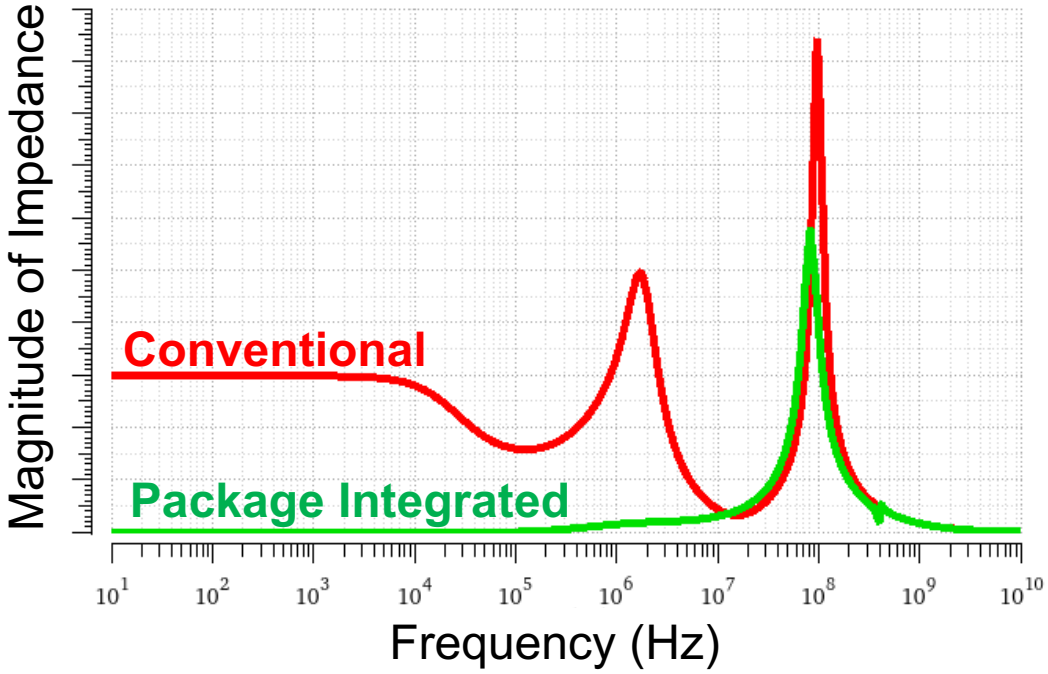
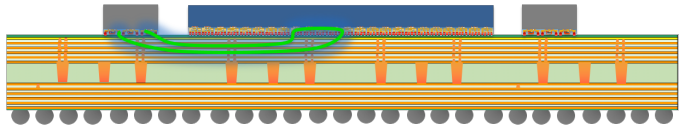




Smaller loop inductance

Less bulk capacitance

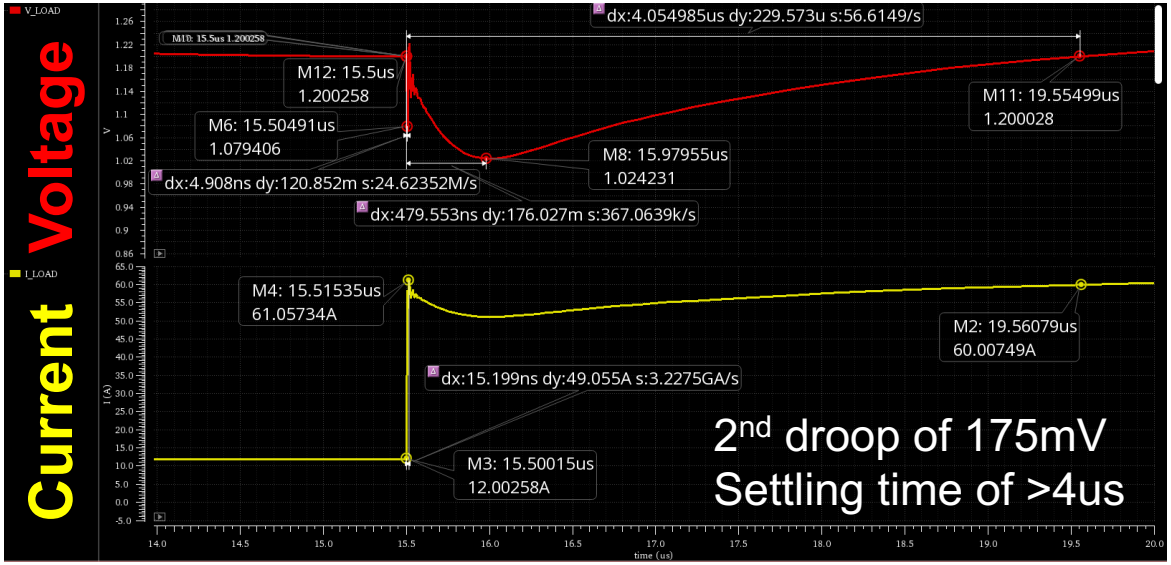
Higher feedback bandwidth

Fewer parasitics

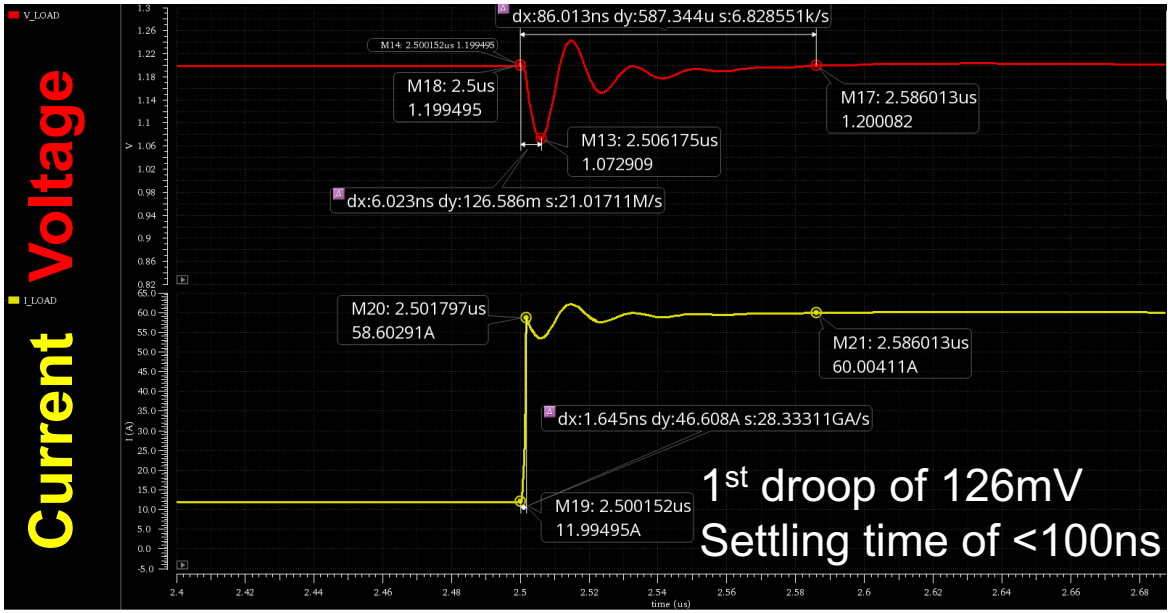
Less impedance overall

PACKAGE VR Improved Power Integrity

60A Processor Load Step with Mother Board VR

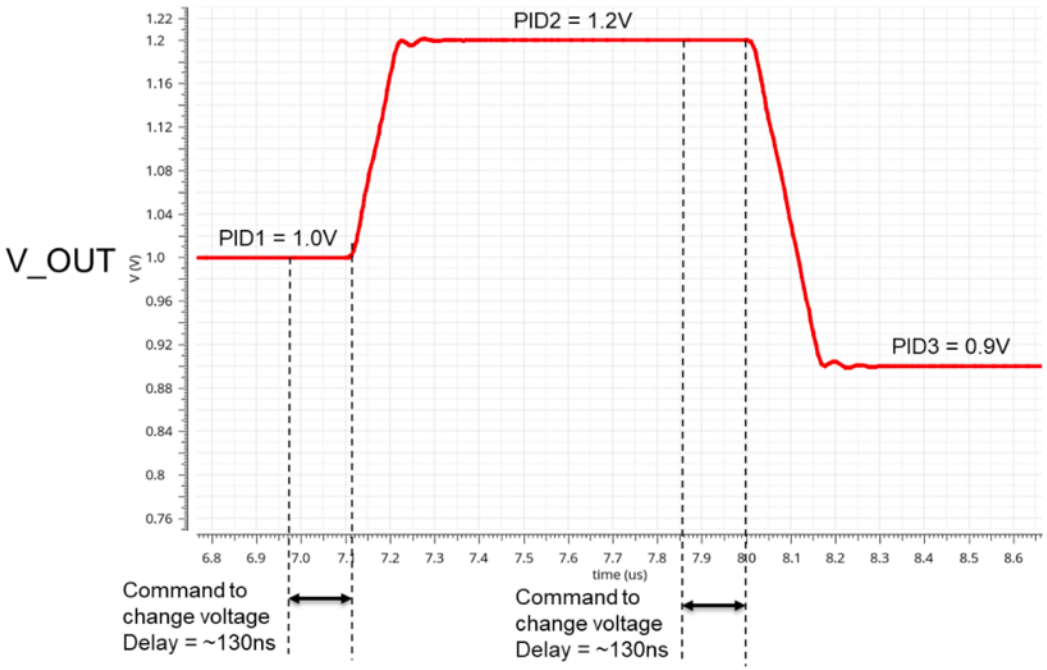


60A Processor Load Step with Ferric Package VR



PACKAGE VR Dynamic Voltage Scaling

- **Steep Voltage Transitions**: Many interleaved buck converter phases, each operating at 100MHz+ switching frequency enables fast voltage transitions ~2mV/ns
- **Low Interface Latency**: ~200ns of total latency for voltage/state transitions enable aggressive dynamic voltage scaling with associated power savings
- **Reduced Transition Penalty**: 100x reduction in decoupling capacitance reduces power loss associated with charging and discharging decoupling capacitors



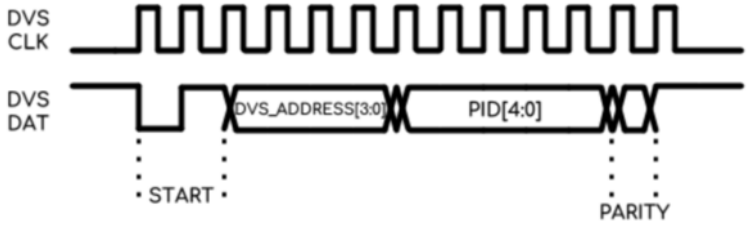


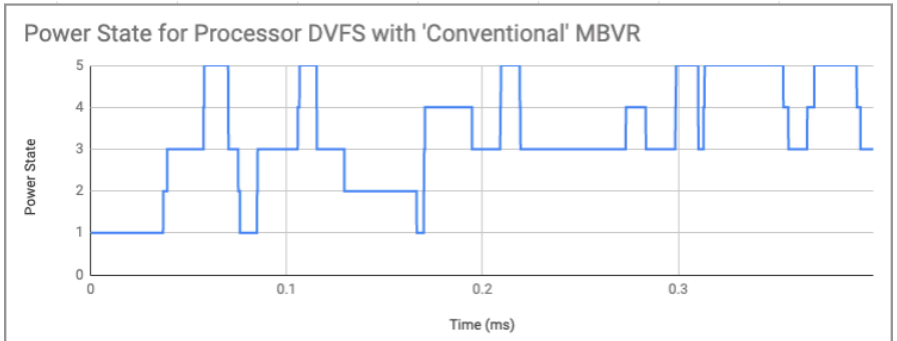
Figure 1: DVS Bus protocol

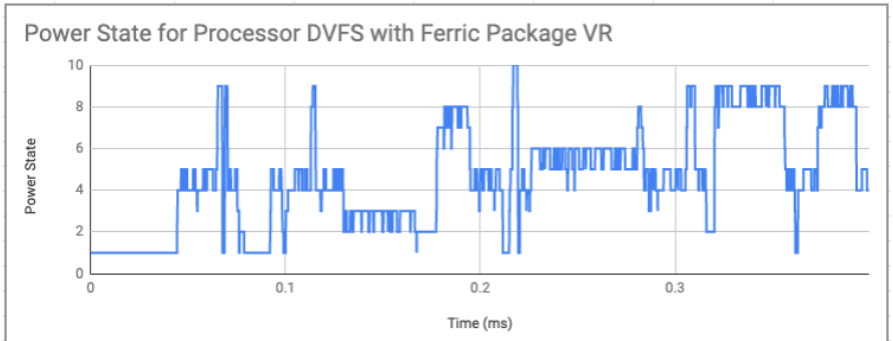
PID	VOUT_COMMAND[15:0]	OCP_THRESH[15:0]	RLL_RES[7:0]
5'b00000	16'h8000 (900mV)	16'h3DE0 (15A)	8'h38 (2.08mOhm)
5'b00001	16'h6380 (700mv)	16'h2F40 (5A)	8'h18 (1.04mOhm)
.	.	.	.
.	.	.	.
.	.	.	.
5'b11111	16'h8E40 (1V)	16'hBD40 (20A)	8'h80 (4.03mOhm)

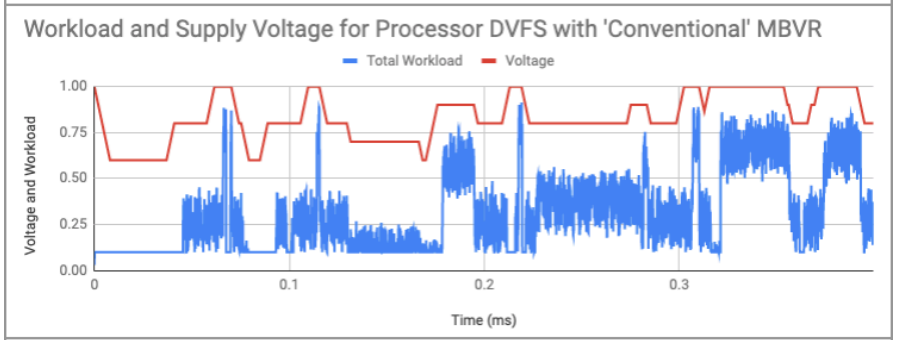
Table 1: Example PID Table

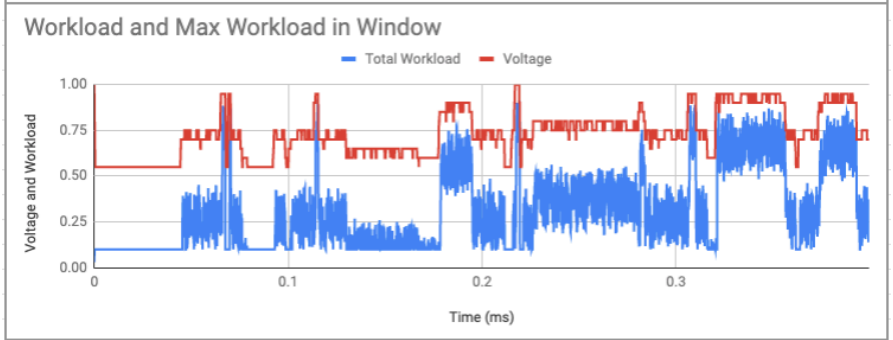
Fine Grain DVFS with Ferric PVRs

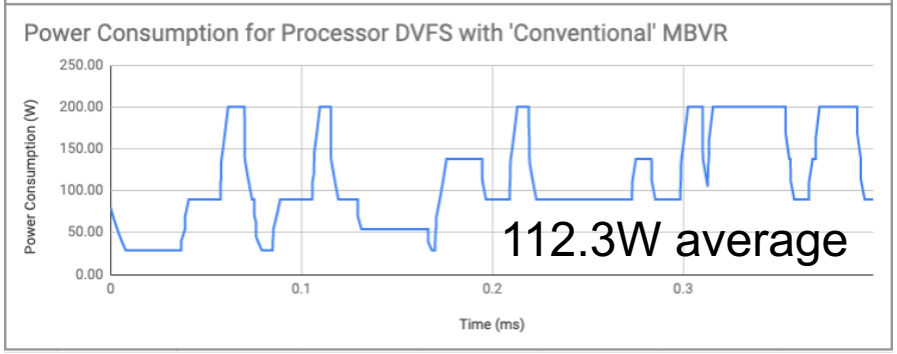
Identical Workload and Performance with 35% less power consumption!

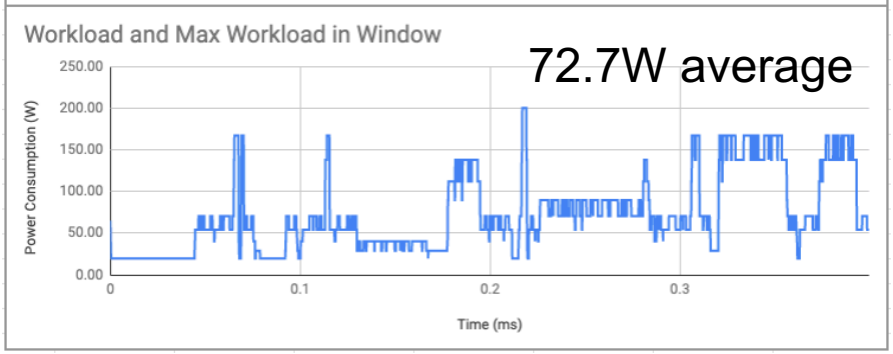










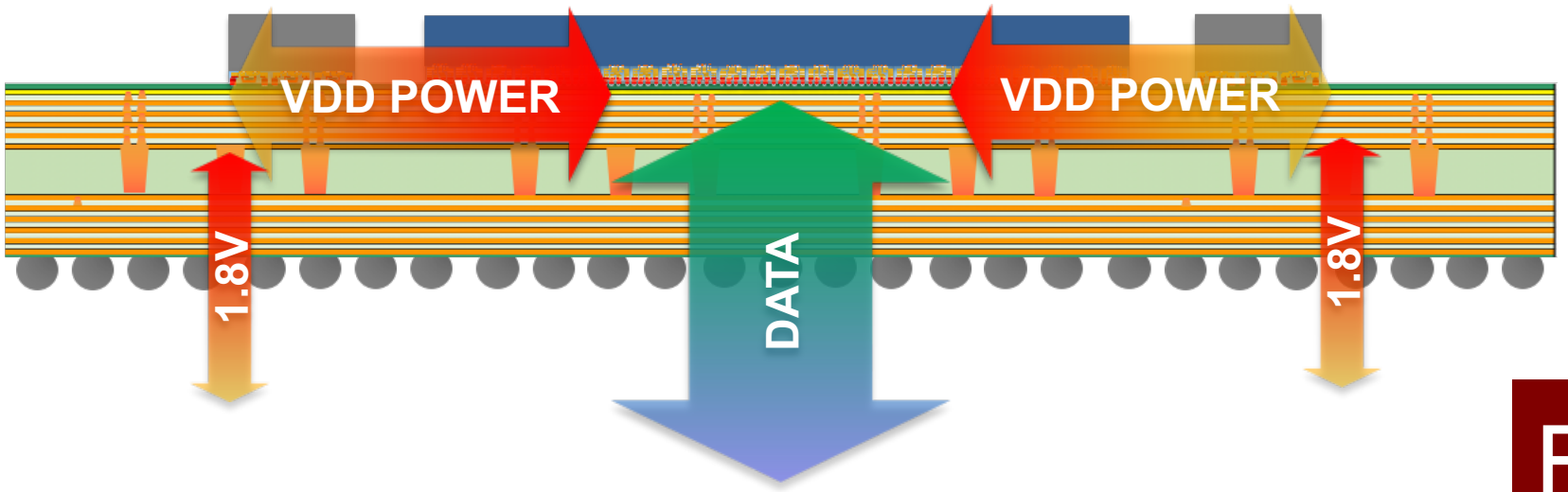


PACKAGE VR Power & Data Bottlenecks

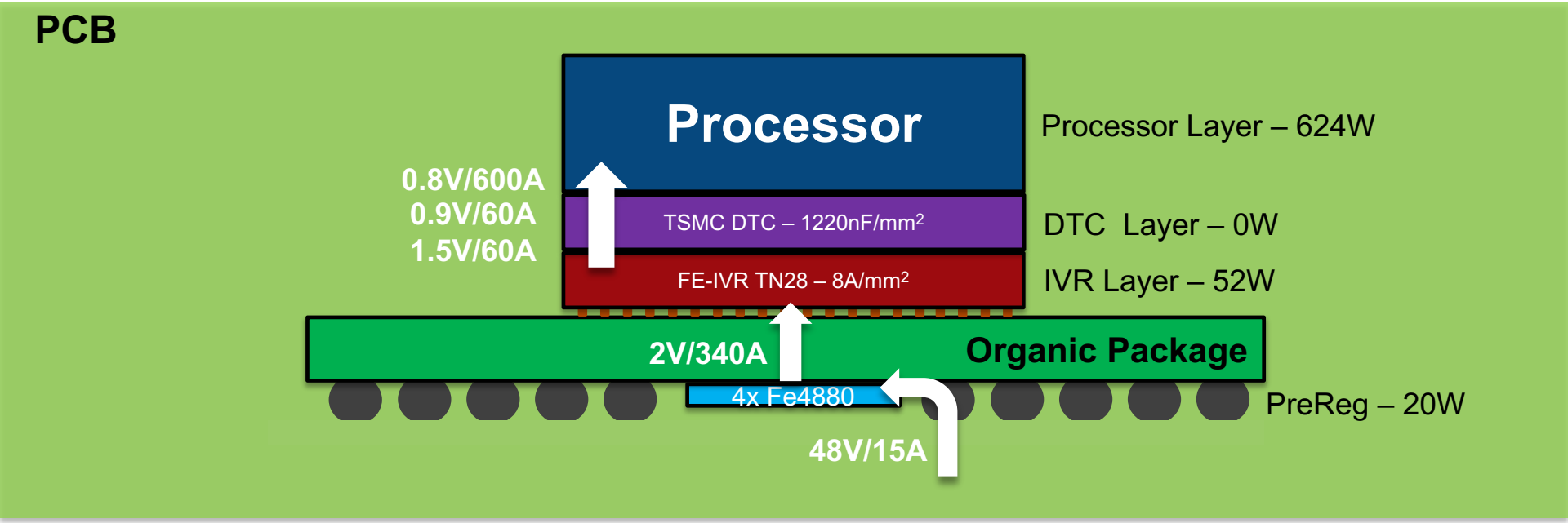
- Package Voltage Regulators reduce power supply current at Package-to-board interface by ~3x, allowing:

  ~2x higher signal bandwidth or ~40% reduction in pin count

- New bottlenecks for in-package power delivery must be avoided
- Power & Data bottlenecks can still occur at chip-to-package interface



Stacked IVR | Example Datacenter Solution

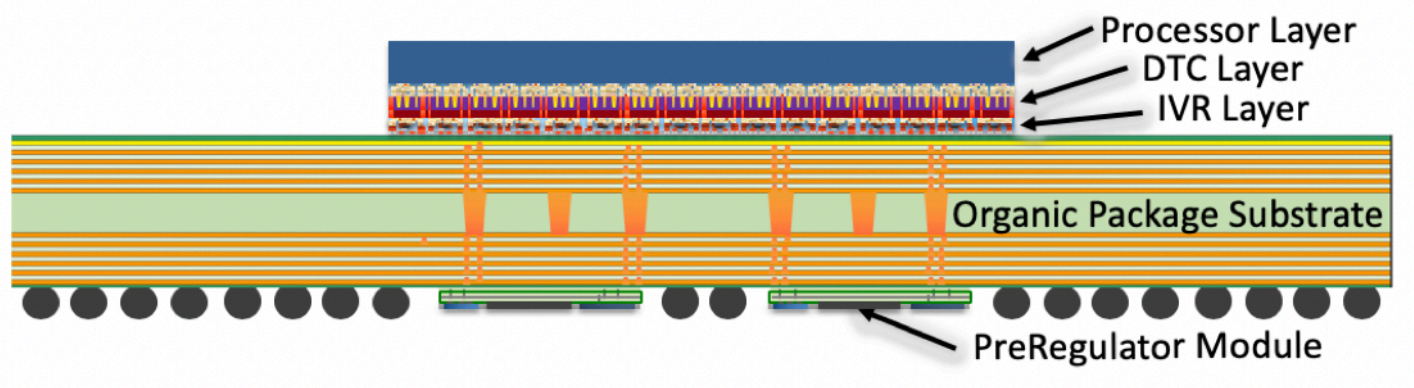


Supply	Converter	Converter Count	Converter Area (mm2)	Decap Area (mm2)	Decap (uF)	Voltage Ripple (mV)	ASIC Supply	Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Total Eff. %	Power Dissipated (W)
1	FE-IVR TN28	1 Chip	75	45	54.9	<1	VDDC	2	260.9	521.7	0.8	600	480	92%	41.7
2			7.5	4.5	5.5	<1	AUX A	2	29.3	58.7	0.9	60	54	92%	4.7
3			7.5	4.5	5.5	<1	AUX B	2	47.9	95.7	1.5	60	90	94%	5.7
SUBTOTAL			90	54	65.9				338.1	676.2		720.0	624.0		52.2
INT	FE4880	4 Modules	480	N/A	N/A	<20	PVDD_PVR	48	14.5	697.1	2	338.1	676.2	97%	20.9
TOTAL								48	14.5	697.1			624.0	89.5%	73.1

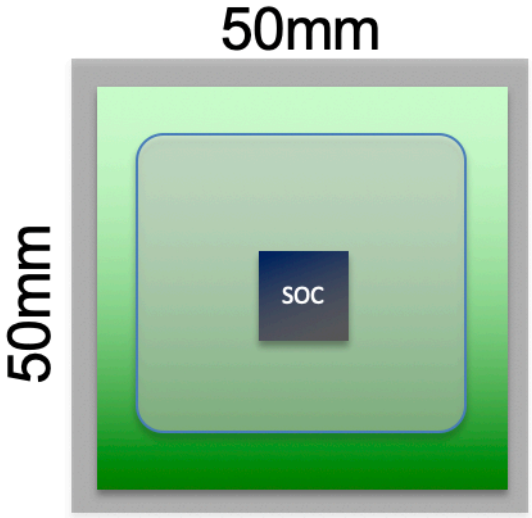
*assume IVR junction temperature is 85C, otherwise ambient temperature of 75C

Stacked IVR | Datacenter Solution - Package

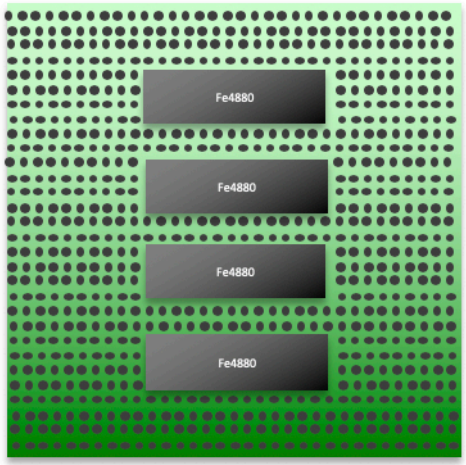
Cross Sectional View



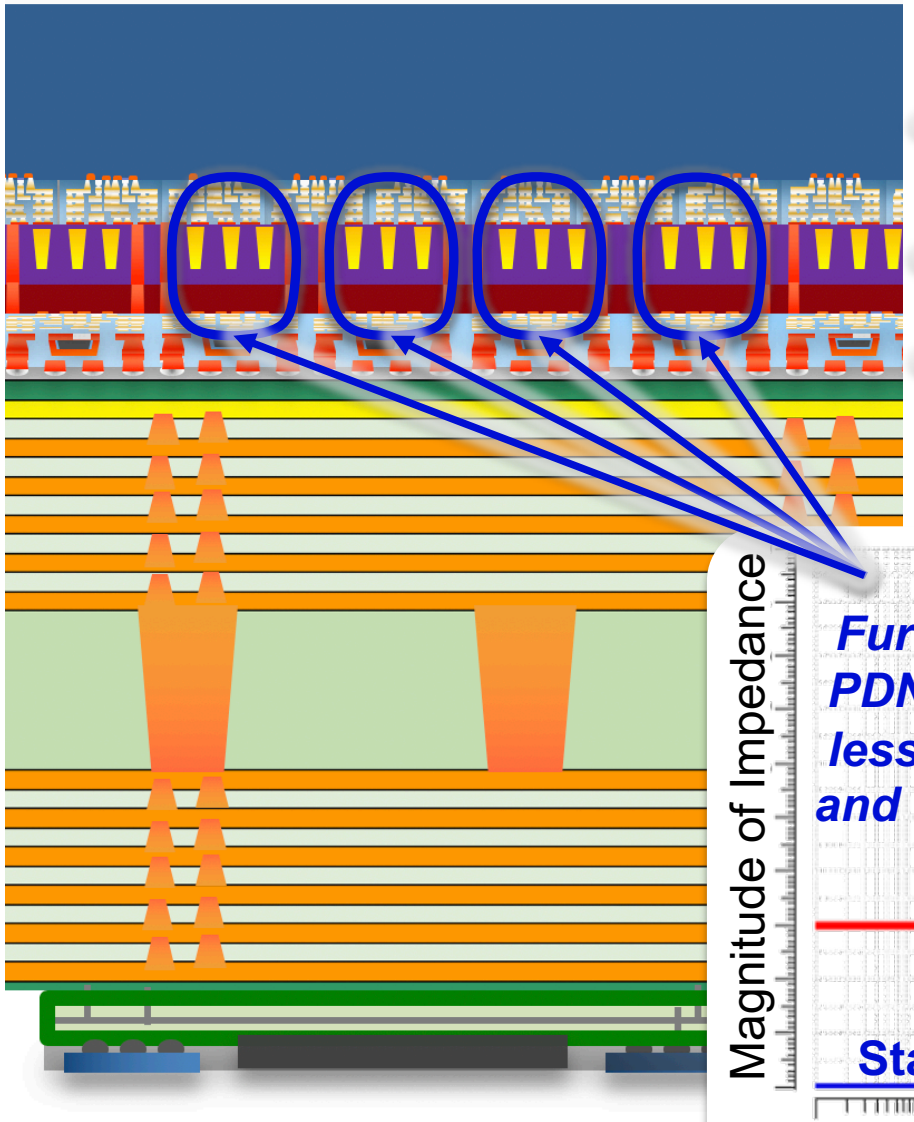
Top View



Bottom View



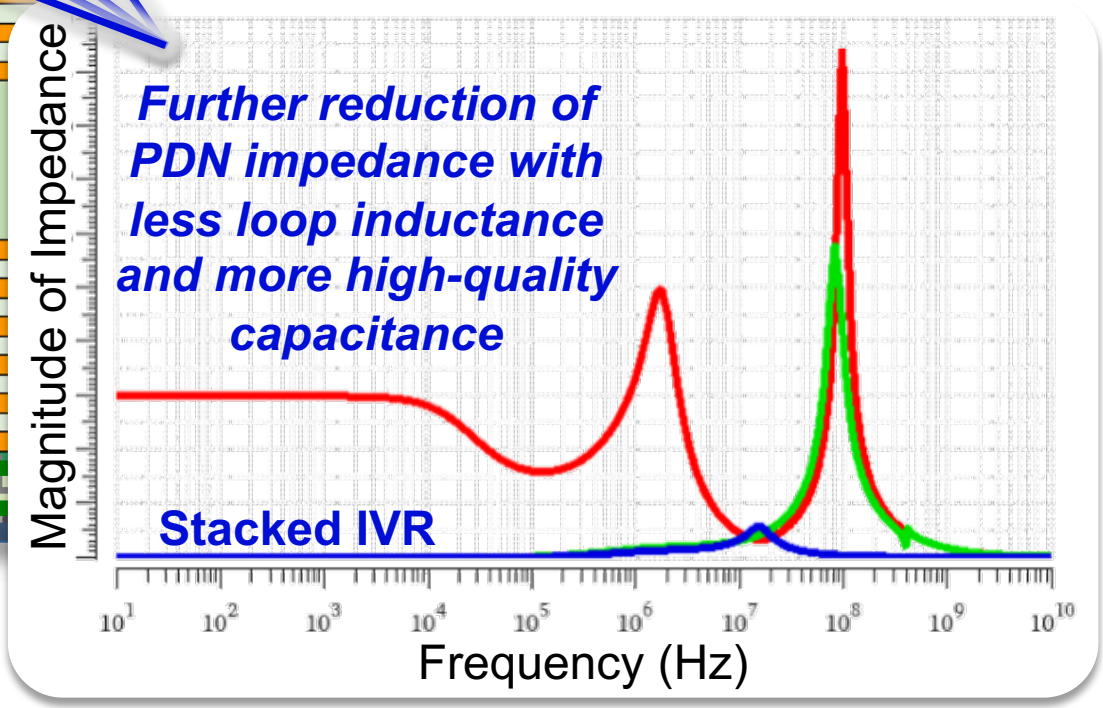
Stacked IVR | Datacenter Solution – Cross Section

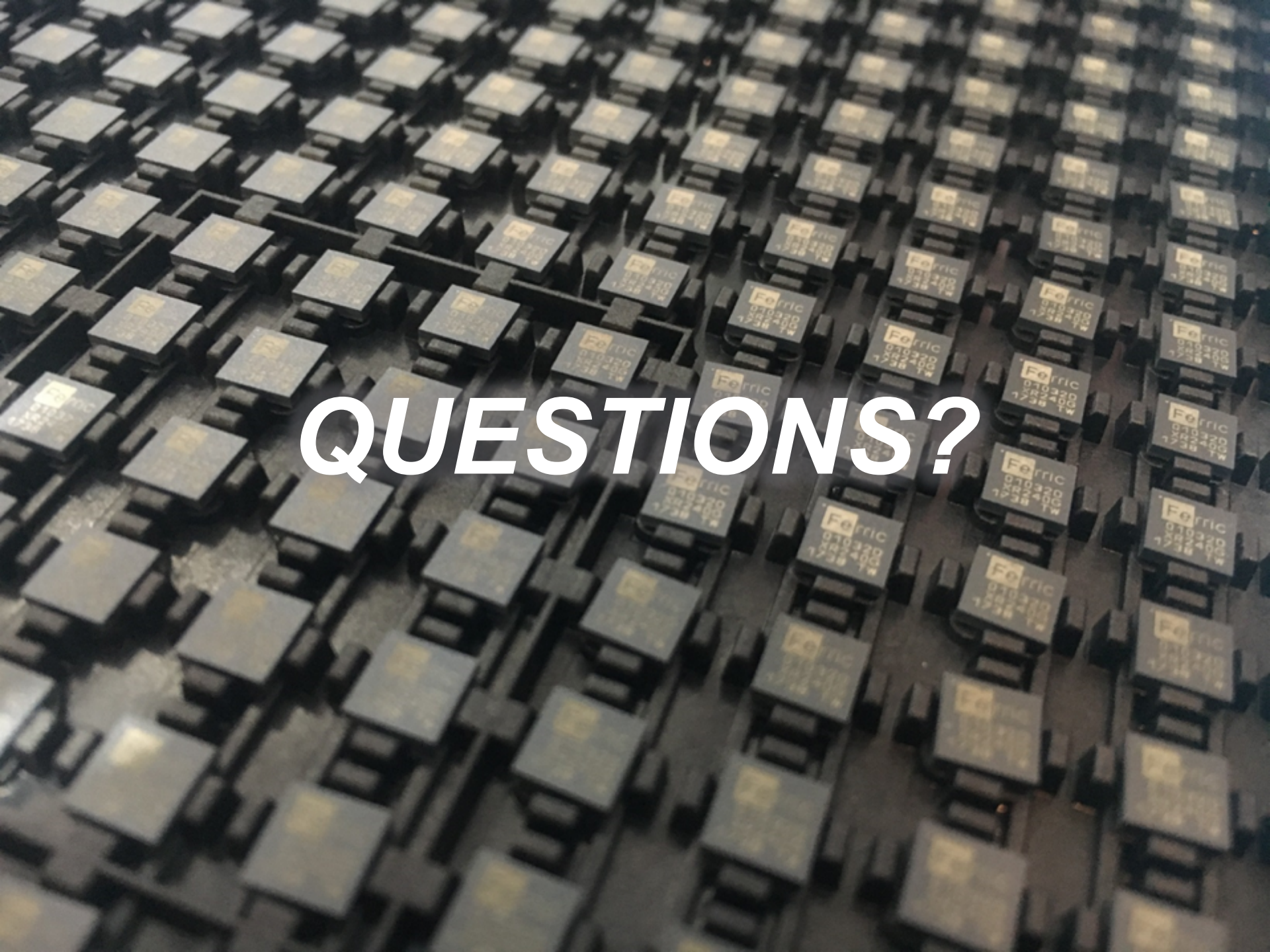


← Processor Layer – N7,N5,N3, etc.

← DTC Layer – TSMC 1220 DTC

← IVR Layer
– TSMC 28HPC+ w/ Ferric-2




QUESTIONS?