

Low profile & Multi-term Silicon Capacitors

PowerSoc 2018

Murata Integrated Passive Solutions
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- MIS introduction & PICS technology
- Trends & Roadmap Low profile & Low-ESL
- Murata Multi-term Silicon capacitors
- ESL of multi-term Silicon capacitors
- Summary

Company name



Murata Integrated Passive Solutions S.A.



Murata Integrated Passive Solutions



- Part of Murata since October 2016
- Murata Integrated Passives division
- Manufacturing, R&D and Innovation center

Europe (14) The Netherlands

- | | |
|------------|------------------|
| Finland ▲● | Spain |
| France ▲● | Switzerland |
| Germany | United Kingdom ● |
| Hungary | |
| Italy | |

Americas (11) United States

- | | |
|----|--------|
| ▲● | |
| ● | Brazil |
| ● | Canada |
| | Mexico |

Japan (31) ▲●

Greater China (29) ▲●

Asia and others (15)

- | | |
|---|------------------|
| ▲ | <u>Singapore</u> |
| | India |
| ▲ | Malaysia |
| ▲ | Philippines |
| ▲ | Thailand |
| | Vietnam |

**(No of companies)
Regional Head Offices**

- | | |
|---|-------------------|
| ▲ | Production plants |
| ● | R&D Centers |

*Murata Manufacturing Co., Ltd. is not included in the number of subsidiaries



MIS introduction
PICS technology

What is Silicon capacitor?

➤ Key Feature

500 nF/mm²

Miniaturization
No cap degradation



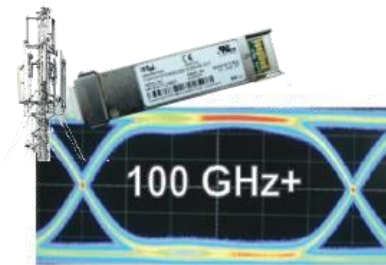
80 μm

Ultra low profile



Up to 100 GHz

Broadband performance
Ultra low insertion loss

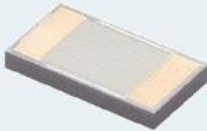
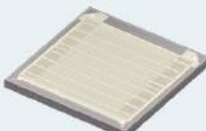
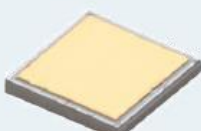
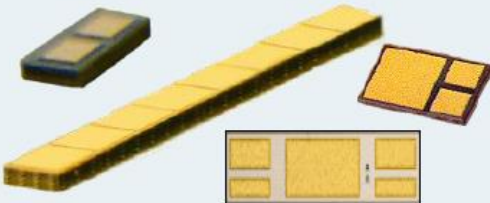
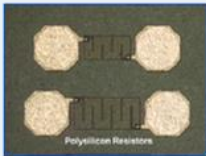


Up to 250°C

High Reliability
Stable Life

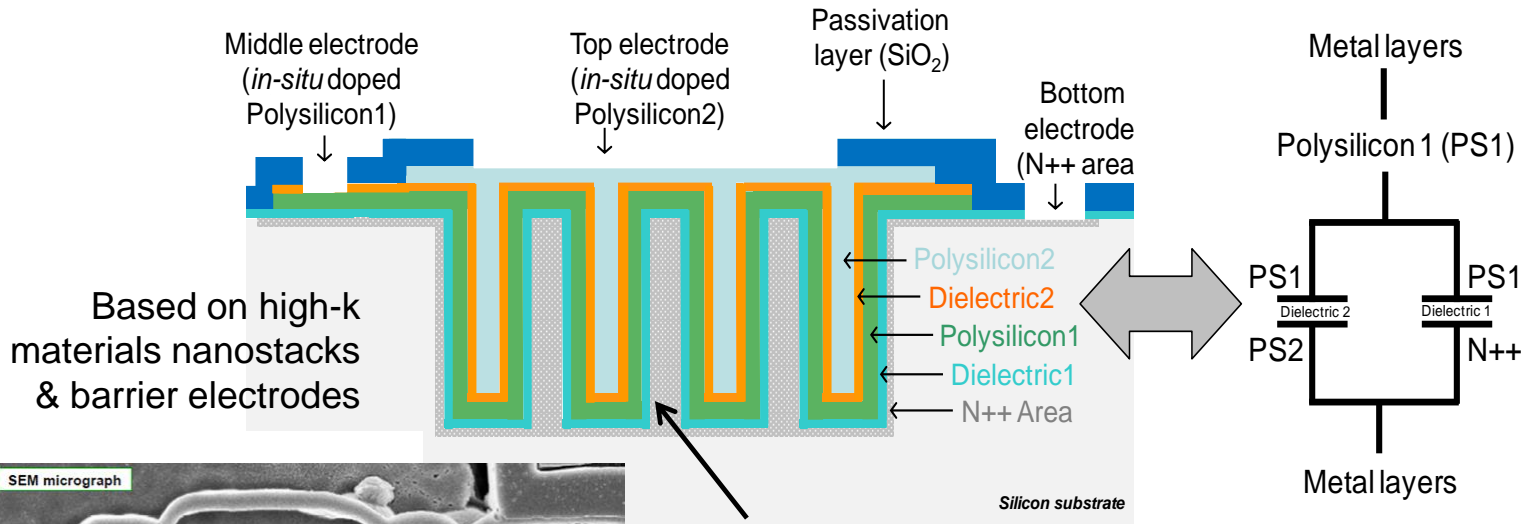


➤ Si Capacitor - Product Type

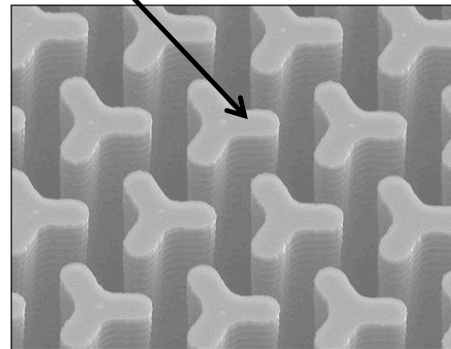
Off-the-Shelf			Customized Solution	
Solder mounting	Wire-bonding / Embedded	Wire-bonding	Capacitor Array Binary Capacitor	IPD (Integrated Passive Device)
				
2 terminal	4 terminal	Vertical		Capacitor + Resistor

3D structure

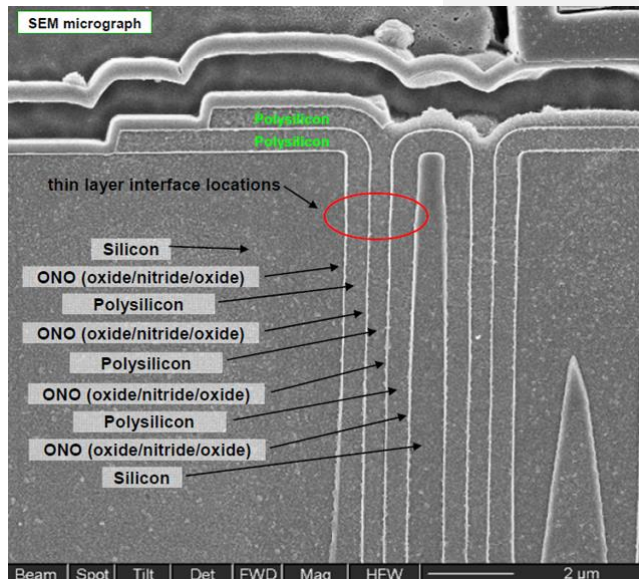
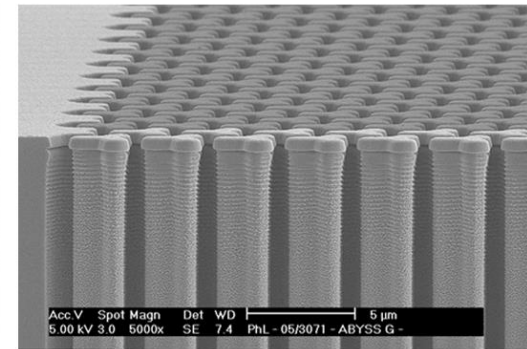
2 parallelized capacitors in a MIMIM architecture to increase the capacitance value



Tripod

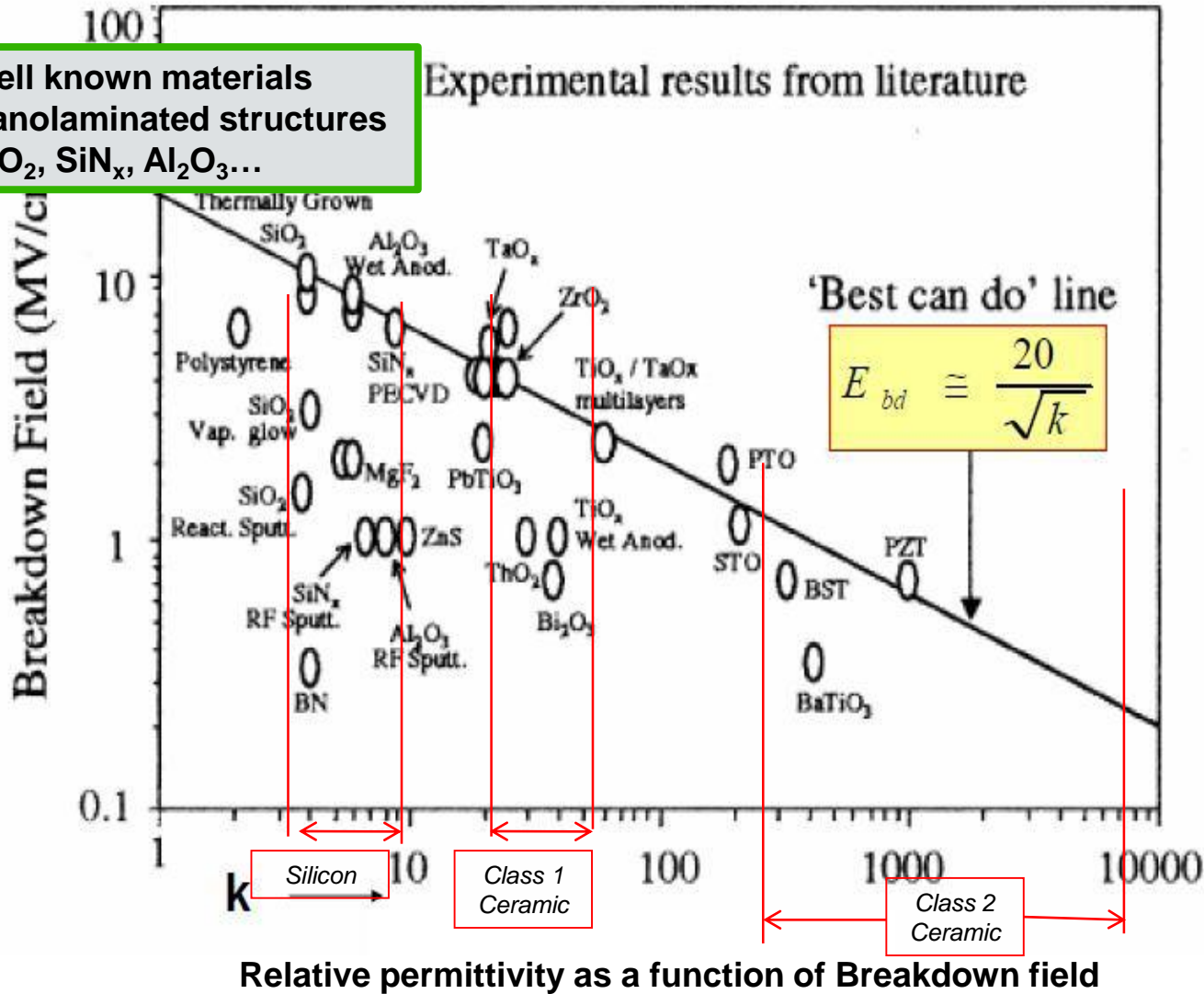


Tilted SEM view



Dielectric materials

Well known materials
Nanolaminated structures
SiO₂, SiN_x, Al₂O₃...

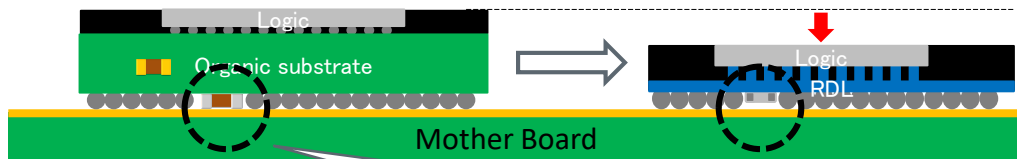




Trends & Roadmap
Low profile & Low-ESL

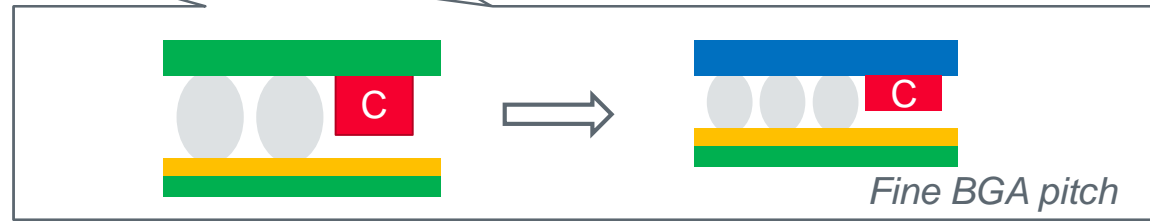
Trends of IC package & Package capacitor

Thickness



FOWLP / FOPLP

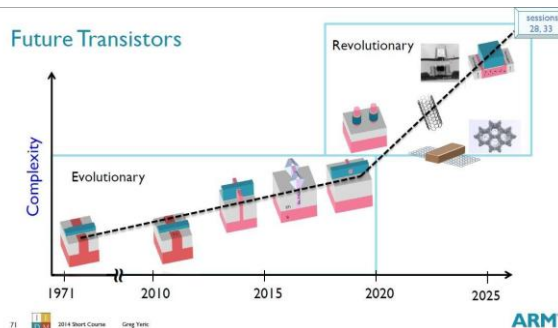
- Fine L/S (→ Fine BGA pitch)
- Low profile



Low profile capacitor is needed

ESL

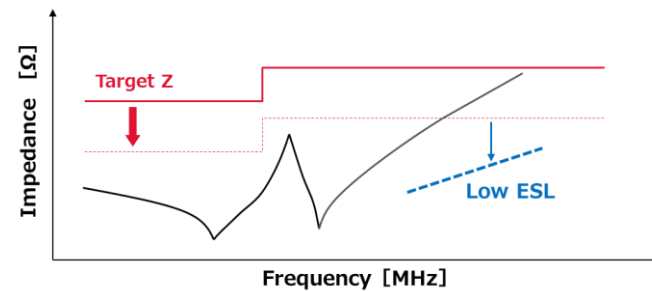
Microfabrication of process



10 nm → 7 nm → 5 nm...



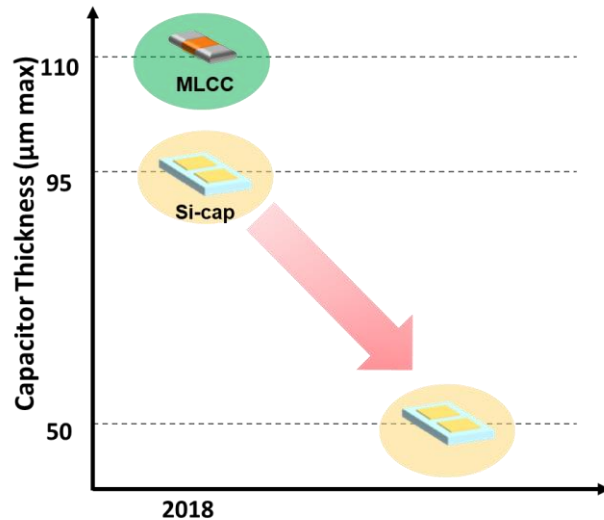
Lower target impedance



Low ESL capacitor is needed

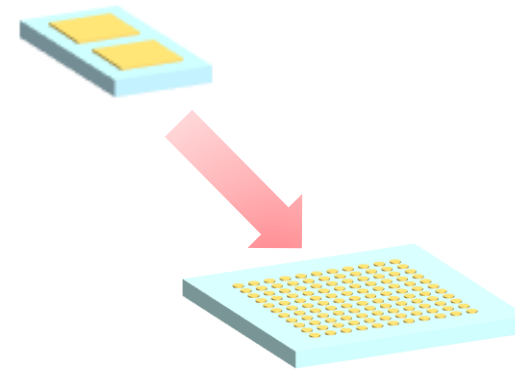
Advantage of Silicon Capacitor

● Low profile



- Achieve low thickness (~ 50 µm)
- Higher robustness

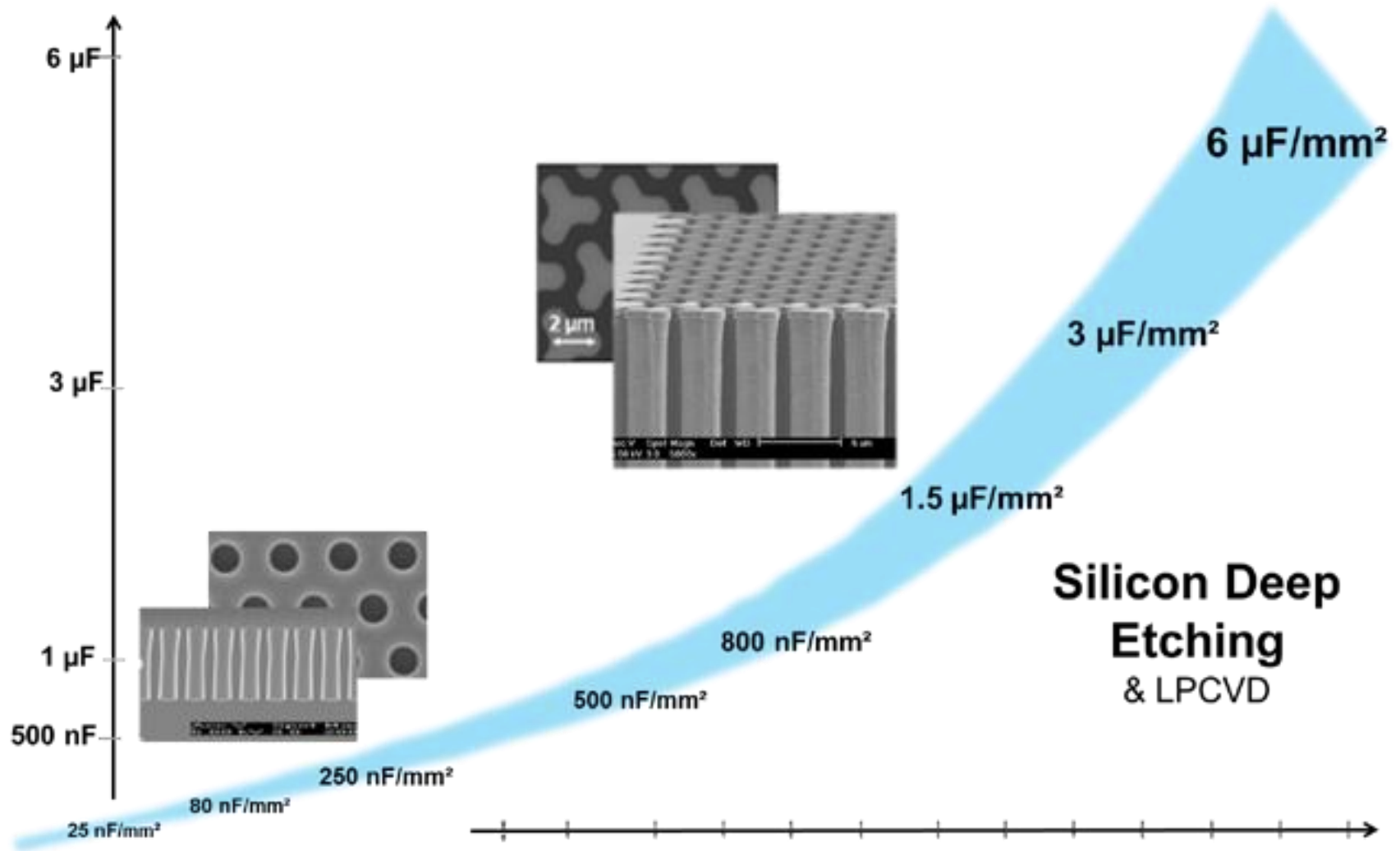
● Multi-terminal



- Design many terminals on capacitor
Extremely low ESL < 10pH

Silicon capacitor is good answer for PKG capacitor!

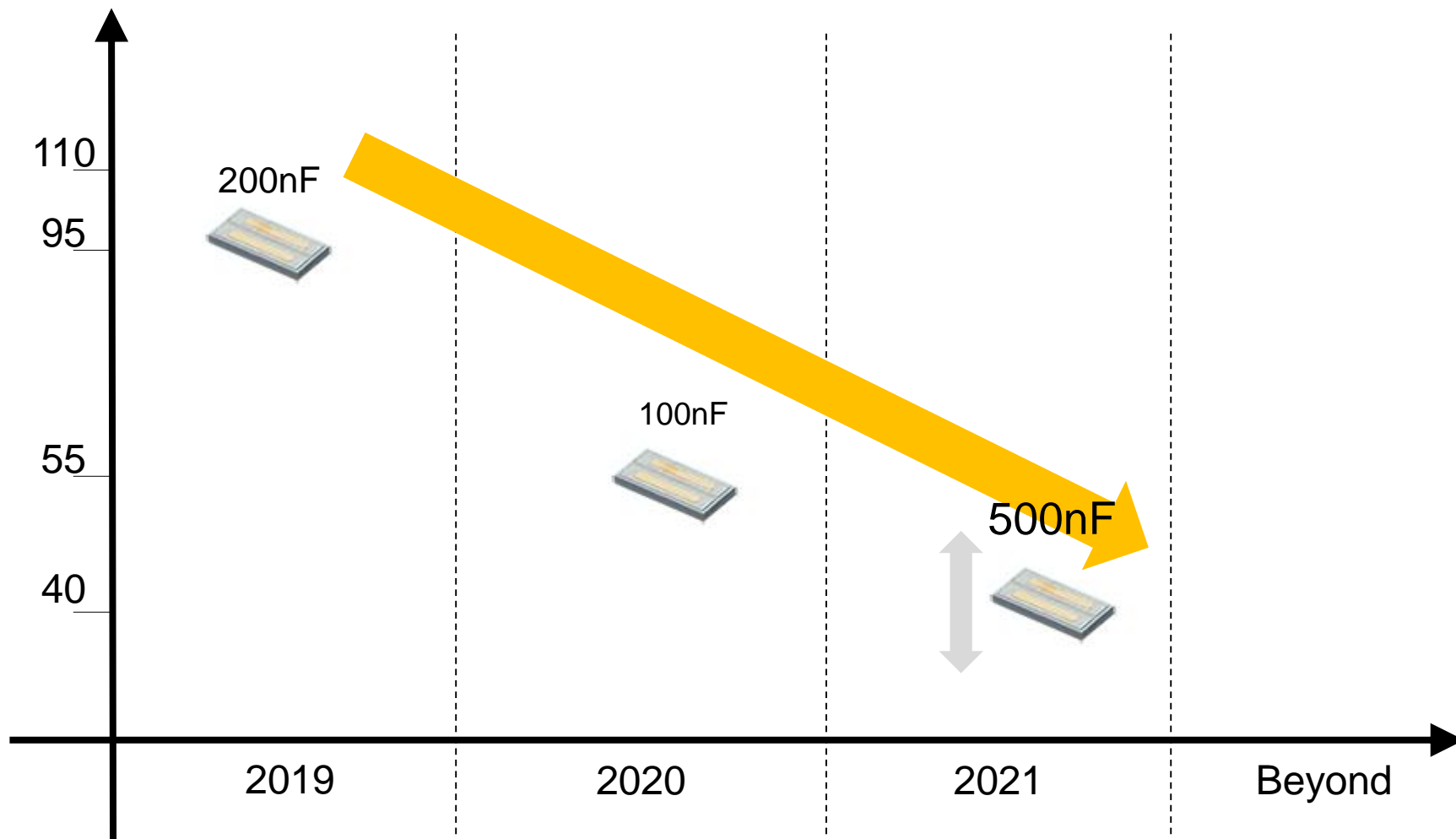
Low voltage technology roadmap



UESL Capacitor Roadmap

Max thickness
(μm)

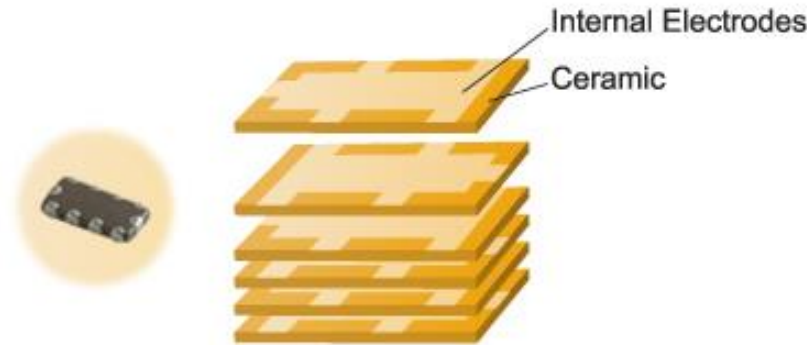
0204 form factor





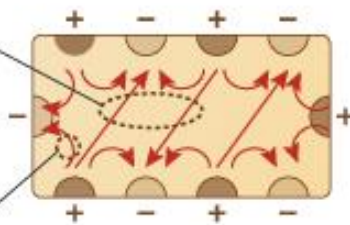
Murata Multi-term
Silicon capacitors

Murata Multi-term MLCC capacitor



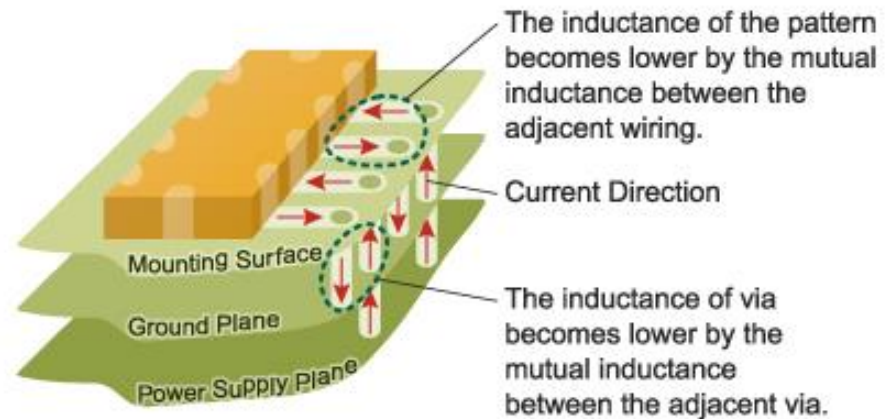
<Example of Structure>

Since the current is the reverse direction, the ESL becomes lower with mutual inductance.



The current flows into the adjacent electrode, which reduces the current loop and lowers the ESL.

Effectiveness of Cancelling Out Inductance by Mutual Inductance



The inductance of the pattern becomes lower by the mutual inductance between the adjacent wiring.

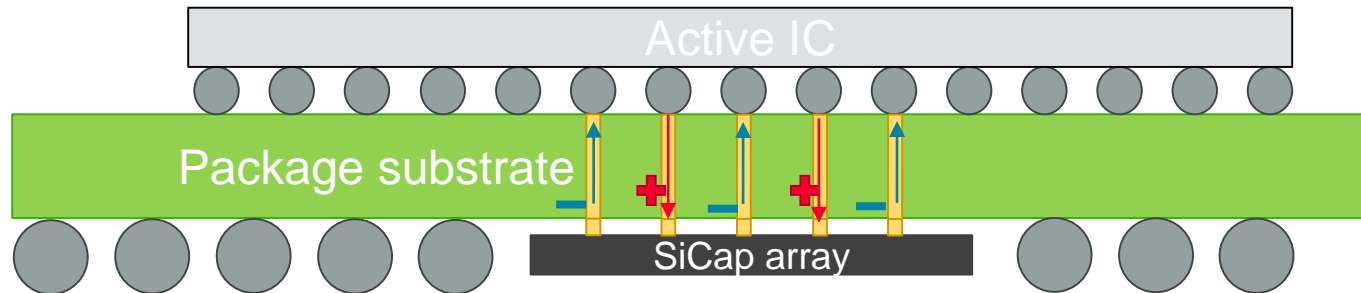
Current Direction

The inductance of via becomes lower by the mutual inductance between the adjacent via.

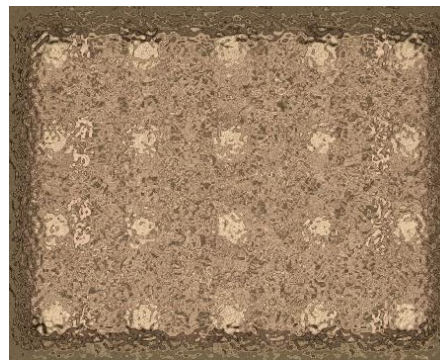
Effectiveness of Suppressing Inductance when Mounting a Multi-terminal Capacitor

The inductance for the boards also becomes lower, not only the capacitor.

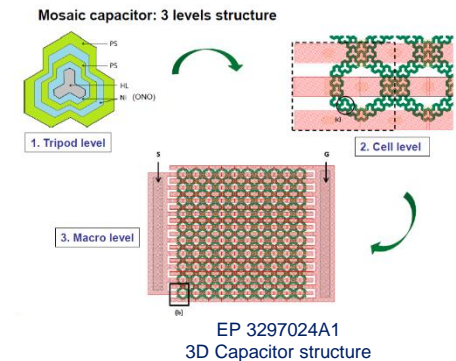
Murata's Multi-term Silicon capacitors



Typical Assembly Schema - Cross section view



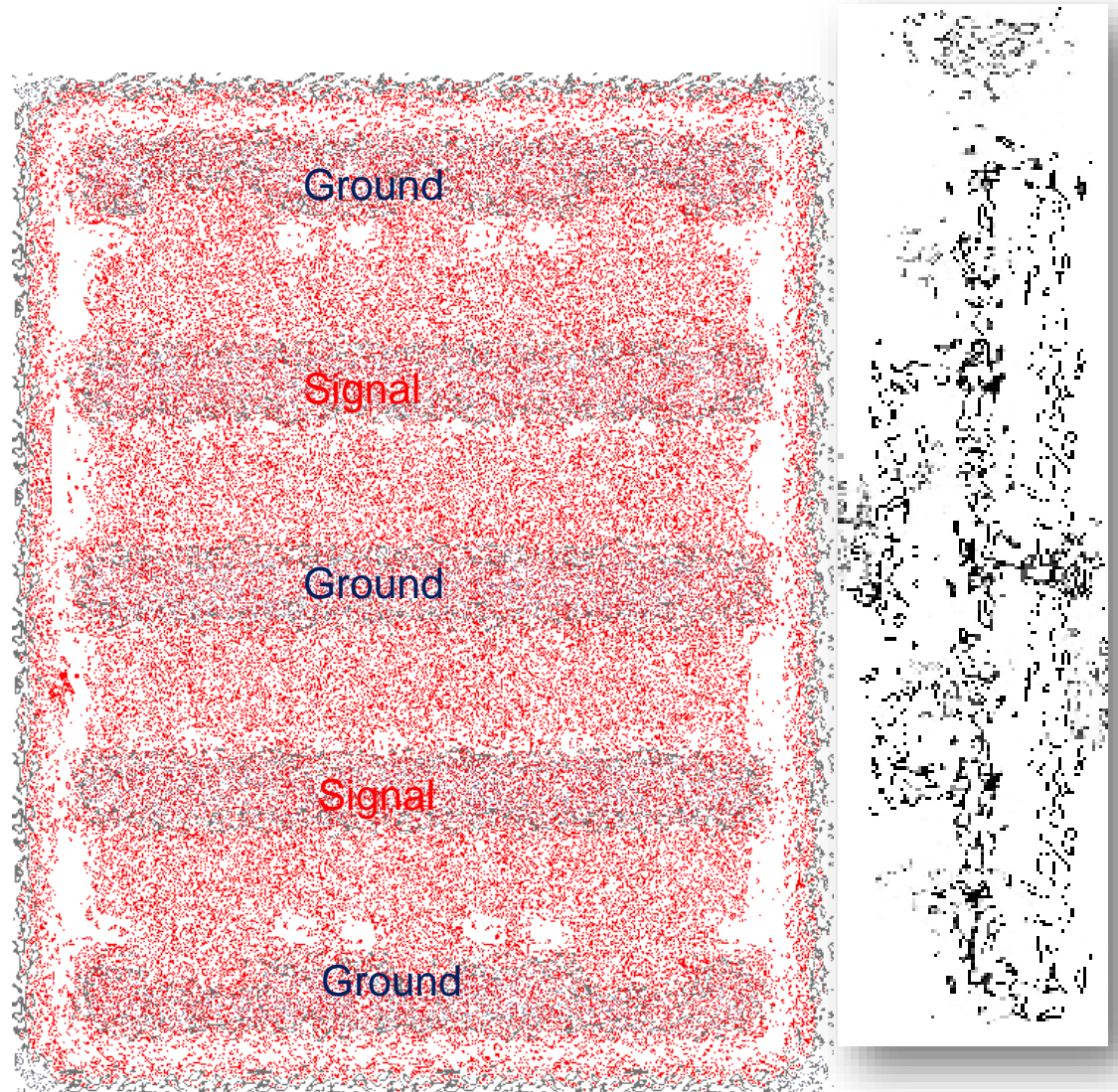
Murata Multi-terminal Si Cap - Top view



- Use of Mosaic Architecture → Lowest obtainable ESL and ESR by internal design
- Preserving the Low ESL and low ESR Through C4 solder bumps in flip-chip attachment → This offers the ultimate in low inductance since it results in many current injection points.
- This reduces the mutual inductance and minimizes the effective path length of the charging current.

Structure overview

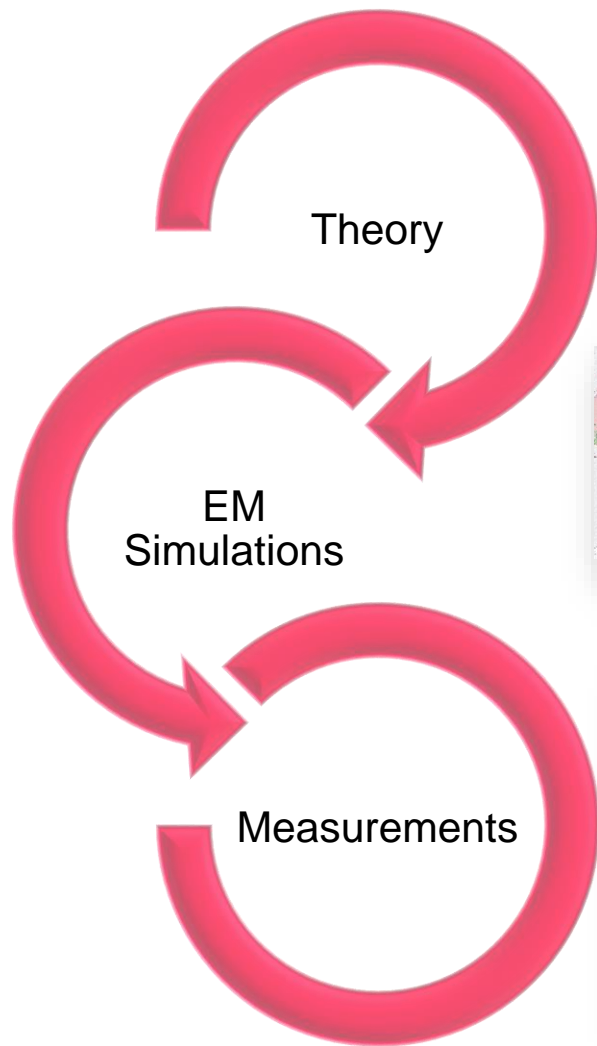
- Current Multi-injection points
 - 2 Signals rows
 - 3 Ground rows
- Many caps in //



ESL of Multi-terminal Silicon capacitors

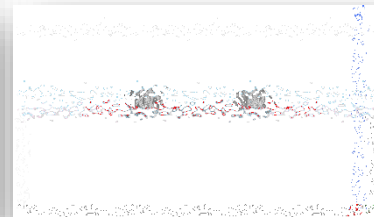
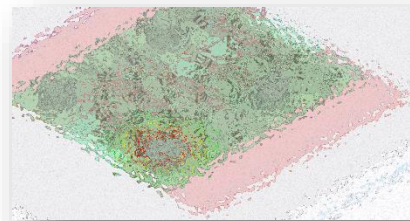
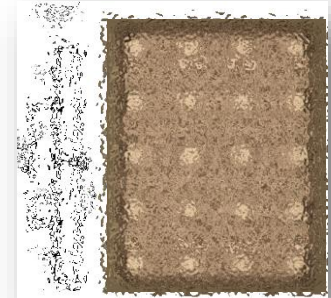


ESL estimation flow

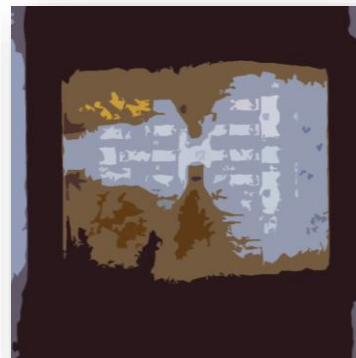


Basic calculation of ESL

$$L = 0.2 \cdot len \cdot \left(\ln \left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$



→ [S] Parameters



C (nF)

L (pH)

Z (Ω)

Measurements

Summary



Silicon Capacitors addressing market trends

- Increased density
- Low thickness



0204 500nF 40um



- Multi-terminals Silicon Capacitors
 - Development on-going
 - ESL computation
 - Comparison Full EM simulation Vs Measurements
 - Generating product [S] param



Thank you!

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