Parallel-Multiple-Output Switched-Capacitor Power Converters

Yan Lu

Assistant Professor, University of Macau

Email: yanlu@umac.mo

Hsinchu, Taiwan, Oct. 19th, 2018

Outline

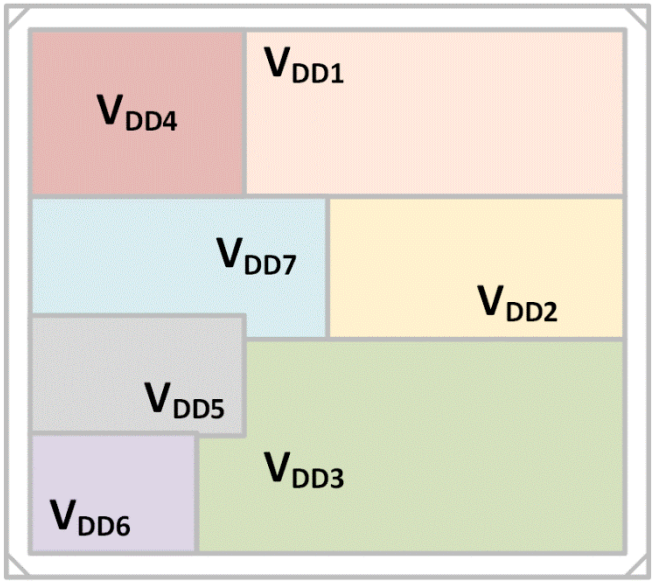
- Motivations
- Review of Prior Multiple Output SC Converters
- A Dual-Symmetrical-Output SC Converter
- Discussions and Conclusions

Outline

- Motivations
- Review of Prior Multiple Output SC Converters
- A Dual-Symmetrical-Output SC Converter
- Discussions and Conclusions

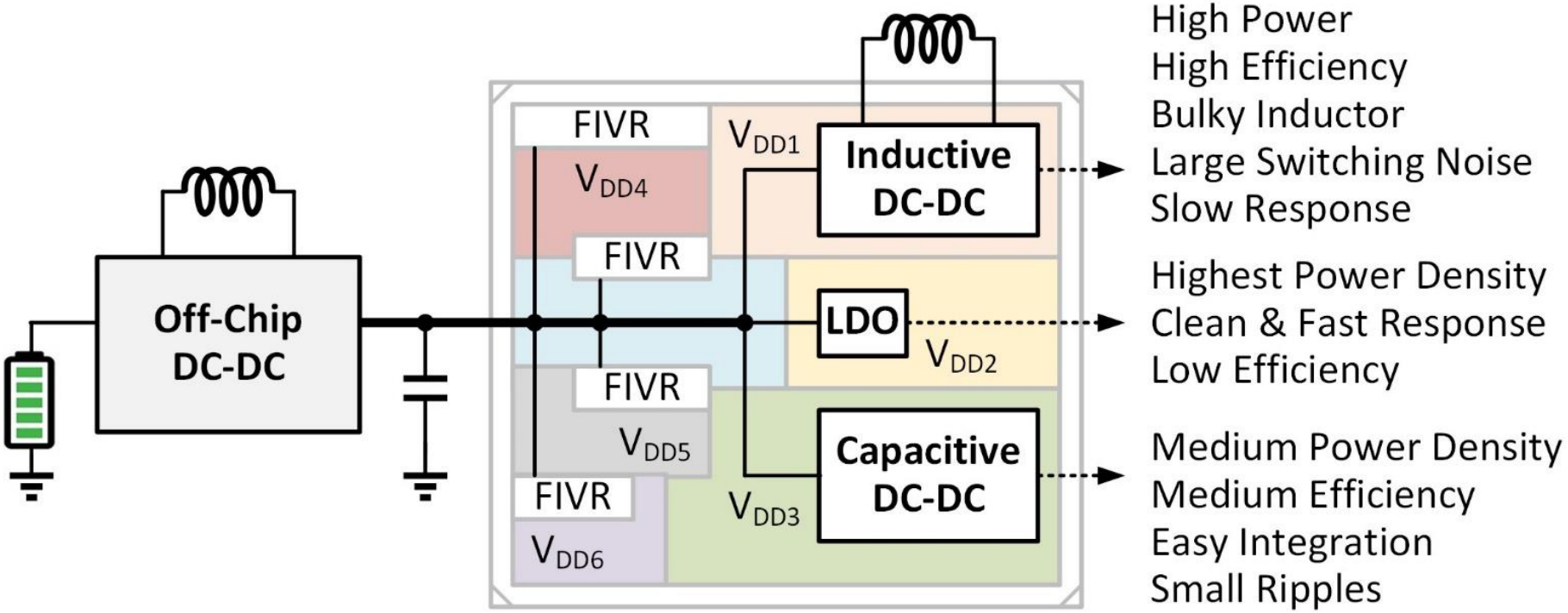
Motivations for Multi-Output PwrSoC

- **Applications**
  - Multi-core processors, per-core DVFS.
  - Granular power for digital systems.
  - Low-power IoT devices.
  - Small-size wearable or medical devices.
- **Benefits**
  - Energy-efficient computing.
  - Reduce number of capacitors.
  - Reduce area overheads.



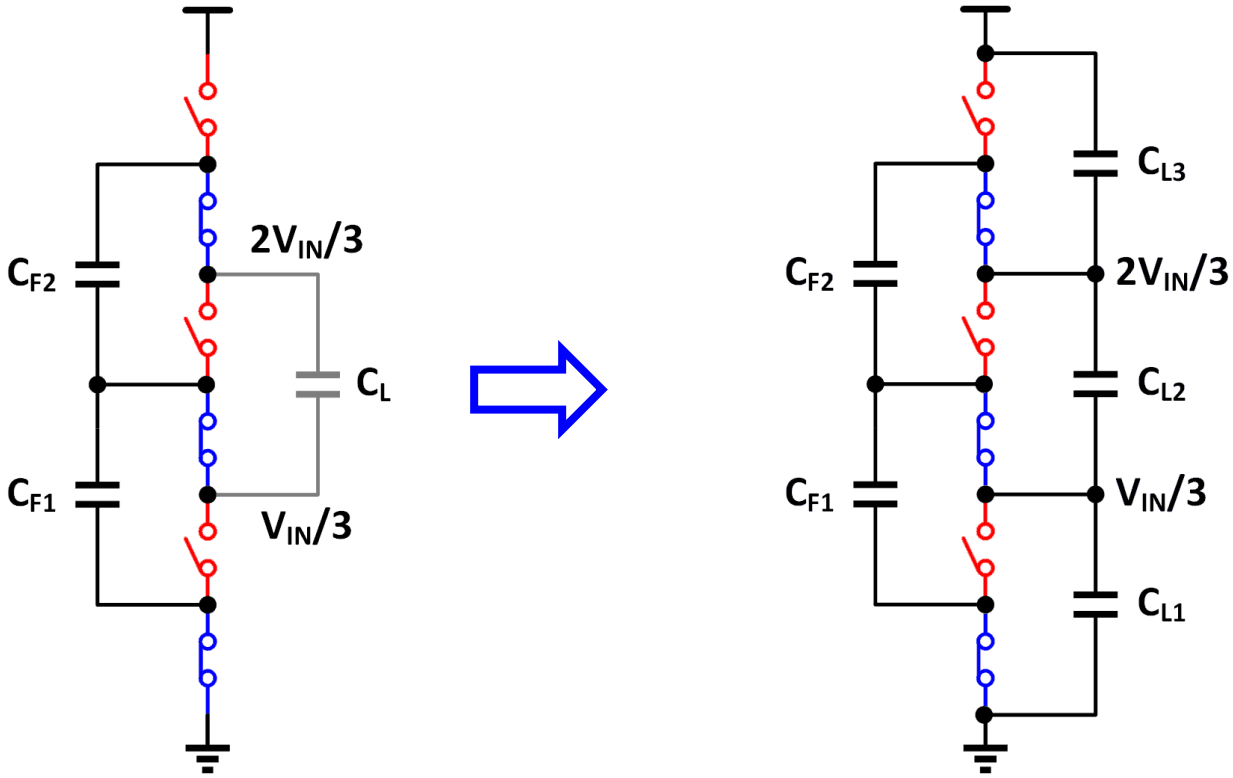
Fully-Integrated Voltage Regulators (FIVRs)

- Three choices.
- Granular power needs FIVRs with small area and fast response.



The Ladder Topology was Born to Have Multiple Outputs

- It can be used for stacked or parallel voltage domains.
- For step-down, the ladder topology is simple and intuitive, with all the capacitor voltages the same.
- For step-up, Dickson & Fibonacci are also friendly to multiple outputs.

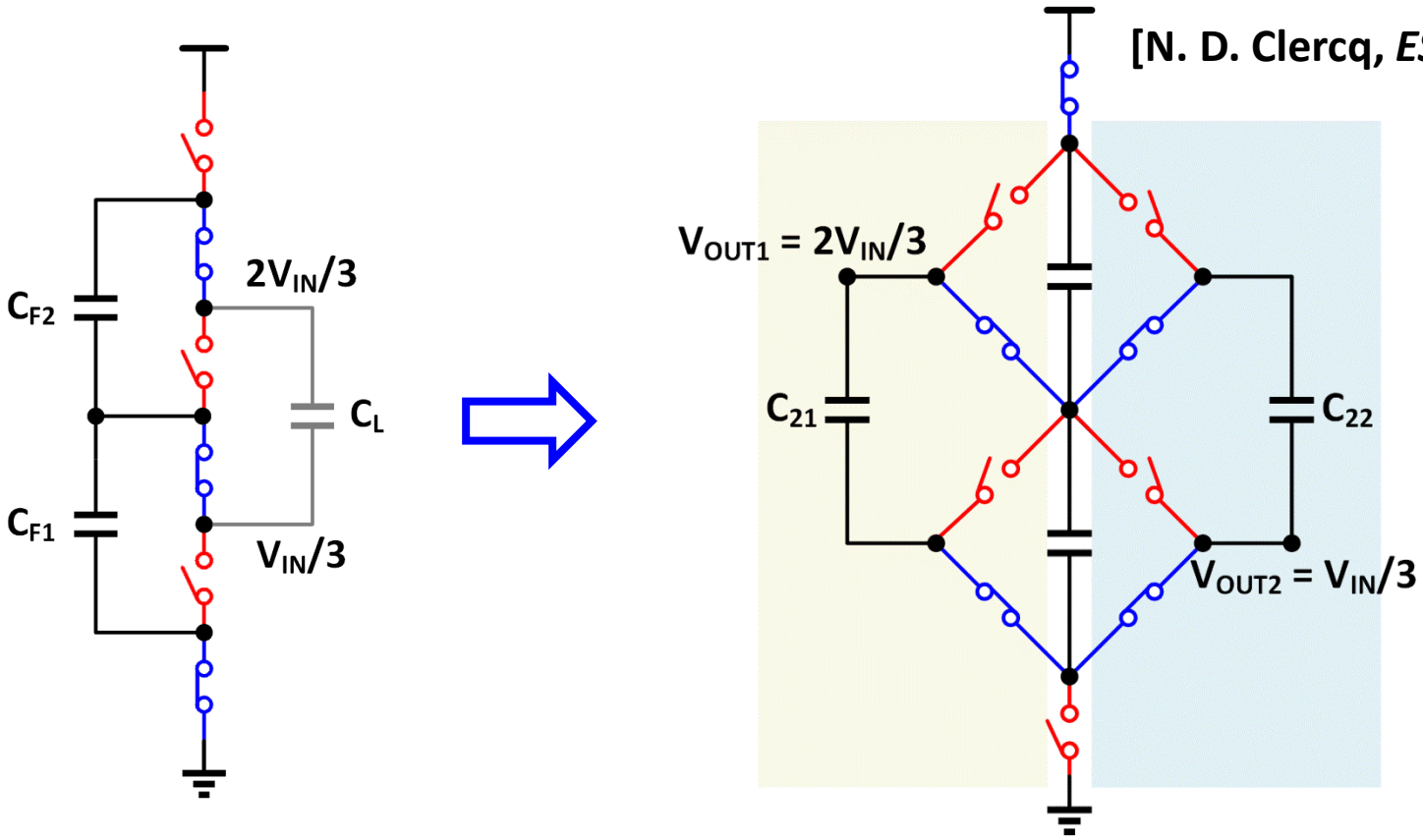


Outline

- Motivations
- Review of Prior Multiple Output SC Converters
- A Dual-Symmetrical-Output SC Converter
- Discussions and Conclusions

Dual-Output with Ladder Topology (1)

- Sharing 2 fly capacitors with time-interleaving operation.
- Results in larger output ripples for both outputs.
- Reduced cross regulation.

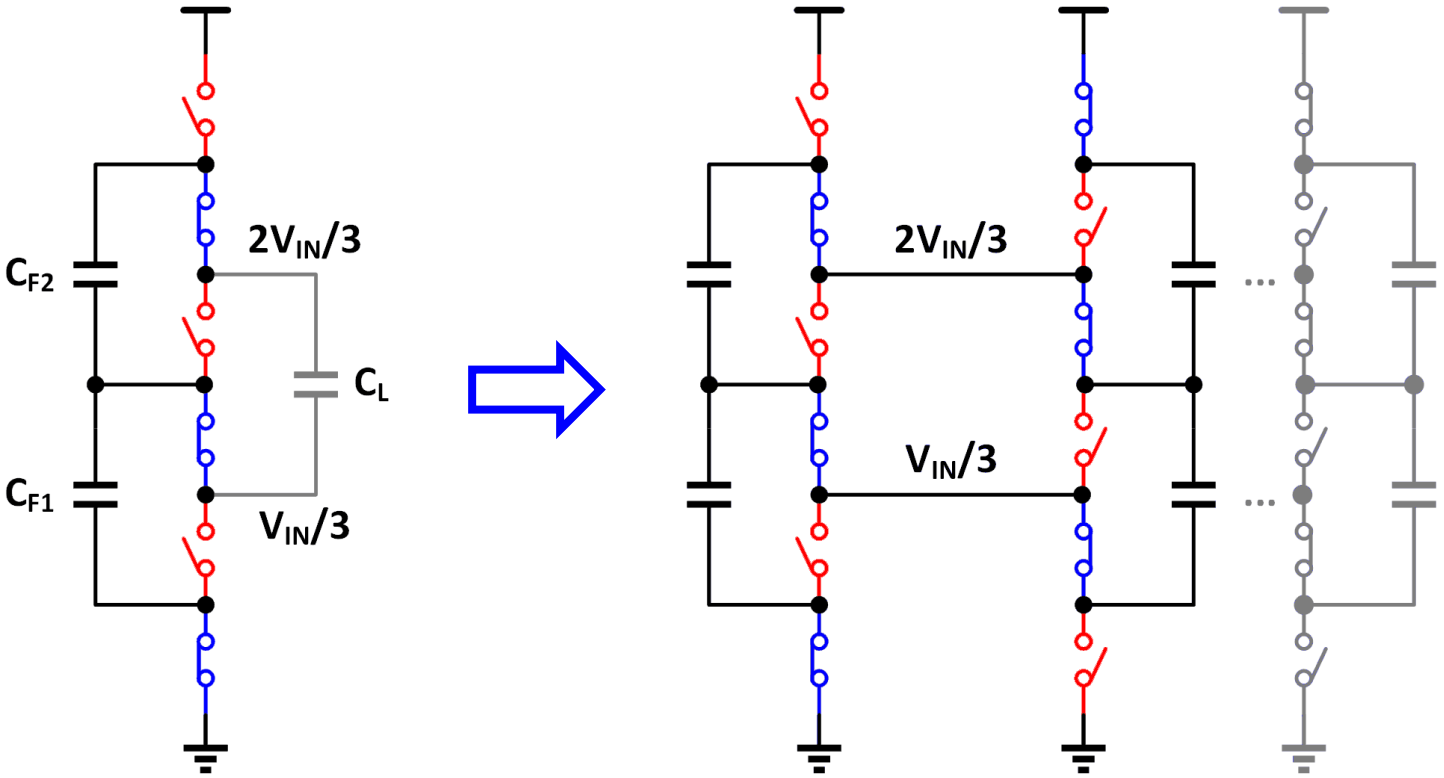


[N. D. Clercq, *ESSCIRC*, 2012]

Dual-Output with Ladder Topology (2)

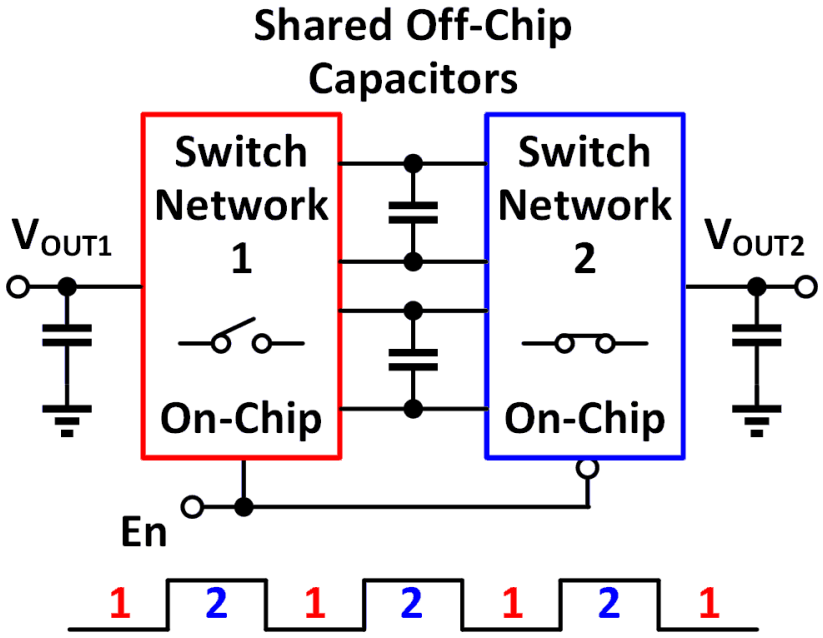
- Fully-on-chip.
- Saving filter capacitors with many interleaving phases.

[Y. Zhao, *ISCAS*, 2014]



Dual-Output with Shared Off-Chip Capacitors

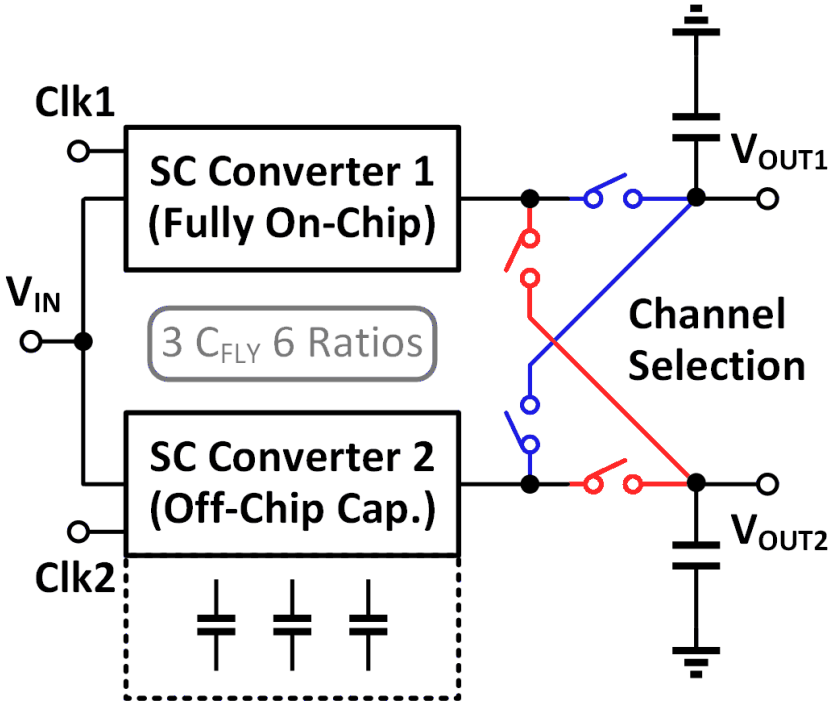
- Shared off-chip fly capacitors, individual on-chip switches.
- Time-interleaving operation.
- $V_{OUT1}=(1/3)\ V_{IN}$, $V_{OUT2}=(2/3)\ V_{IN}$.
- Fly caps have the same voltages for different outputs.

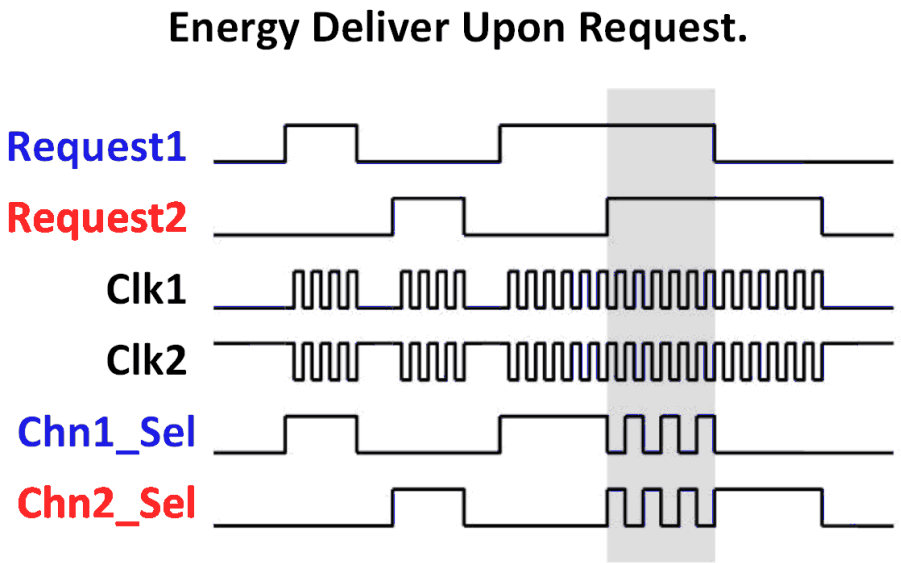


[Z. Safarian, *Electronics Letters*, 2014]

Dual-Output with Two SC Converters

- One fully-integrated converter for light load (1mA).
- One converter with off-chip caps for heavy load (10mA).
- Large output ripple or large load capacitors (10µF).
- Low efficiencies when two outputs need different VCRs.

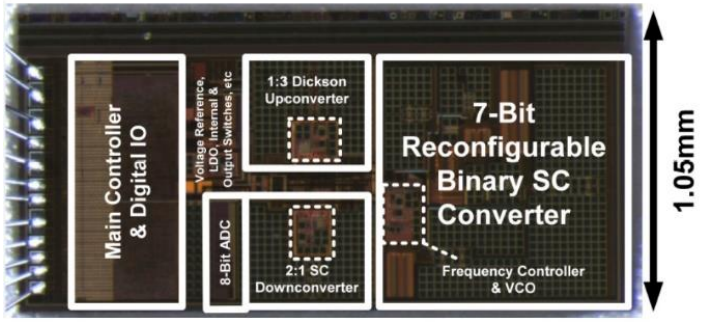




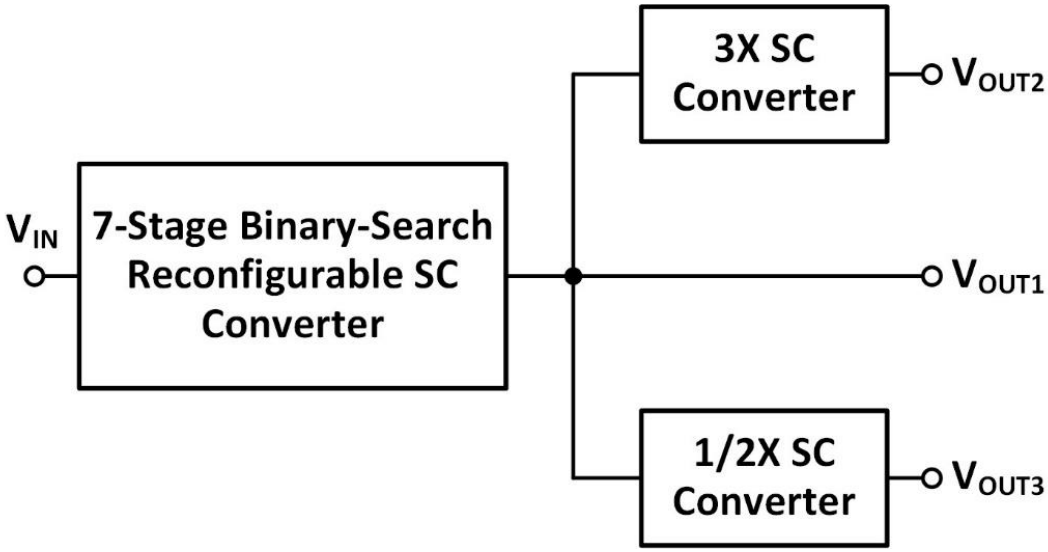
[C. K. Teh, *ISSCC*, 2016]

Tri-Output with Cascade SC Converters

- The 1st stage is a 7-bit binary search reconfigurable SC converter which can provide 127 fine VCRs. But, large area.
- Cascaded 1/2X, 3X SC converters generate step-down and step-up outputs, respectively. Degrade total efficiency (~60%).
- Advantage: fine VCRs for all the three outputs, with only one large-area reconfigurable converter.

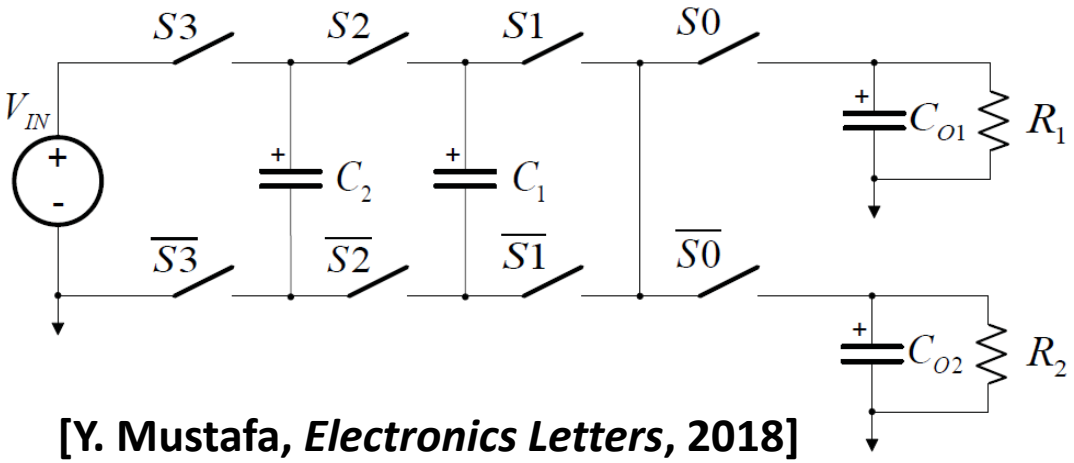


[W. Jung, *ISSCC*, 2016]



Dual-Output with Multiple Topology Phases

- VCRs = 1/2, 1/4, 3/4, with two fly capacitors.
- Two different VCRs with 4 topology phases.
  - one example: {1, 3, 2, 4}
- Output impedances and cross regulation can be reduced with balanced switching (8 topology phases).
  - {3, 2, 4, 2, 3, 1, 5, 1}

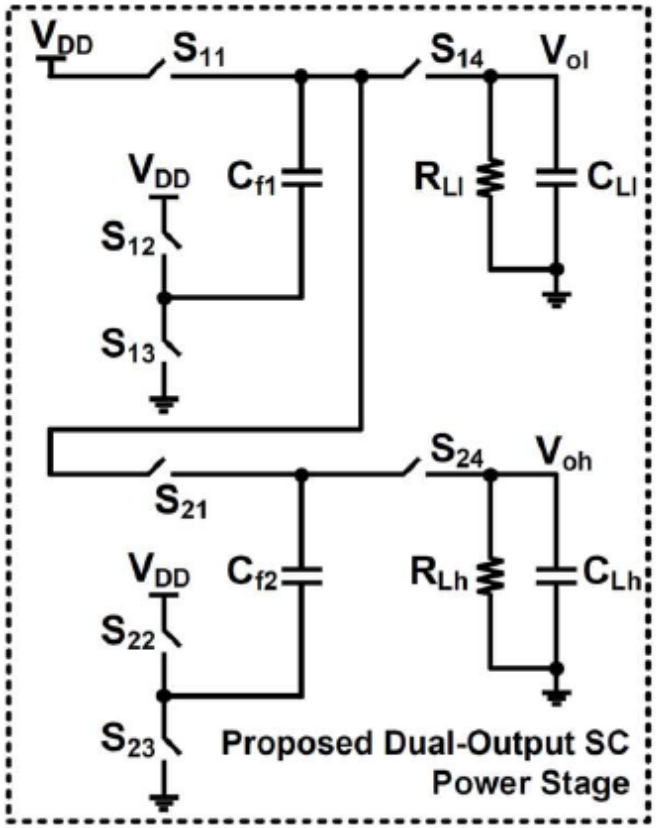


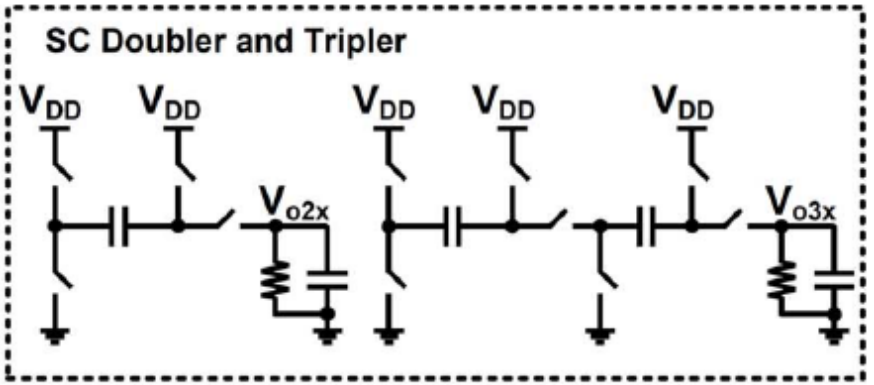
[Y. Mustafa, *Electronics Letters*, 2018]

	Topology	VCR	V_{IN}	C2	C1
ϕ1	1	1/2	0	1	0
ϕ3	2	1/2	1	-1	0
ϕ2	3	1/4	0	0	1
ϕ4	4	1/4	0	1	-1
	5	1/4	1	-1	-1
	6	3/4	0	1	1
	7	3/4	1	-1	1
	8	3/4	1	0	-1

Step-Up Dual-Output with Off-Chip Capacitors

- Saved one off-chip capacitor.
- $V_{OH}=3xV_{IN}$, $V_{OL}=2xV_{IN}$.





	2x SC	3x SC	This work
Number of Power Switches	4	7	8
Number of Flying Cpacitors	1	2	2
Number of Output	1	1	2

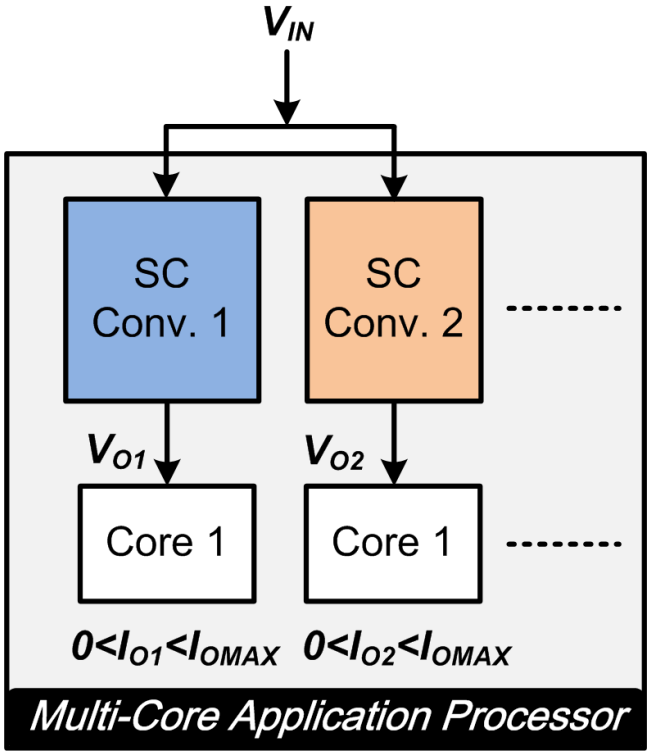
[Z. Hua, *JSSC*, 2015]

Outline

- Motivations
- Review of Prior Multiple Output SC Converters
- A Dual-Symmetrical-Output SC Converter
- Discussions and Conclusions

A Dual-Symmetrical-Output SC Converter

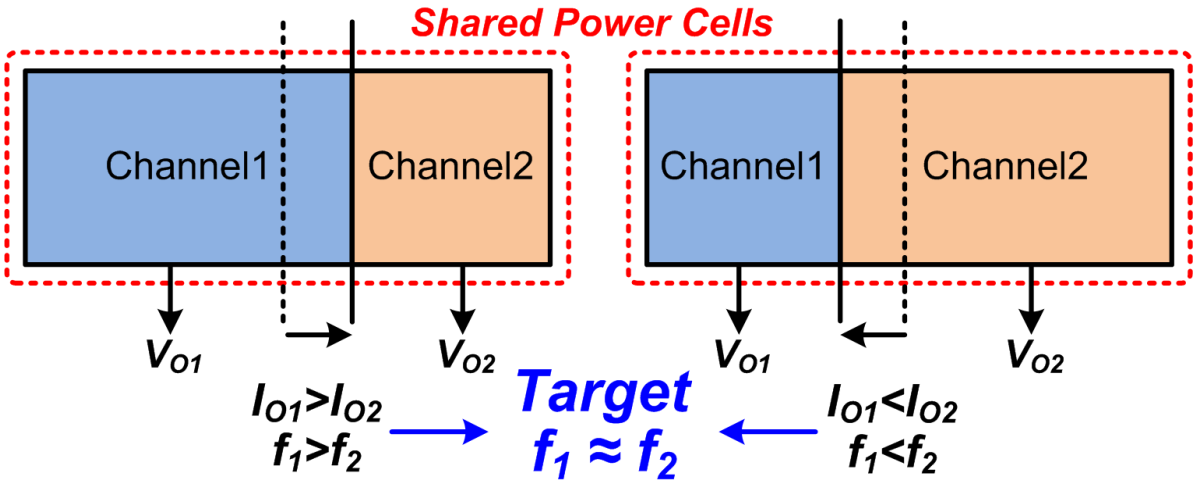
- Individual supply for each core for per-core DVS.
- Each supply requires power and area overheads.

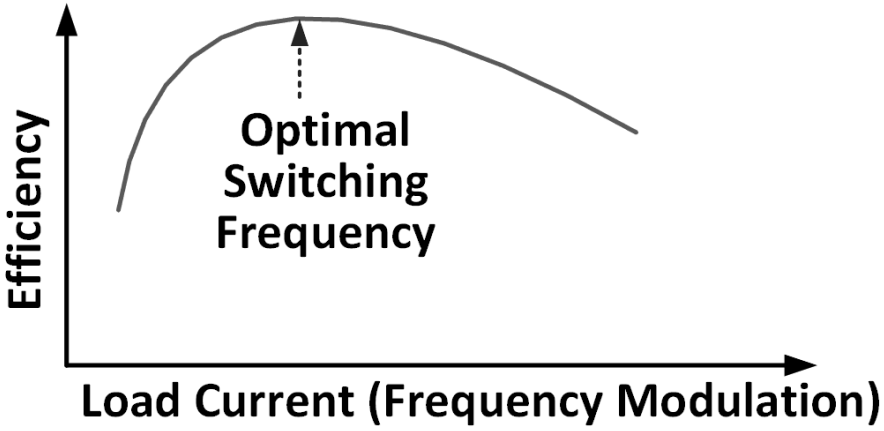


[J. Jiang, *ISSCC*, 2017]

A Dual-Symmetrical-Output SC Converter

- Shared power cells for two SC converters, for reducing the area overheads on each converter.
- Also for a higher total efficiency of the two converters.

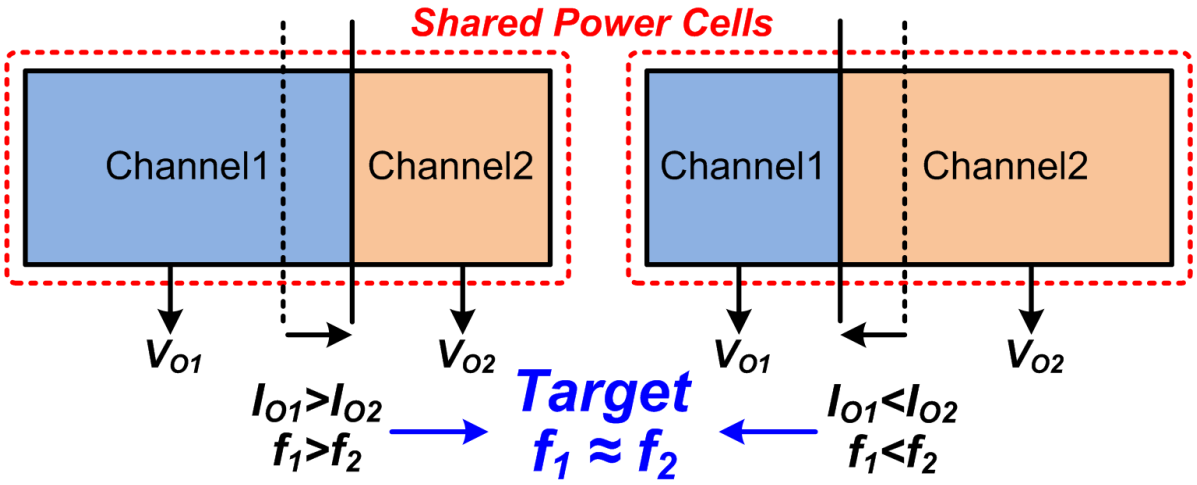


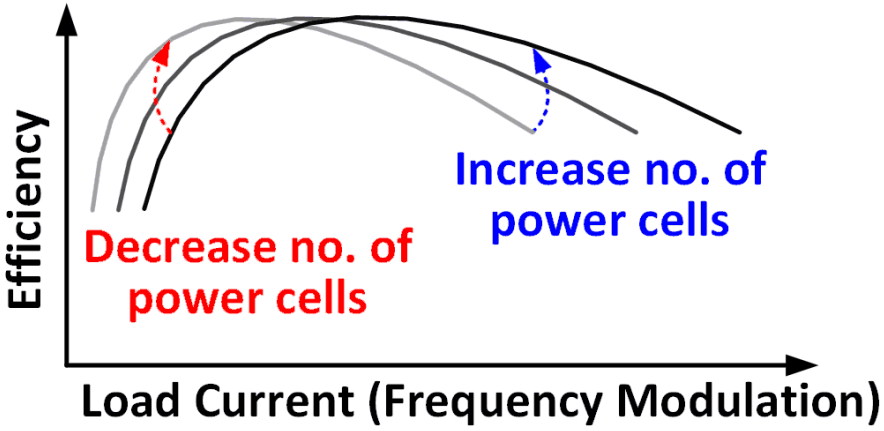


[J. Jiang, *ISSCC*, 2017]

A Dual-Symmetrical-Output SC Converter

- Shared power cells for two SC converters, for reducing the area overheads on each converter.
- Also for a higher total efficiency of the two converters.

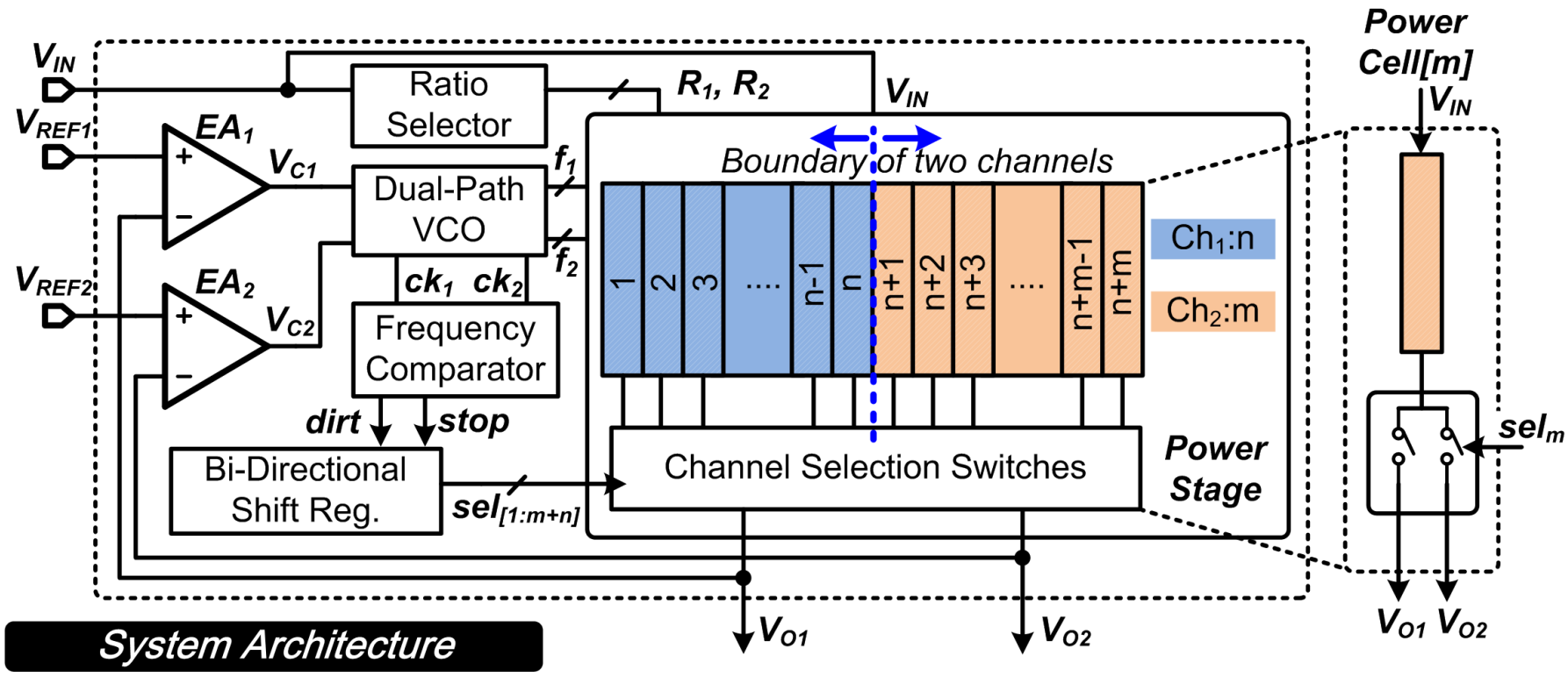




[J. Jiang, *ISSCC*, 2017]

System Architecture of the SC Converter

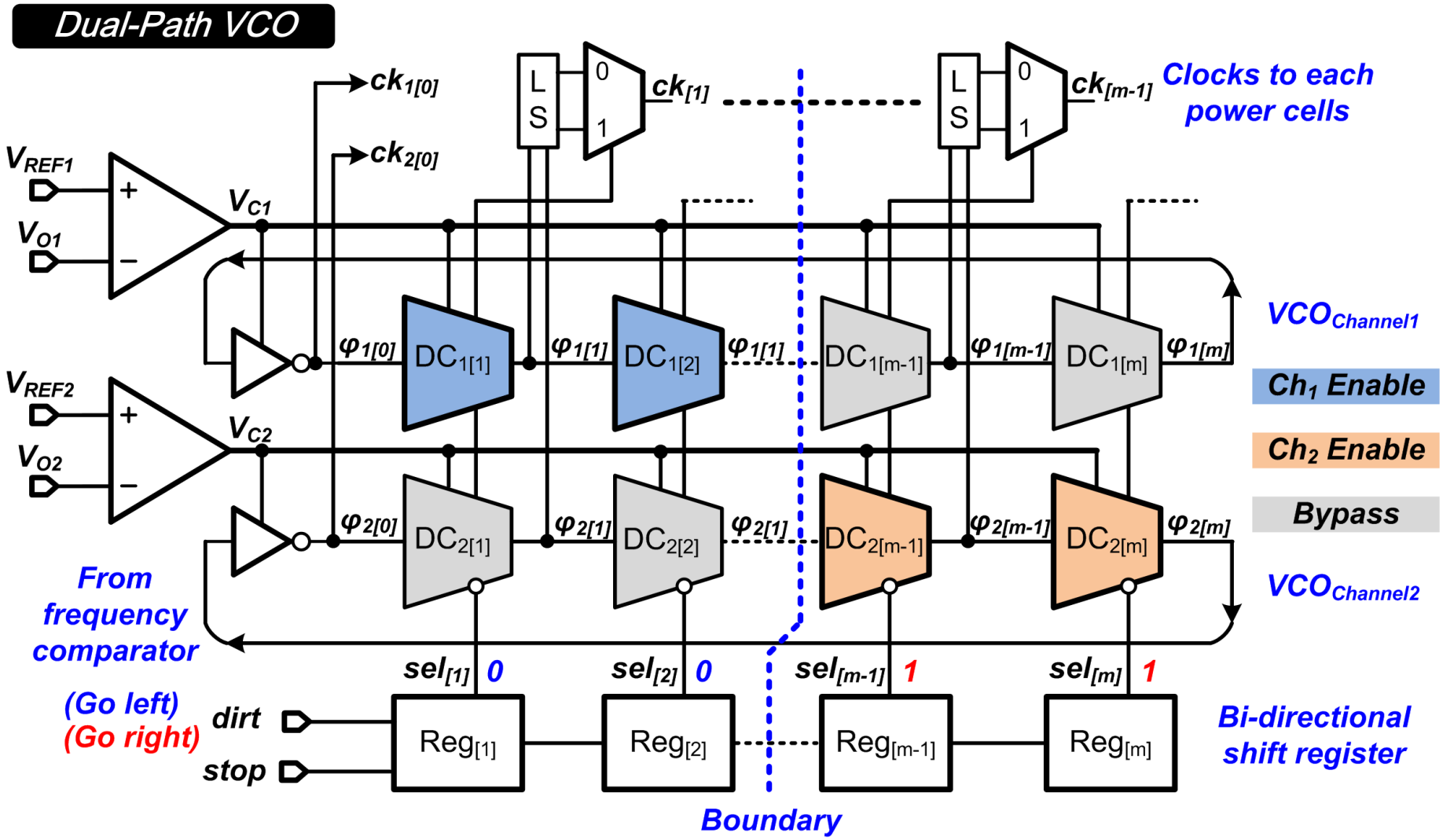
- Two channels are individually regulated by frequency modulation.



System Architecture

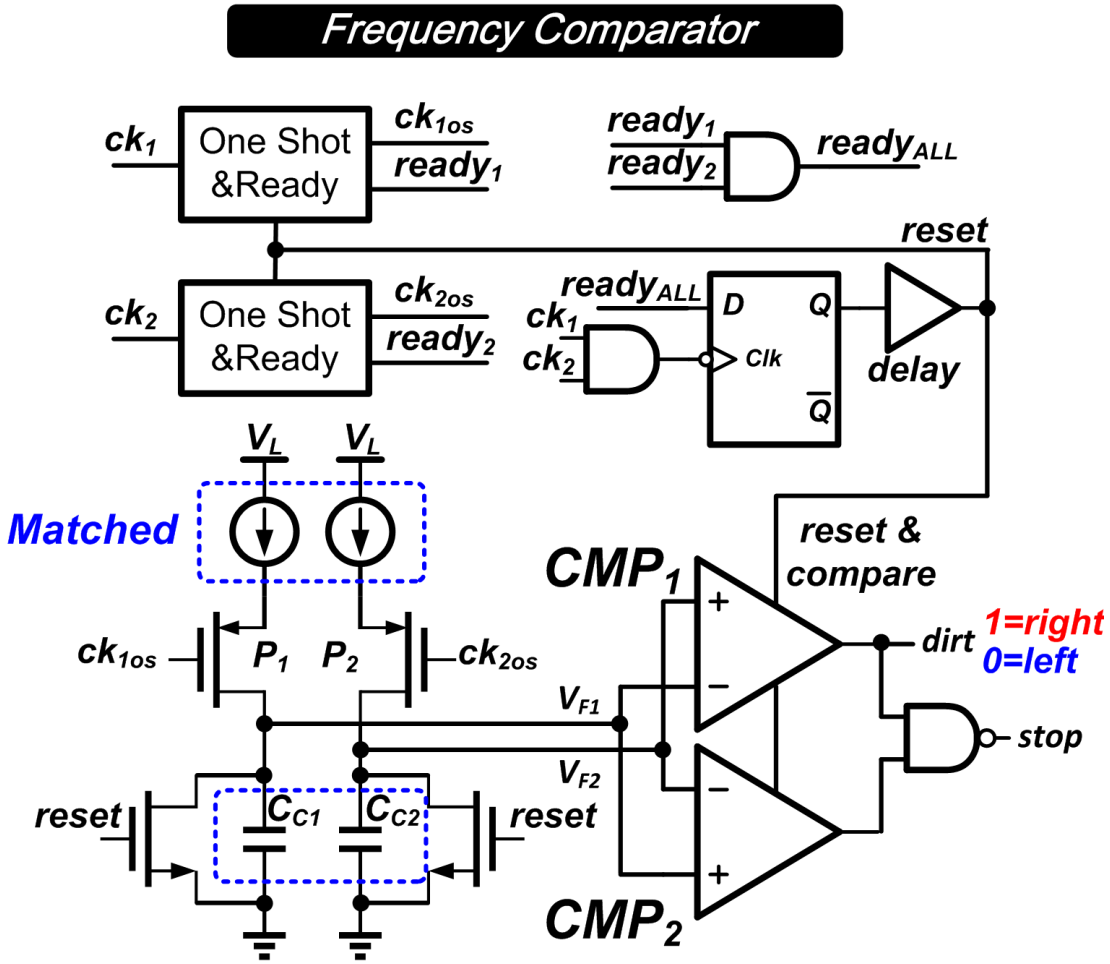
Control Loop Design: A Dual-Path VCO

- The delay cells (DCs) are selected by the shift register outputs.



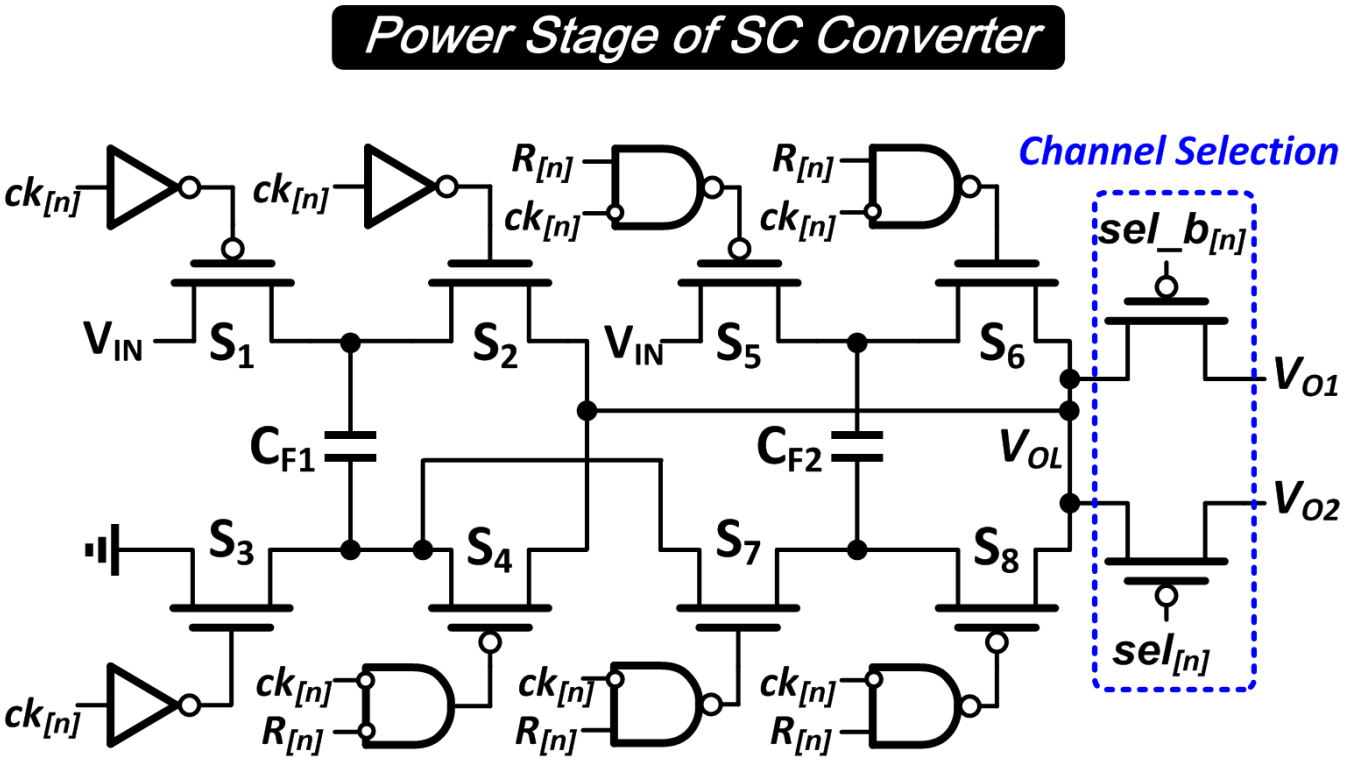
Frequency Comparator

- The frequency comparator is used to compare two frequencies without additional system clock.



Power Stage of the SC Converter

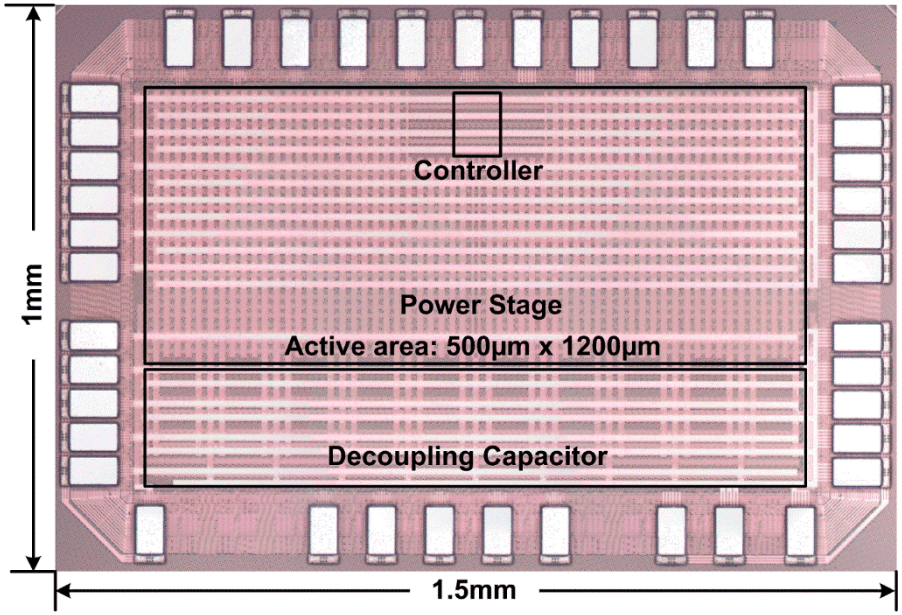
- The two outputs can have different VCRs of 1/2 or 2/3 with our power cell allocation scheme.

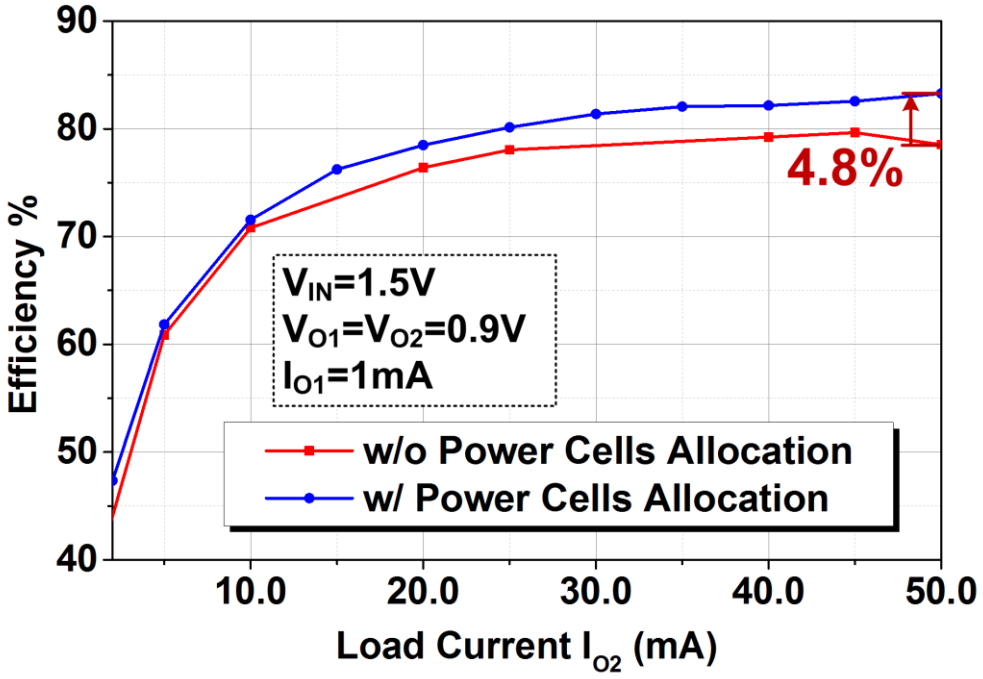


Verification of the Dual-Output SC Converter

- 28nm bulk CMOS
- Chip area: 1 x 1.5mm^2 (Active area: 0.5 x 1.2mm^2)

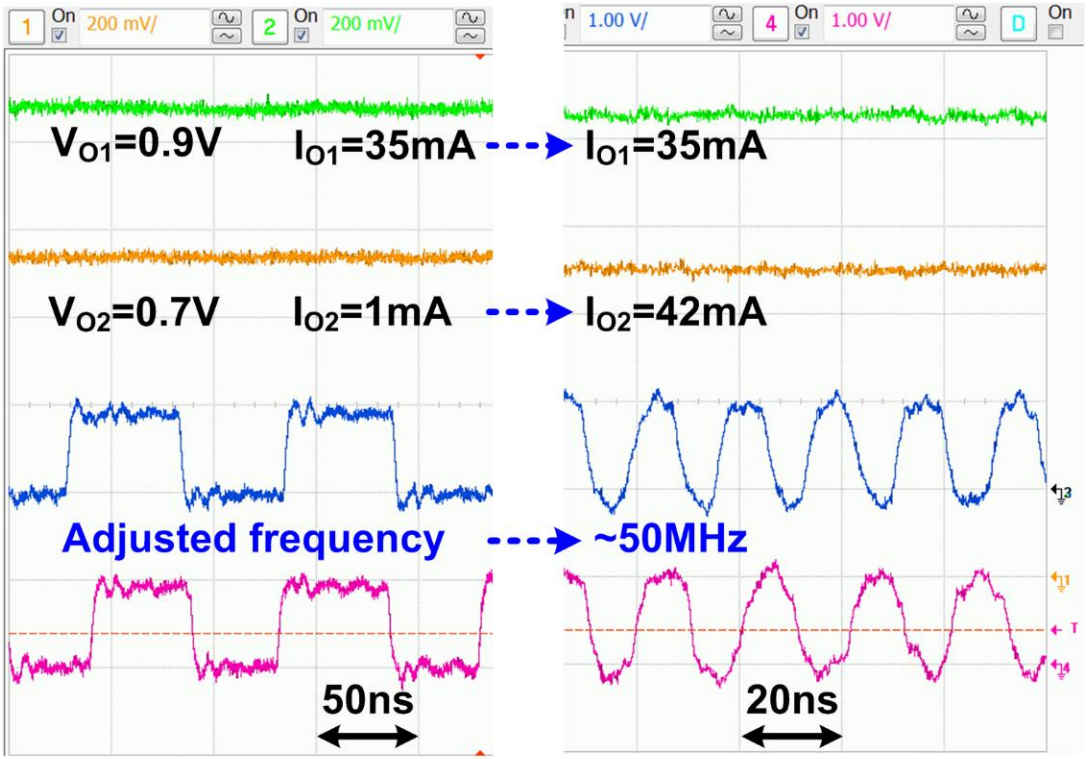
- 4.8% efficiency improvement measured.





Steady-State Waveforms

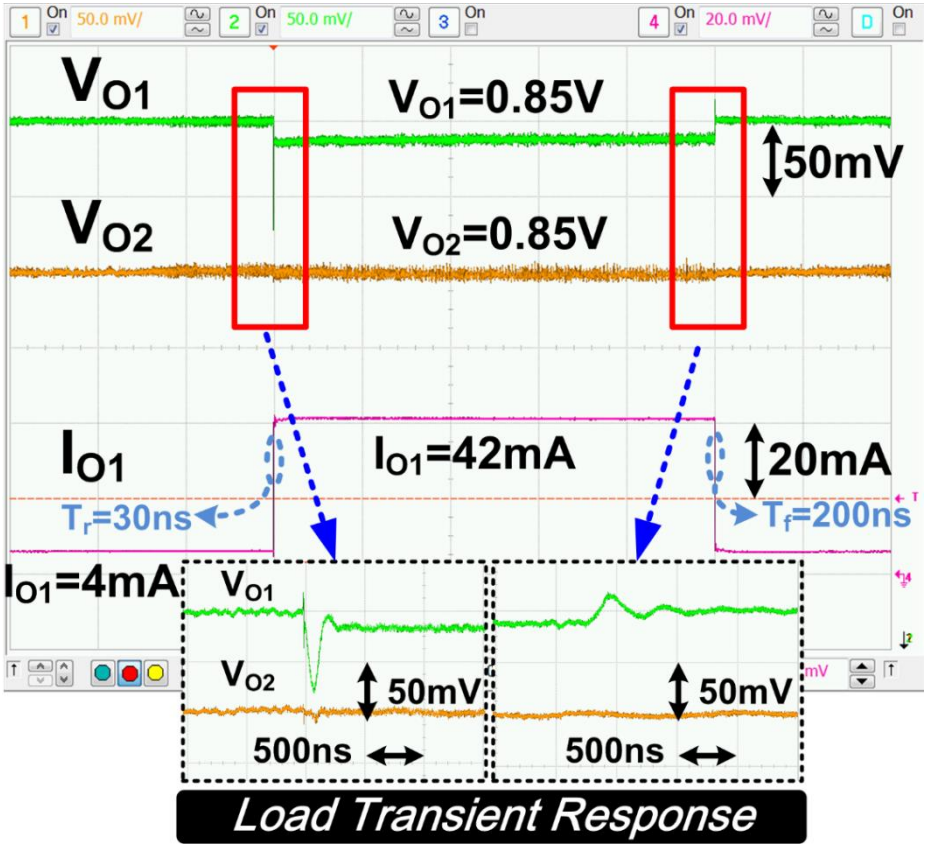
- Different output voltages and currents for V_{O1} and V_{O2}.
- Same switching frequencies for two channels.

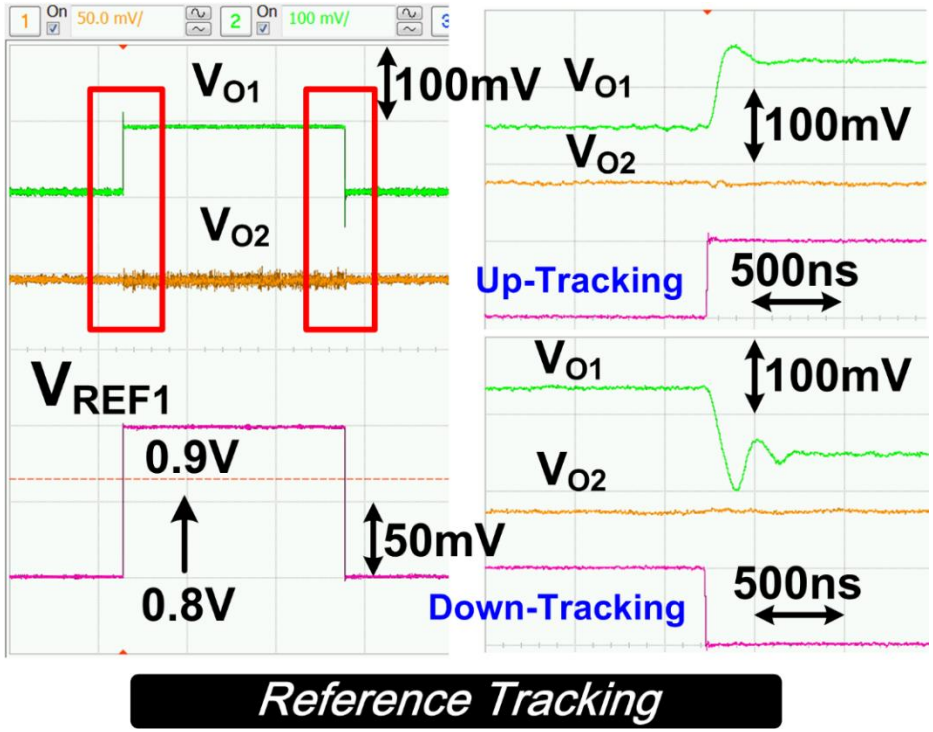


Steady-State Waveform

Transient Performances

- Very small cross regulation observed.





Comparison with Prior Arts

Work	ISSCC`16	JSSC`15	ISSCC`16	This work
Technology	65nm	0.35μm	180nm	**28nm**
Topology	Step-Up/Down	Step-Up	Step-Down	**Step-Down**
Number of Outputs	2	2	3	**2**
Passive Type	On-chip Off-chip	Off-chip	On-chip (MIM+MOS)	**On-chip** **(MOM+MOS)**
V_{IN}	0.85-3.6V	1.1-1.8V	0.9-4V	**1.3-1.6V**
V_{OUT}	0.1-1.9V	2V, 3V	0.6V, 1.2V, 3.3V	**0.4-0.9V**
$I_{O,\,MAX}$	10mA	24mA	100uA*	**100mA**
Total C_{FLY}	1μF	9.4μF	3nF	**8.1nF**
η_{peak}	95.8%	89.5%	81%	**83.3%**
Power Density	N/A	N/A	250μW/mm^2	**150mW/mm^2**
Max. Load per Output	V_{O1}: 1mA V_{O2}: 10mA	V_{O1}: 12mA V_{O2}: 12mA	V_{O1}: 33μA V_{O2}: 33μA V_{O3}: 33μA *	**V_{O1}: 0-100mA** **V_{O2}: 100-0mA**
Symmetrical Outputs	No	No	No	**Yes**

*Extracted from measurement results.

Outline

- Motivations
- Review of Prior Multiple Output SC Converters
- A Dual-Symmetrical-Output SC Converter
- Discussions and Conclusions

Dual-Output Converters Categorized by Size

- 1 + 1 = 2
  - SC converters: output power proportional to area.
  - Two parallel converters.

- 1 + 1 < 2
  - Our goal, of course.
  - Single-inductor dual-output, save one inductor.

- 1 + 1 > 2
  - Some SC dual-output converters belong to this category!

Conclusions

- Our dual-symmetrical-output SC converter marginally belongs to the **1+1<2** category.
- Our scheme can have different VCRs for each outputs, without degrading the efficiency.
- Multiple output SC converters can be realized at the **circuit level** by sharing capacitors and switches; or at the **system level** by sharing power stages/cells.
- Ladder topology is good for multiple output.

References

1. M. D. Seeman and S. R. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
2. N. De Clercq, T. Van Breussegem, W. Dehaene, and M. Steyaert, “Dual-output capacitive DC-DC converter with power distribution regulator in 90 nm CMOS,” *ESSCIRC*, 2012.
3. Z. Safarian and H. Hashemi, “Capacitance-sharing, dual-output, compact, switched-capacitor DC-DC converter for low-power biomedical implants,” *Electronics Letters*, 2014.
4. Z. Hua, H. Lee, “A Reconfigurable Dual-Output Switched-Capacitor DC-DC Regulator With Sub-Harmonic Adaptive-On-Time Control for Low-Power Applications,” *JSSC*, pp. 724-736, Mar. 2015.
5. Y. Mustafa, A. Zhaikhan, and A. Ruderman, “Dual-output switched capacitor converter model for cross-regulation effects,” *Electronics Letters*, Aug. 2018.
6. C. K. Teh and A. Suzuki, “A 2-Output Step-Up/Step-Down Switched-Capacitor DC-DC Converter with 95.8% Peak Efficiency and 0.85-to-3.6V Input Voltage Range,” *ISSCC*, pp. 222-223, 2016.
7. W. Jung, et al., “A 60%-efficiency 20nW-500µW tri-output fully integrated power management unit with environmental adaptation and load-proportional biasing for IoT systems,” *ISSCC*, 2016.
8. J. Jiang, Y. Lu, W. H. Ki, S. P. U, and R. P. Martins, “A dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28nm CMOS,” *ISSCC*, pp. 344–345, 2017.

Acknowledgements

- Junmin Jiang, HKUST & U. of Macau, now TI, Kilby Labs.
- Wing-Hung Ki, HKUST
- Rui P. Martins, U. of Macau

Macao Science and Technology Development Fund

科學技術發展基金
F | D | C | T

澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

Thank You for Your Attention!

Yan Lu
Oct. 19th, 2018