Non-linear Control for Linear Regulators

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PowerSoC 2018

Outline

- Motivation
  - Digitally Assisted and All-Digital LDOs
- Discrete Time All-Digital LDOs
  - Loop Architecture and Circuit Design
  - Reduced Dynamic Stability
  - Measured Results
- Switched Mode Control
  - Hybrid, Dual-Loop Topologies
  - Measured Results
- Unified Voltage and Frequency Regulation
  - Loop Architecture and Circuits
  - Measured Results
- Conclusions

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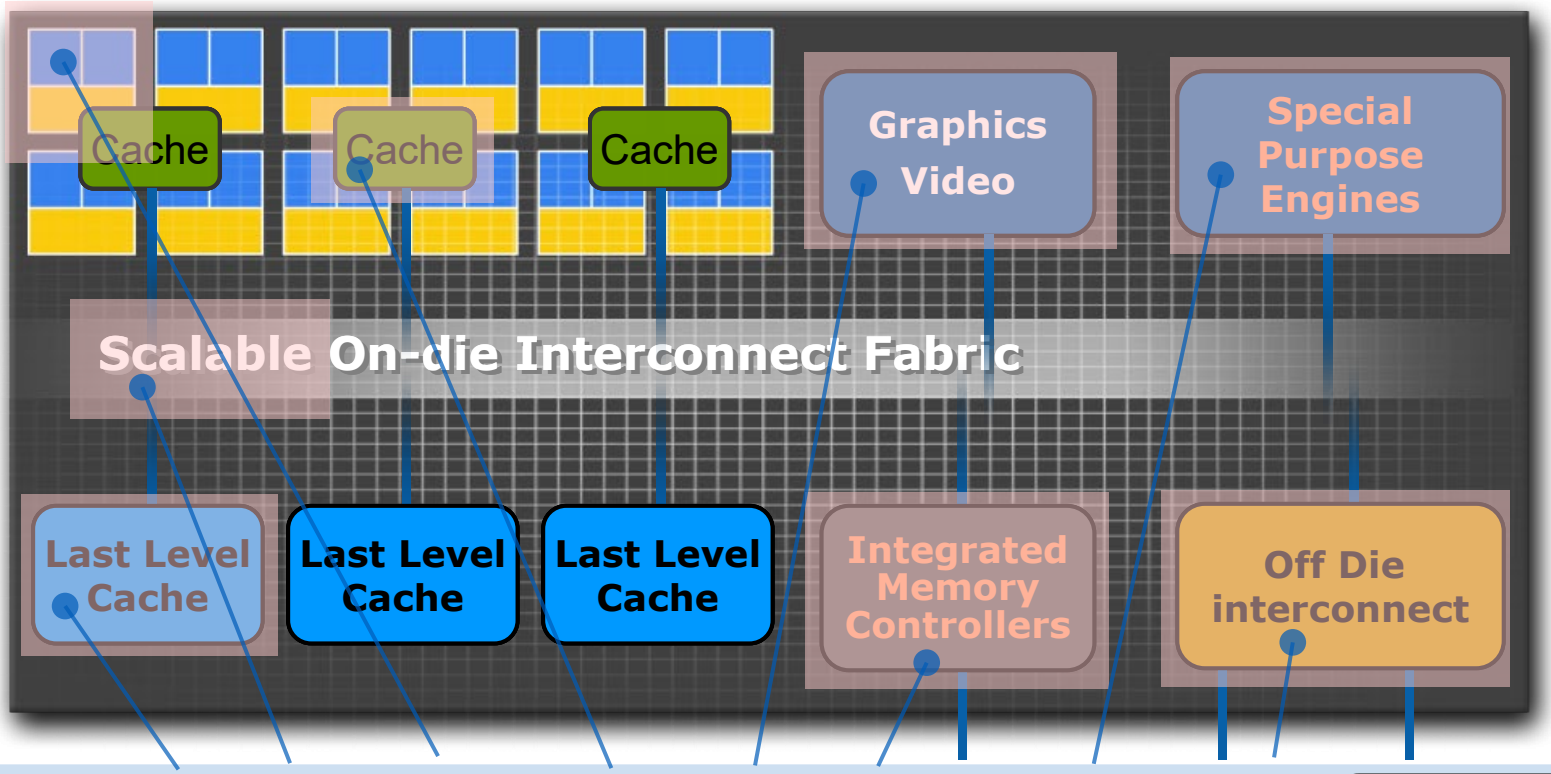
SoC as a Dynamic Platform



Source :Intel

Maximize performance & efficiency

- Independent V/F control regions
- Scenario-based power allocation
- Dynamic V/F control
- Workload-based core activation & shutdown

Deliver optimal power for just-in-time performance

Linear and Low Dropout Regulators

LC-VR

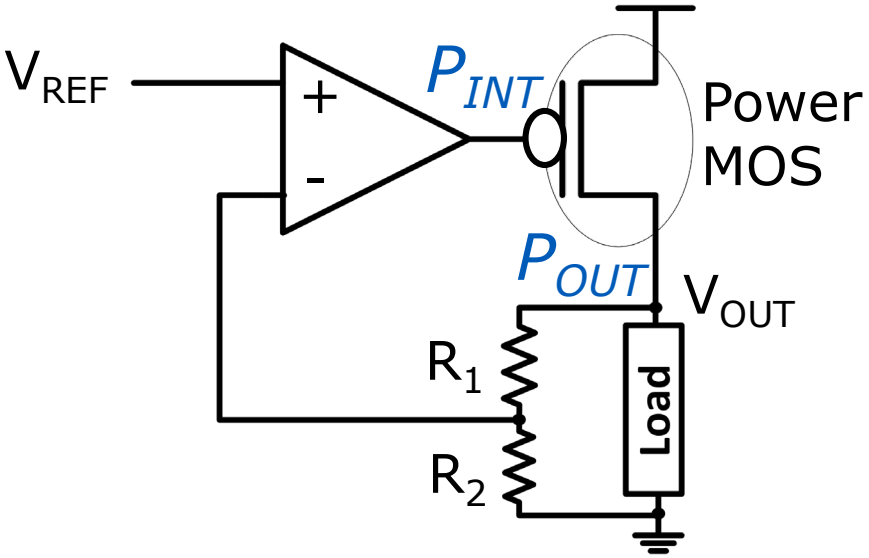
- High efficiency
- Package integration
- Continuous Vout
- Large domains
- Fast response

SC-VR

- High efficiency
- Discrete Vout
- Medium response
- Low energy density

Linear Regulator

- Lower efficiency
- Die integration
- Finest domains
- Fastest response



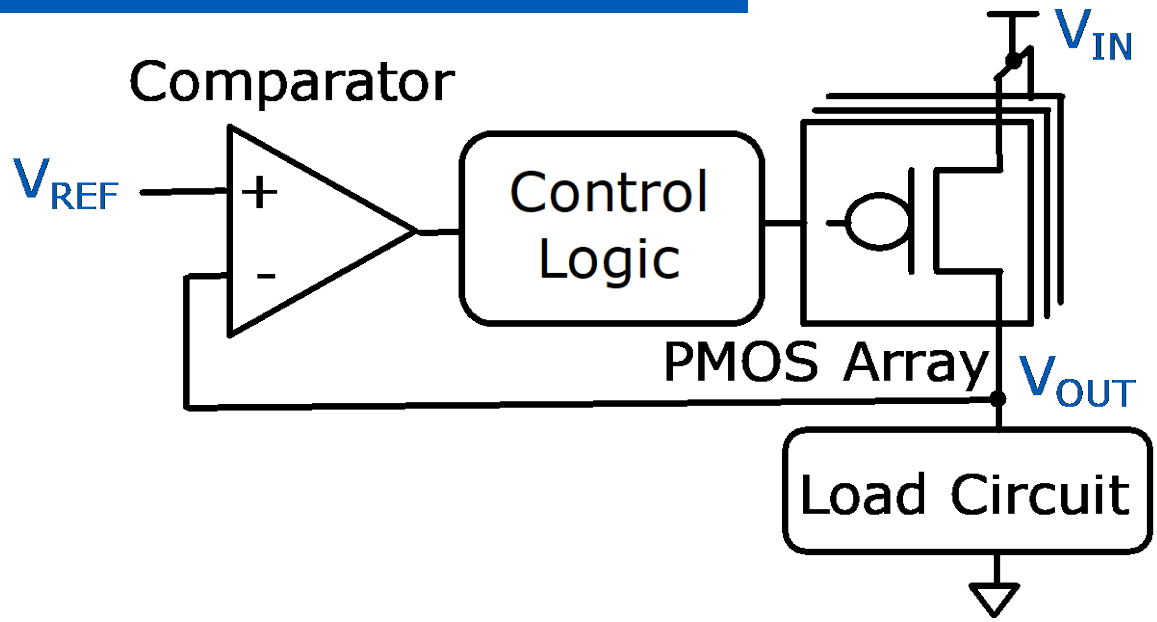
$$A_V = \frac{\beta . A_{AMP} . g_m . Z_{LOAD}}{(s - P_{INT})(s - P_{OUT})}$$

$$\beta = \frac{R_2}{R_1 + R_2}$$

The important poles are internal (P_{INT}) and output (P_{OUT})

Analog PMOS based LDO

All-Digital Discrete-Time LDO



All-Digital LDO

- Mostly synchronous; Continuous time systems are also possible
- Single stage comparator
- Control Logic can implement PI control

LDO Regulators: Analog vs Digital

Analog LDO Regulator

+High bandwidth

+Excellent small signal performance

+High power supply rejection (PSR)

+No Noticeable Ripple

-Limited by slew rate of the power PMOS

-Narrow operating range

Ideal for supply sensitive analog load

Digital LDO Regulator

+No analog Components with synthesizable control

+Decouples loop gain from operating voltage

+Large operating range (both supply voltage and load current)

-Output ripple

-Low PSR, Low Bandwidth

Ideal for digital load supporting DVFS

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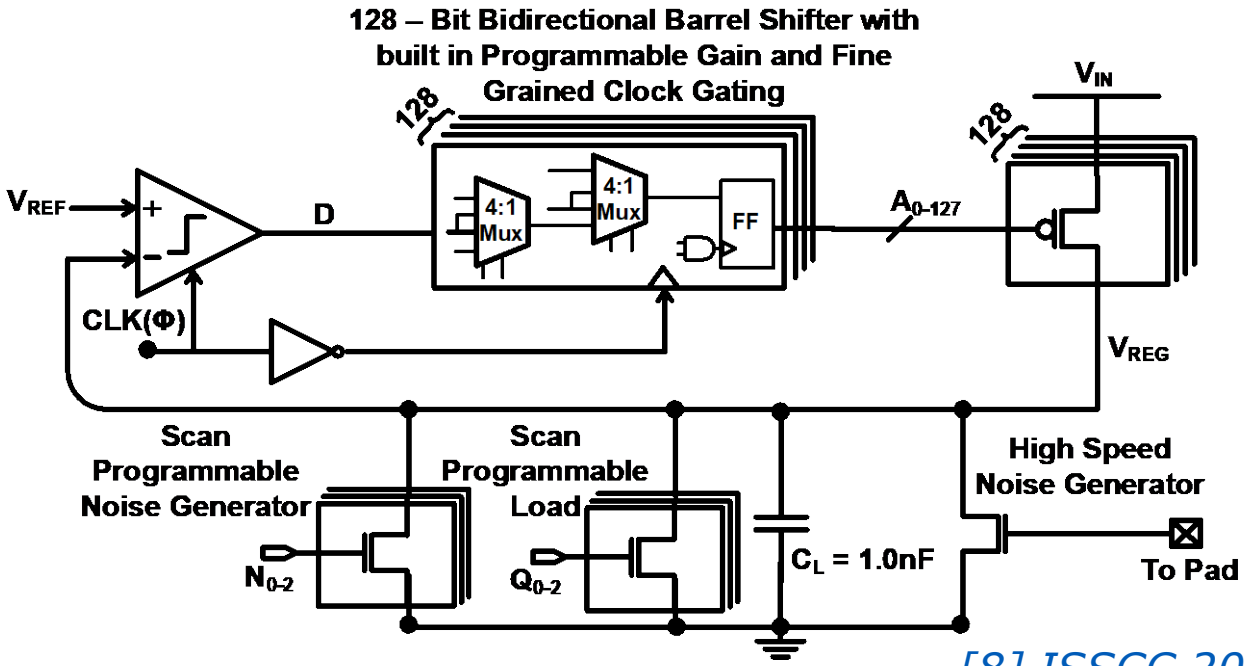
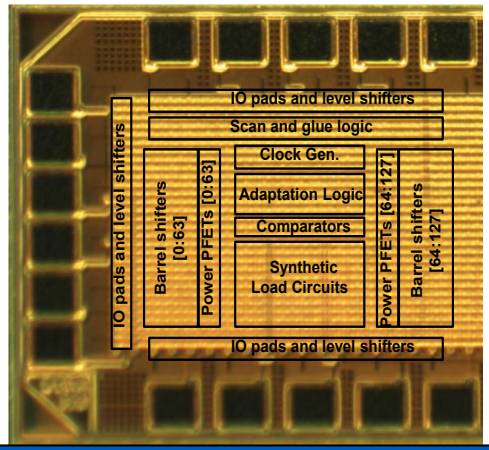
All-Digital Discrete Time LDOs



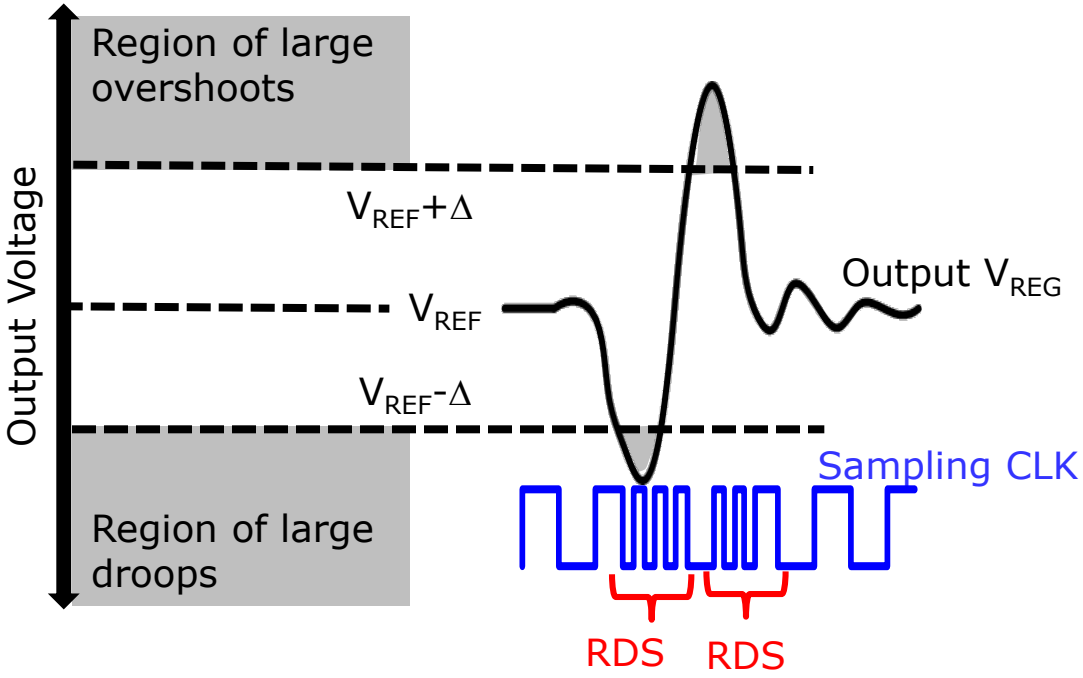


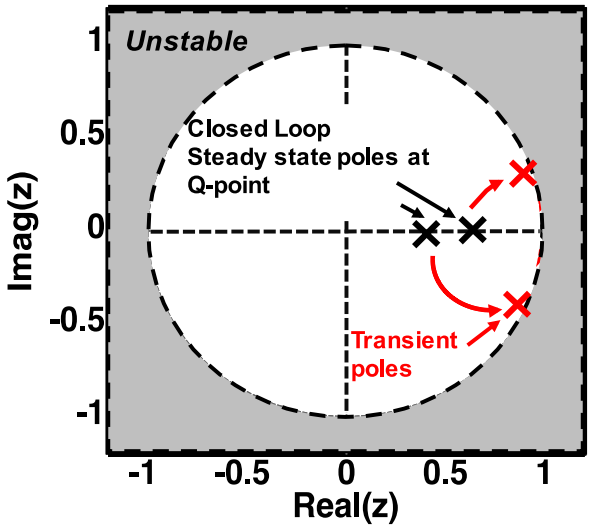
[8] ISSCC 2015
[9] TPEL 2016

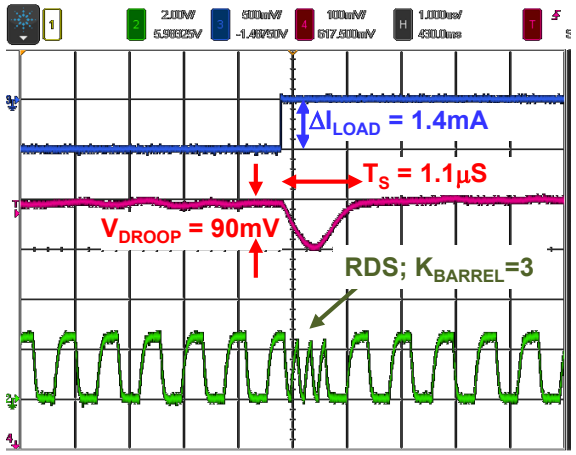
- IBM 130nm Process
- V_{IN}=1.0V -0.50V
- V_{OUT}=0.9V -0.45V
- Max I_{LOAD}=5mA

- Fully digital and synchronous design with variable gain control through a 128-bit barrel shifter
- Fine-grained clock gating reduces 30% of controller power
- Clocked comparator input provides high input gain.

Enhancing Transient Performance



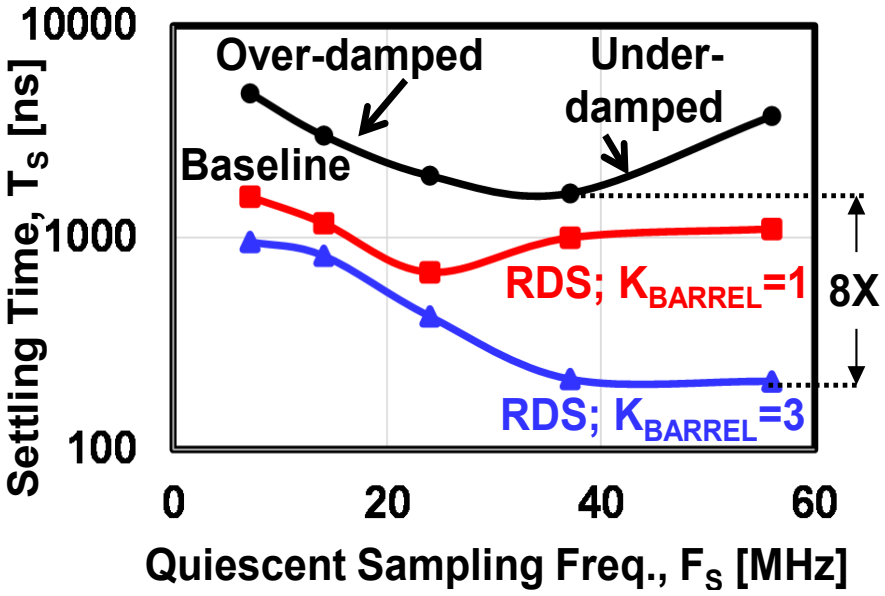


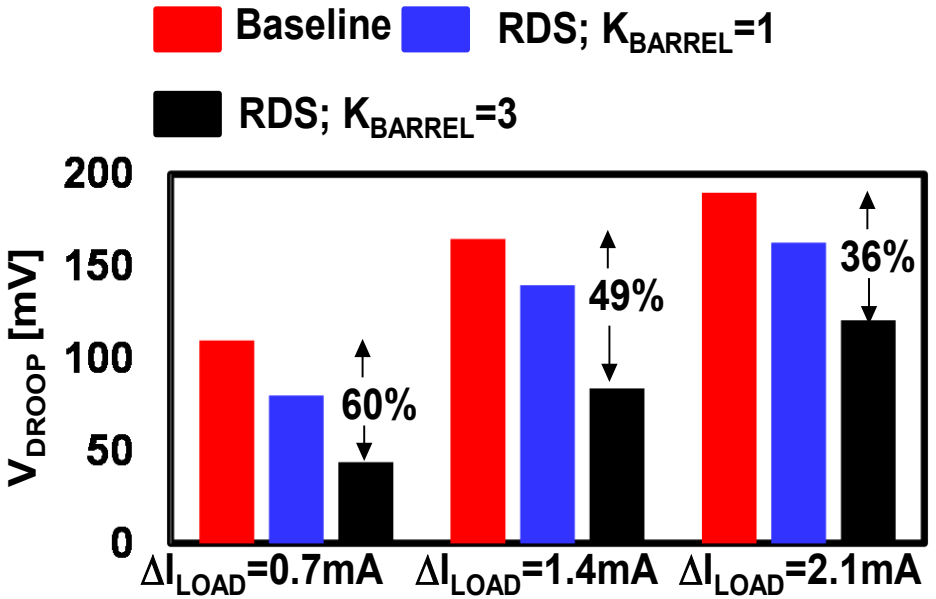


RDS for faster response to large droops

- Higher CLK Frequency & Gain for large load steps enable RDS
- An externally programmable Δ (nominally 50mV) and fast, transient clocks (nominally 400MHz) are employed.

Reduced Dynamic Stability (RDS)





[8] ISSCC 2015

- RDS results in 8x improvement in measured settling time.
- RDS reduces the voltage droop in response to a load step by as much as 60%.

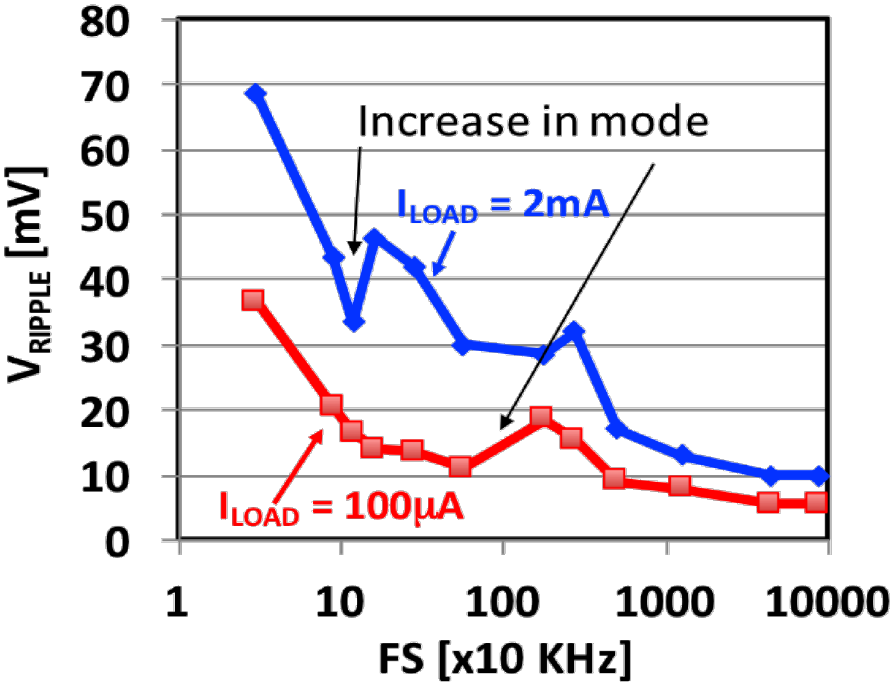
Limit Cycle Oscillations and Ripple

Origin of Limit Cycle Oscillations

- Quantization of the control loop at the comparator and at the output plant
- Relay based control is the key quantizing block in the loop

Control Principle and Modeling

- Describing function models the interaction of linear and non-linear components of the control loop



[16] APEC 2015
[9] TPEL 2016

Key Results and Observations

- Increasing sampling frequency increases the mode of oscillation
- F_{LOAD}/F_S needs to be bounded to limit output ripple

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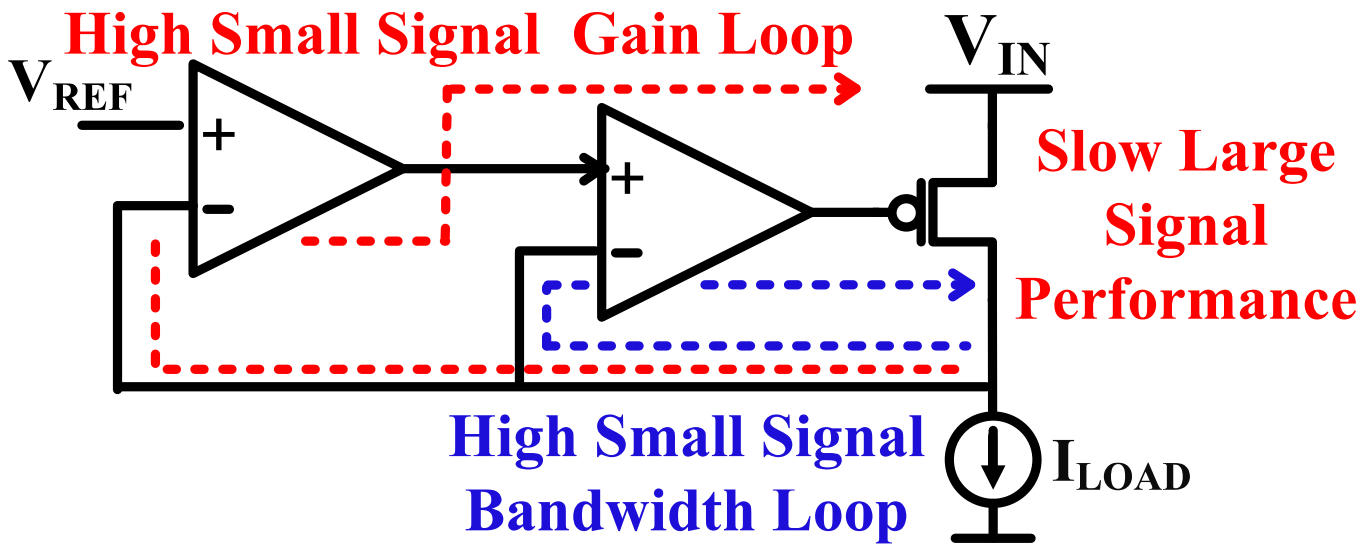
Conventional LDOs with Two Loops

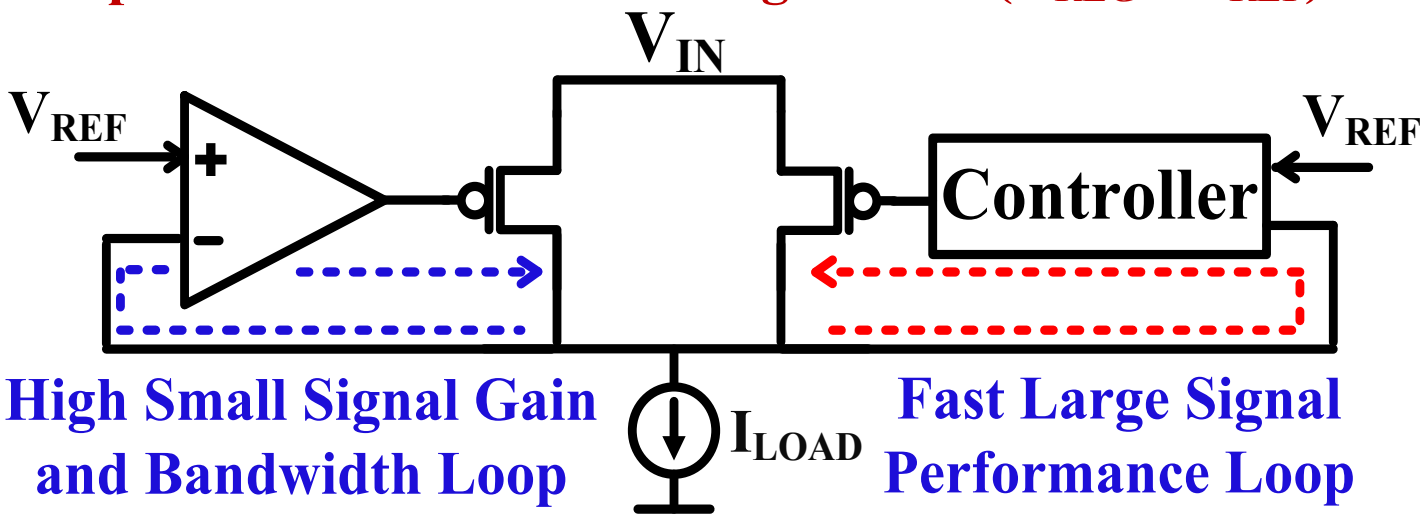


Conventional LDOs with two Loops

- Fast transient loop
- Slow reference tracking loop
- Limited large signal performance
- Slew limited for large current transients

Switched Mode Control (SMC) LDOs

Operation Divided on Voltage Error (V_{REG} - V_{REF})

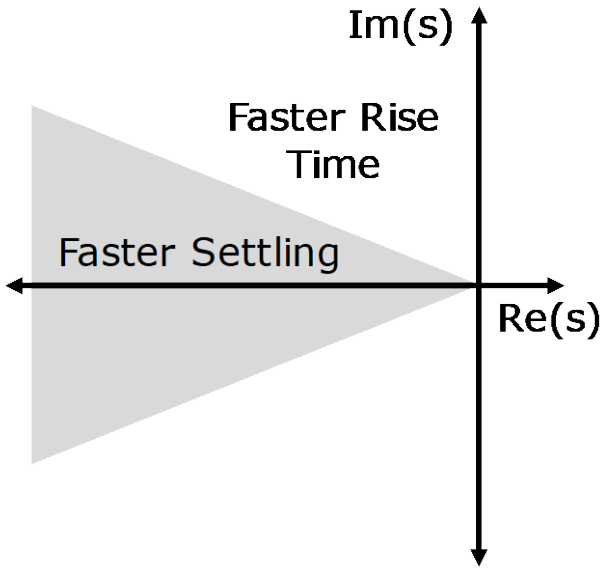


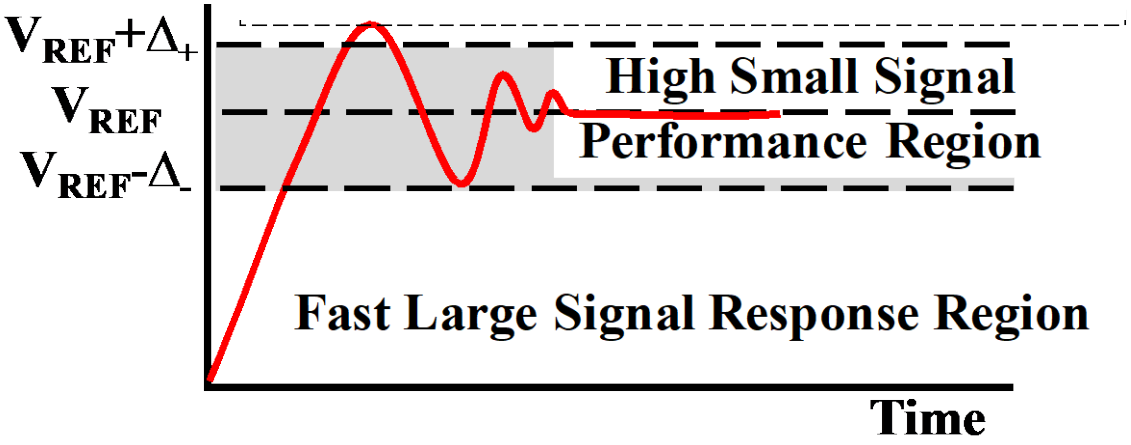
Dual Loop Switched Mode Hybrid Control

- Two loops separated not in frequency, but in time (or voltage error)
- Good small signal performance (analog loop)
- Fast large signal performance (digital controller)

[18] ESSCIRC 2016

Optimality in SMC LDO Designs

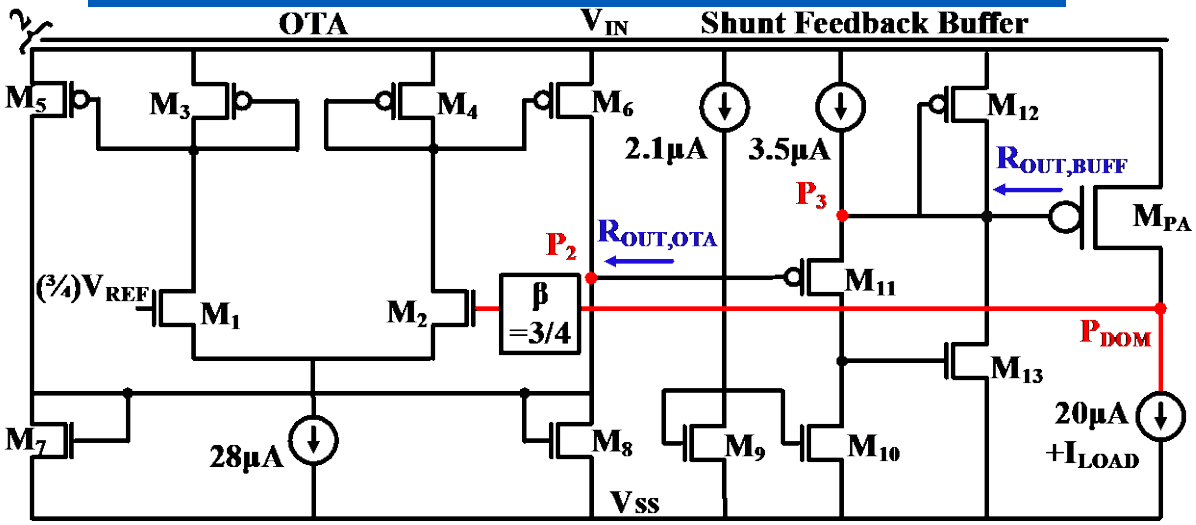




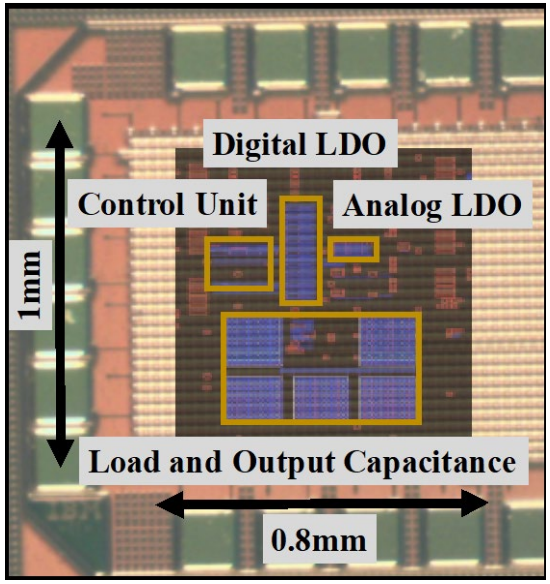
SMC Design Principle

- Large transients ($|V_{OUT} - V_{REF}| > \Delta$):
  - Place poles in unshaded region for faster rise time (Underdamped)
- Near regulation ($|V_{OUT} - V_{REF}| < \Delta$):
  - Place poles in shaded region for faster settling (Overdamped)

Output Pole Dominant Analog Loop



Capacitor Less Output Pole Dominant Analog LDO

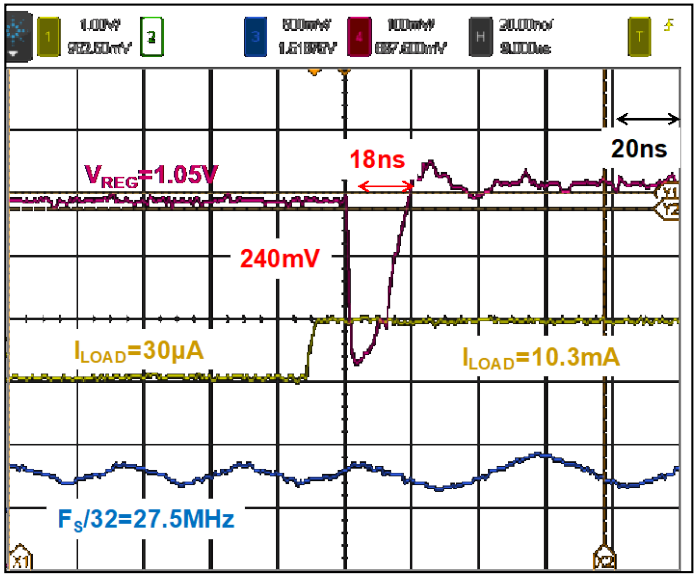


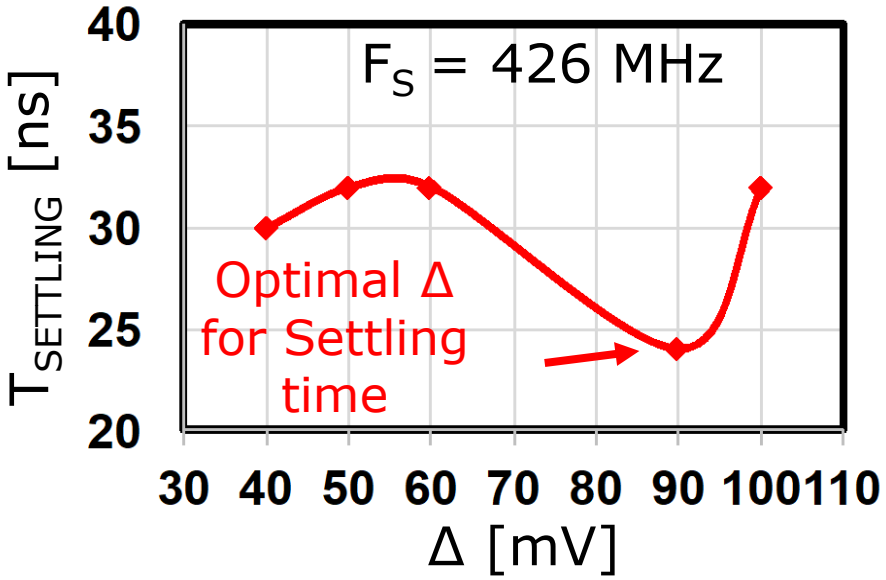
[18] ESSCIRC 2016

- Three stage output-pole dominant analog small signal regulator
- Input transconductance stage is followed by a shunt feedback buffer, pushes internal poles to high frequency (100s of MHz)

- IBM 130nm Process
- V_{IN}=1.2V -0.60V
- V_{OUT}=1.0V -0.5V
- Max I_{LOAD}=12.6mA

Key Measurement Results





- SMC enables us to synthesize a system with near-optimal droop response over a large load range.
- Optimal Δ of 90mV is measured.
- Transient rise time of 18ns is measured for a load step of >10mA.

Summary: All-digital and Hybrid SMC LDOs

All-Digital Loop

+Wide operating range

+High current efficiency with adaptive control

+Low-overhead adaptation with clock control

+Fast transient response enabled by RDS

-Output ripple

-Limited small signal performance

- Limited Clock Frequency

Hybrid SMC Loop

+Excellent small signal gain and performance

+No ripple

+Fast transient response with high speed digital loop

+Output pole dominant analog

-Limited operating range

-Lower current efficiency

-Not synthesizable

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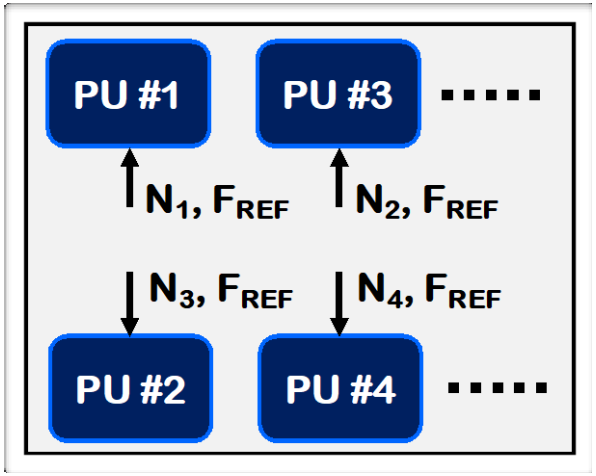
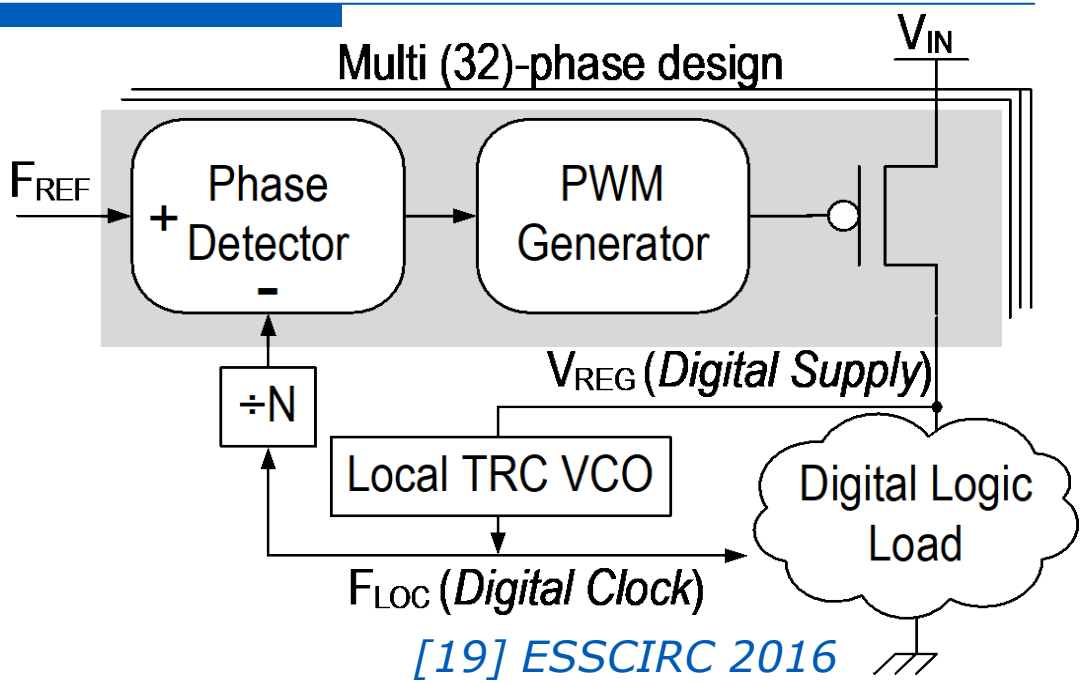
Unifying LDO VR and Clocking



SoC PM Vision

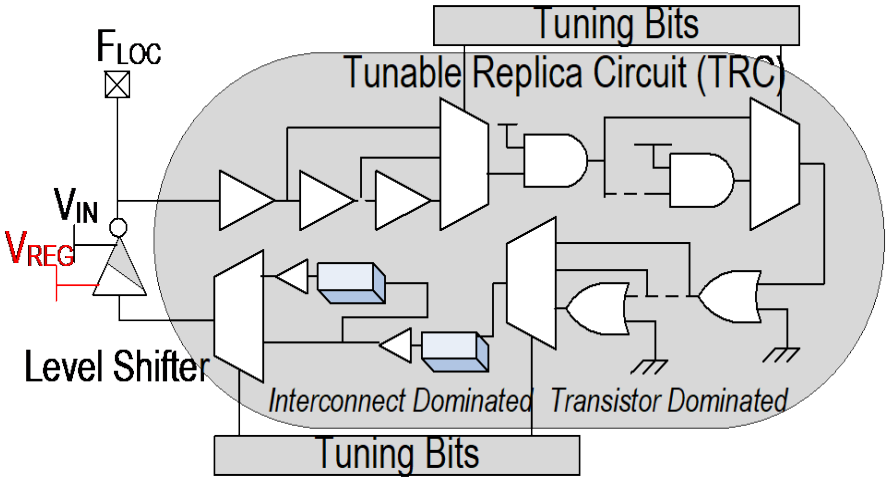


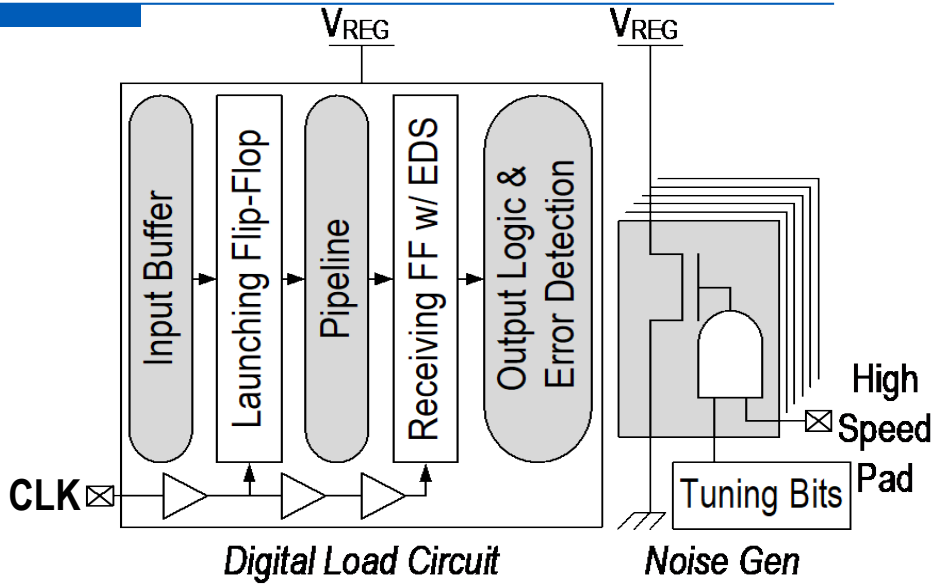
[19] ESSCIRC 2016

Loop Transfer Characteristics

- The local clock and the local supply are generated from the same control loop
- Clock jitter correlated with V_{REG}
- No small signal sensing

TRC VCO and Load Circuits





Tunable Replica Circuit VCO

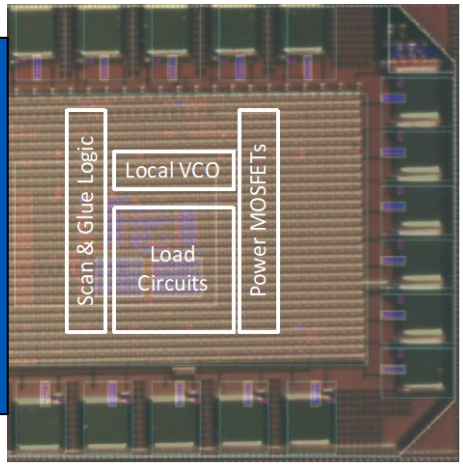
- Composed of logic and interconnect dominant paths
- Programmable to tens of ps resolution
- Non-inverting path closed via level shifting inverter to create a tunable VCO

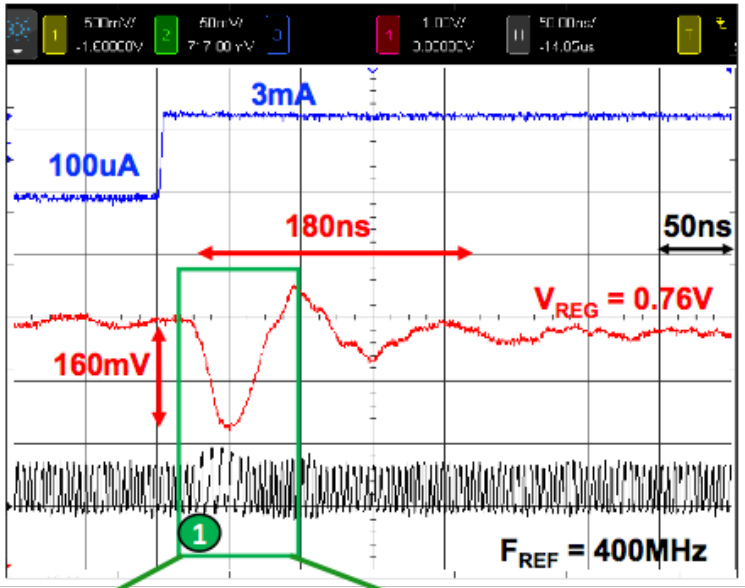
Prototypical Load Circuit

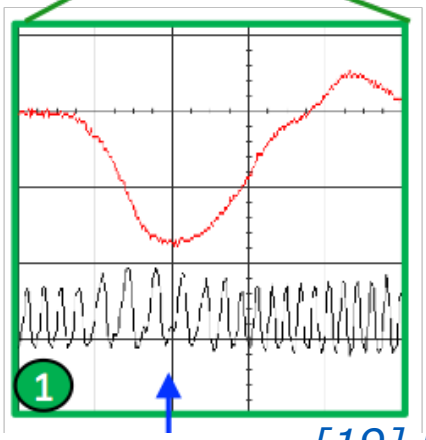
- Three stage pipeline with built in self-test
- Error Detection Sequentials to detect timing errors
- High-speed noise generator replicates power state transitions

Key Measurement Results

- IBM 130nm Process
- V_{IN}=0.1V -0.6V
- V_{REG}=0.81V -0.27V
- F_{REF}=10-500MHz
- Max I_{LOAD}=2.5mA



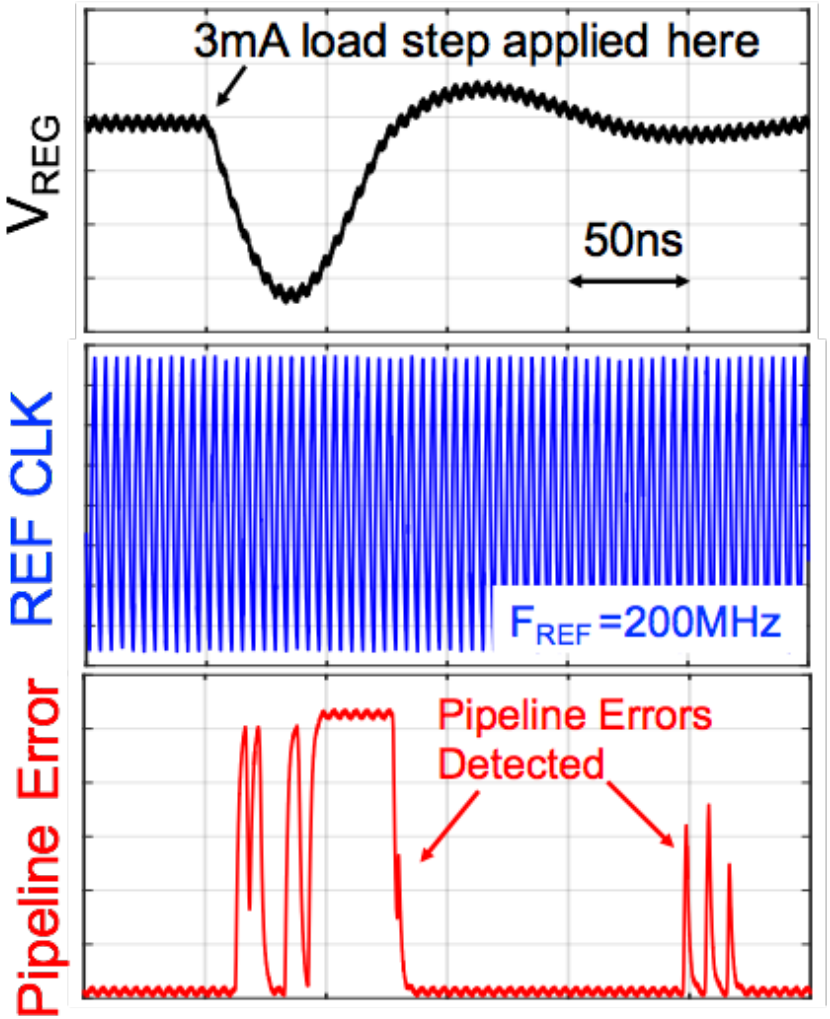




- TRC VCO always tracks V_{OUT}
- Frequency & amplitude independent Clock-Data compensation
- Controller current scales with logic frequency and provides high current efficiency

[19] ESSCIRC 2016

Response to Voltage Droops



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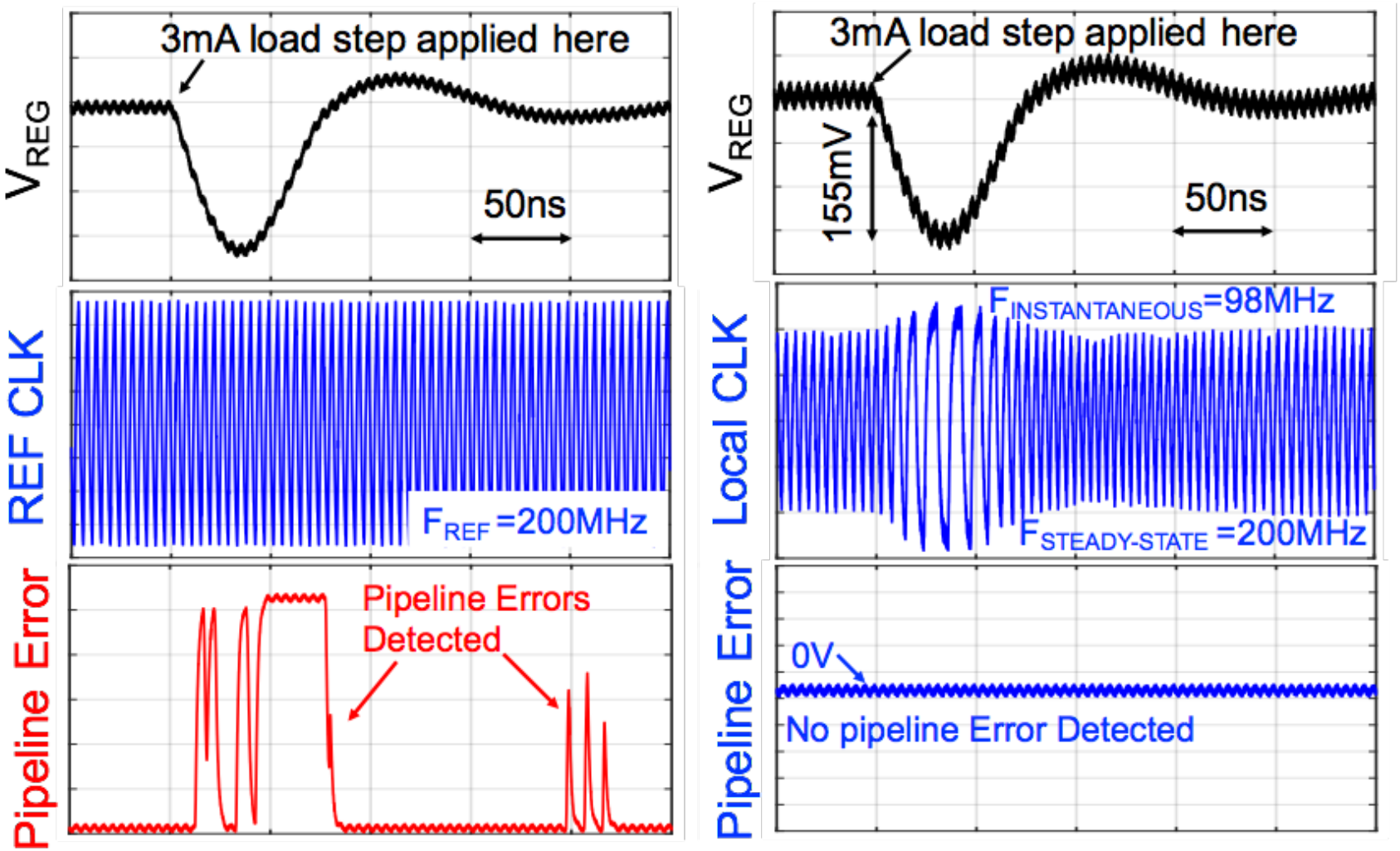
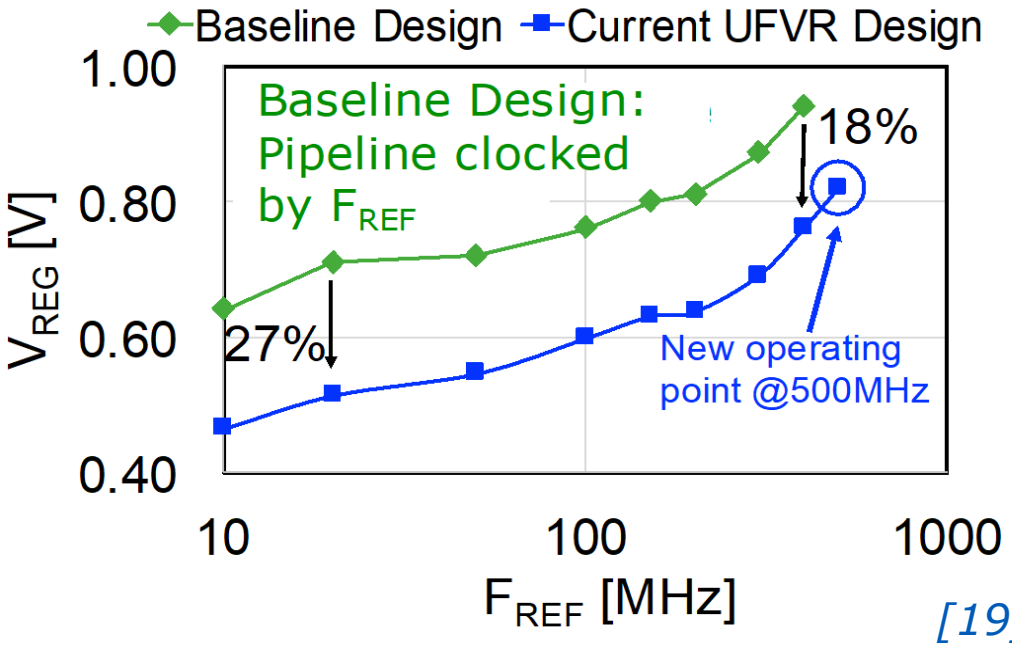


Resiliency through UVFR Design



[19] ESSCIRC 2016

- UVFR allows co-regulation of the load supply and the local clock frequency
- A maximum reduction of 27% of voltage guard-band is measured at 10MHz

Summary: Continuous Time LDOs

Phase Based Design

+Continuous time control

+Designed with digital gates only

+Low-overhead multi-phase design

+Fast transient response and no ripple

-Larger area and controller power

-Limited bandwidth (dominant pole at the origin)

Unified Voltage and Frequency Regulation

+Single loop control for both supply and clocking

+Local clock tracks dynamic variations; no timing error

-Droop response limited by the reference frequency

Conclusions

- Digital LDO regulators demonstrate
  - Low Operating Voltage (to NTV) & Low Dropout Voltage (~50mV)
  - Fast Transients with DVFS Support for Digital Load Circuits
- Switched Mode Control (SMC) allows
  - Excellent Small Signal Analog Performance
  - Fast Transient Response enabled by the Digital Loop
- Phase Based regulation allows ripple free operation
- UVFR allows voltage-clock co-regulation and reduction of voltage guard-band in digital load circuits
  - Further demonstrations of UVFR in buck converters (ISSCC 2019 paper with Qualcomm)

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  - Qualcomm Inc.
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