EMPOWER SEMICONDUCTOR

Your Inner Power

PwrSoC 2018: IVR Driven Energy Savings in SoCs

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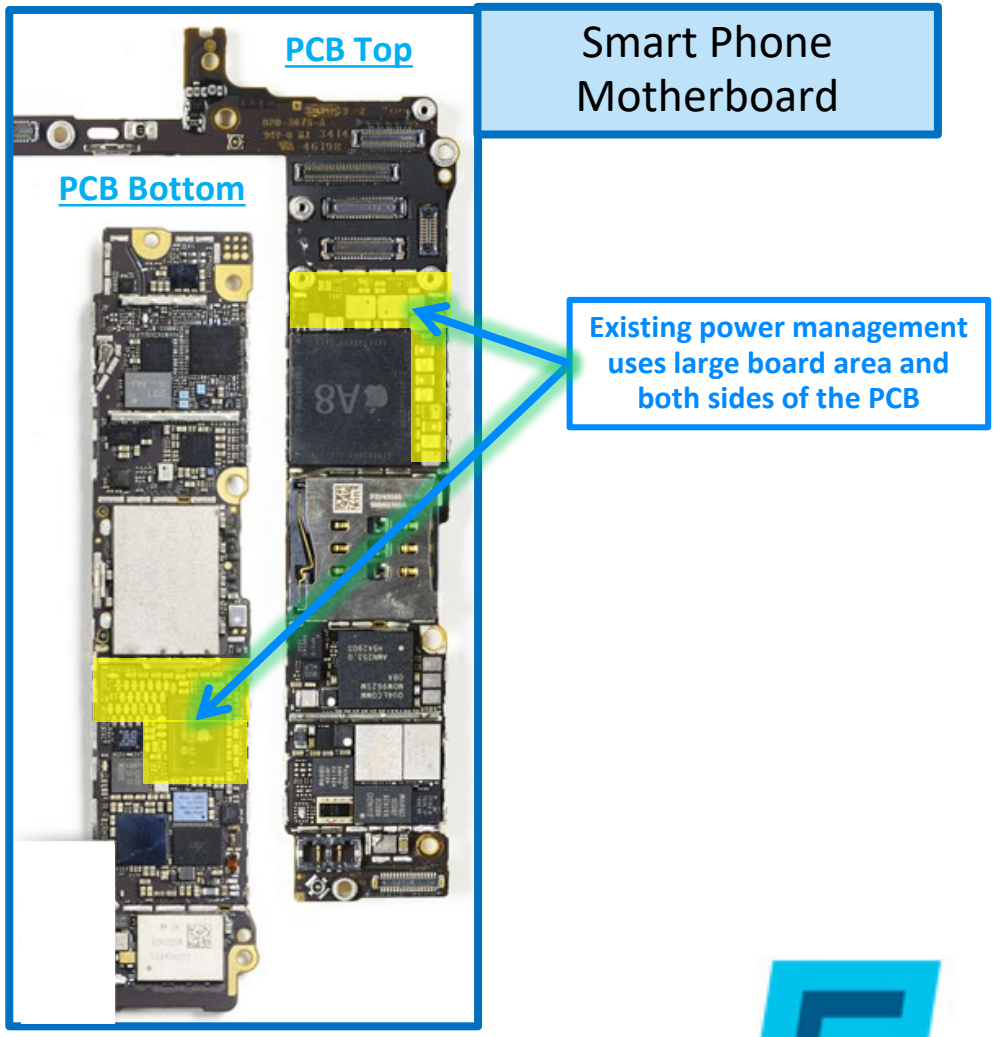
Outline

- The need for and challenges of full power management integration
- Empower Resonant IVR (RIVR™) technology
- How RIVR technology speed and accuracy drive significant system energy savings

The Need for Power Management Integration

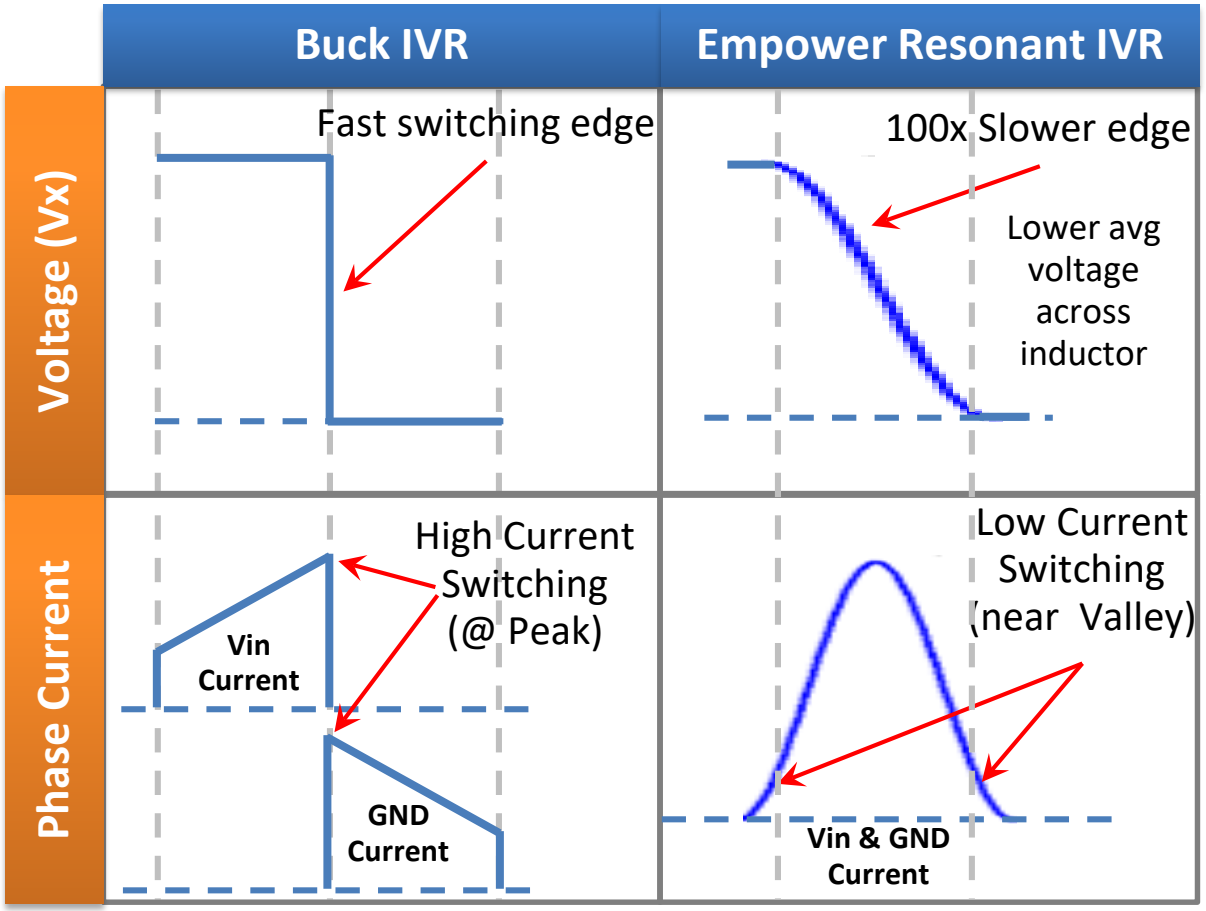
- Moore's Law drives SoC power challenge
  - Logic di/dt increases, metal thins
  - Reduced operating voltage squeezes voltage margin
  - Voltage rail proliferation: IP blocks and islands demand independent voltage rails
  - Multi-channel VRs (PMICs) now supply 20-40+ rails; are consuming massive PCB space
  - Package & PCB rail routing & filtering complex, area intensive, and expensive
- Traditional Solutions have run out of steam …
  - Power Deliver Network (PDN) far too slow for modern di/dt → forces significant voltage margining
  - PMIC area/cost/speed/efficiency tradeoff at limit



The Challenges of Integrated Voltage Regulators (IVR)

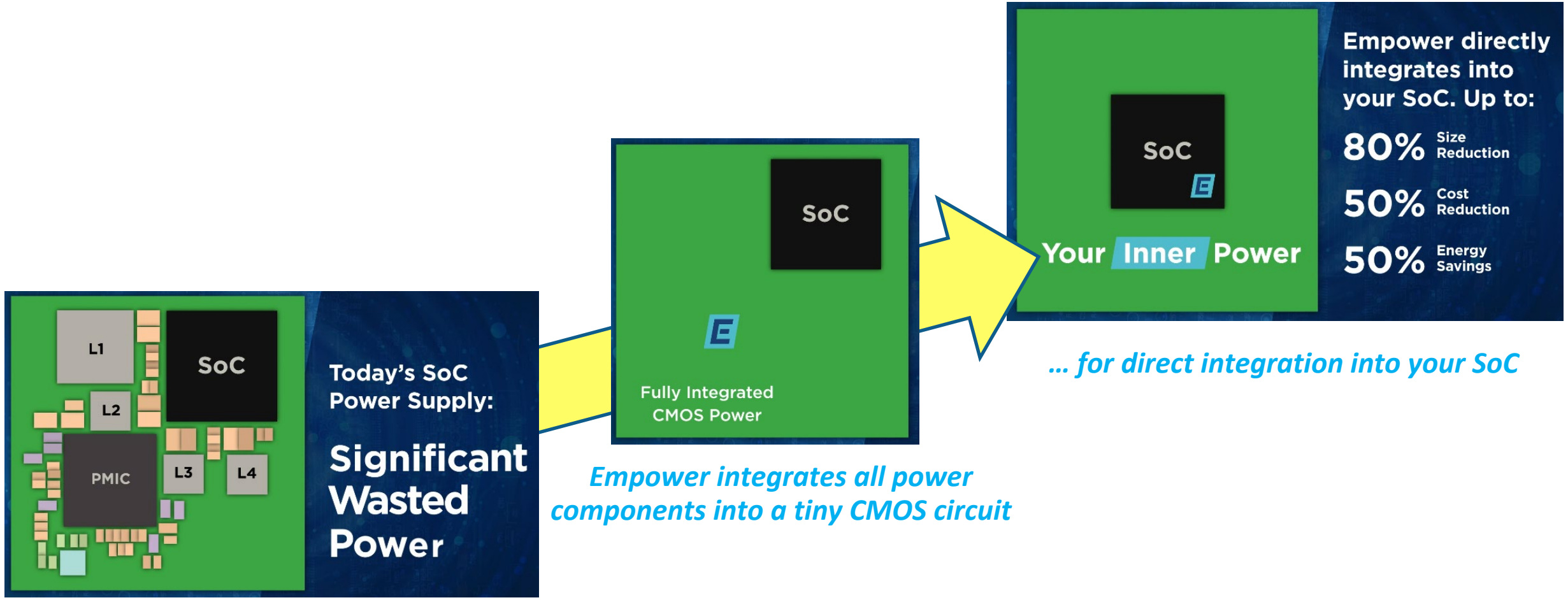
- Area of Passive Components
  - Inductor size presents significant challenge in adoption & scalability of IVRs
  - Traditional Buck architecture requires very high frequency to shrink L's enough
    - High Freq → low efficiency, high switching noise
  - Switch cap architectures can require very large caps and display low granularity and/or efficiency
- High Efficiency with Low Noise and Low EMI
  - LDO's, while low noise, require low dropout, and are an inefficient architecture when multiple rails with different voltages are required
  - Most switching regulators switch at peak currents and cause high input noise, radiated EMI, and minority carrier substrate injection when body diodes conduct
- Cost
  - Special SoC processing or added package layers are typically required

Empower Resonant Integrated Voltage Regulators (RIVR™)



- Full component integration
  - All rails can be fully integrated
  - Industry's smallest passives
  - No discrete components, no special process steps or packaging
- Highest System Efficiency
  - Soft-switching → low loss
  - Tiny Inductors → low DCR
  - 1,000x faster DVS → lower SoC loss
- Ultra-wide Bandwidth
  - SoC voltage accuracy 5x better
- Low Noise & EMI
  - Soft-switching, no diode conduction

A Fully Integrable Power Solution for All SoCs



PMIC Solutions are typically larger than the SoC they power

Empower integrates all power components into a tiny CMOS circuit

… for direct integration into your SoC

RIVR™ Enables Significant Energy Savings

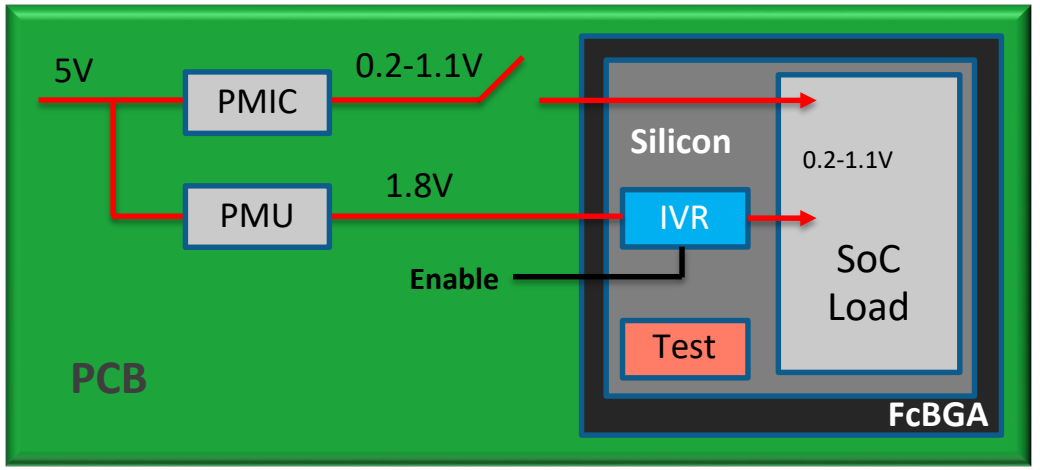
- Three main sources of Significant Energy Savings
  1) Wide-bandwidth regulation enables tight voltage accuracy
  2) Wide-bandwidth regulation enables on-demand DVFS
  3) 2-Stage power conversion enables performance and energy optimization for each stage

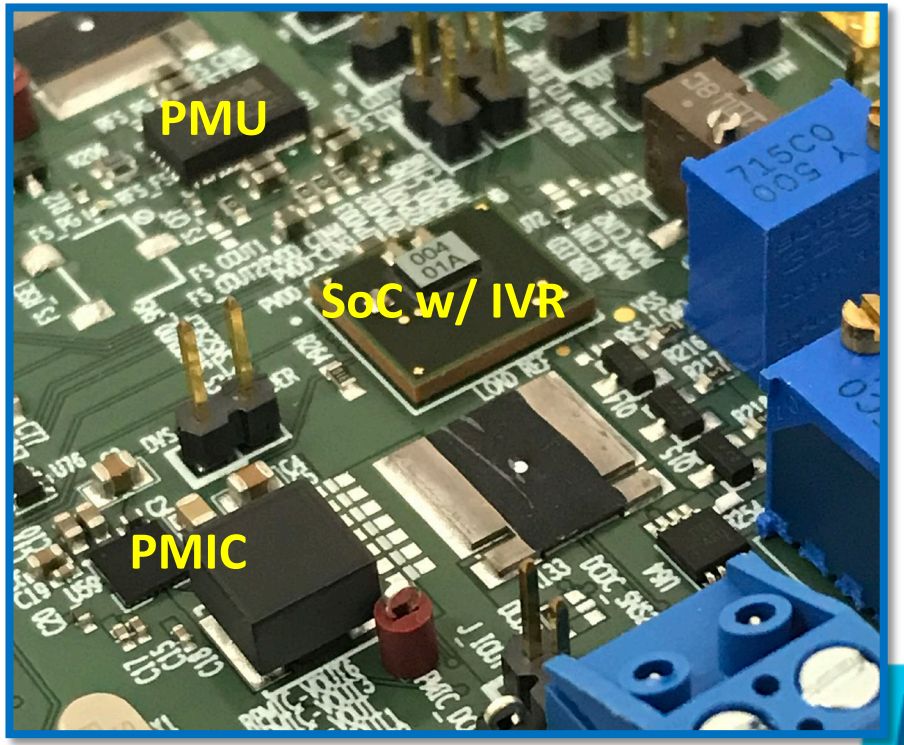
- With 2-stage conversion and wide-bandwidth second stage response, VR efficiency is no longer a useful metric of system energy savings

Benefit 1:
Voltage Accuracy

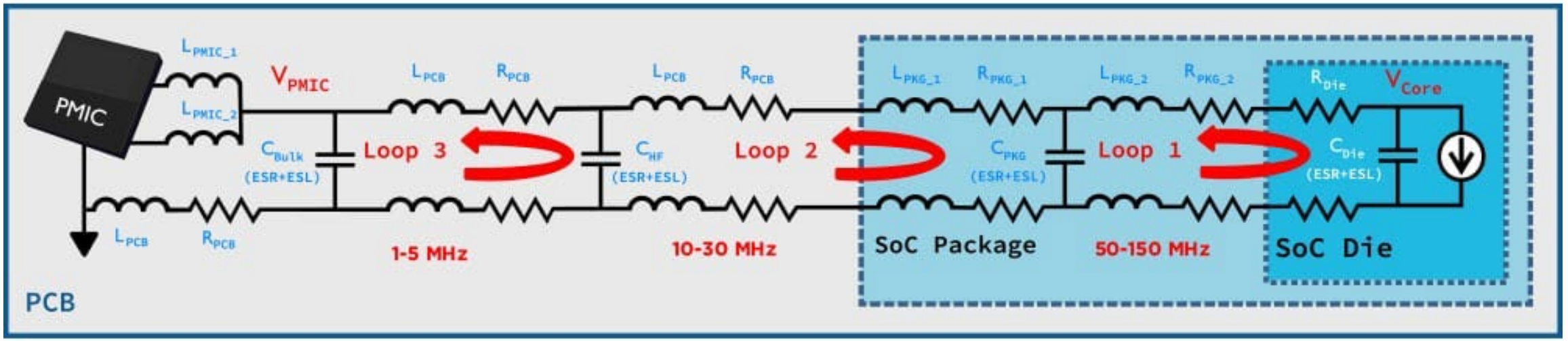
RIVR vs. PMIC Test Platform

- Provides apples-to-apples comparison of RIVR vs. PMIC performance
  - "SoC" in 16nm silicon, FcBGA package:
    - On-chip programmable, emulated high-speed, high-current load & MOS caps
    - High-speed, fine resolution on-chip transient test circuits w/ readback
    - Full integrated wide-bandwidth IVR
    - Fully programmable through GUI
  - Test Board configured to either power SoC load directly -OR- power IVR:
    - PMIC can directly power the SoC load
    - 5V → 1.8V PMU to power the IVR in the SoC

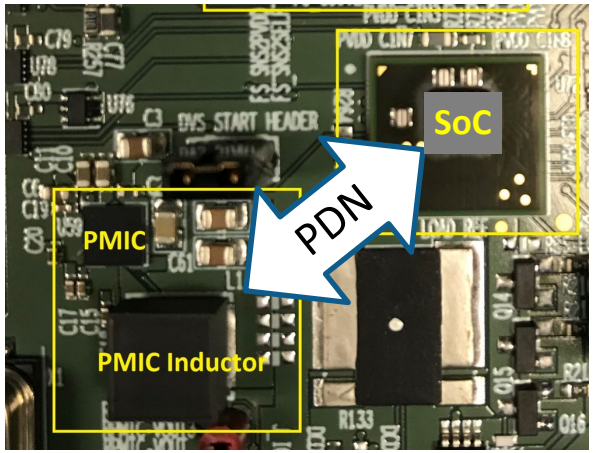




The Power Delivery Network (PDN) Problem



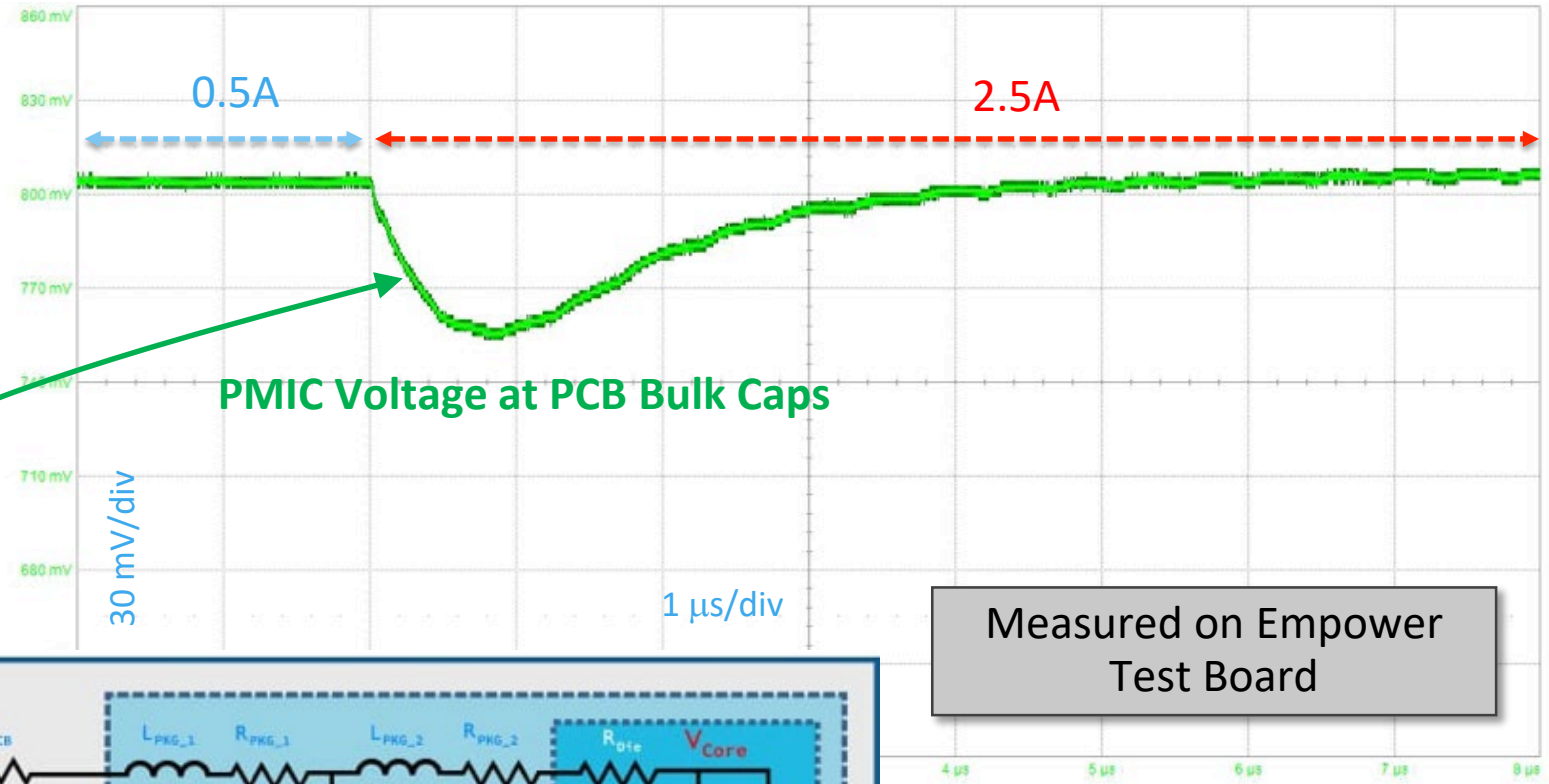
- External PMIC solutions have significant impedance between their regulated output (V_{PMIC}) and the SoC's Core (V_{Core})
- As nodes shrink, currents change much faster
- This current change through the PDN causes significant voltage excursions with long recovery times



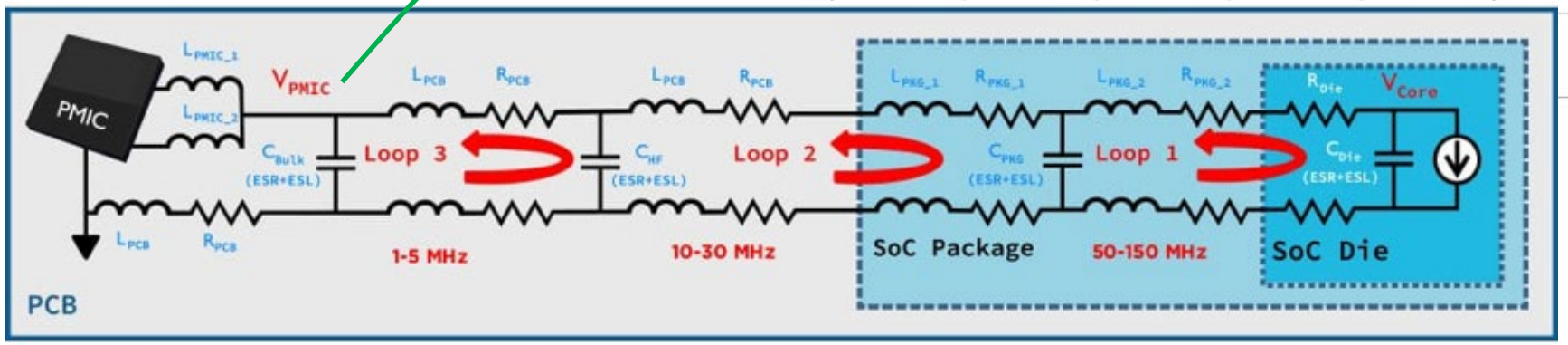
Note: Freq range is loop resonance peak impedance

PMIC Voltage Transient Response @ PCB Bulk Caps

- Typical 3-5% accuracy at the PMIC bypass caps on the PCB
- Empower Test Board:
  - ~ 45mV dip
  - 4µs recovery time



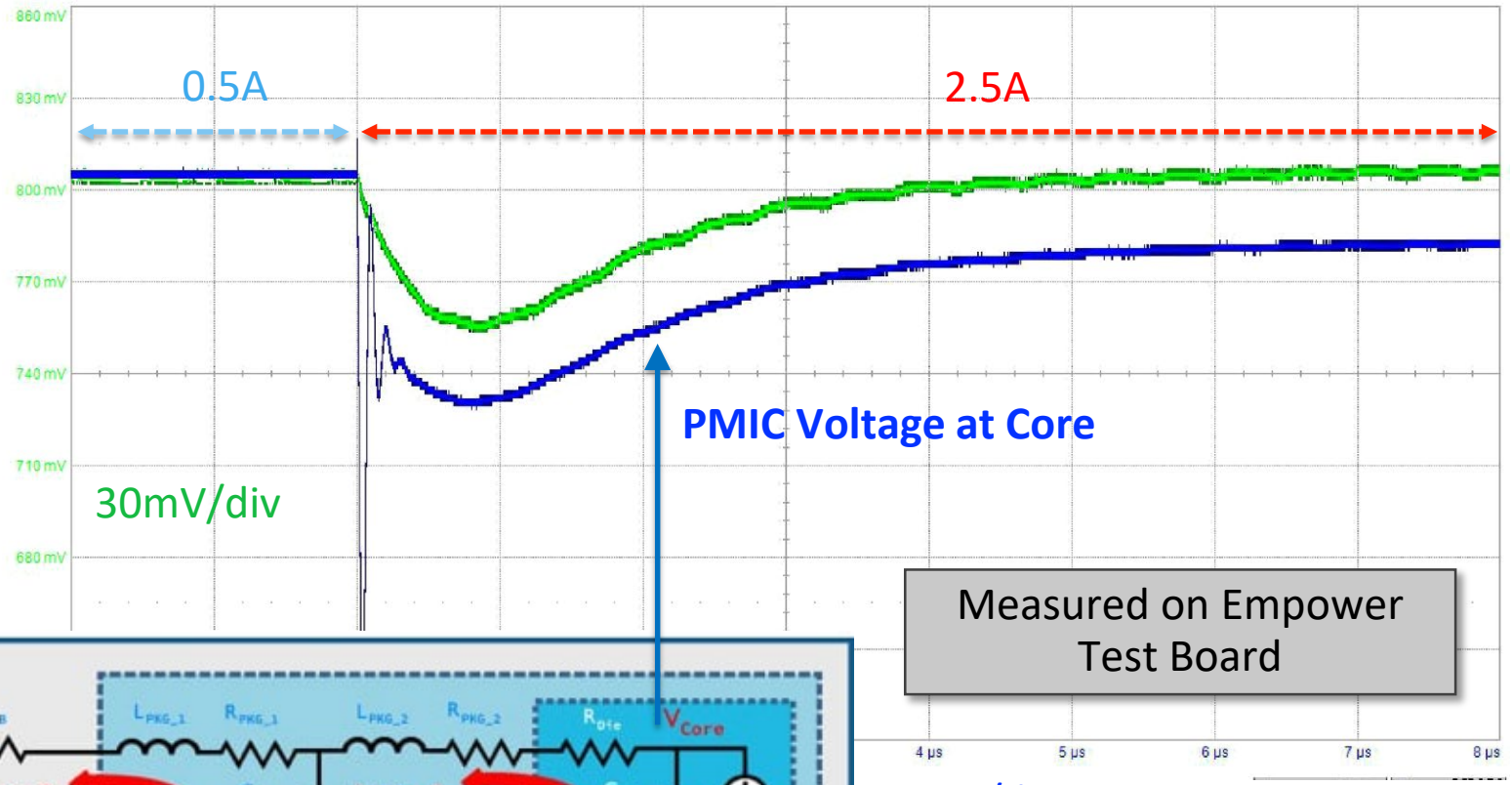
Measured on Empower Test Board



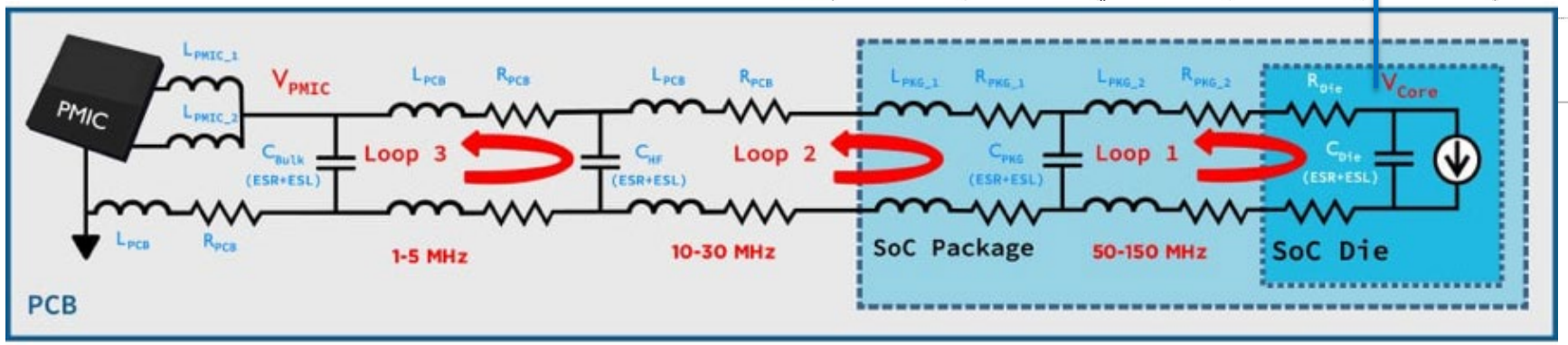
Transient: 0.5A → 2.5A in 10ns

PMIC Voltage Transient Response @ the SoC Core

- Typically 10-20% accuracy
- Empower Test Board
  - ~ 150mV dip
  - 5µs recovery time
  - DC drop in Blue curve includes PCB sense resistor of 10mΩ



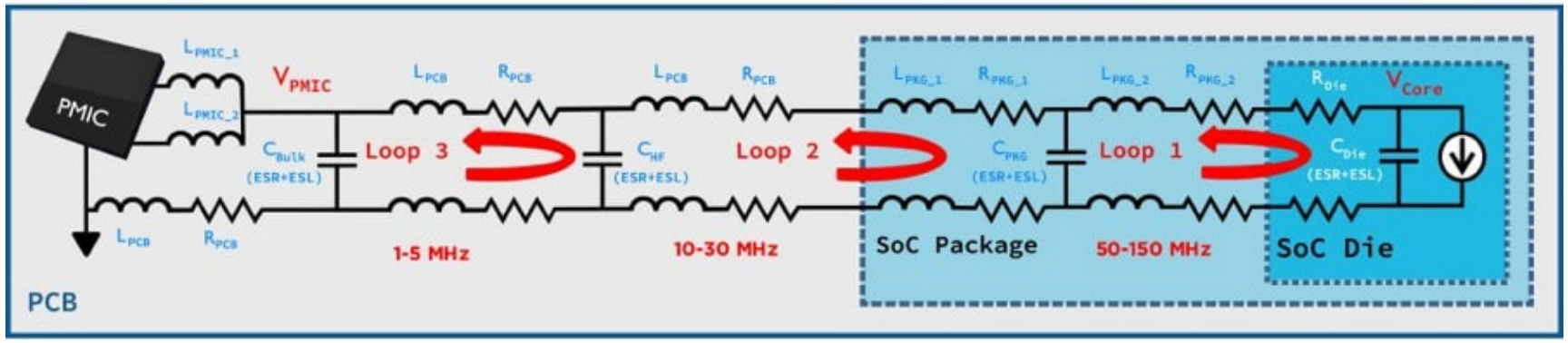
Measured on Empower Test Board



Transient: 0.5A → 2.5A in 10ns

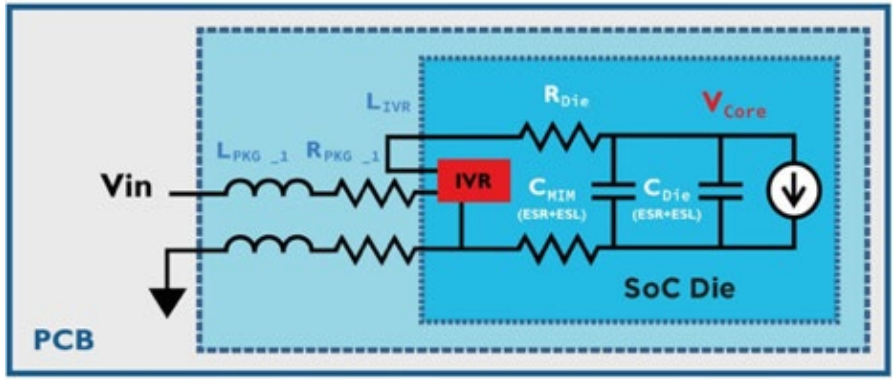
RIVR Solves the PDN Problem

PMIC PDN



RIVR PDN

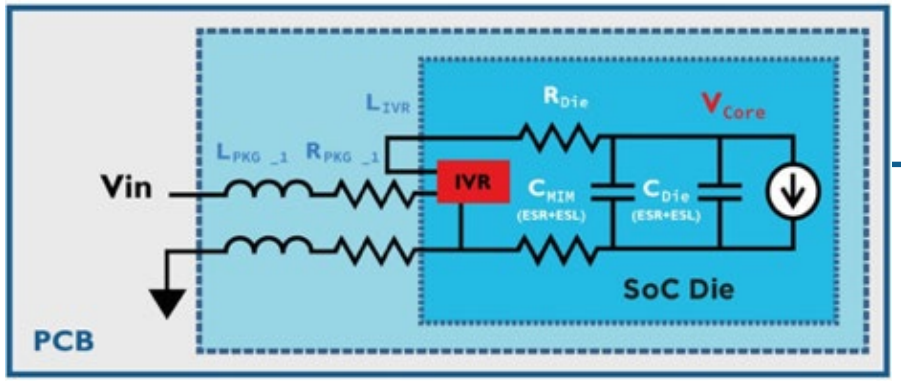
RIVR lowers the impedance to the SoC over a wide frequency band



RIVR Solves the PDN Problem

- RIVR delivers very tight voltage accuracy at the core
  - Very small voltage dip
  - Ultra-fast recovery
  - Ability for nearly zero DC drop

Contact Empower for Data

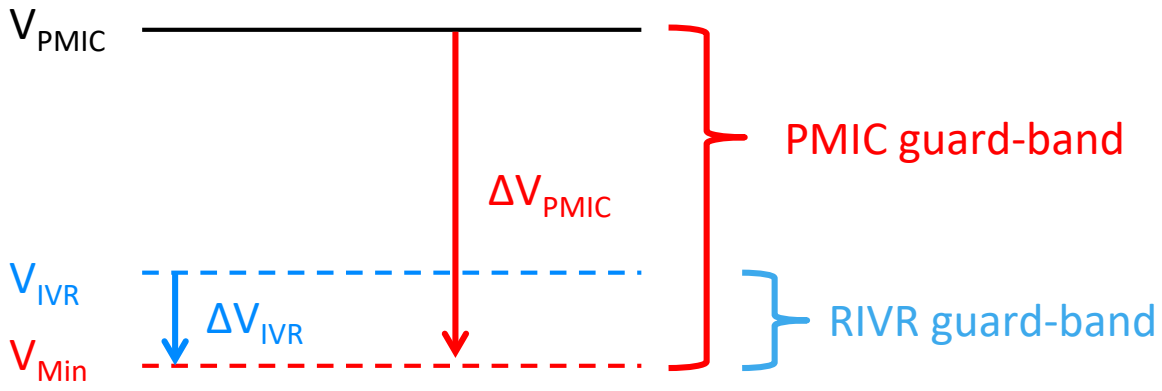


Measured on Empower Test Board

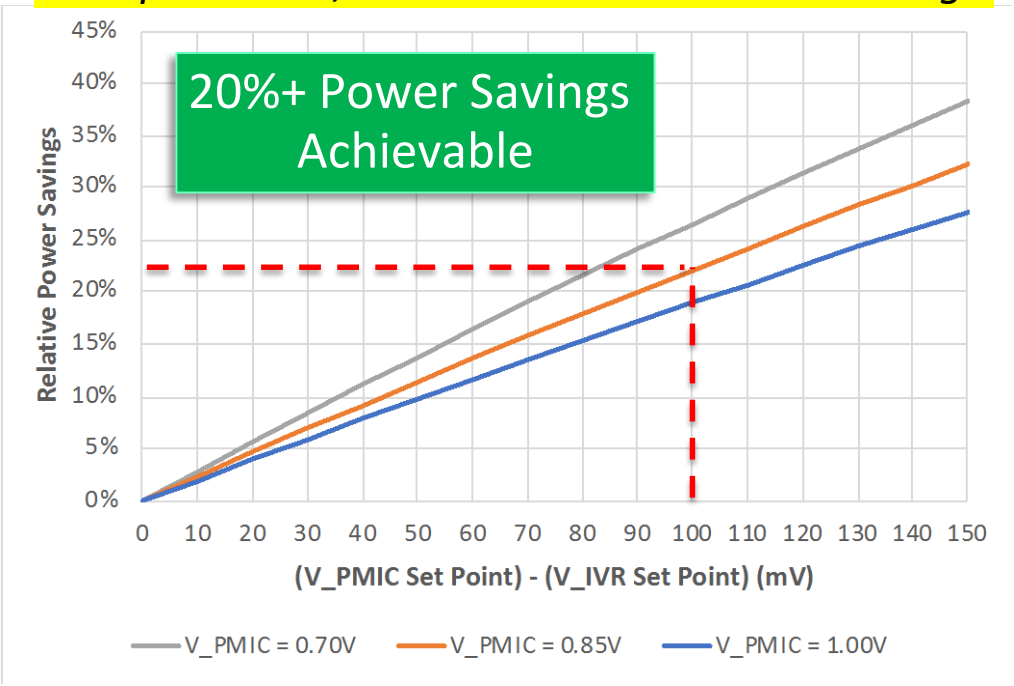
Transient: 0.5A → 2.5A in 10ns

RIVR Accuracy Reduces Voltage Guard-Band

Guard-band problem gets worse with Reduced V_{core} Voltage



Example: 0.85V, 100mV ΔV = 23% Power Savings



V_{Min}	Lowest voltage at selected operating frequency
V_{IVR}	V_{Min} + IVR guard-band
V_{PMIC}	V_{Min} + PMIC guard-band

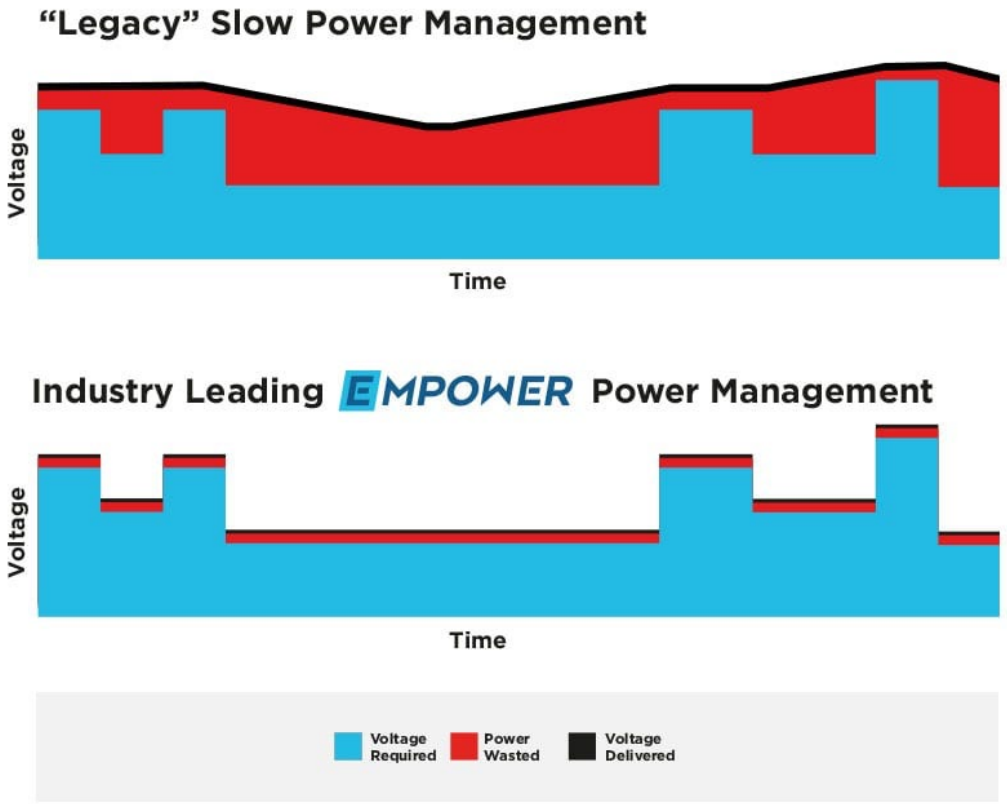
$$\textbf{Power Savings} = 1 - \frac{(V_{IVR})^2}{(V_{PMIC})^2}$$

Benefit 2:
Ultra-Fast DVFS

Empower Enables Fast Dynamic Voltage Scaling

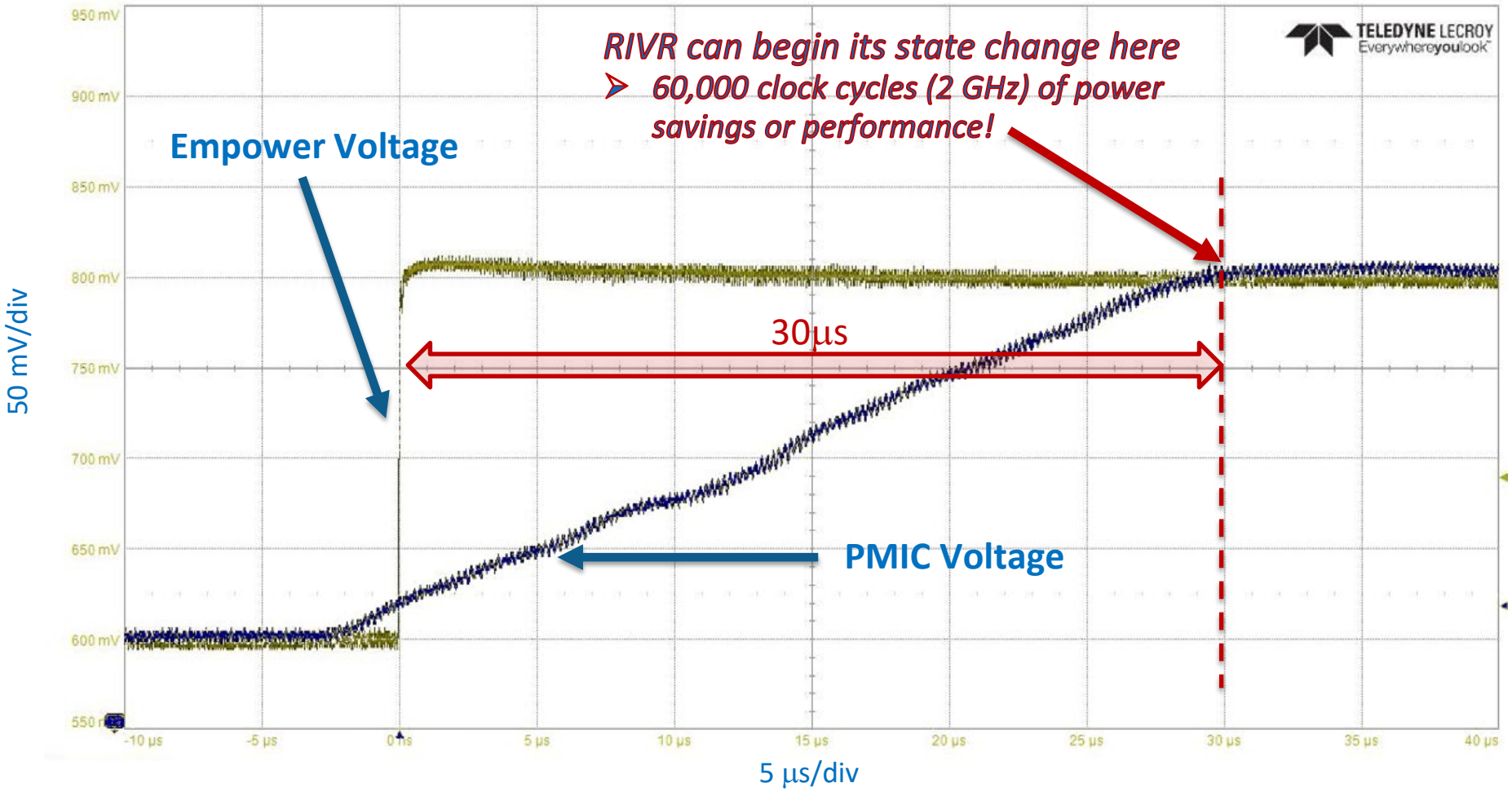
>1,000x faster power delivery translates up to 50% power savings

- **Today's Solution**
  - Existing power mgmt ICs (PMIC) are too slow to react to voltage changes of the system
  - Significant power is wasted with the excess voltage ($P \sim V^2$)
- **Empower Ultra-Fast DVS**
  - Nearly instantaneous voltage delivery eliminates the excess voltage & wasted power
  - >1,000x faster voltage delivery vs existing PMICs
  - 30-50% power savings achieved



Empower RIVR vs. PMIC DVS

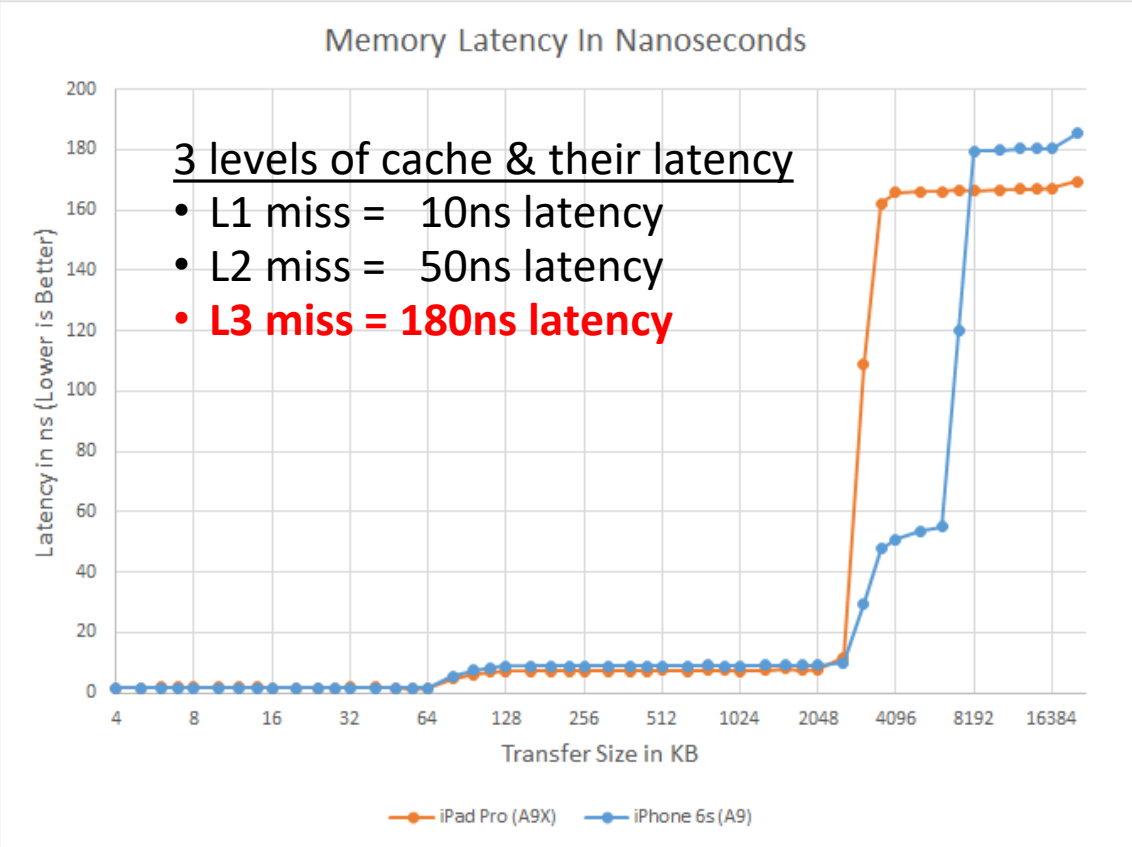
On-demand power state changes deliver much lower power loss and higher performance



Yellow: RIVR Voltage
Blue: PMIC Voltage

An Example Opportunity for Ultra-Fast DVS

Cache misses drive processor idle time at full power with a slow VR



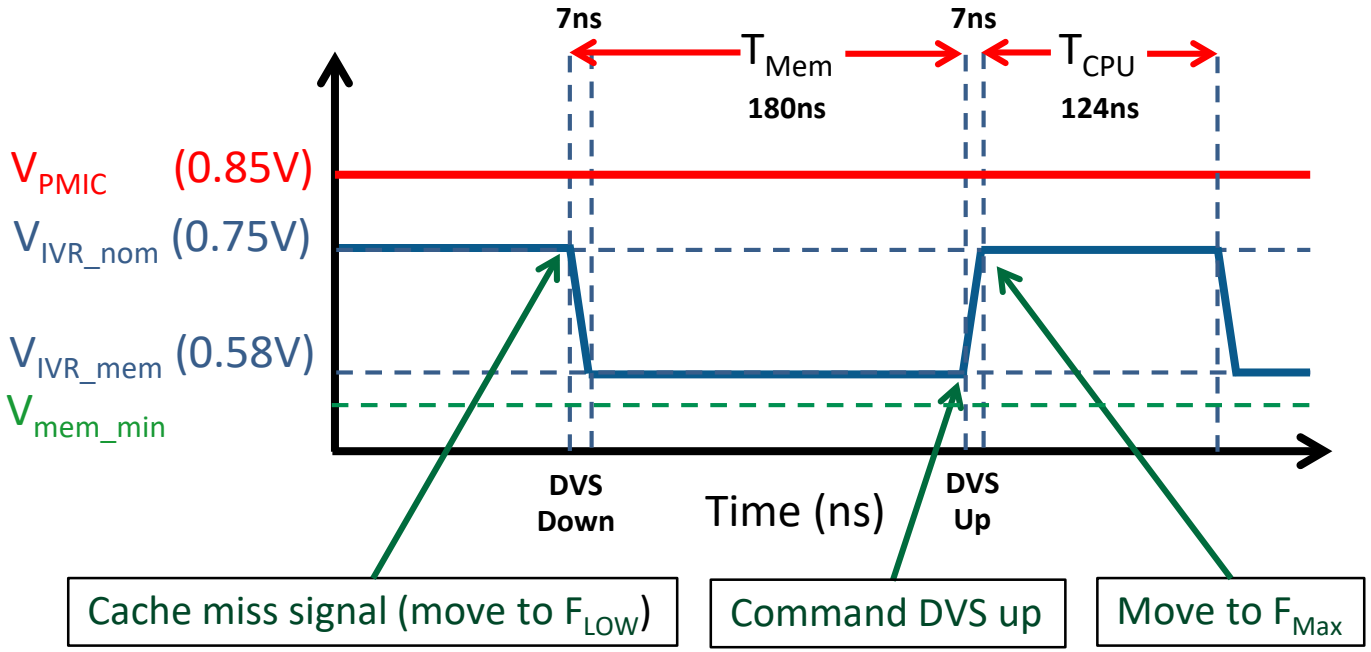
- Assumptions:
  - 1.6 GHz processor clock
  - 0.5% L3 cache miss rate
- Every 200th clock cycle is a 180ns cache miss wait cycle at full power
  - CPU work time: 199 cycles / 1.6 GHz = 124ns
  - CPU wait time = 180ns
  - Work Duty Cycle: 41%

Source: www.anandtech.com

A wide-bandwidth VR can take advantage of memory latency

RIVR™ DVFS Energy Savings Potential During Cache Miss

Utilize Ultra-Fast DVS saves energy during cache misses ($P \propto F * V^2$)



Metric	VR Type	Operating Segment			SoC Total per Cycle
		Mem Wait Cycle	DVFS (Up & Down)	CPU Cycle	
Time (ns)	RIVR	173	7 + 7	124	311
	PMIC	180	0	124	304
Avg Voltage (V)	RIVR	0.58	0.67	0.75	0.65
	PMIC	0.85	0.85	0.85	0.85
Current (A)	RIVR	4.49	5.14	7.50	5.9
	PMIC	8.5	8.5	8.5	8.5
Avg Power (W)	RIVR	2.60	3.42	5.63	3.9
	PMIC	7.2	7.2	7.2	7.2
Energy (µJ)	RIVR	0.45	0.05	0.70	***1.20***
	PMIC	1.30	0	0.90	***2.20***

Model Example Assumptions:

- CPU Fmax = 1.6 GHz, 1.0 clock cycle per instruction
- CPU Fmin = 0.55 / 0.75 * 1.6 GHz = 1.24 GHz
- Cache miss rate = 0.5%
- Memory access time = 180ns (includes DVS down)
- Empower DVS up & down time of 7ns

~65% savings during wait cycle

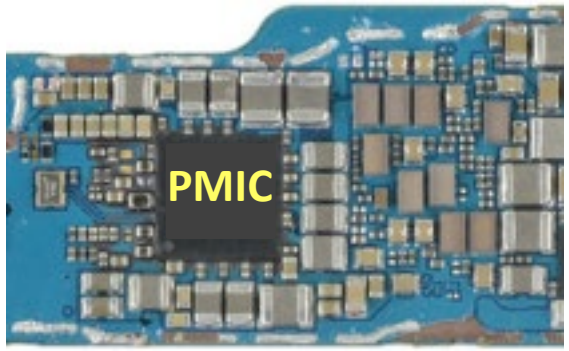
Total System Comparison → *45%* Power Savings

1-Stage Solution

8.8W

3.8V @ 2.3A
Power: 8.8W

Stage 1 (Many VRs)



Efficiency: 82%
P_{Loss}: 1.59W

0.85V @ 8.5A
Power: 7.2W

7.2W

45% Power Savings

2-Stage Solution

4.8W

3.8V @ 1.3A
Power: 4.8W

Stage 1 (Single VR)

Efficiency: 94%
P_{Loss}: 0.29W

1.8V @ 2.5A
Power: 4.5W

Stage 2

4.5W

0.65V Avg @ 5.9A
CPU: 3.85W
IVR: 0.68W

2-Stage Benefits:

- Accurate IVR lowers SoC voltage & power
- Ultra-fast IVR reduces power during CPU wait cycles
- Each stage optimized for its own V_{out} & I_{out}

Resonant IVR (RIVR™) Drives SoC Energy Efficiency

- Integration of RIVR directly in the SoC significantly lowers impedance to the processor core over wide frequency range
- Accuracy and speed drive significant energy savings
  - 44% total energy savings vs. PMIC exhibited
- Up to 80% power management area & component savings with up to 50% power management cost reduction can be realized
- Samples available in 16nm; being ported to other nodes
- Many customer projects underway