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Understanding the Dynamic Behavior in GaN-on-Si Power Devices and IC's

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Outline

- Dynamic R_{ON} and beyond
- Other important dynamic behavior
  - Dynamic V_{TH}
  - Dynamic I_{OFF}
- Integrated gate driver for enhanced reliability
  - Rail-to-rail output
  - Suppressed gate ringing and false turn-on
- Summary

Commercial GaN-on-Si power devices
COMPARISON OF KEY FIGURES-OF-MERIT

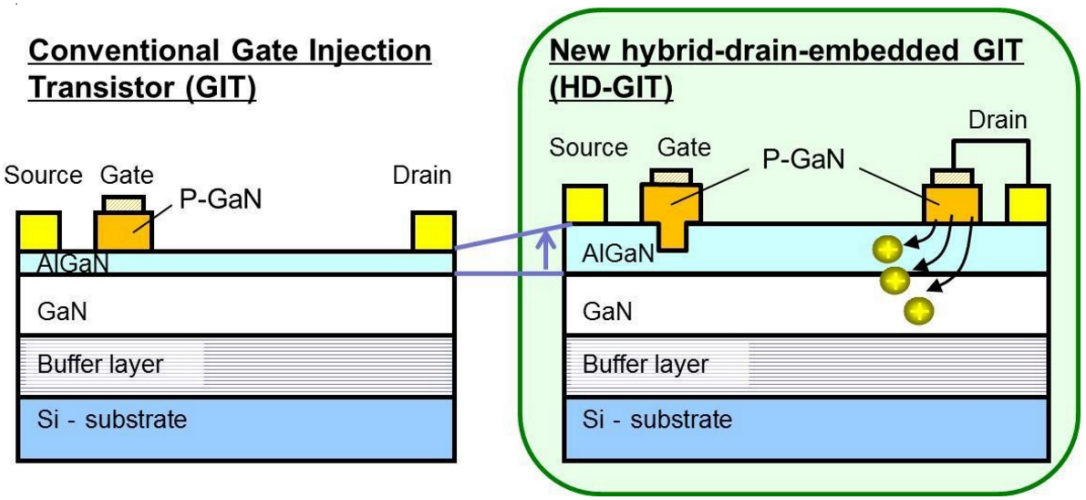
Device	Rating [V]	R_{DSON} [mΩ]	$R_{DSON}\cdot Q_{OSS}$ [mΩ·μC]	$R_{DSON}\cdot Q_{RR}$ [mΩ·μC]	$R_{DSON}\cdot E_{OSS}$ [mΩ·μJ]	$R_{DSON}\cdot Q_G$ [mΩ·nC]	V_{GS}_max [V]
Si SJ	600	56	23.5	336.0	450	3800	20
GaN E-mode GIT	600	55	2.2	2.2	350	300	N.A.
GaN E-mode	650	50	2.8	2.8	350	290	7
GaN Cascode	650	52	5	7.0	730	1460	18
SiC DMOS	900	65	4.5	8.5	570	1950	18
SiC TMOS	650	60	3.8	3.3	540	3480	22

* GIT is a current driven device typically used with an RC network and a standard gate driver.

K. J. Chen, O. Häberlen, A. Lidow, C.-L. Tsai, T. Ueda, Y. Uemoto and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," IEEE Trans. Electron Devices, vol. 64, p. 779, 2017.

Commercial E-mode *p*-GaN HEMTs

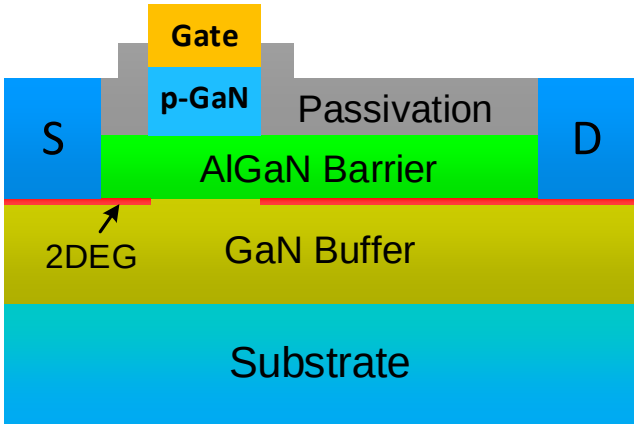
Type I: ohmic-type gate



Panasonic

Current-driving

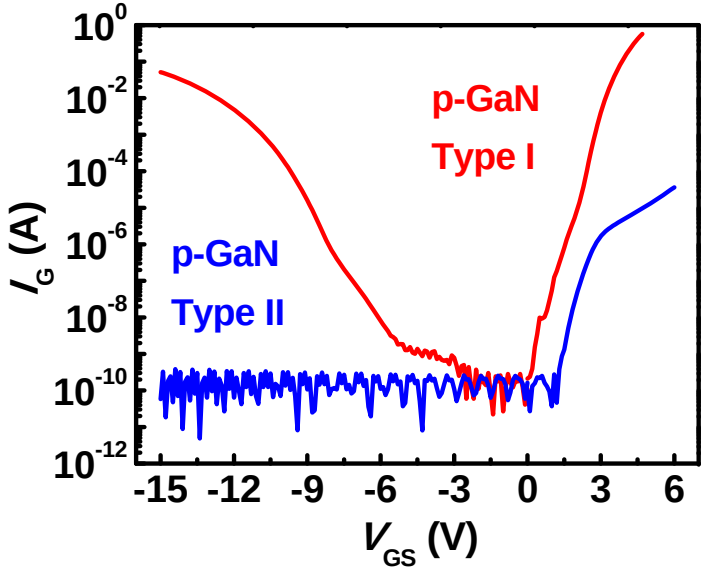
Type II: Schottky-type gate



Voltage-driving

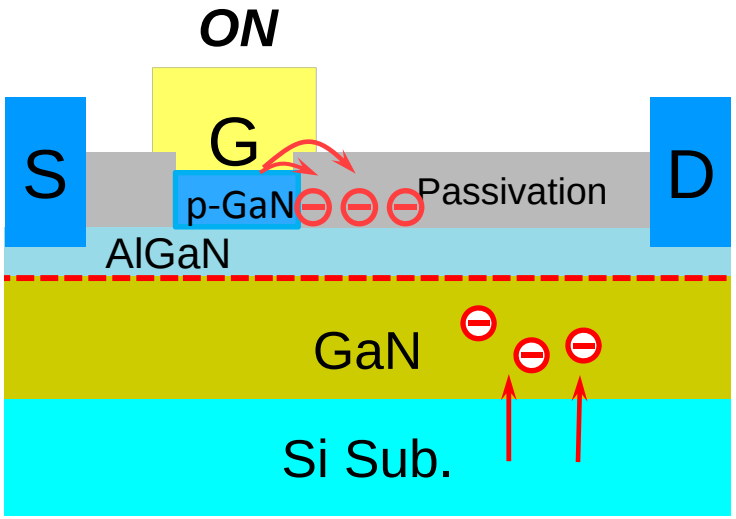
Different gate contact

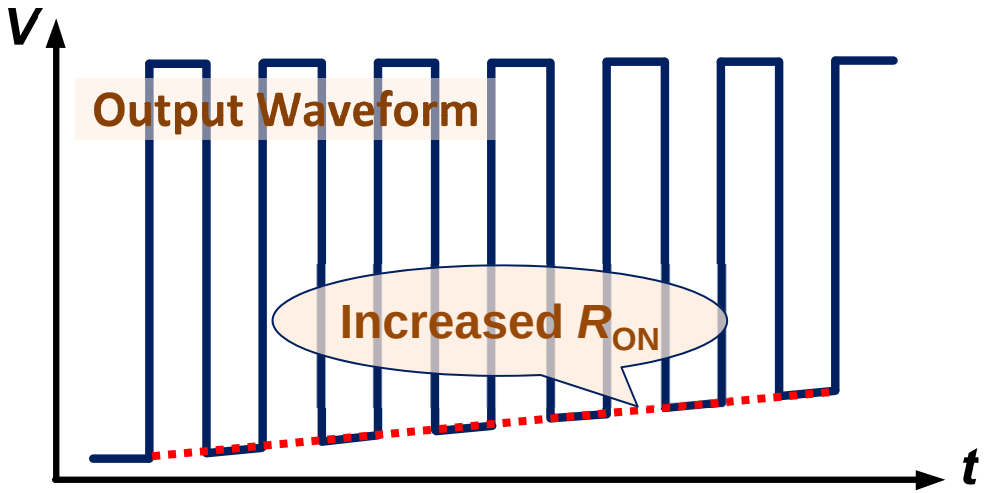
- Different gate driving schemes
- Different dynamic V_{TH} behavior



Dynamic behavior in GaN power devices

Dynamic R_{ON} has been the major focus.





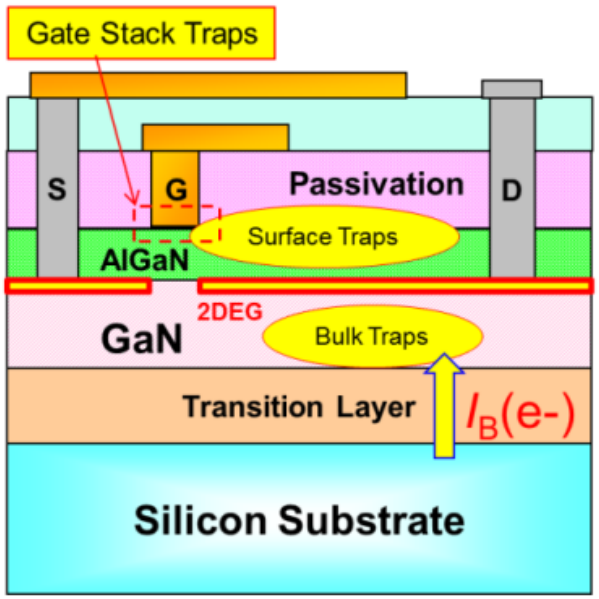
- Electron trapping at the OFF state (at large V_D)
  - Interface traps
  - buffer traps

- Reduced carrier density
- Dynamic R_{ON} degradation
- Increased V_{ON}

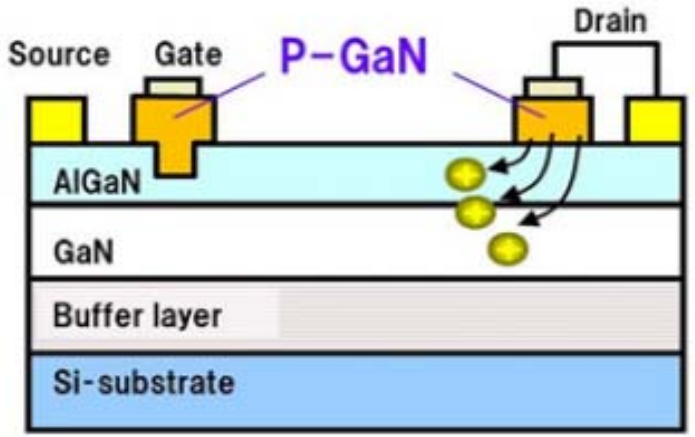
Increased conduction loss and lower efficiency!

Suppression of dynamic R_{ON} degradation

- Passivation technology + field plate
- Hole injection for trap compensation
- Buffer optimization (carbon doping profile, “leaky buffer”, etc.)



TSMC, IEDM’14



Panasonic, ISPSD’15

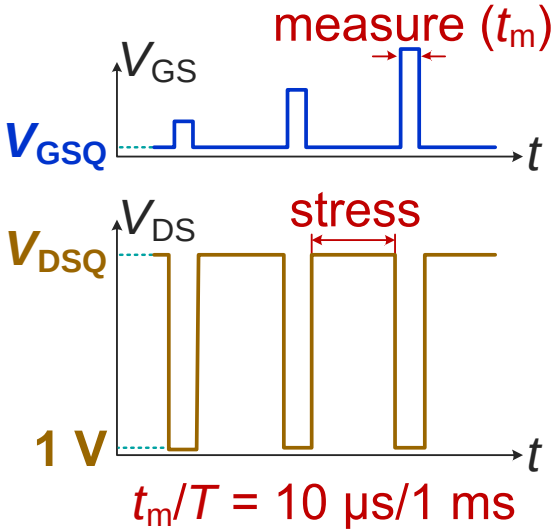
Other dynamic behavior?

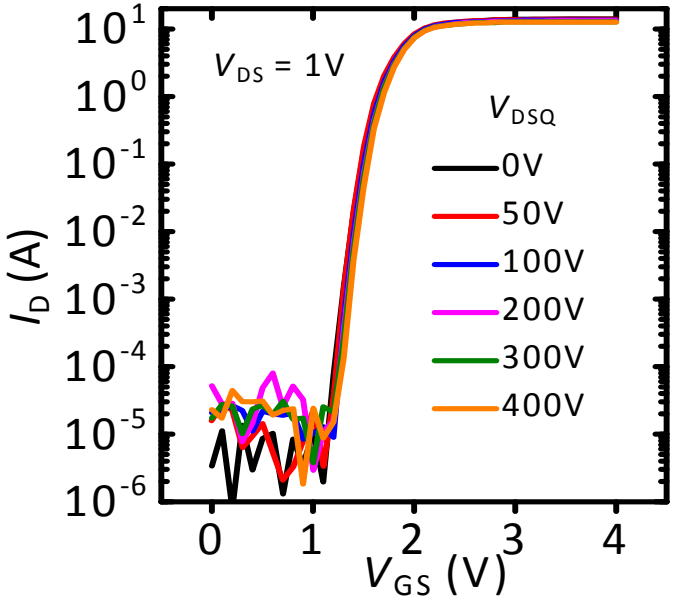
Equally important (if not more) but less studied

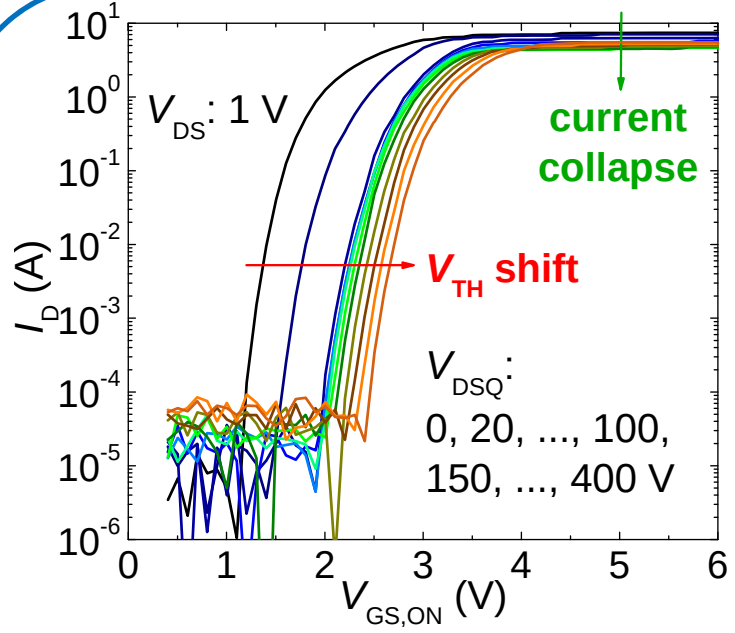
- **Dynamic V_{TH} and impact to:**
  - gate driver design (e.g. how much overdrive is sufficient?)
  - transient behavior/performance evaluation
- **Dynamic I_{OFF} and impact to:**
  - OFF-state power consumption evaluation
  - choice of *gate turn-off voltage*

Dynamic V_{TH} in E-mode *p*-GaN HEMT

Pulsed transfer curve measurement:





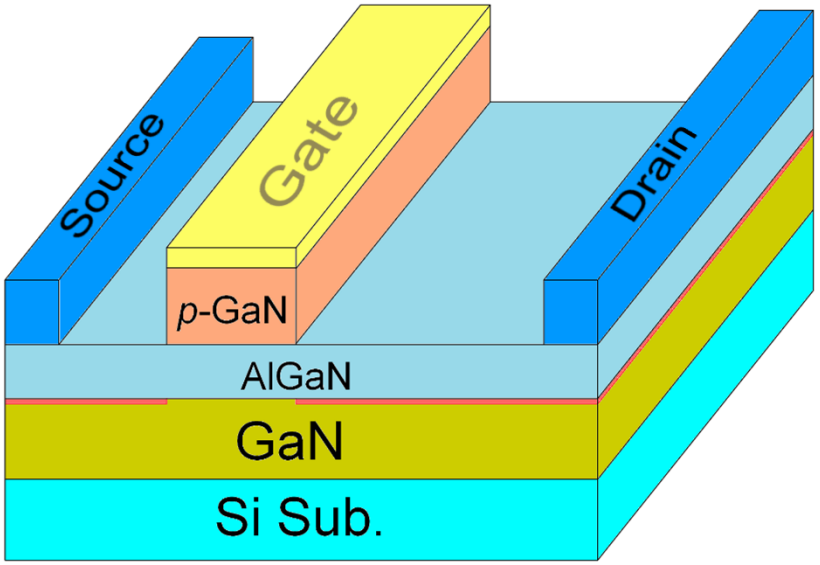


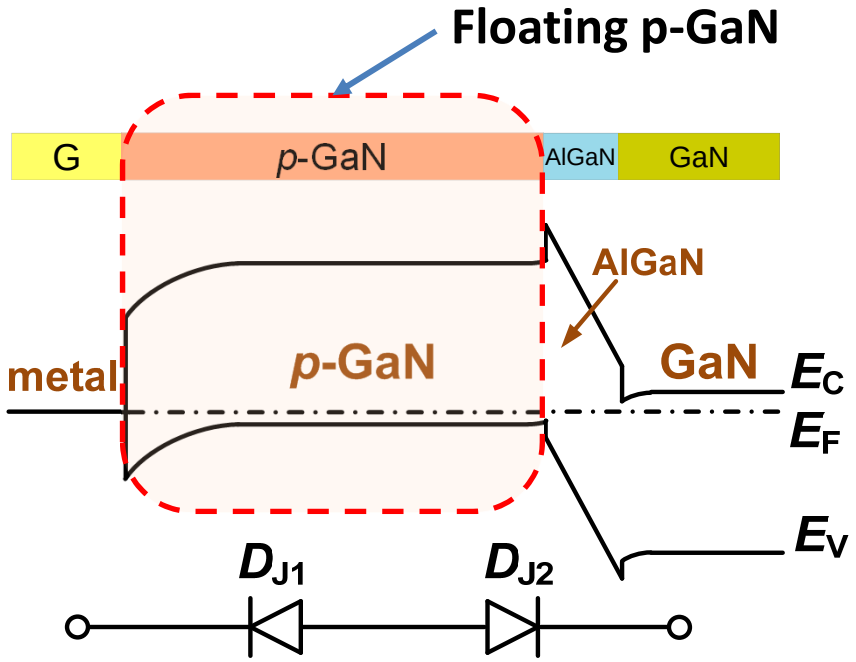
Schottky-type gate:
Drain-induced positive ΔV_{TH} as large as ~1.5 V

Ohmic-type gate, e.g. GIT:
Stable V_{TH} with small ΔV_{TH}

Dynamic V_{TH} in Schottky p-GaN HEMT

Root cause: the floating *p*-GaN





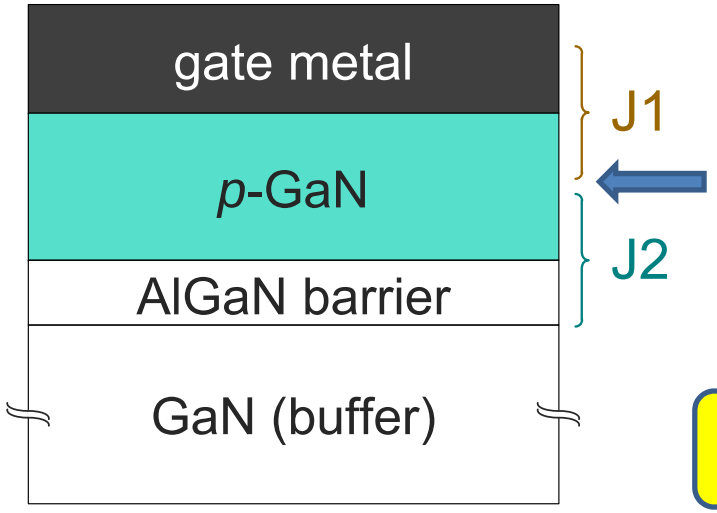
- Model: Schottky junction (D_{J1}) + p-i-n heterojunction (D_{J2})
- Charge storage/emission in the floating *p*-GaN → V_{TH} instability

Dynamic V_{TH}

Mechanism of the drain induced ΔV_{TH}

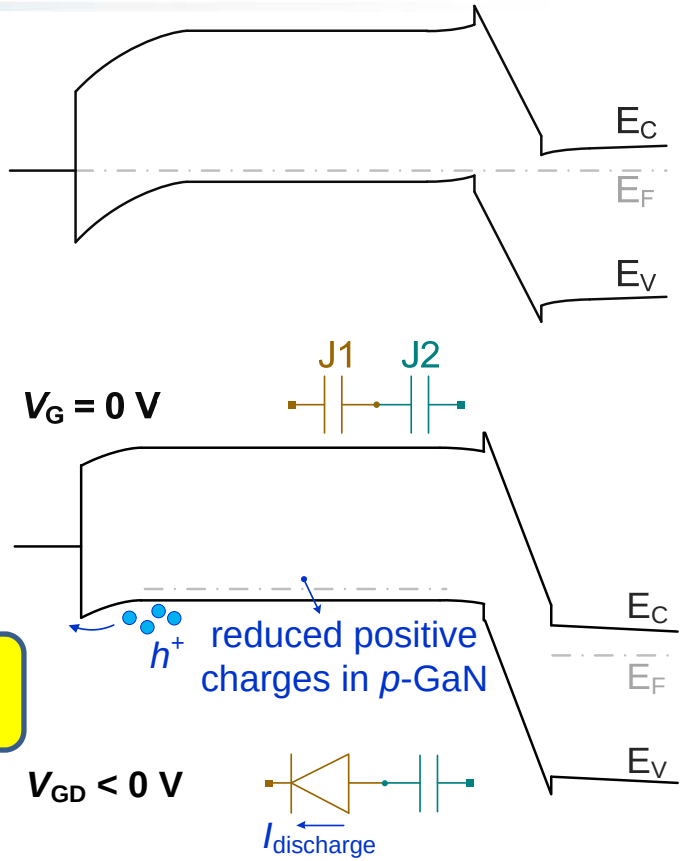
J1 & J2: back-to-back

p-GaN: floating



"floating"

High drain bias
OFF-state



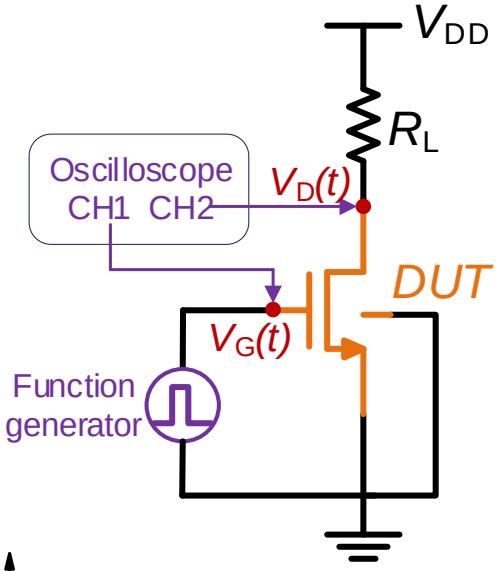
Stress: $V_{GD} < 0$, J1 forward-biased, h^+ emission from *p*-GaN to metal

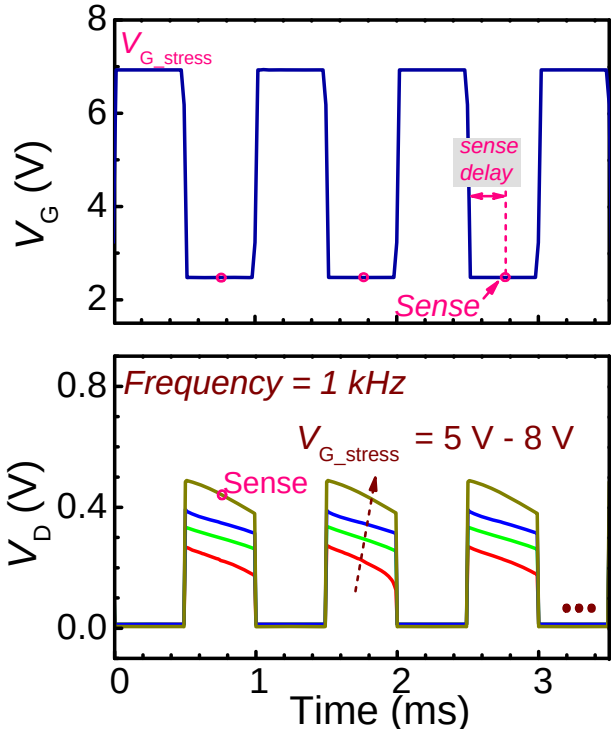
Measure: reduced positive charges cannot be recovered immediately.

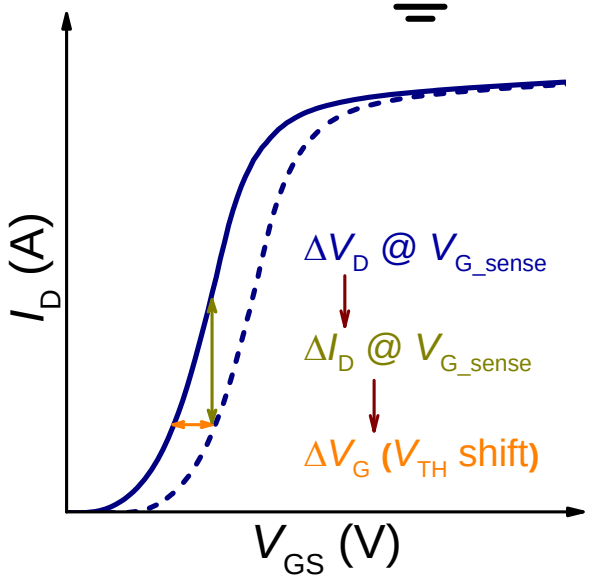
Hanxing Wang, et al., "Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic R_{ON} Degradation and Circuit Design Considerations," *IEEE Trans. Power Electronics*, July, 2017

Gate induced ΔV_{TH}

Dynamic gate stress







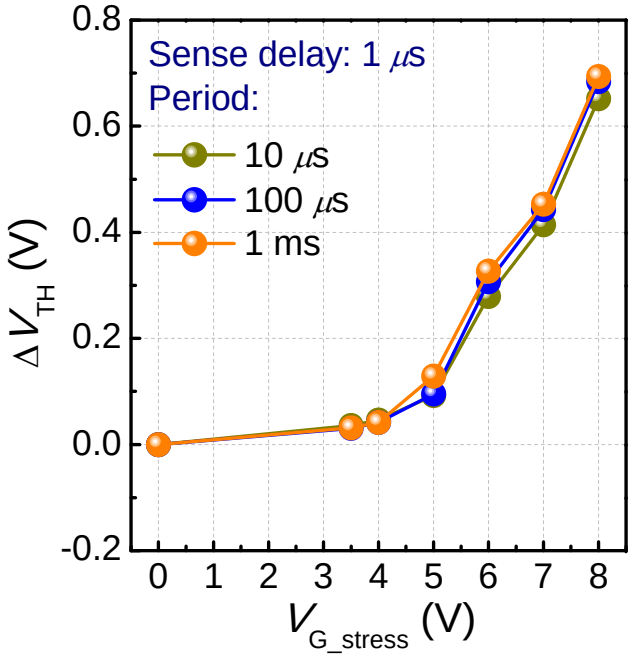
$$I_D = \frac{V_{DD} - V_{DS}(t)}{R_L}$$

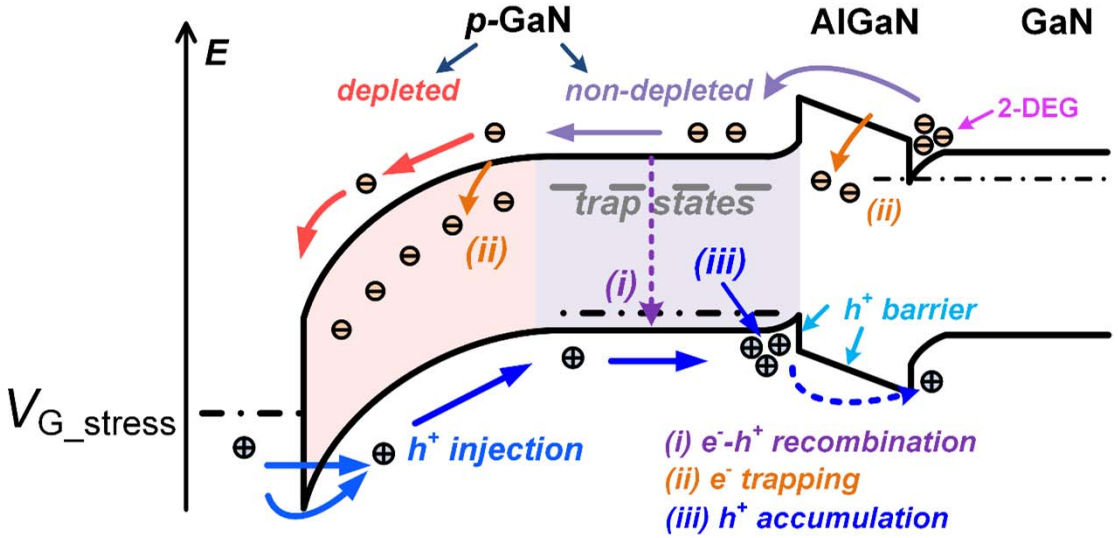
- Dynamic V_{TH} is extracted from V_D(t).

Gate induced positive ΔV_{TH}

Positive V_{TH} shift after gate turn-on

Mechanism: electron trapping in the depleted region of the *p*-GaN layer

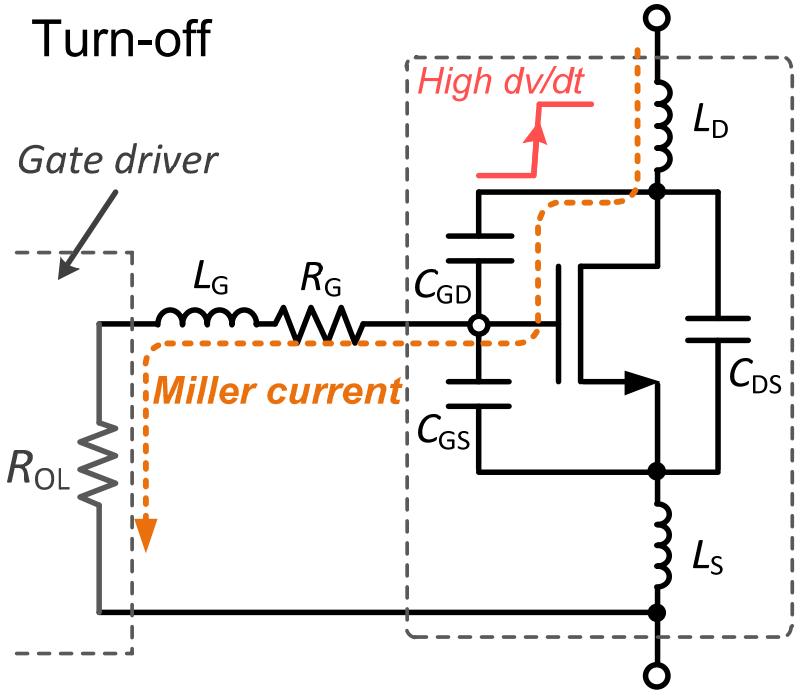


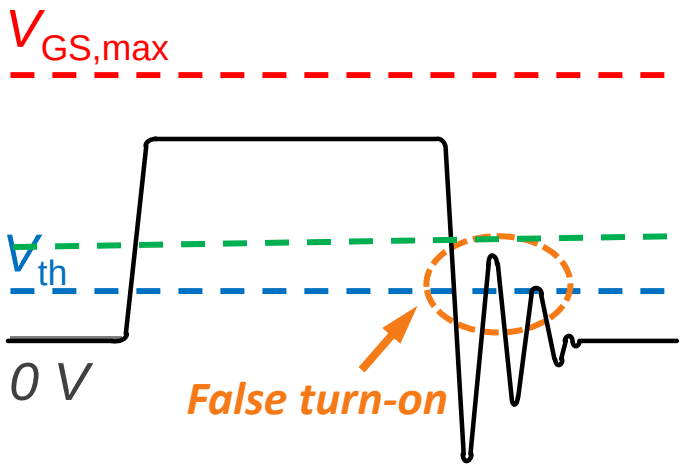


J. He, T. Gao and K. J. Chen, IEEE Electron Device Lett., p. 1576, Oct. 2018.

Impact of V_{TH} shift

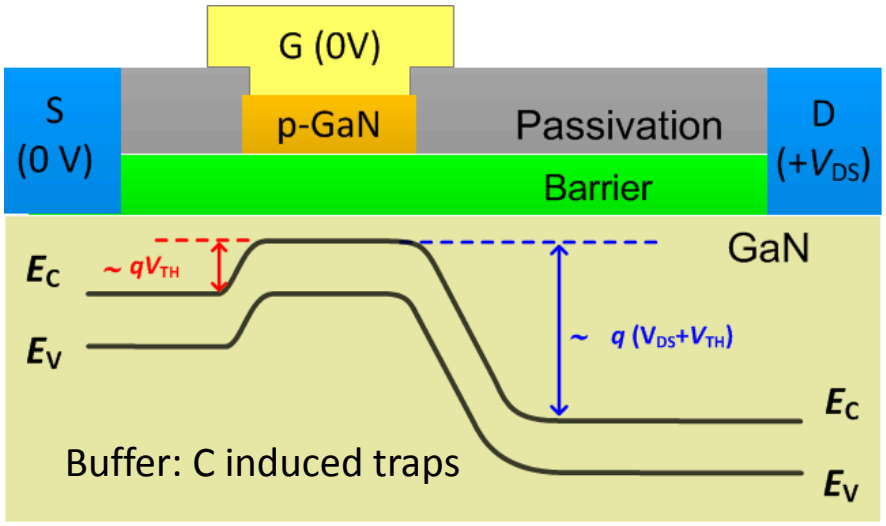
- **Drain induced positive ΔV_{TH}** → more positive V_G (i.e. gate overdrive) to turn on the switch and narrower $V_{G,ON}$ range
- **Gate induced positive ΔV_{TH}** → raised V_{TH} at OFF state → enhanced false turn-on immunity

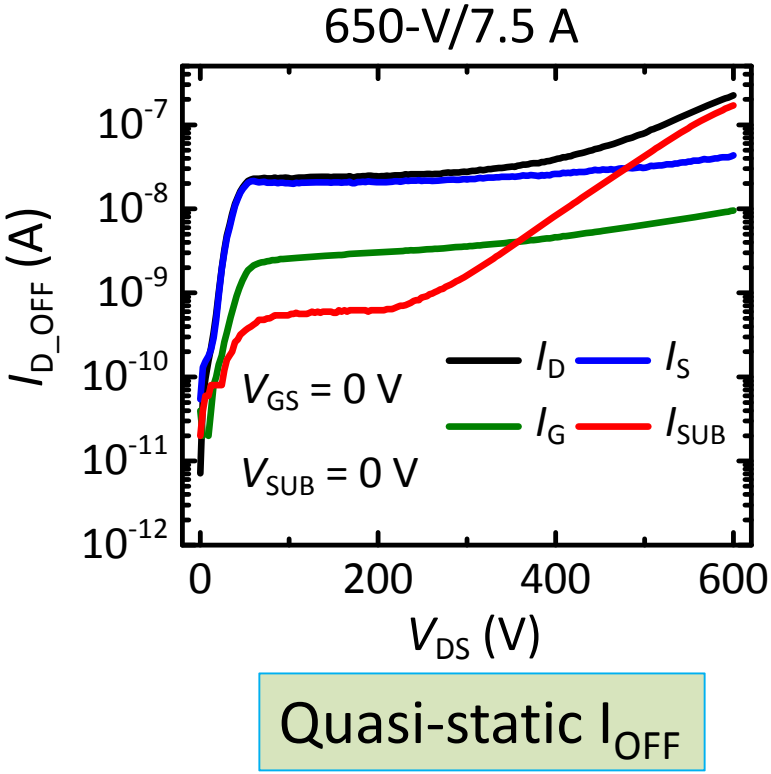




OFF-state leakage current

- No *p-n* junctions between source and drain in the leakage path (e.g. buffer layer)
- Low leakage current is attributed to the buffer with raised energy band -- a result of C-doping.

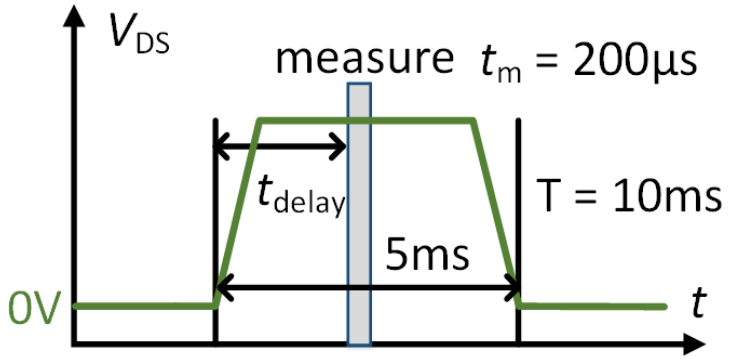


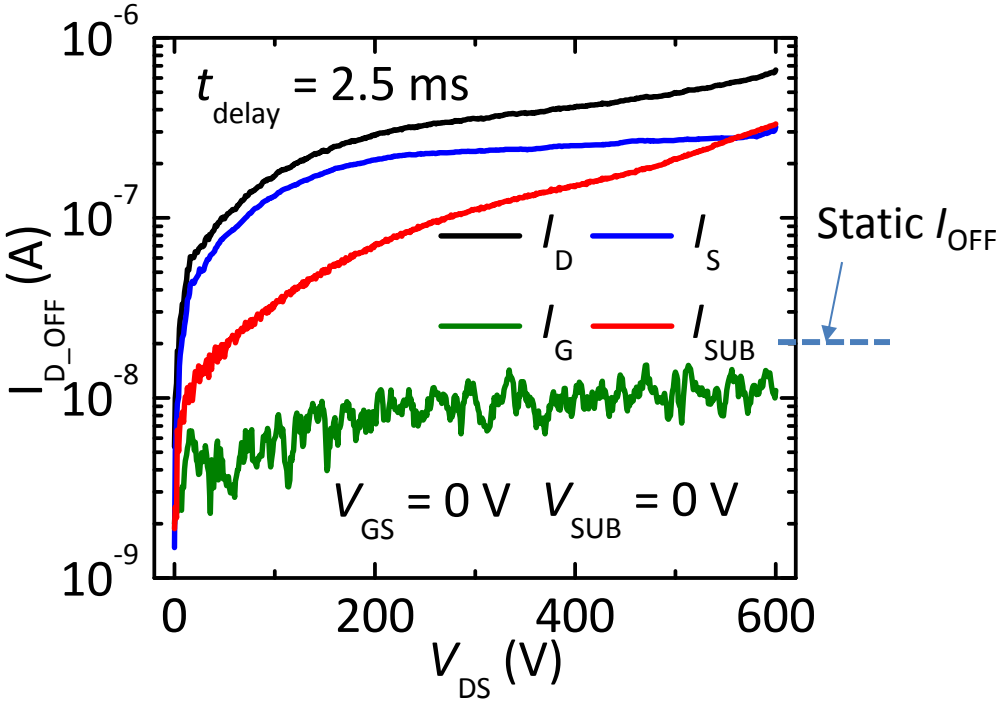


Quasi-static I_{OFF}

Dynamic I_{OFF}

Slow dynamic measurement



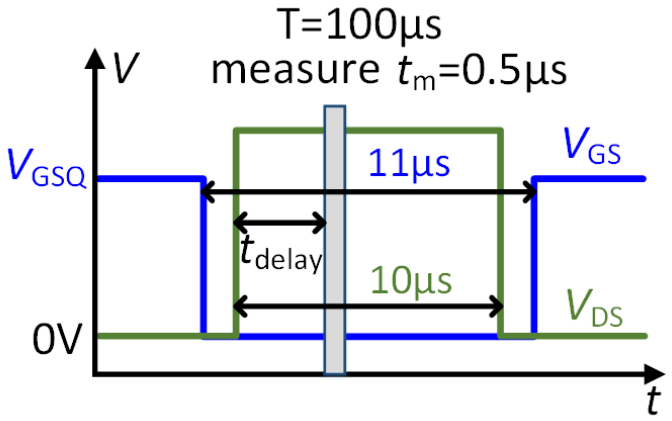


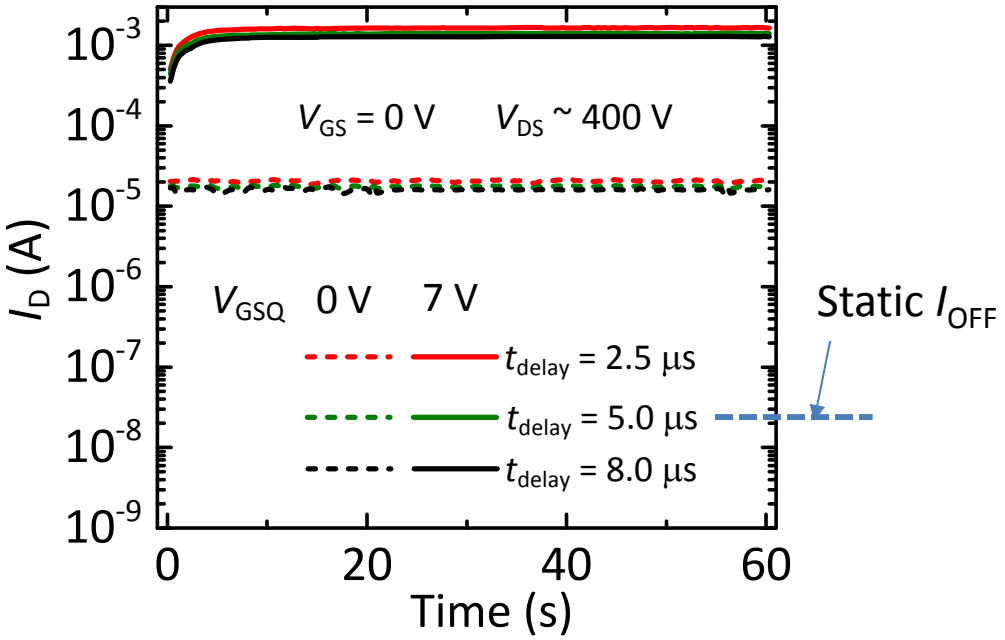
- Reduced voltage blocking capability in the buffer (both lateral and vertical)
- Reduced energy barrier due to unfilled electron traps in the buffer

Y. Wang, et al., IEEE EDL, p. 1366, Sep. 2018

Dynamic I_{OFF} under fast switching

fast dynamic measurement



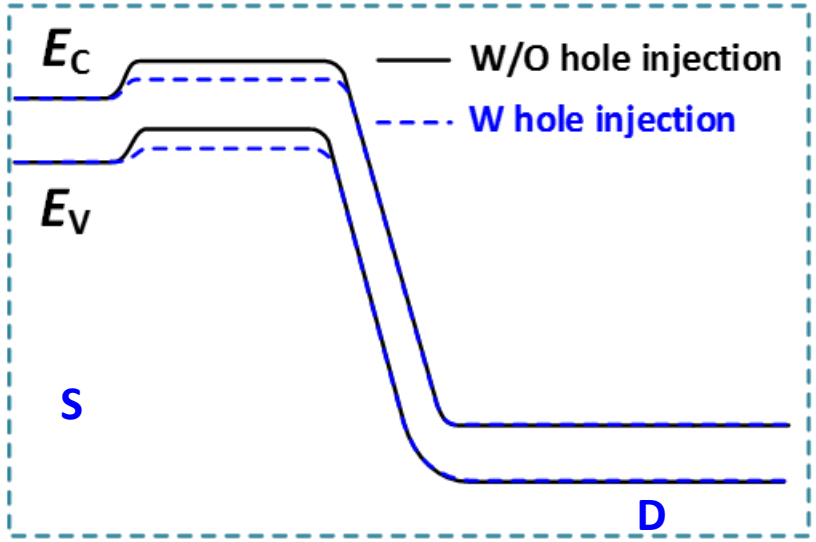


Dynamic I_{OFF} vs. Static I_{OFF}

- 1000 x increase without turning on the switch
- 10^5 x increase after $V_{G,ON}$ = 7 V → induced by hole injection into the buffer

OFF-state power loss is ~10% of the ON-state conduction loss.

Dynamic I_{OFF} increase from hole injection

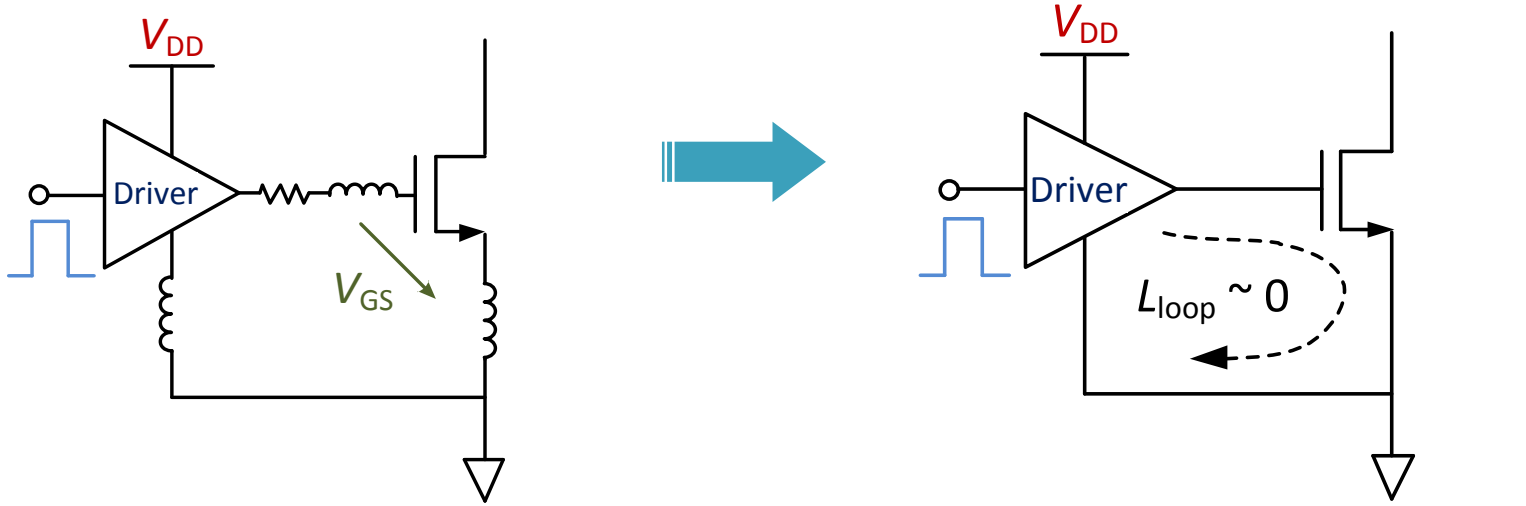


Hole injection into the buffer → lower barrier

Critical gate drive margin

- Lower threshold voltage V_{th} ⇨ False turn-on (miller effect)
- Narrower gate drive voltage $V_{GS,ON}$ ⇨ Lower noise immunity (gate ringing)

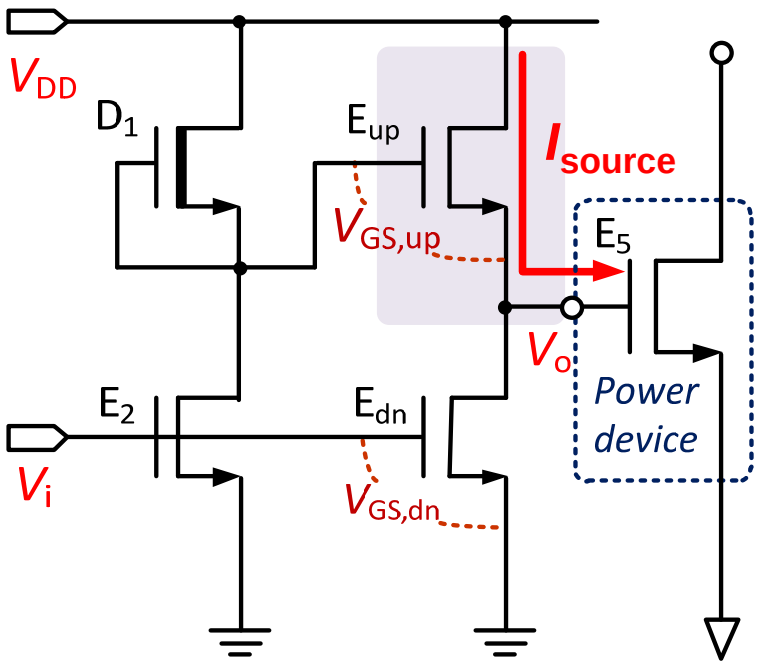
Suppression of parasitic inductance by integration

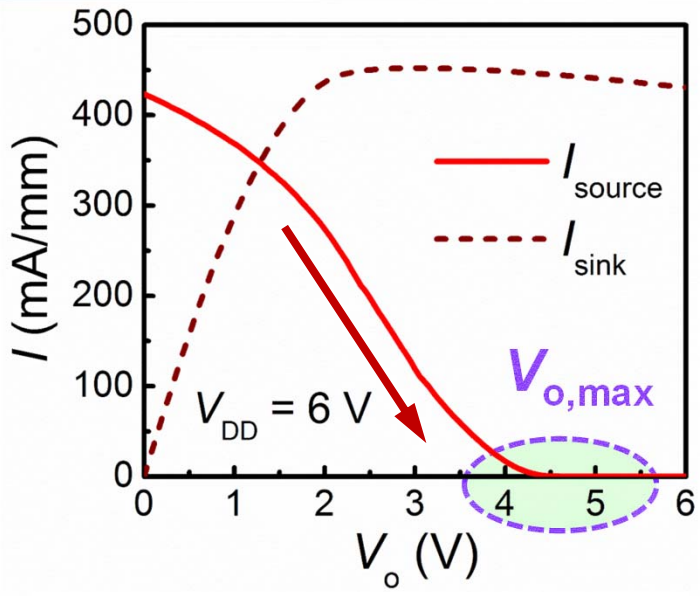


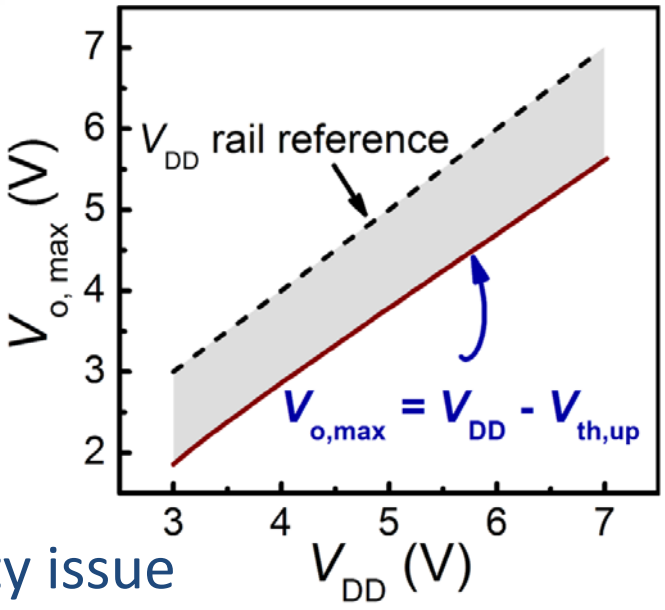
Si driver + GaN switch

GaN driver + GaN switch

Gen-I integrated gate drive: issues





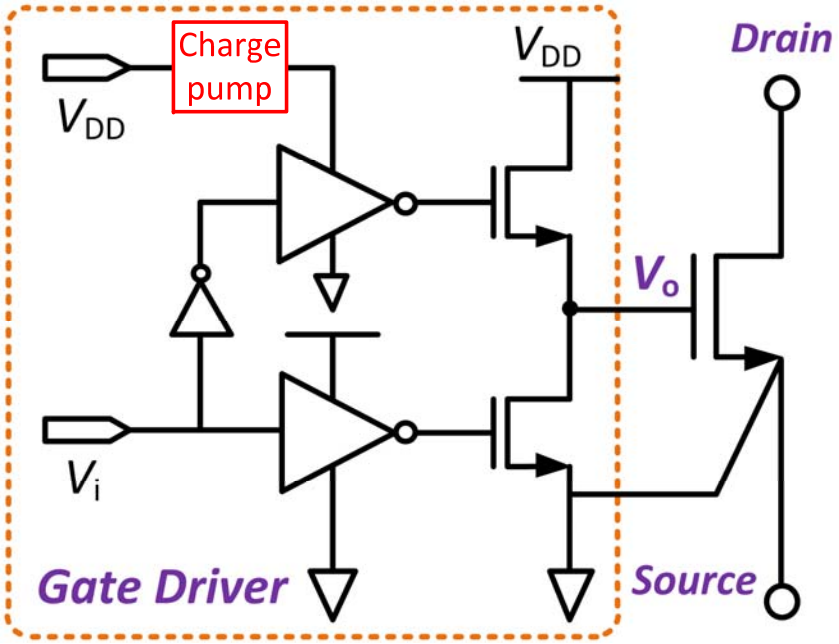


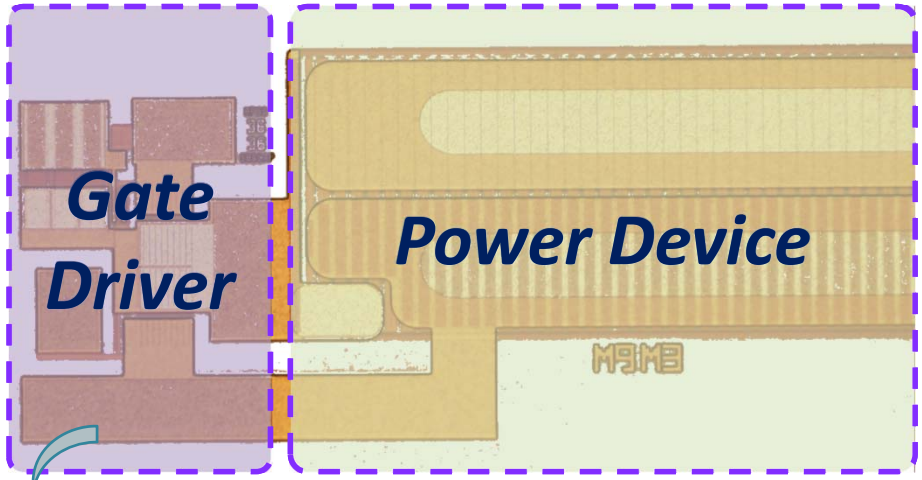
During the charging process:

- Charging current reduction
- $V_{o,\,max} = V_{DD} - V_{th,up}$

- Larger V_{DD} (> 7.5 V)
  → exceeding $V_{G,max}$ → gate reliability issue

Gen-II gate drive scheme

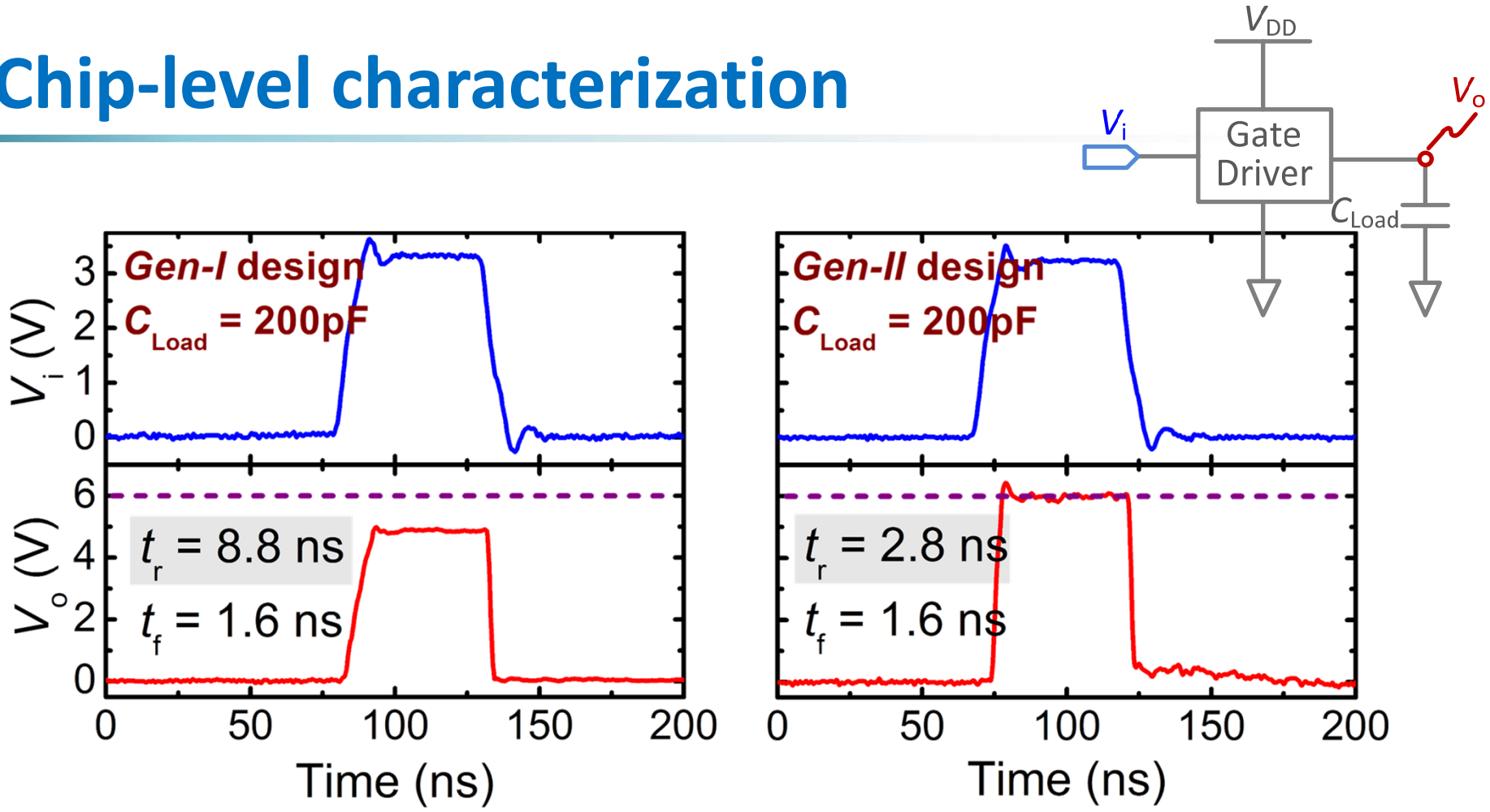




Novel gate driver design (Gen-II)

- Charge pump unit → Help maintain the charging current
- Chip size: 4.6 mm × 1.1 mm (~5 mm^2 including 130-mΩ switch)

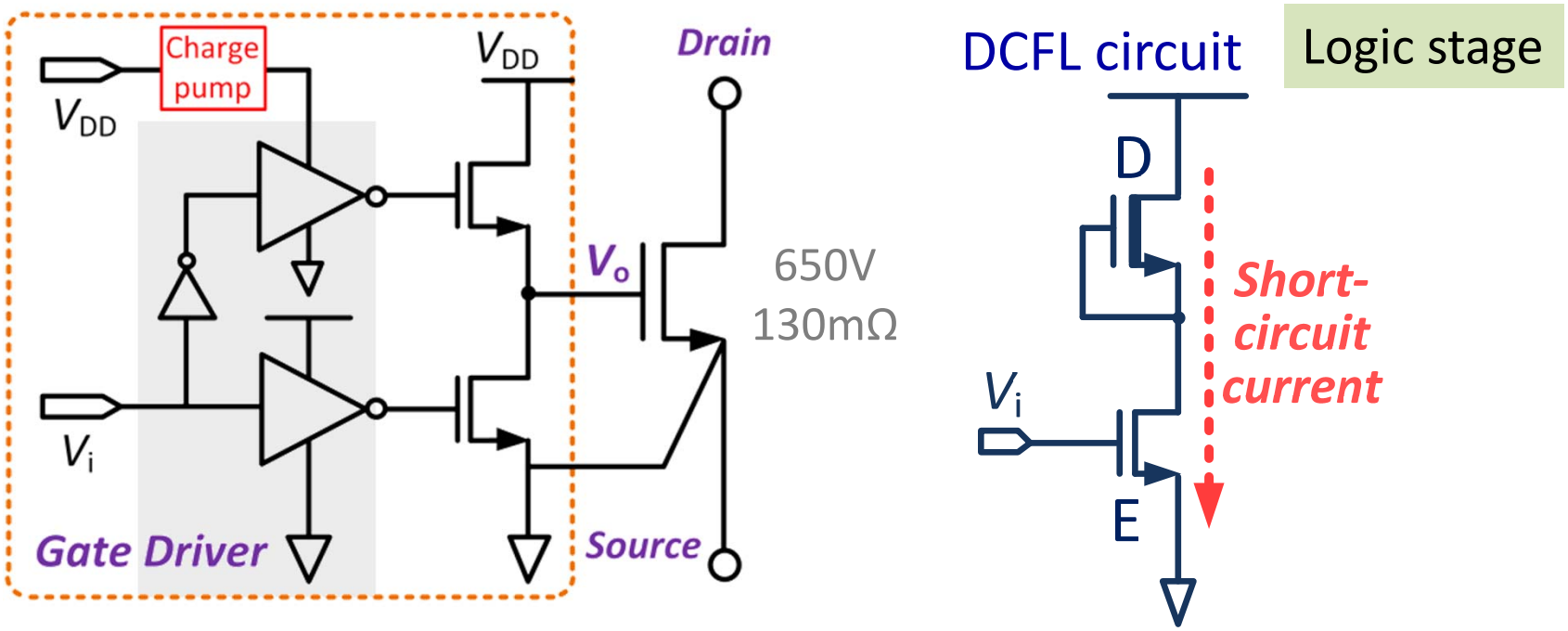
Chip-level characterization



Driving capability

The *Gen-II* gate driver can provide with both enhanced driving capability (3X) and rail-to-rail output ($V_{o,max} = V_{DD}$).

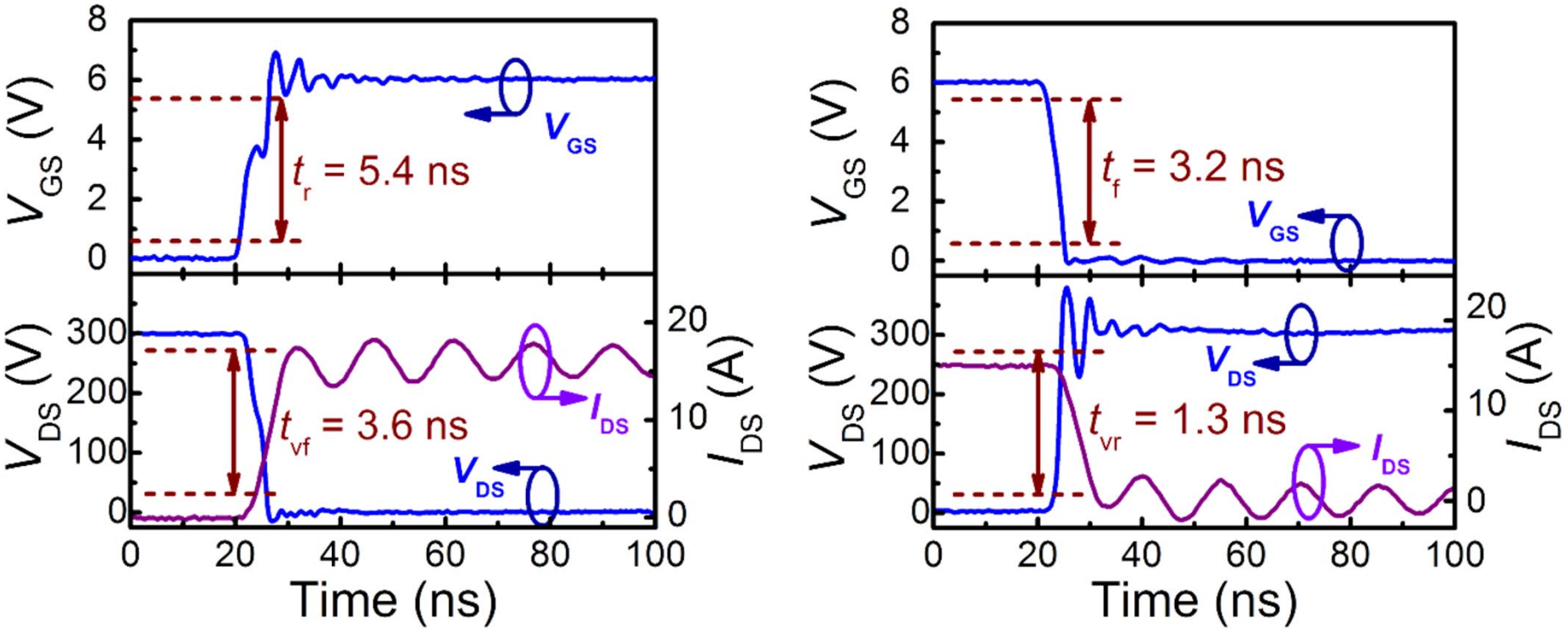
Power consumption



Power consumption (from integrated gate driver)

- Caused by the DCFL (direct coupled FET logic) circuits (not CMOS)
- Standby power consumption (I_{DD} ~ 6 mA @ V_{DD} = 6 V)

Switching performance using a double-pulse tester



- Small ringing & suppressed false turn-on
- Without the need of negative V_{GS}
- Minimum turn-off time: 1.3 ns ($dv/dt_{(max)}$ = 336 V/ns)

Summary

- In addition to dynamic R_{ON}, the deployment of GaN-on-Si power devices is also affected by other critical dynamic characteristics including
  - Dynamic V_{TH} : impact on gate overdrive $V_{G,ON}$
  - Dynamic I_{OFF} : impact on OFF-state power consumption

- Monolithically integrated gate driver leads to reduced parasitic inductance and offers several benefits including
  - Higher switching speed
  - Higher tolerance of tight gate driving voltage range

Thank you!

Acknowledgement

Collaboration and support:

- TSMC

Funding support:

- Hong Kong Innovation and Technology Fund