Hybrid Integrated GaN-CMOS Power Converters and High-density Modules Based on Vertical GaN Transistors

Ken Shepard

Columbia University, Ferric

Daniel Pedra, Yuhao Zhang, Min Sun, Tomas Palacios; MIT

John Barth, Kevin Tien, Eyal Aklimi, Fengqi Zhang; Columbia University

Steve Bedell; IBM

Outline

- Motivation for hybrid GaN/CMOS integration by face-to-face bonding.
- Hybrid GaN-CMOS PoL converter design using lateral GaN HEMTs
- Wafer thinning approaches for advanced packaging of power devices.
- Design of a small-form-factor 1200-V, 40-A half-bridge using vertical GaN devices

Monolithic heterogeneous integration is hard…

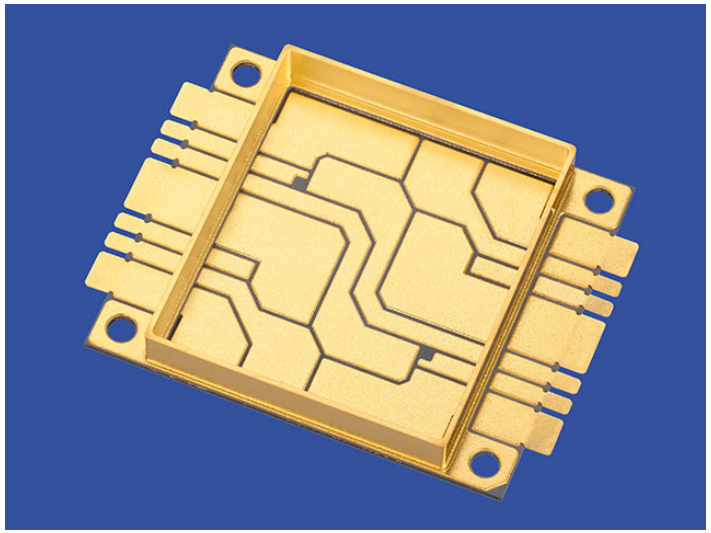
- Modern technology has traditionally been about eventual monolithic integration.
  - Generally lowest cost
  - Generally highest performance – lowest parasitics, highest interconnect density
- For III-Vs, people have been trying for a long time. GaAs-on-Si, GaN-on-Si.
  - Thermal budgets are challenging
  - Contamination issues are real
  - Economics are hard – yield issues are more challenging.

Packaging used to be “boring”… but things are changing

- Packaging technologies are moving to the fore in mainstream electronics
- These new packaging approaches support heterogeneous integration of different technology nodes, semiconductor technologies, and passives
- Power electronics packaging and “regular” packaging are converging.
  - Power dissipation and current levels in “traditional” electronic systems are rising. “Traditional” electronics is power electronics.
  - Increasing levels of integration and higher operating frequencies are driving power systems to higher fan-out requirements and lower interconnect parasitic requirements.
  - WBG semiconductors only accelerate these trends.

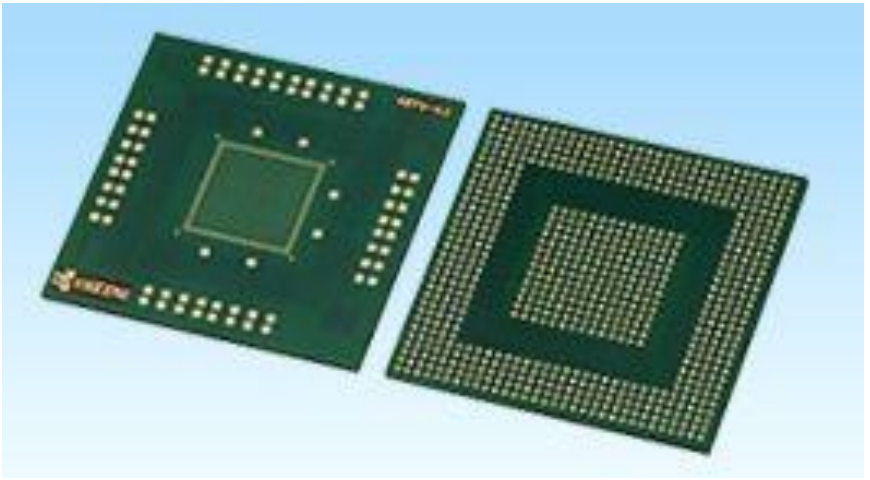
Traditional packaging approaches

- **Ceramic packages**



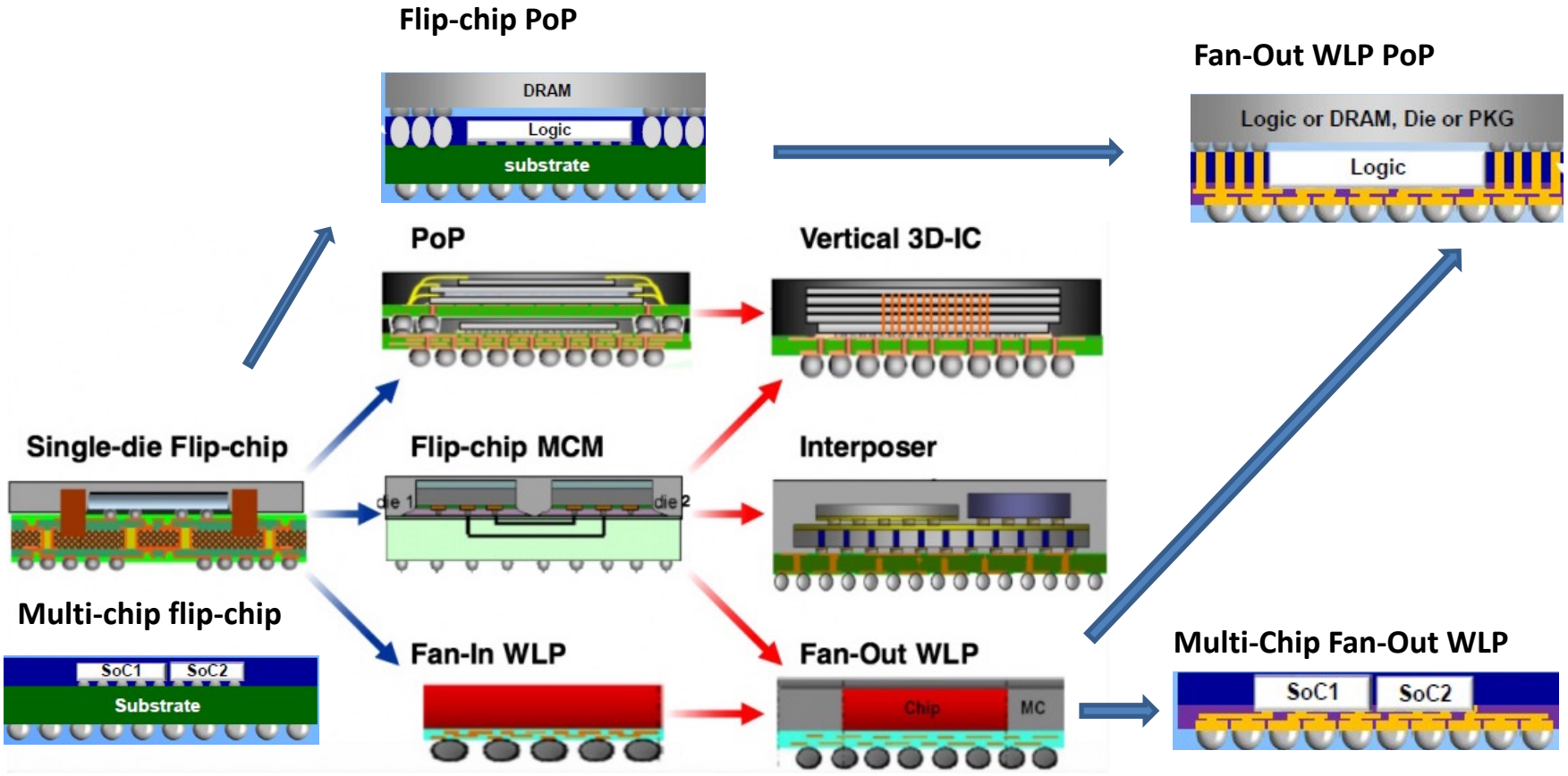
Traditional packaging for power electronics.

- **Organic packages**



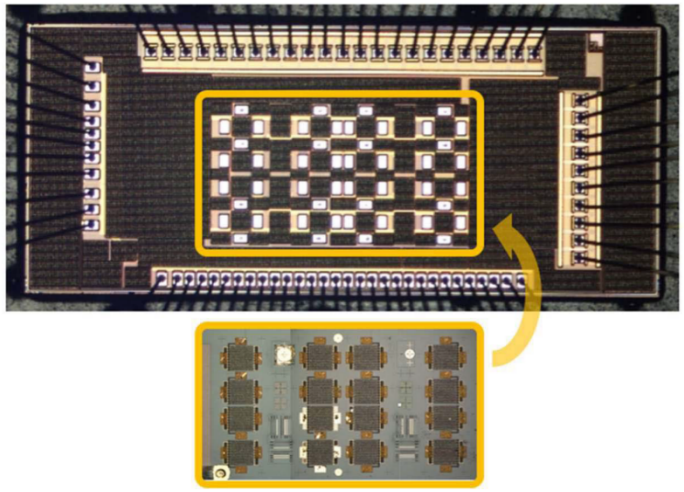
Packaging of choice for mainstream electronics.
Not generally associated with high current requirements, but things are changing.

General taxonomy of advanced packaging technologies..

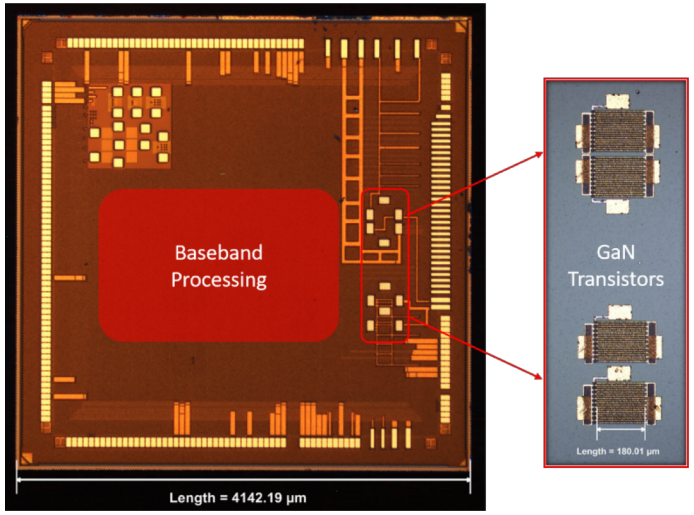


Many of these packaging approaches are achieving interconnection quality similar to monolithic integration.

Two examples of CMOS die as active interposer for GaN device integration



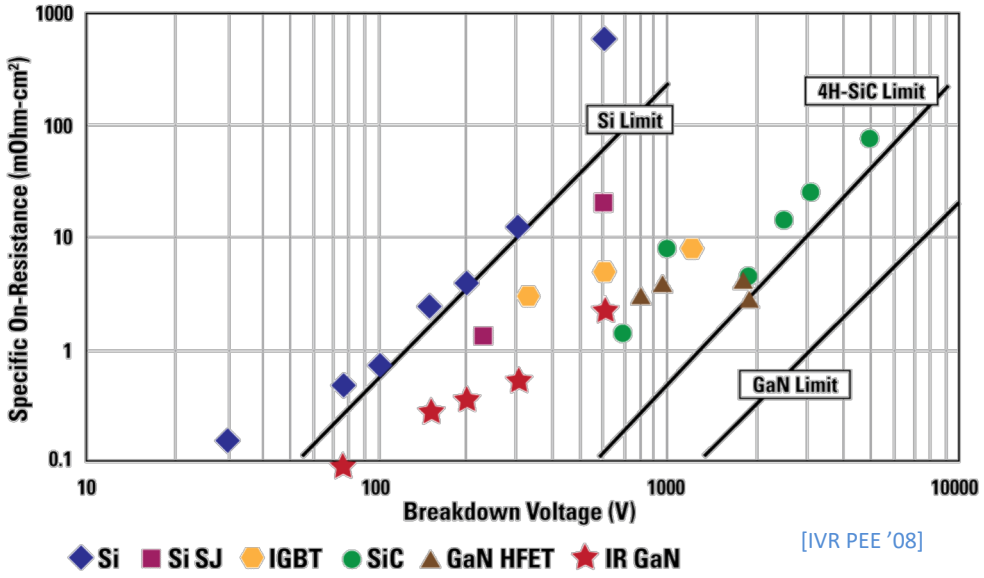
- *Hybrid GaN-CMOS power converter operating from 40-V power supply.*



- *Hybrid GaN-CMOS power amplifier*

GaN-CMOS Hybrid Converter

- GaN high electron mobility transistors (HEMTs) are able to ***outperform*** Si in almost every power application metric
- Critically, higher switching frequency for a target efficiency allows aggressive reduction of inductor size



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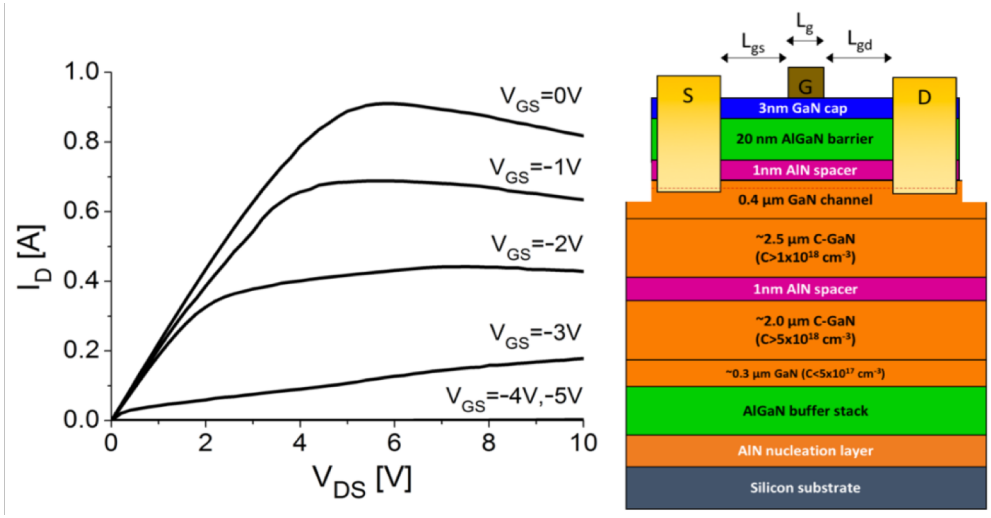
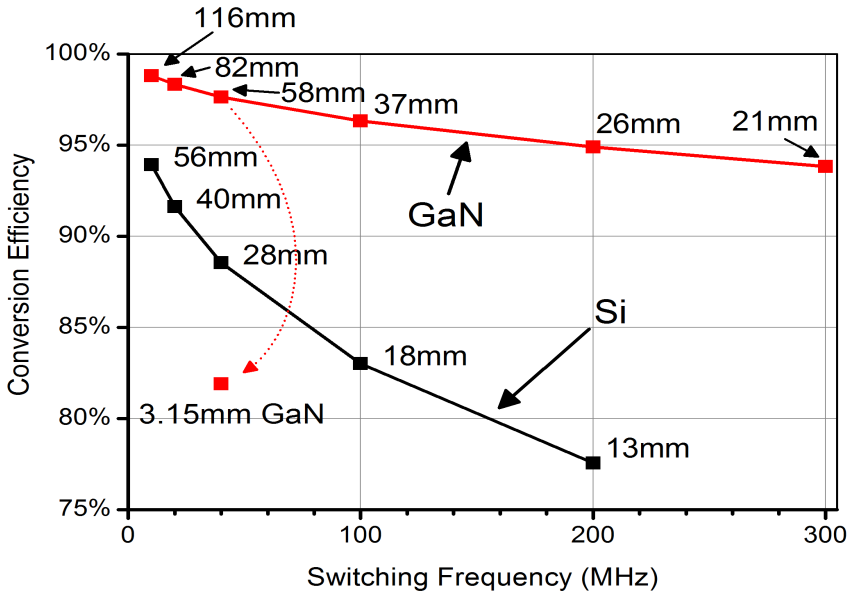


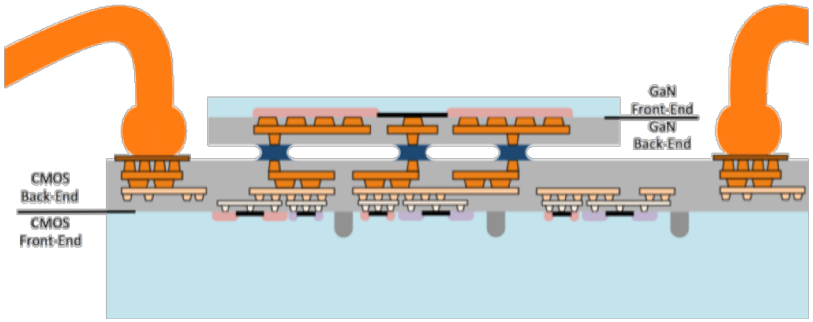
LDMOS versus GaN

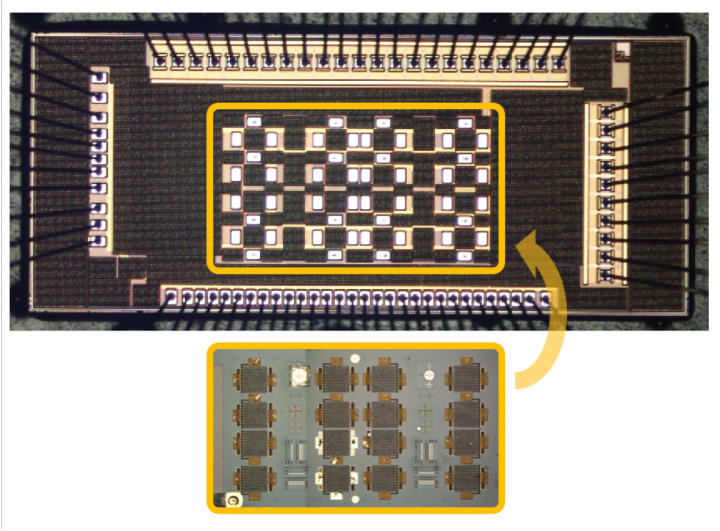
Converter	Number of phases	8
	Conversion ratio D	0.125
	Total converter (load) current	3 A
	Phase current	375 mA
	Input voltage	20 V
	Output voltage	2.5 V
GaN	On-state resistance R_{on}	3.47 $\Omega \cdot mm$
	Input capacitance C_{iss}	0.195 pF/mm
Si LDMOS	On-state resistance R_{on}	9.07 $\Omega \cdot mm$
	Input capacitance C_{iss}	2.16 pF/mm



GaN-CMOS Hybrid Converter

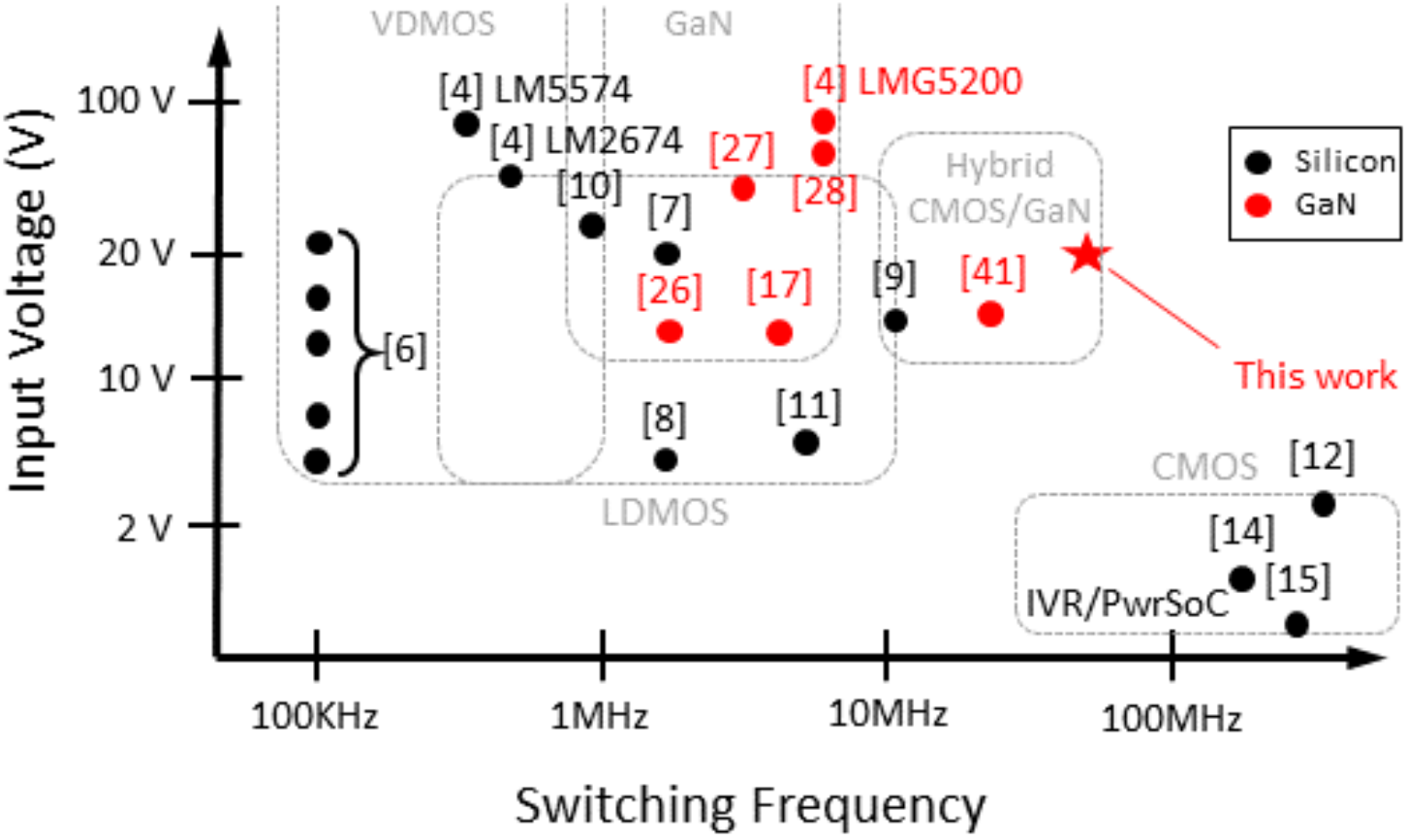
- Aggressively integrated GaN-CMOS converters are enabled by ***face-to-face bonding***
- Drastic reduction in interconnect parasitics, allowing for even higher switching frequency than in PSiP solutions using discrete GaN HEMTs (inductance less than ***15 pH***)
- Allows continued use of scaled CMOS for complex control circuitry





With aggressive die thinning, this can be compatible with C4 bonding.

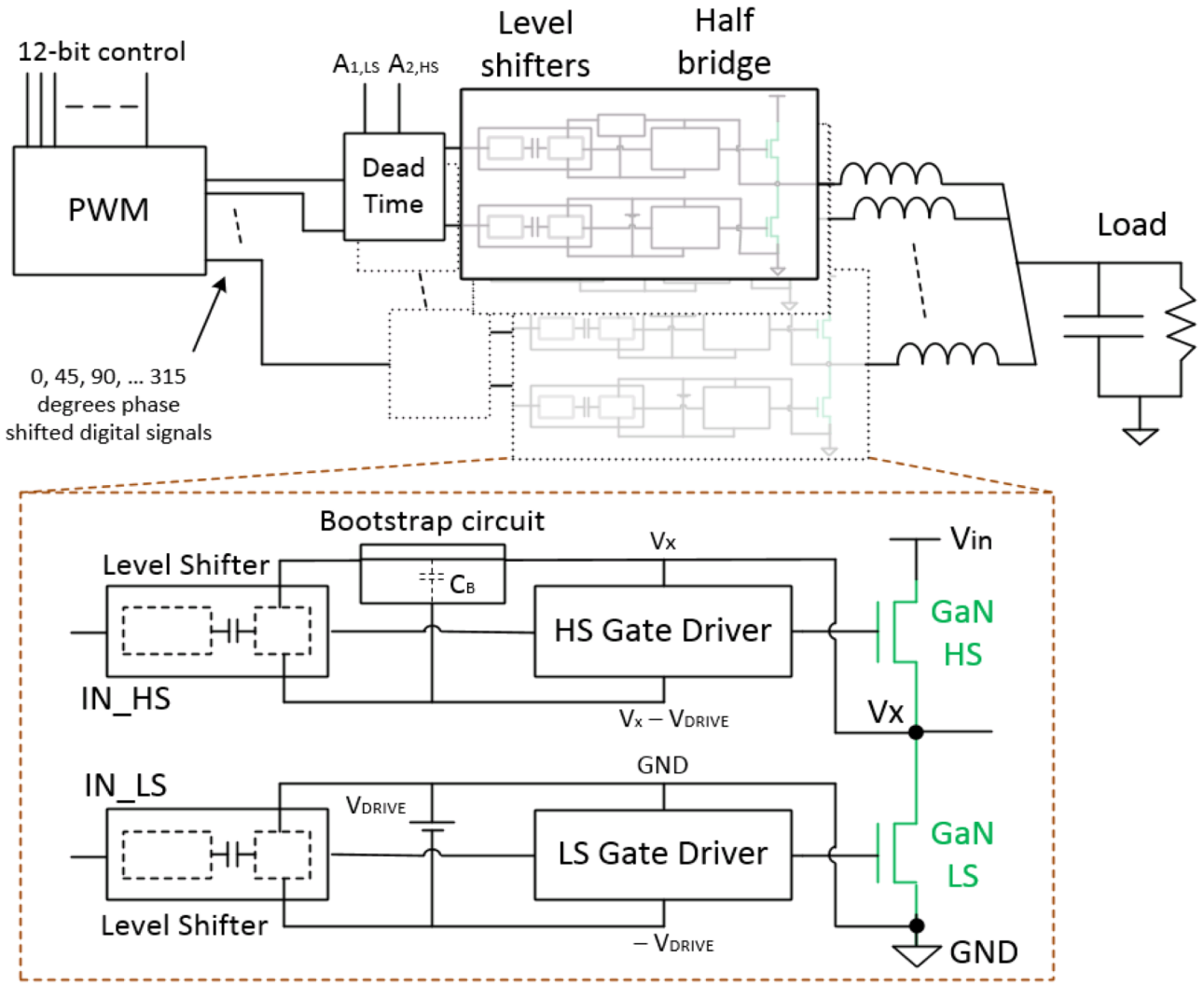
GaN-CMOS Hybrid Converter



Input voltage and ***switching frequency*** for various converter topologies using silicon and GaN switches

GaN-CMOS Hybrid Converter

Circuit topology



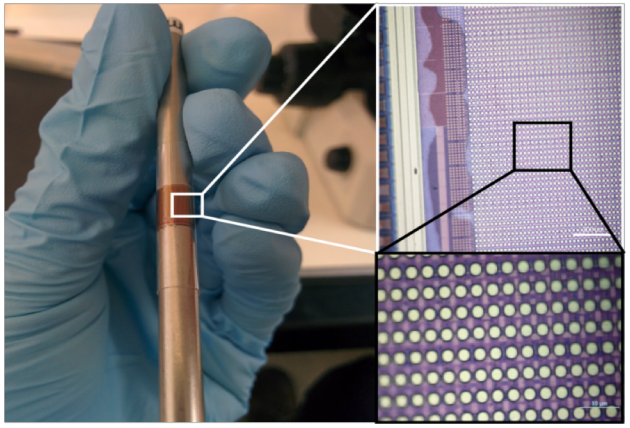
GaN-CMOS Hybrid Converter

- A three-phase 40 MHz chip-to-chip-integrated GaN-CMOS DC-DC converter is demonstrated, with peak efficiency of ***76% at an 8:1*** conversion
- Highest switching speed to date for GaN-CMOS IVRs

Measurement	1	2	3	4
V_{in}	12 V	8 V	20 V	16 V
V_{out}	1 V	1 V	2.5 V	1 V
Conversion Ratio	12:1	8:1	8:1	16:1
Frequency	40 MHz	40 MHz	40 MHz	20 MHz
# of Phases	3 phases	3 phases	1 phases	7 phases
Max load current	204mA	198mA	30mA	825mA
Max efficiency	68% at 50mA	76% at 51mA	65% at 30mA	62% at 104mA
V_{DRIVE}	>3.5 V	>3.5 V	=5 V	>2.5 V

Many of these packaging approaches benefit from die thinning…

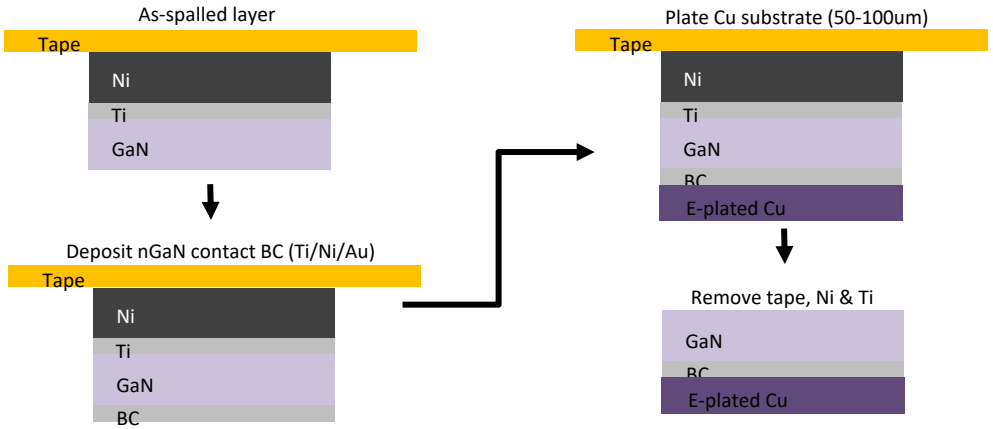
- Reduces total thickness of packages – very important for certain applications which are form-factor constrained
- Improved thermal conduction through substrate removal.
- Improved device resistance for vertical devices
- Substrate removal also allows for some really usual packaging options – such as flexible substrates



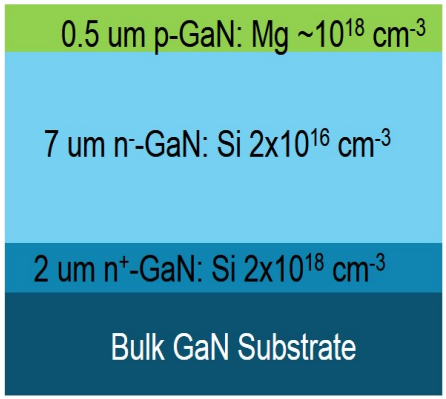
Several approaches to thinning..

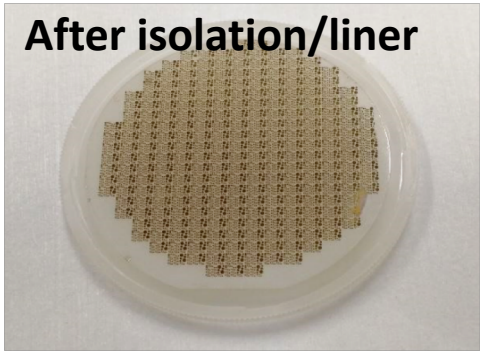
- Wet and dry etching. For silicon, the buried oxide in SOI creates a convenient etch stop.
- Mechanical grinding. Back grinding and chemical-mechanical polishing.
- Laser lift off and other lift off techniques.
- Controlled spalling.

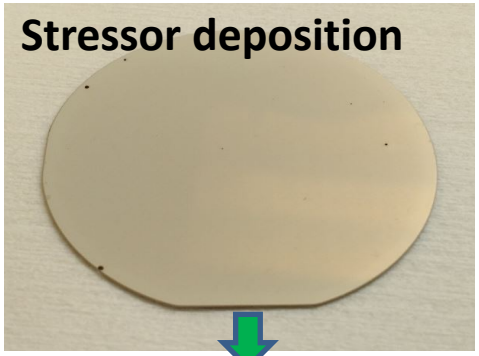
Controlled spalling

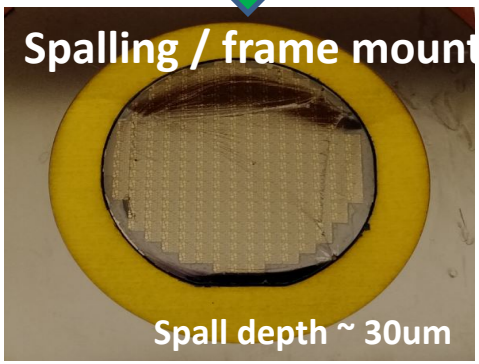


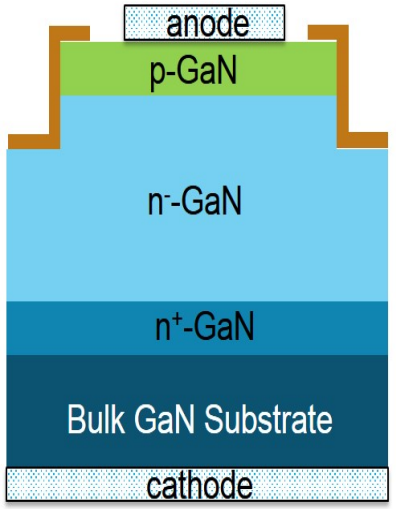
R_{on}: 1.5~3 mΩ·cm^2; BV: 600-800 V



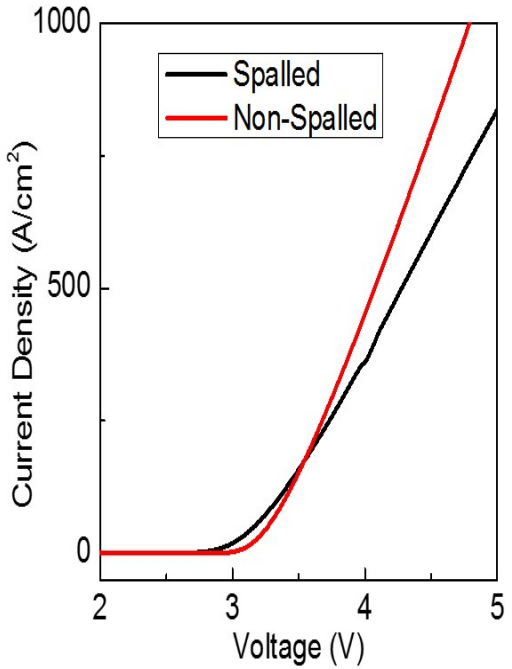


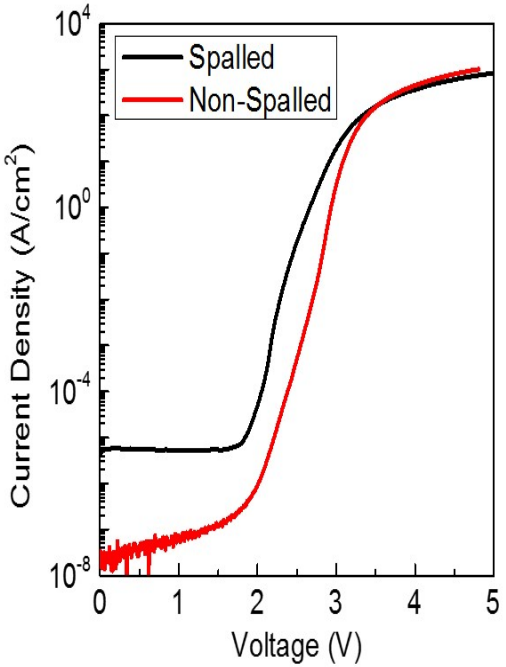


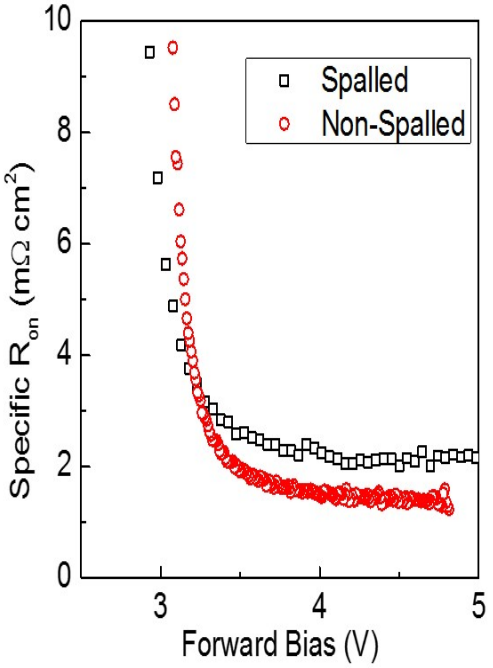




Forward I-V Characteristics

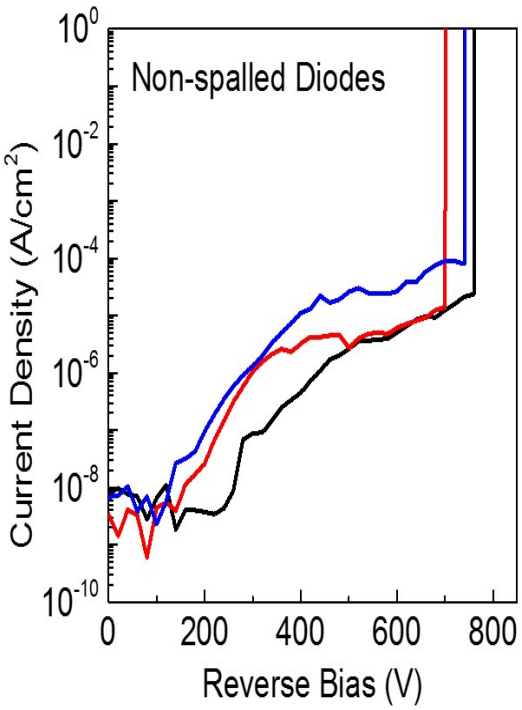


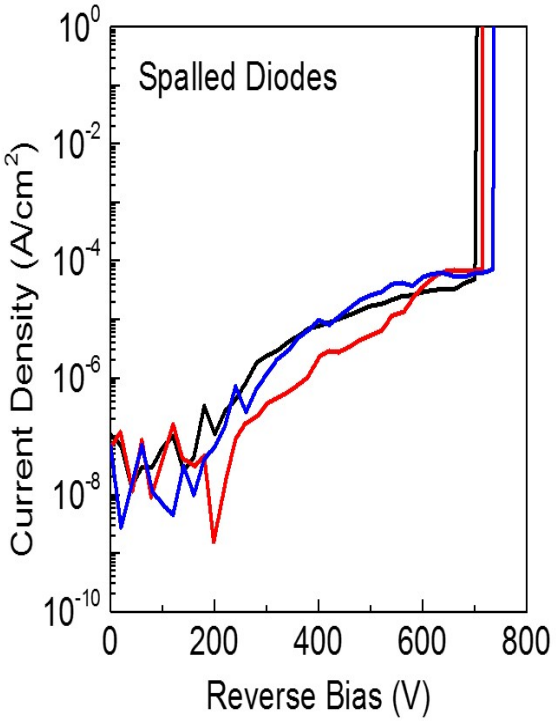




- Low V_{on} of 3 V, I_{on}/I_{off}~10^8, specific R_{on}: ~2 m$\Omega\cdot$cm^2
- Slightly larger off-state leakage and R_{on} than original diodes
- This may be due to the very rough N-face GaN surface after spalling

Reverse Characteristics

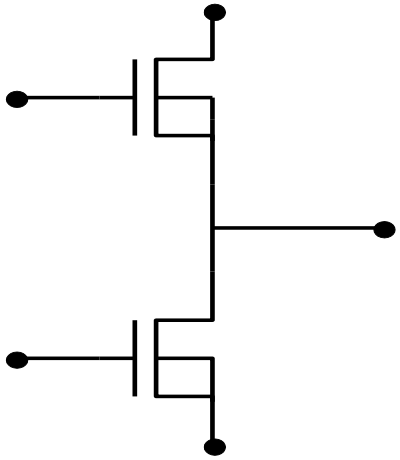




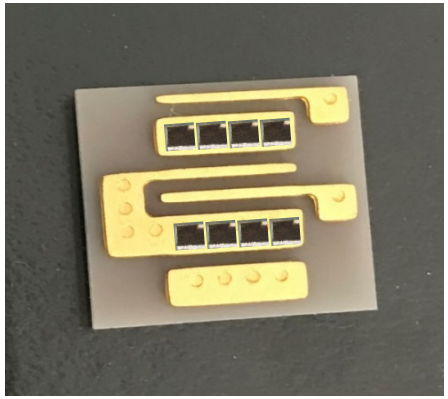
- Measured over 10 devices, with BV in the realm of 600~750 V, similar to original diodes
- Figures show the breakdown curves for three diodes measured at different locations
- In this measurement, a high current compliance (10 mA) was used; device exhibiting destructive breakdown and burning trace at the anode edge

1200-V, 40-A GaN half-bridge module

- We have built a half-bridge module with two vertical enhancement-mode GaN devices.
  - Devices are spalled with backside contact bonded directly to package.



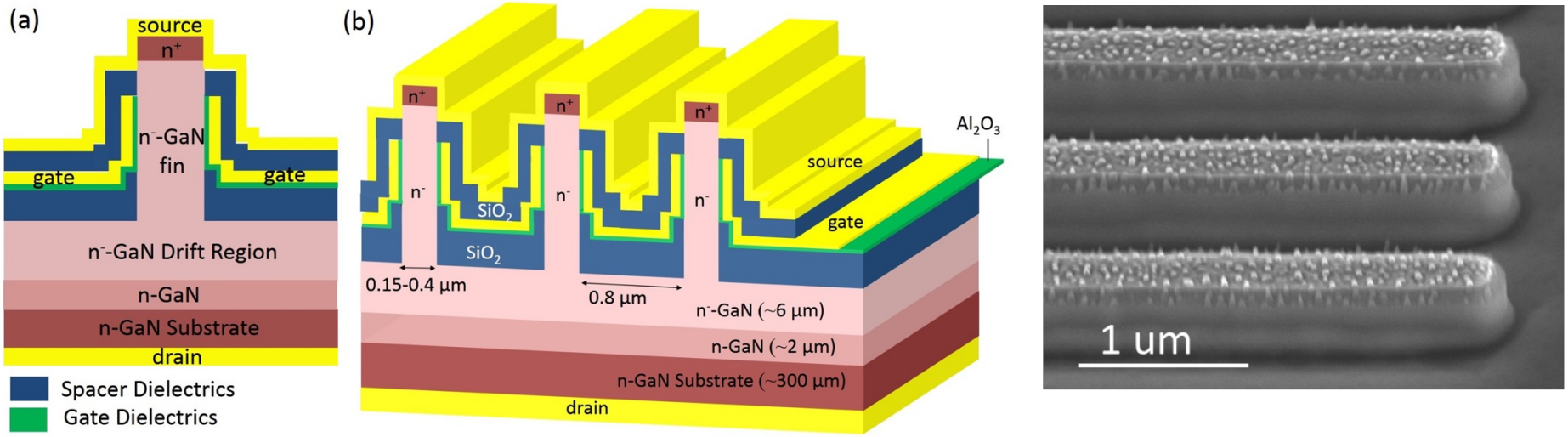
	Volume	Power	Power Density
Cree CAS120	200cm^3	144kW	0.72 kW/cm^3
GaN Systems	0.88cm^2	19.5kW	22 kW/cm^3
This work	0.08cm^3	48kW	600 kW/cm^3



1 cm by 1 cm gold-on-AlN package
Excimer laser cutter used for die singulation.

Intriguing possibilities for integration of very high-voltage power electronics with CMOS

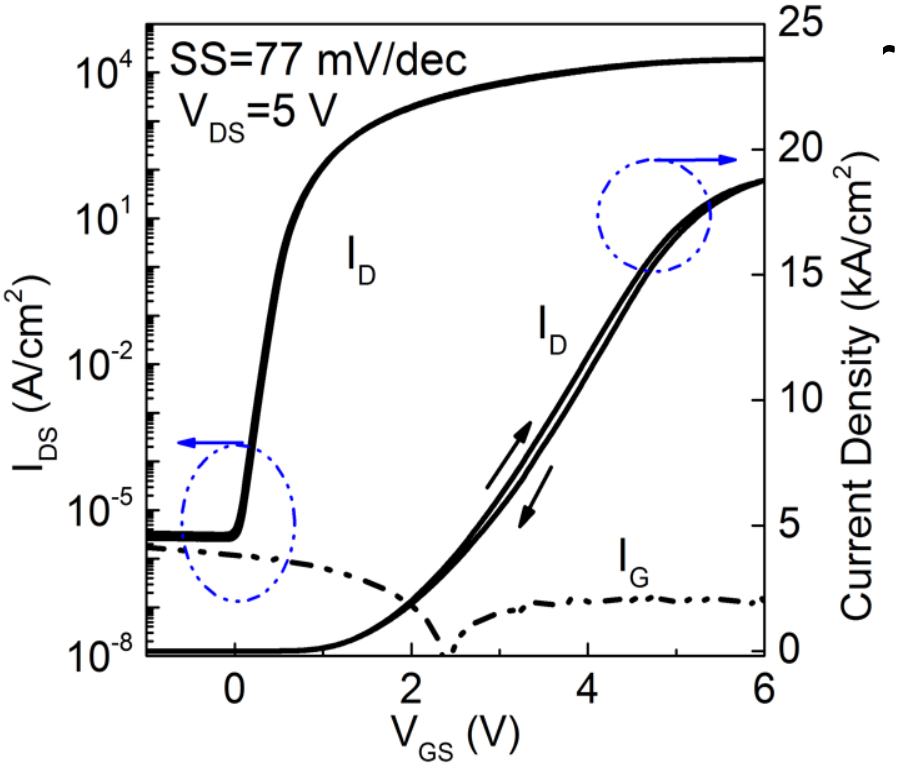
Vertical fin power FETs

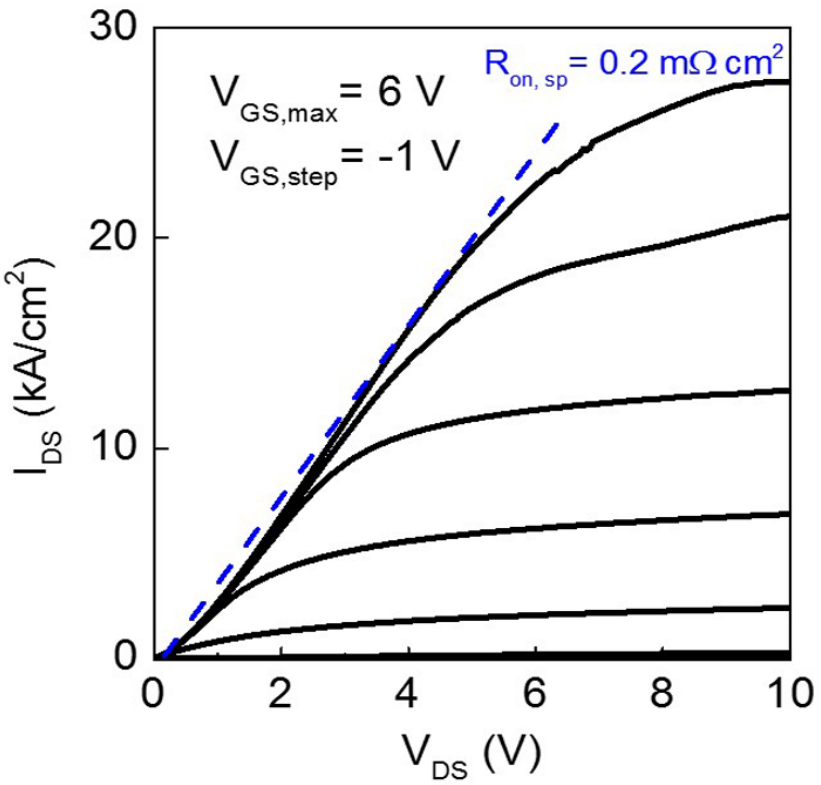


- Small device: 60 fins; fin length: 100 µm; fin width: 0.2-0.5 µm
- Large device (10 A-class): 600 fins; fin length: 350-600 µm; fin width: 0.25 µm

Small Device Forward Characteristics

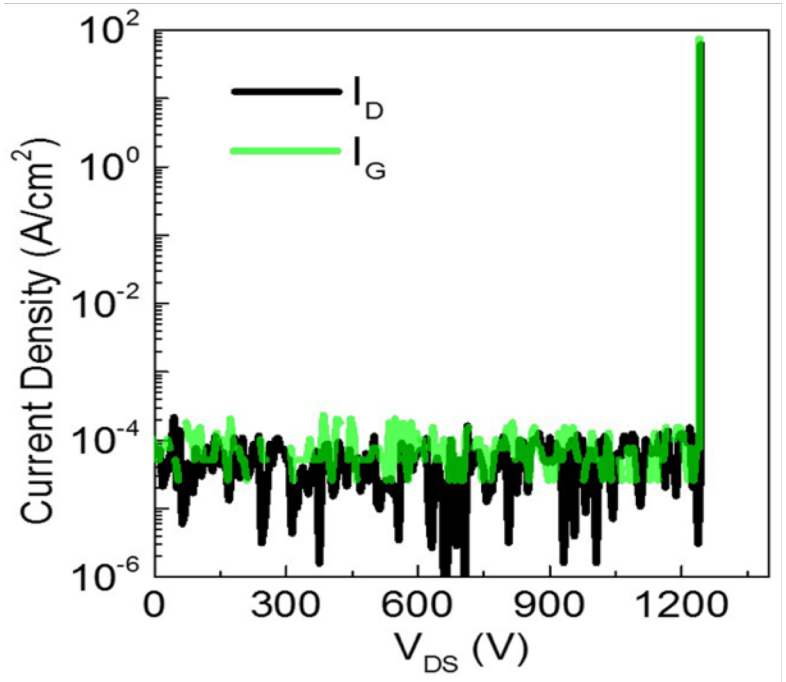
- Normally-off: V_{th}~1 V (extracted at $I_{on}/I_{off}=10^5$)

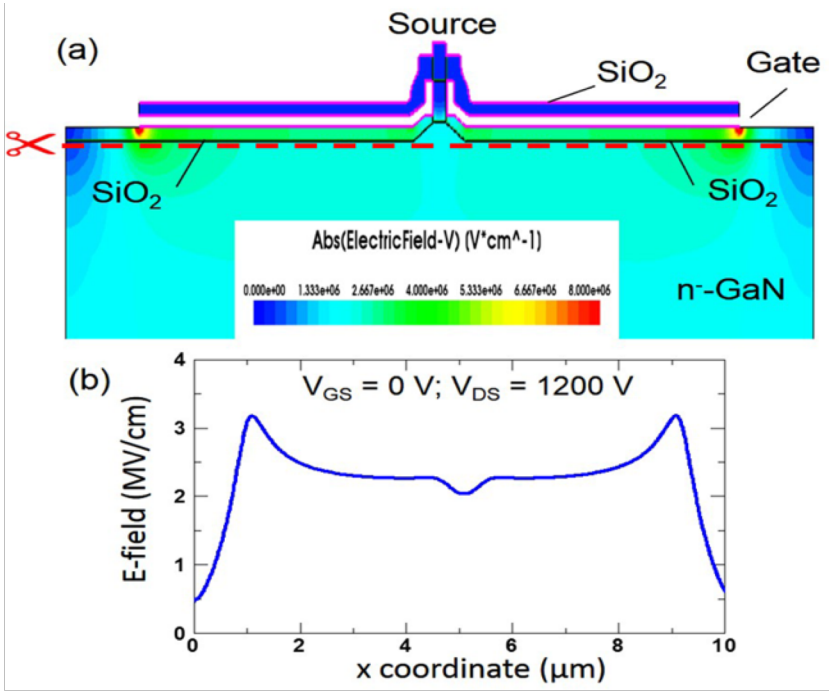




Small Device Reverse Characteristics

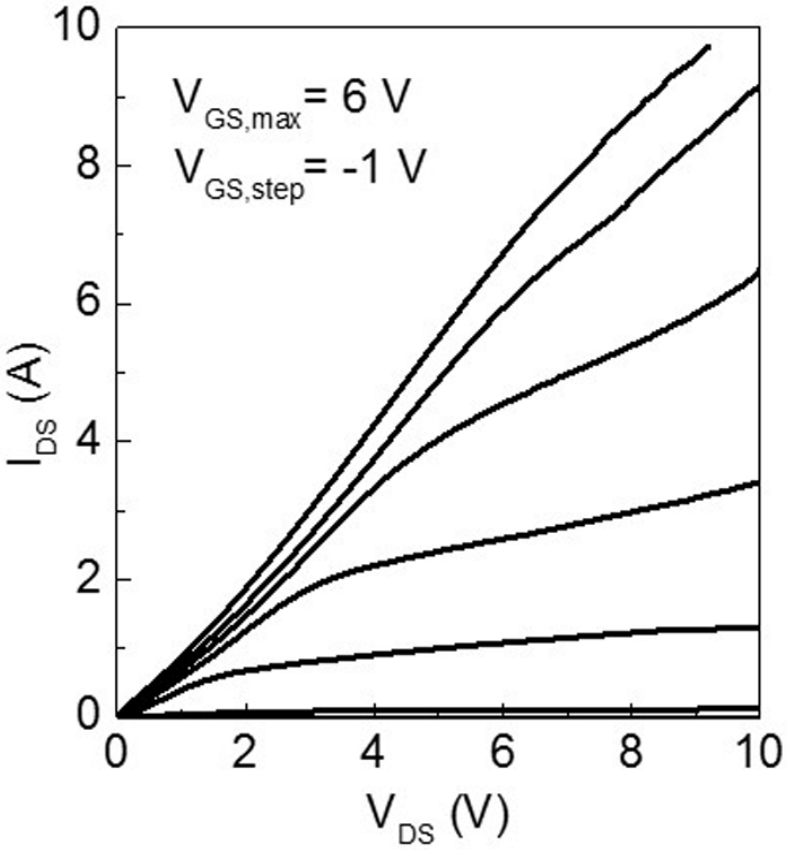
- BV over 1200 V with low I_D/I_G, destructive BV at gate edge
- Simulation verifies the peak E-field at gate edge
- Highest BV measured close to 2000 V, with peak E-field close to the GaN limit, reproducibility needs further validation

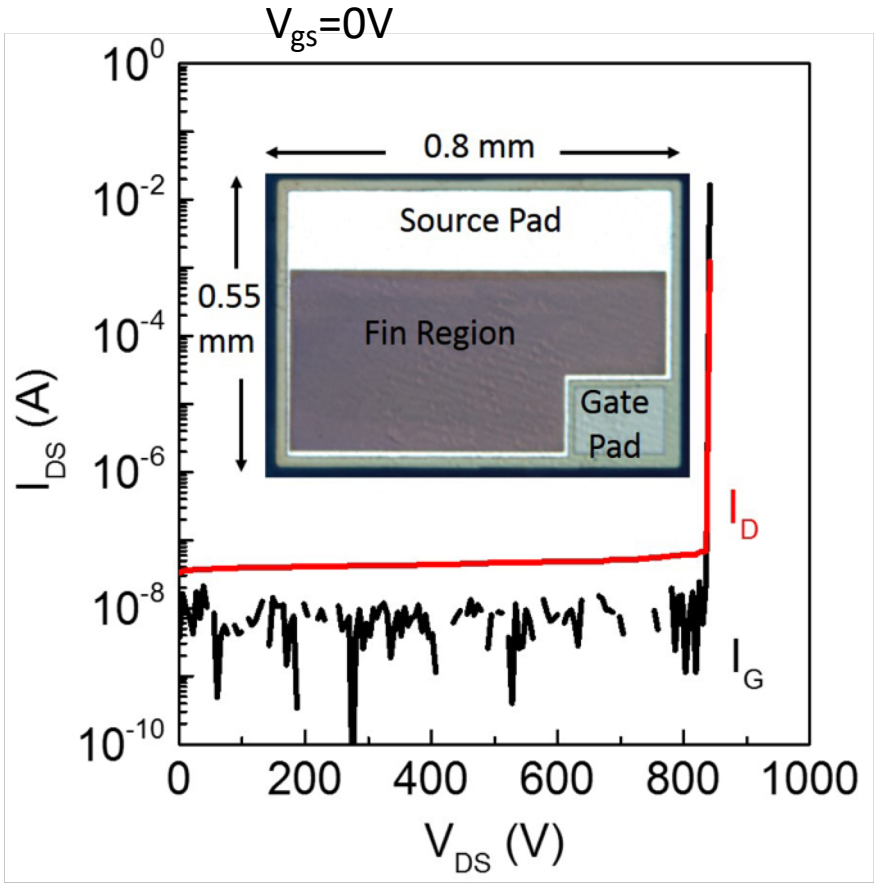




Large Device Performance

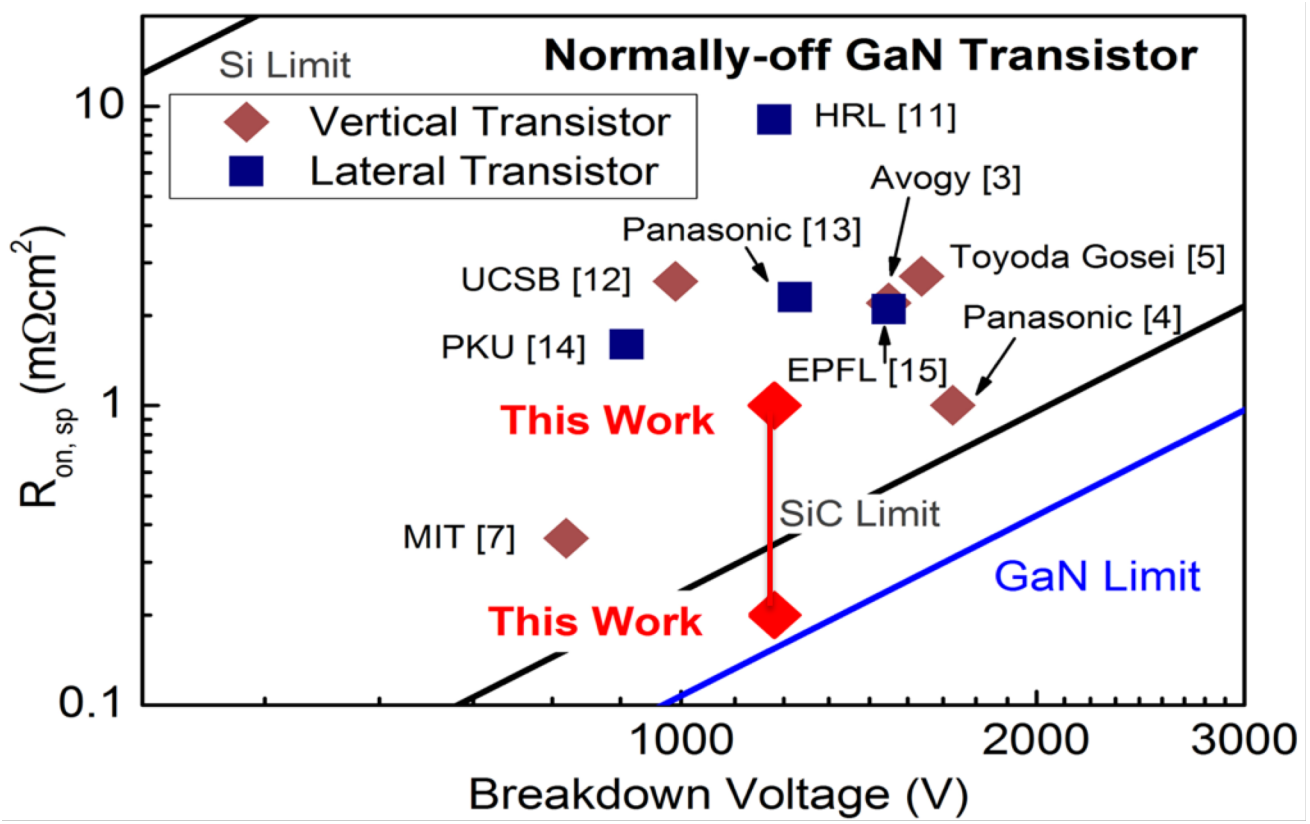
- 10-A class device; 800 V destructive BV





Specific R_{on} *versus BV*

- Top point: $R_{on,sp}$ normalized wrt the total device area
- Bottom point: $R_{on,sp}$ normalized wrt the total fin area



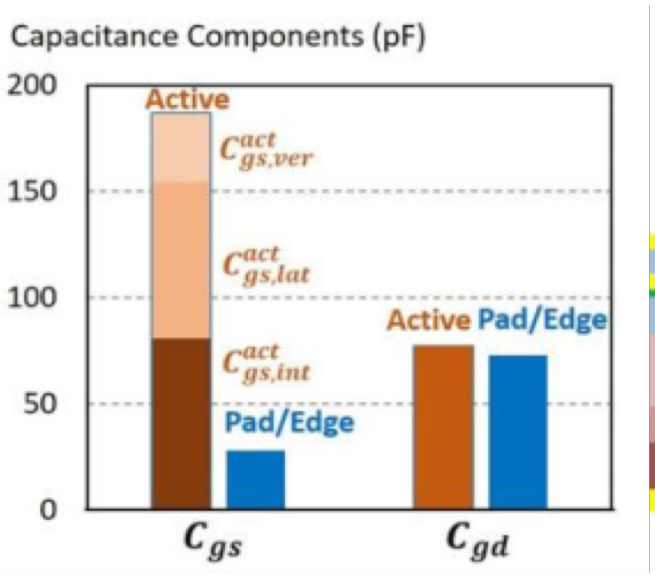
Device comparison

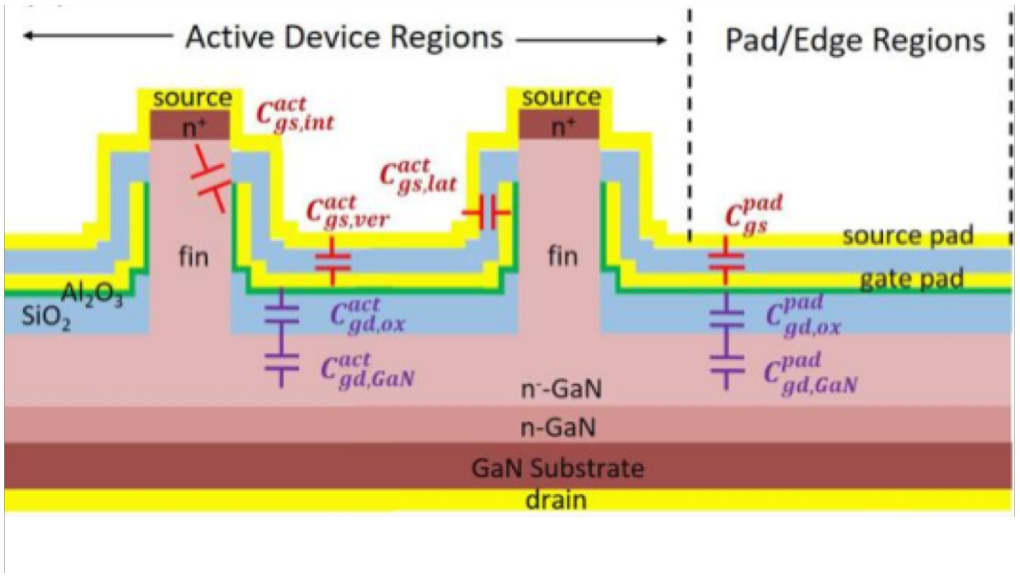
- 1200-V normally-off GaN transistor (V: vertical; L: lateral)
- Highest I_{ON} and second lowest I_{OFF}
- No need for p-GaN or epitaxial regrowth

	Device Structure	R_{on} ($m\Omega cm^2$)	BV (V)	V_{th} (V)	$I_{ON, SAT}$ (A/cm^2)	I_{OFF} @1200 V (A/cm^2)	Large Device
V	Fin FET (This work)	0.2 (1.0)	1200	1	25000	$<10^{-4}$	10 A / 800 V
	CAVET [Avogy]	2.2	1500	0.5	1500	0.02	2.3 A / 1400 V
	Trench CAVET [Panasonic]	1.0	1700	2.5	3500	0.01	15 A / 400 V
	Trench MOSFET [Toyoda-Gosei]	2.7	1600	2	~1100	$<10^{-8}$	23.2 A / 1200 V
L	Gate Injector Transistor [Panasonic]	2.3	1250	3	0.4 A/mm	10^{-7} A/mm	10 A / 600 V
	Gate-recess HEMT [EPFL]	9	1200	0.64	255	0.005	5.5 A / 1200 V

Transistor capacitance analysis

Active and pad/edge capacitance components were estimated through a combination of measurements and simulations





Switching FOMs comparison

Device Technology	Manufacturer / Maker	$R_{on,sp}$ (mΩcm²) (R_{on})	BV (kV)	I_{rating} (A)	Chip Area (mm²)	V_{TH} (V)	C_{ISS} (pF)	C_{OSS} (pF)	Q_G (nC)	Q_{GD} (nC)	Q_{rr} (nC)	Switching FOM (nΩ·C) $R_{on}\cdot(Q_G+Q_{GD})$ $R_{on}\cdot(Q_G+Q_{GD}+Q_{rr})$
GaN Vertical FinFET (this work)	**MIT**	**2.1** (0.91 Ω)	**1.2**	**5**	**0.45**	**1.3**	**248.3***	**42.2***	**1.24**	**2.72**	**~0**	**3.3** **~2.0 (pad optimized)**
SiC MOSFET (CPM2-1200-0160B)	Cree	2.7 [19] (0.16 Ω)	1.2	20	6.28	2.5	525	47	34	14	105	7.68 24.48 (include Q_{rr})
SiC JFET Cascode (UJN1208Z)	United SiC	1.7** (0.15 Ω)	1.2	18.4	>1.13***	4.4	738	58	30	6	63	5.4 14.85 (include Q_{rr})
Si IGBT (NGTB15N120FLWG)	ON Semi	~20 (~0.25 Ω)	1.2	15	320	2	3600	110	150	68	1500	54.5 429.5 (include Q_{rr})
Si CoolMOS (IPD90R1K2C3)	Infineon	~8**** (1.2 Ω)	0.9	5	~23.6	3	710	35	28	12	3700	48 4488 (include Q_{rr})
GaN HEMT Cascode [20]	Transphorm	(0.19 Ω)	1.2	>20	N.A.	2.3	N.A.	43.1	10	N.A.	N.A.	N.A.
Vertical GaN MOSFET [5]	TOYODA GOSEI	2.7	1.2	23.2	2.25	3.5	N. A.					
Vertical GaN CAVET [2]	Avogy	2.2	1.5	2.3	0.17	0.5						

Note: *@V_{DS}=200 V; **Source: http://unitedsic.com/cascodes; ****Calculated by using the R_{on} in the data sheet and the reported $R_{on,sp}$, reflecting the active device area (not including pad/edge areas); ******Source: Infineon's application note titled "CoolMOS™ C7: Mastering the Art of Quickness".

$C_{iss}=C_{gs}+C_{gs}$ (input capacitance)
$C_{oss}=C_{gd}+C_{ds}$ (output capacitance)

Power dissipated due to conduction losses, switching losses, and loses due to reverse conduction.

$P = P_{cond} + (P_{gate} + P_{QOSS}) + P_{rr}$
$= I^2R_{on}D + Q_GV_Gf_{SW} + Q_{gd}V_{DS}f_{SW}I_{DS}/I_G + P_{rr}$ (hard switching)
$= I^2R_{on}D + Q_GV_Gf_{SW} + Q_{oss}V_{DS}f_{SW} + P_{rr}$ (soft switching)

Matching switching and conduction losses predicts an optimal switching frequency of 3.5 MHz, compared to 10-20 kHz for a Si IGBT.

Conclusions

- *Advanced wafer level packaging* approaches are becoming the “method of choice” for heterogeneous integration across all electronic systems.
- Growing *convergence of packaging* approaches for “mainstream” electronics and power electronics.
- Example of face-to-face bonding for *GaN-CMOS system integration*.
- *Substrate removal* (or thinning) is an important part of all these approaches.
- Thinning approaches can be applied to the packaging of *high-voltage, high-current vertical GaN switches*, achieving record high power densities