



**PWR
SOC18**

Integrated Power Conversion and Power Management

next generation technology for emerging business opportunities, October 17, 18, 19, 2018, Hsinchu, Taiwan

new technologies new applications new markets



Navitas

GaNFast™ PwRSoCs

Dan Kinzer, CTO & COO, Navitas Semiconductor

PWRSOC18 Session 5, Hsinchu, Taiwan

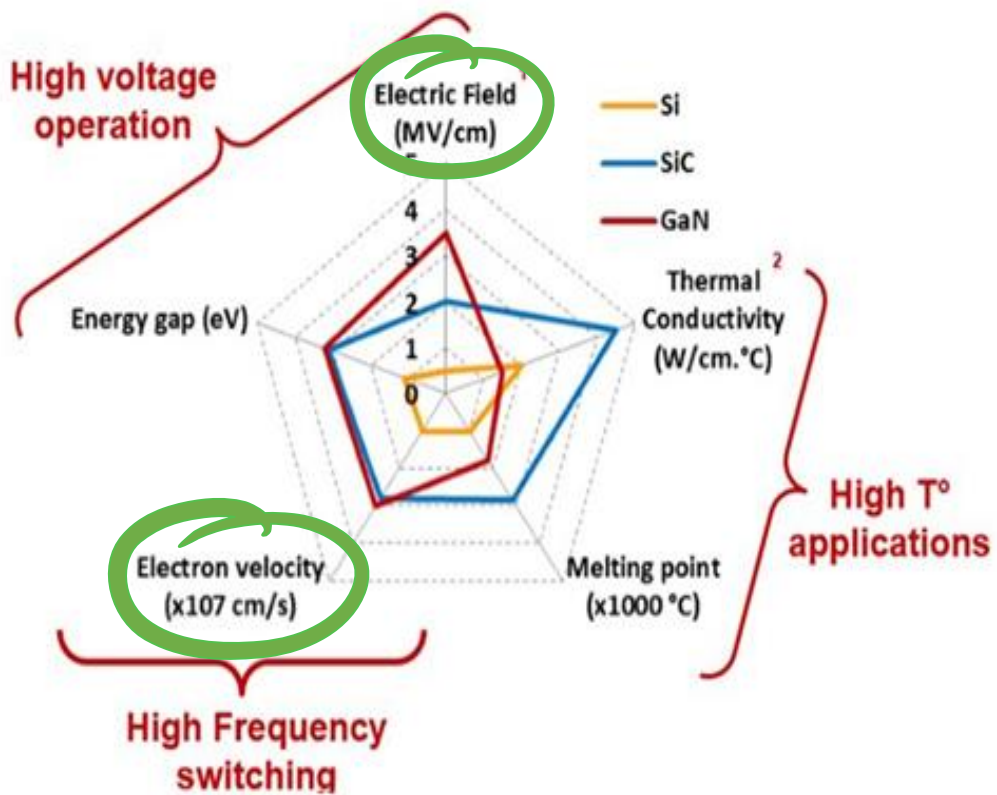
October 18, 2018



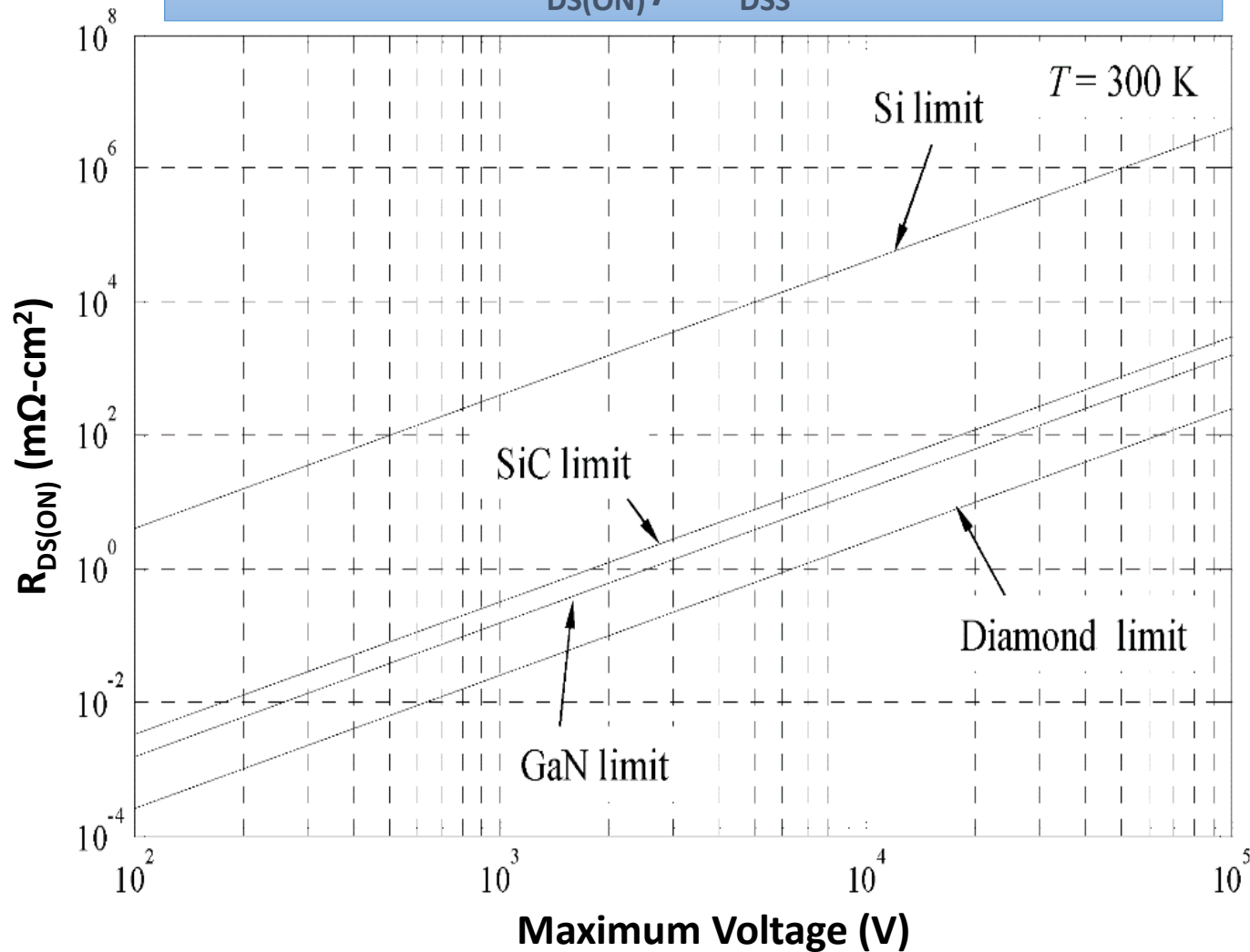


Performance Limits of Power Semi Materials

Important Material Attributes



Theoretical 1-D $R_{DS(ON)} / BV_{DSS}$ for Vertical Devices

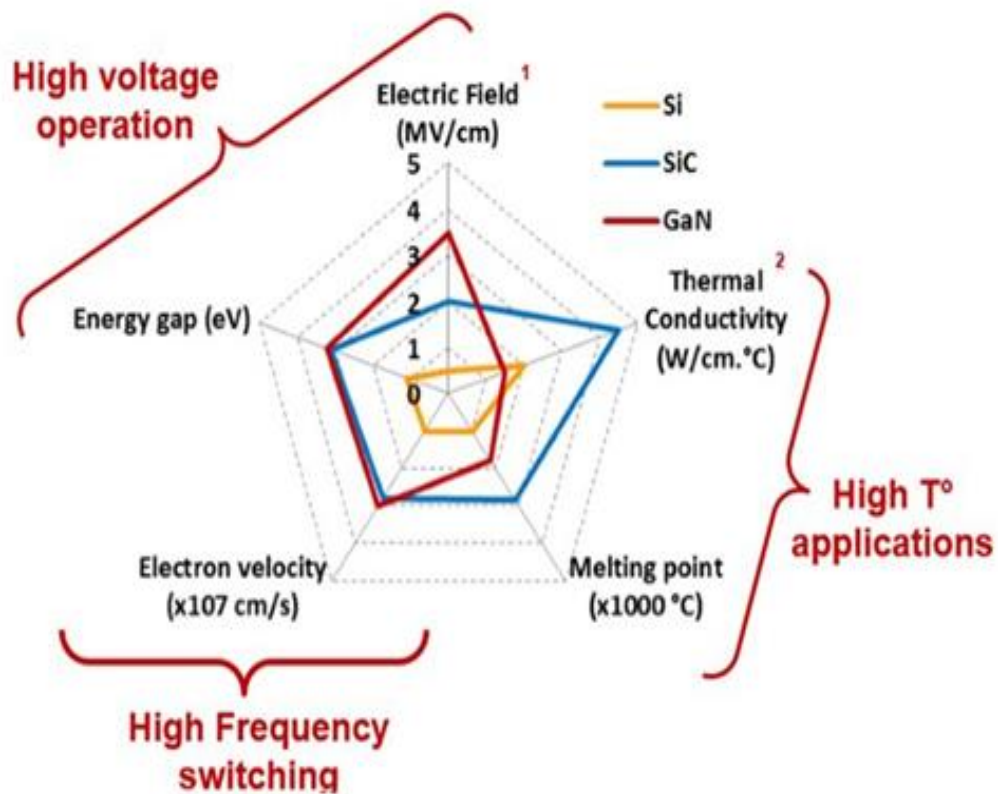




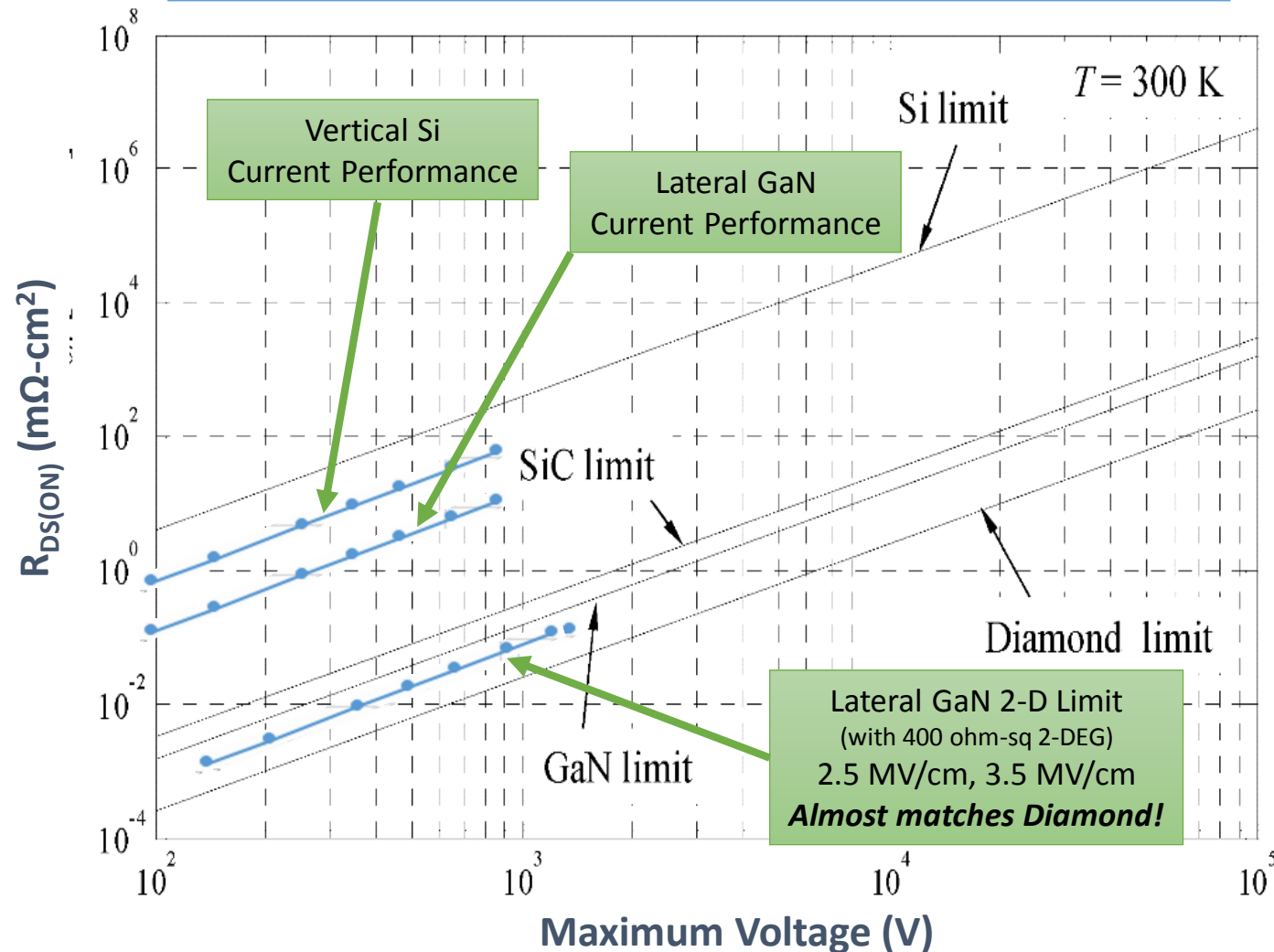
Performance Limits of Power Semi Materials



Important Material Attributes

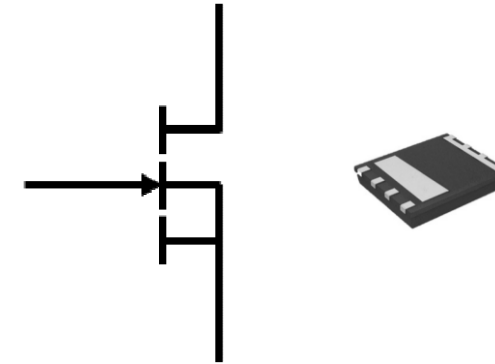
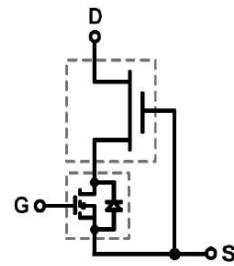
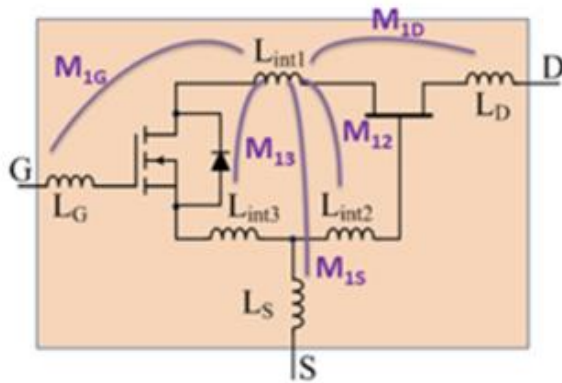


Theoretical 1-D $R_{DS(ON)} / BV_{DSS}$ for Vertical Devices





Two approaches: dMode and eMode GaN



Cascode GaN + Silicon Switch

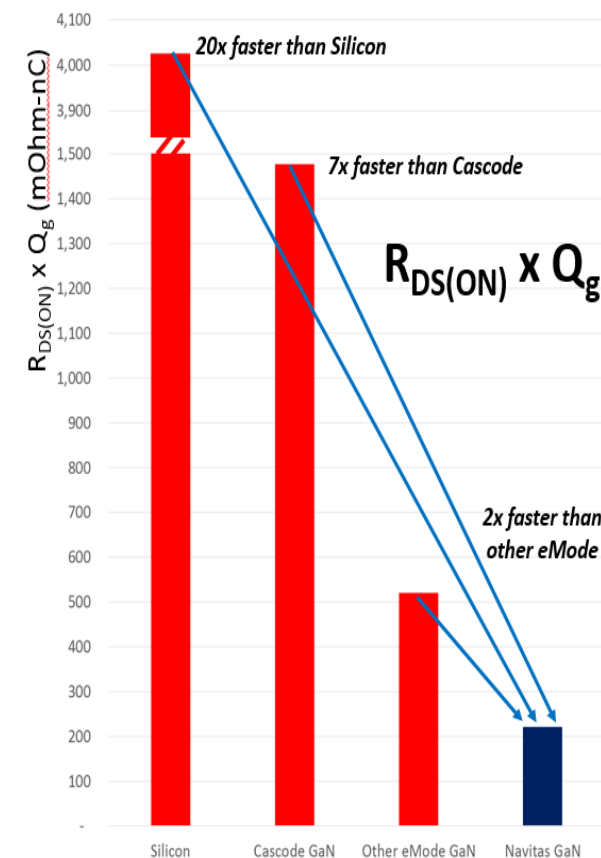
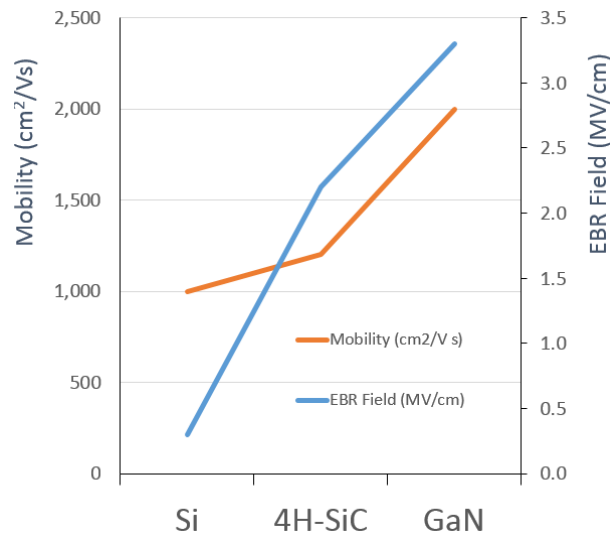
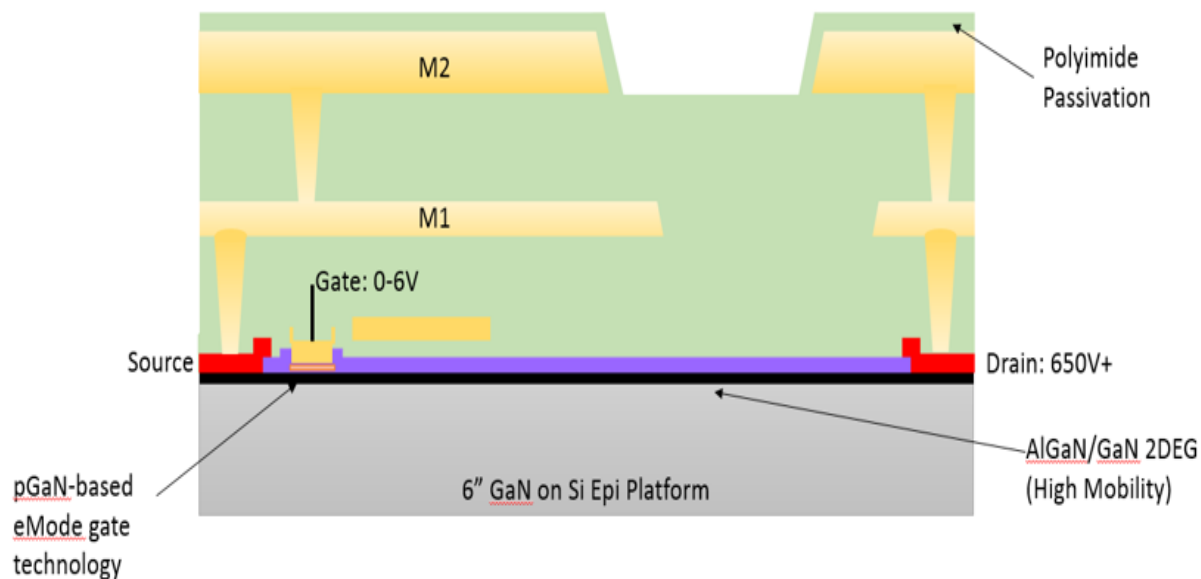
- Standard silicon FET gate
- Traditional packages
- Large package inductance
- Prone to oscillation
- No dV/dt control
- Complicated multi-die package

eMode AllGaN™ Switch

- Extremely low gate charge
- No reverse recovery loss
- Easy to package
- Low package inductance
- Controlled dV/dt
- Careful gate voltage control



Navitas eMode Power FET Technology



- Lateral device technology → Convenient isolation and easy voltage scaling
- High breakdown field (10X) and high mobility (2X) → Low $R_{DS(ON)}$, Low Q_{OSS}
- Lateral device technology → Low Q_G , easy to drive, easy to integrate
- Processed in established CMOS line → High yield, high capacity
- Multiple metal technology using standard CMOS processing equipment



GaN vs Silicon Output AC Characteristics

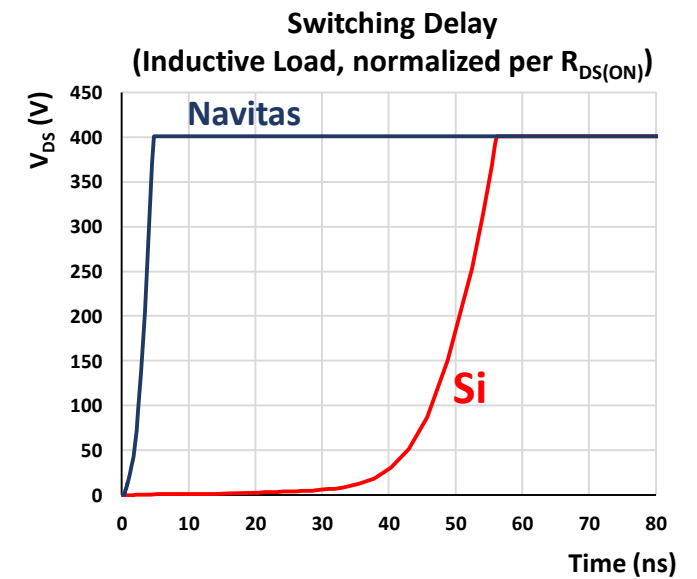
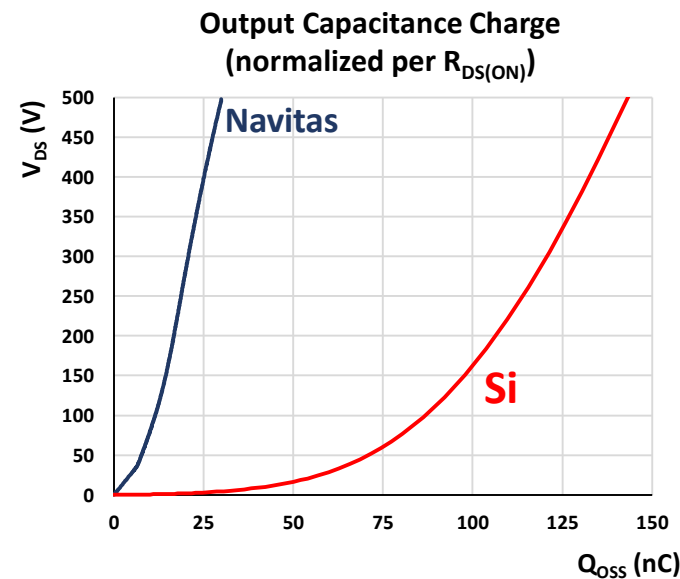
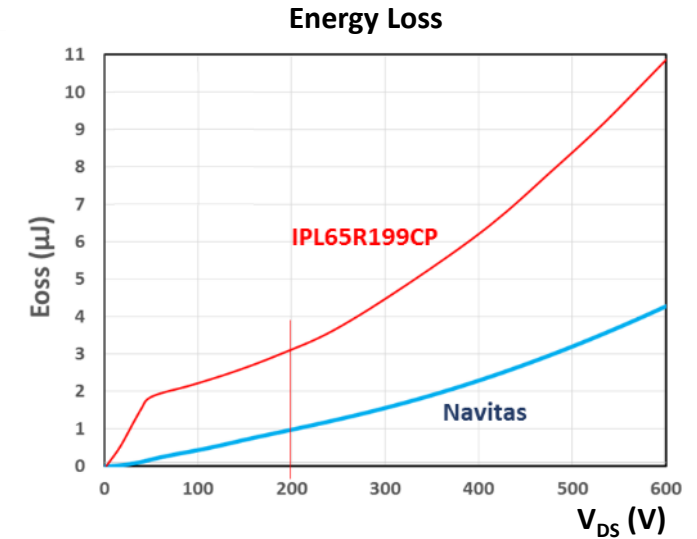
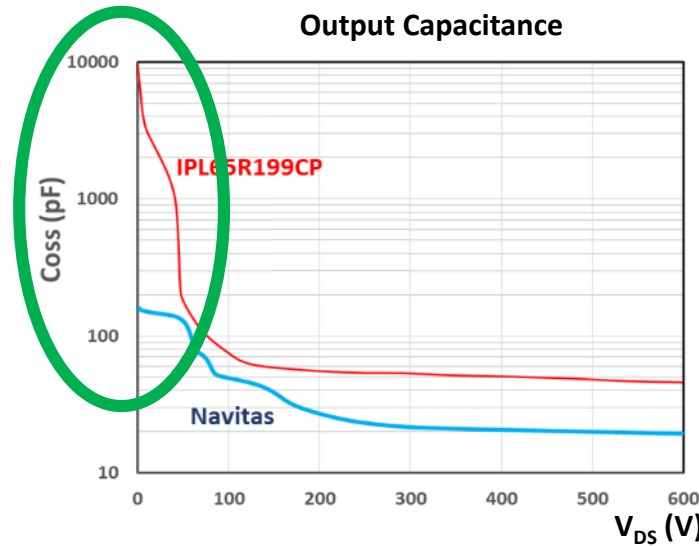


Why is Silicon so High Loss?

- Hard switching loss:

$$P_{LOSS} = E_{OSS} (V_{DS}) * F_{SW}$$
- $C_{OSS} \rightarrow$ Delay (limits F_{SW})
- Too slow \rightarrow partial ZVS $\rightarrow E_{OSS}$ loss
- Si C_{OSS} is 50x-100x higher than GaN at $V_{DS} < 30V$
- Si P_{LOSS} is 3x higher than GaN at 200V (partial ZVS)
- Big effect at full or light load condition

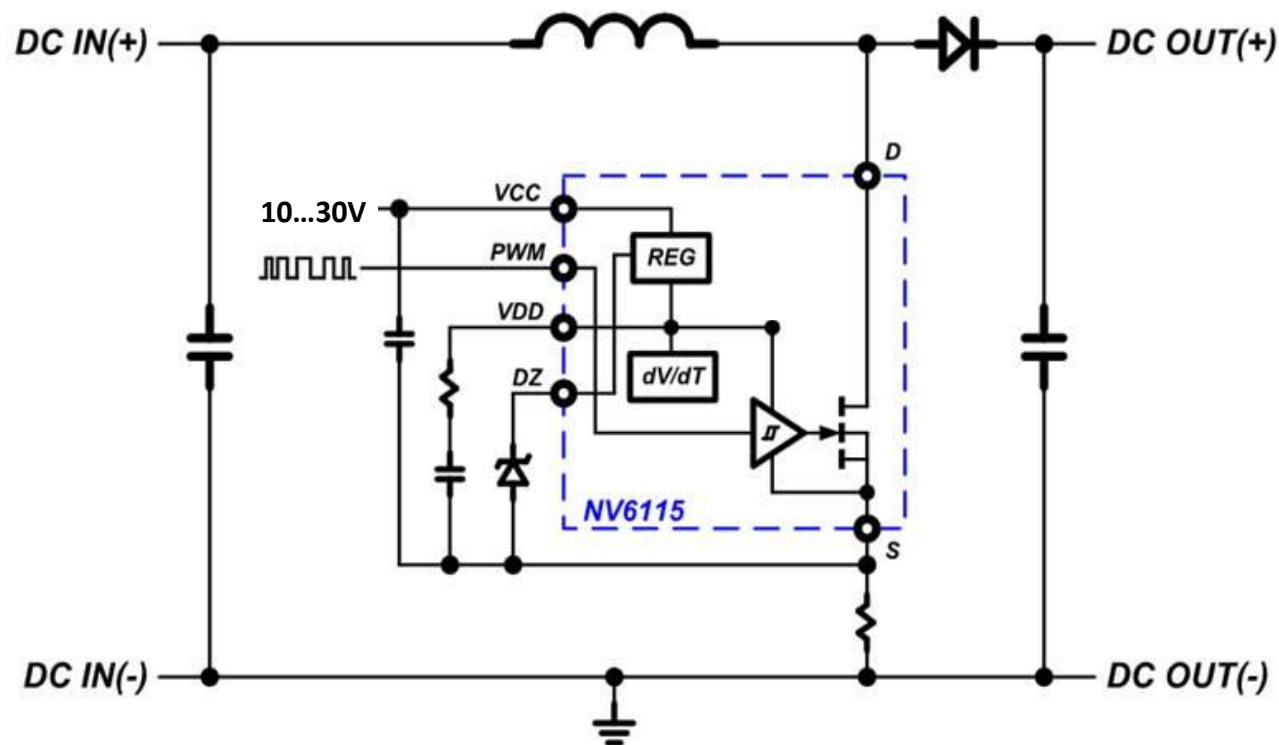
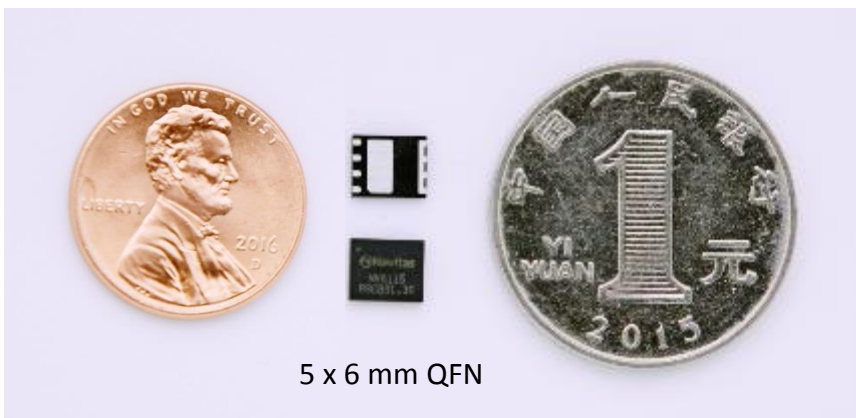
Further information: "C_{OSS} Hysteresis in Advanced Superjunction MOSFETs", Harrison, APEC 2016





Monolithic integration at 650V

- GaN FET (range 120-300 m Ω)
- GaN gate driver (fast, no overshoot)
- Wide input voltage range (10-30V)
- GaN regulator (well controlled gate voltage)
- dV/dt control (programmable 10-100V/nsec)
- Hysteretic input, ESD, fault protection
- Fast and controlled start-up





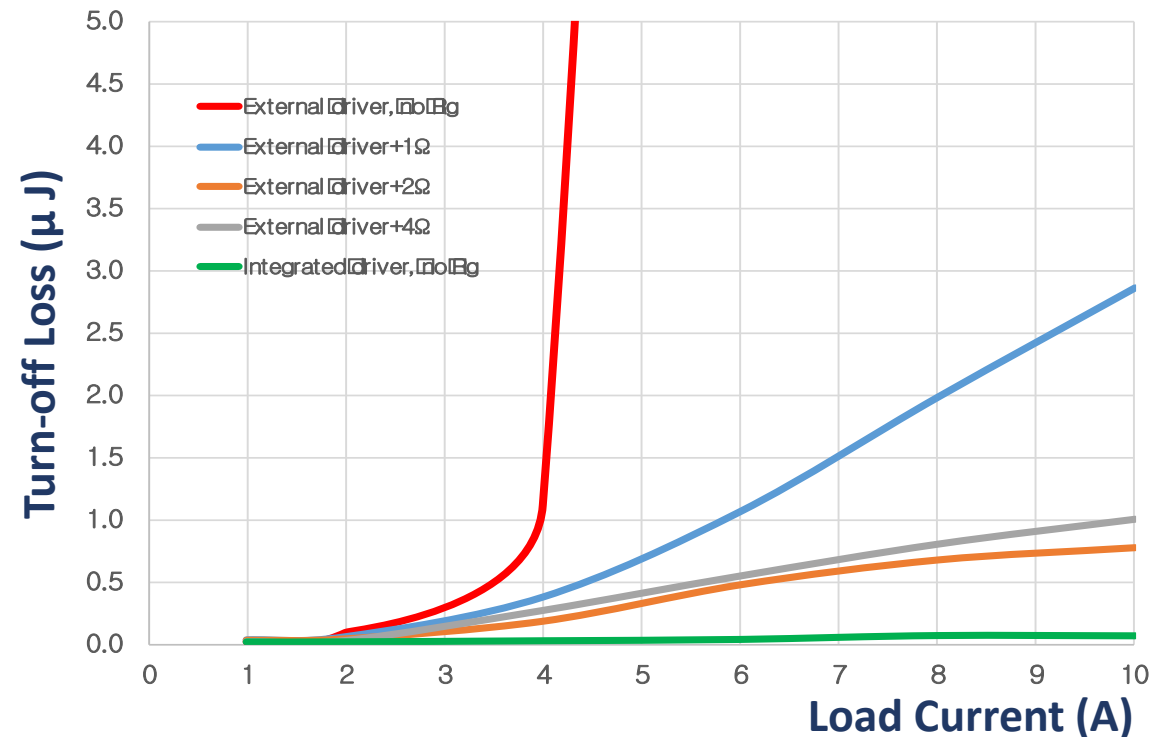
Integration Eliminates Turn-off Losses

External drivers

- Just 1-2 nH of gate loop inductance can cause unintended turn-on
- Gate resistors reduce spikes but create additional losses

Integrated GaN drivers

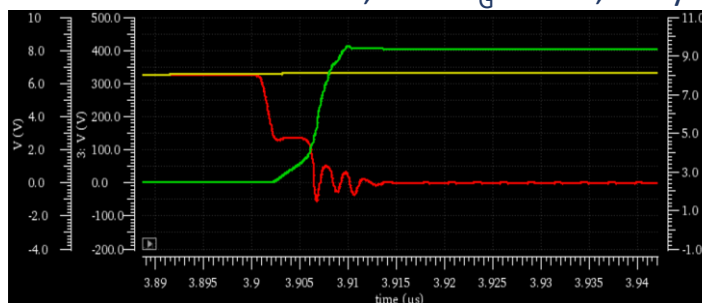
- Eliminate the problem
- Negligible turn-off losses
- Removes unintended turn-on due to high dV/dt



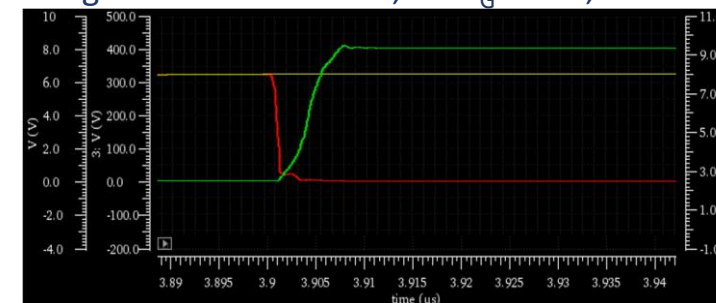
Discrete FET and drive, no R_G = out of control



Discrete FET and drive, with R_G = slow, lossy



Integrated FET and drive, no R_G = fast, efficient

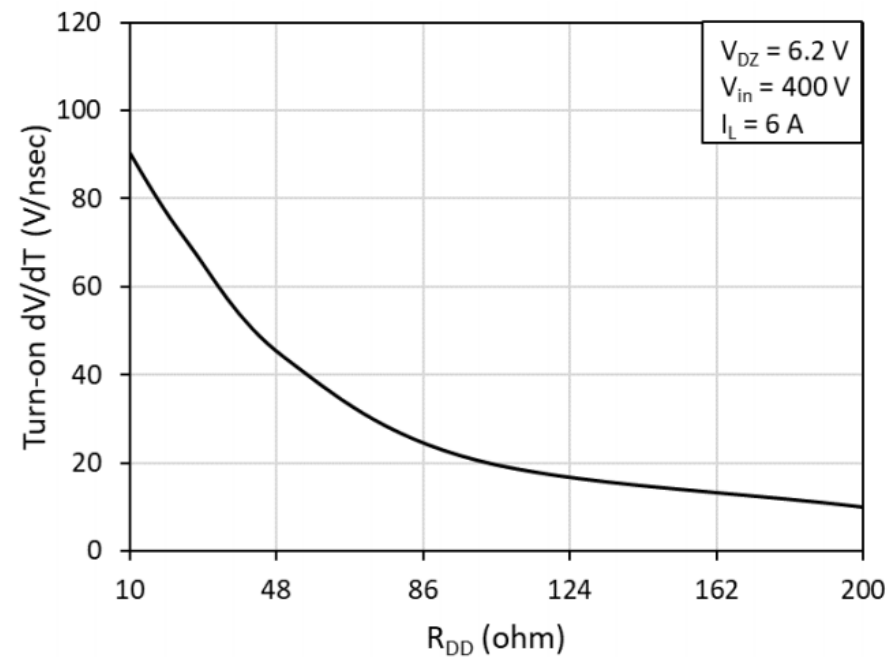
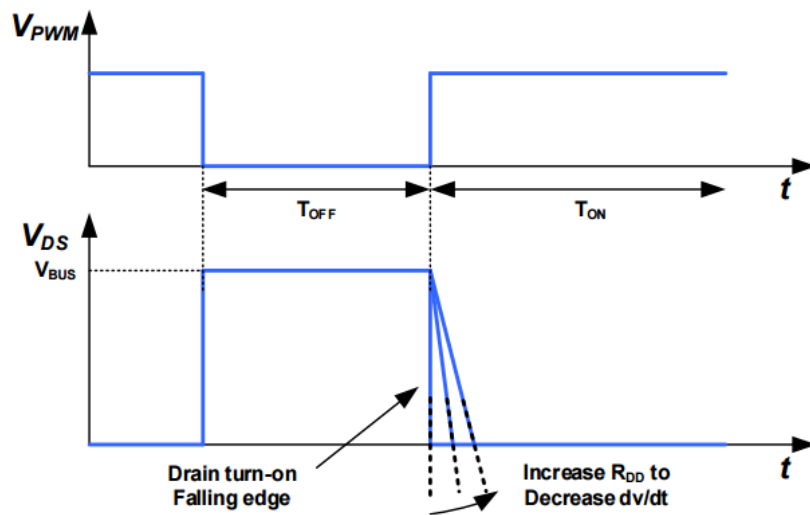
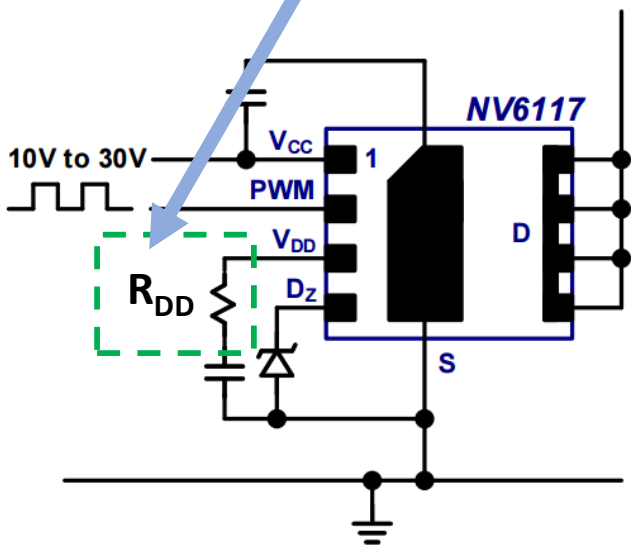




Voltage Slew-Rate Control ... Easy EMI Tuning

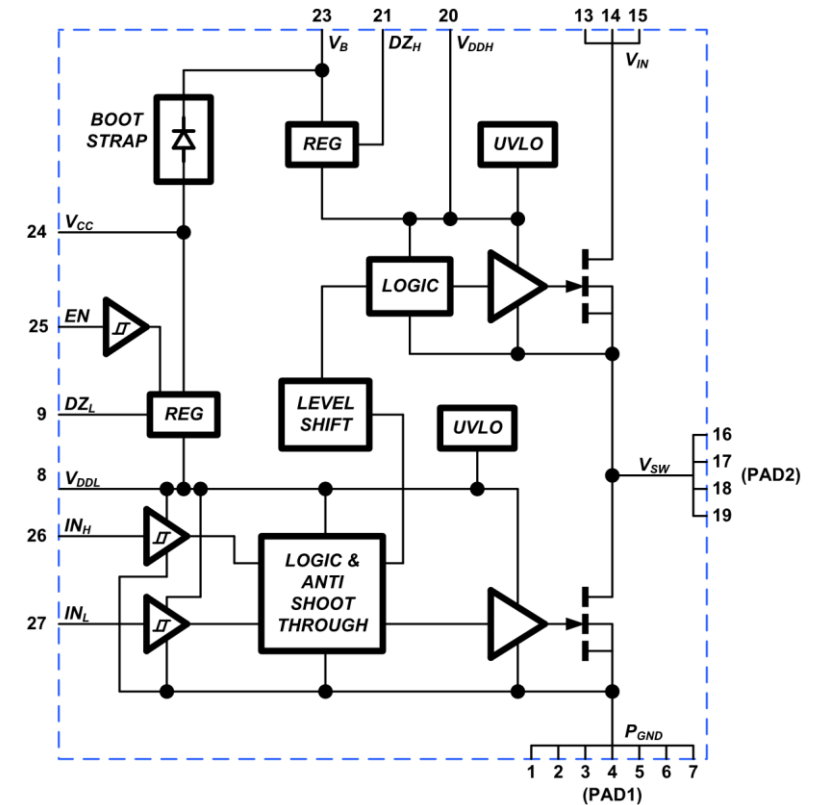
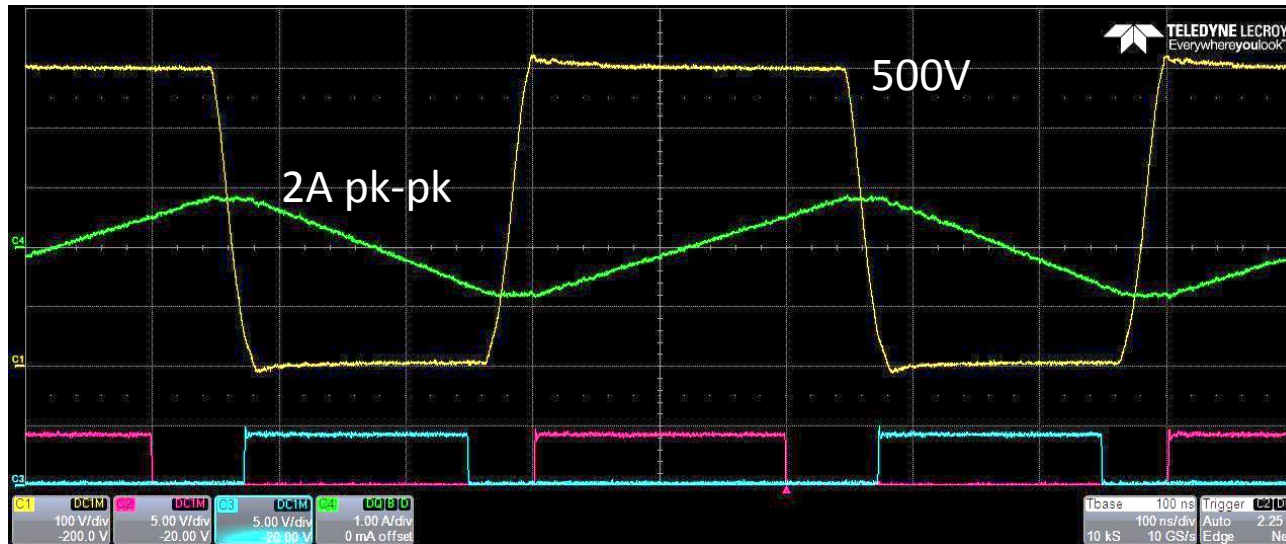


dV/dt controllable with R_{DD} from 10 V/ns to 90 V/ns



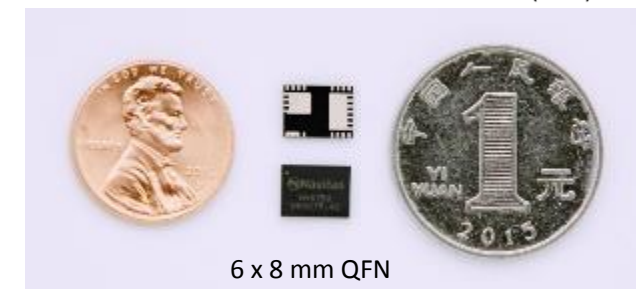


2 MHz Soft-Switching Operation



Monolithic integration at 650V

- 2x 650V eMode GaN FETs (α /symmetrical range 120-600 m Ω)
- 2x 6V GaN gate drivers
- 2x 30V to 6V GaN regulators and UVLO circuits
- 650V GaN level-shifters and bootstrap drivers
- GaN Logic (shoot-through protection, fault mgmt, ESD, etc...)

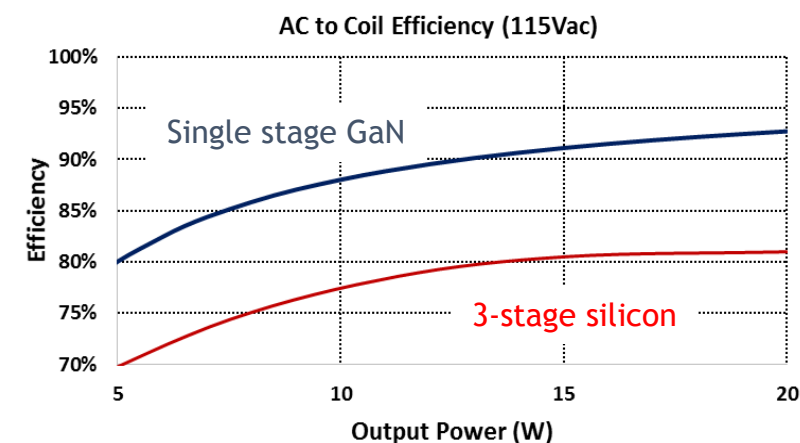
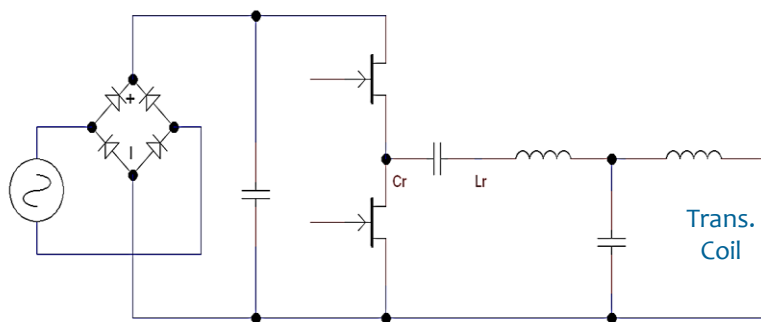
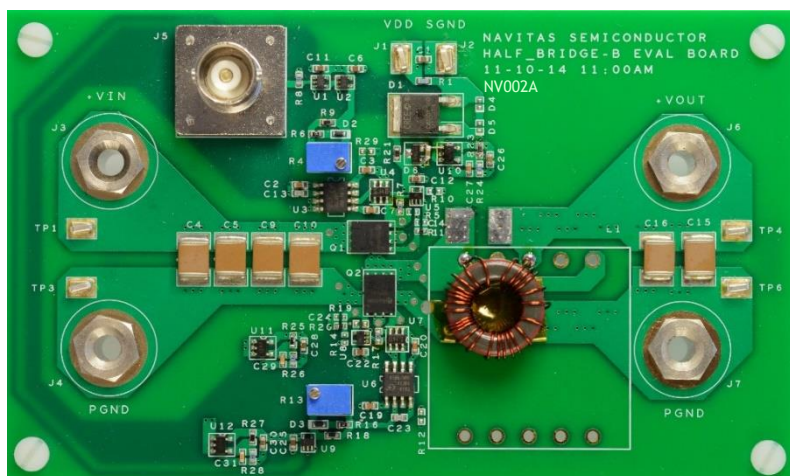
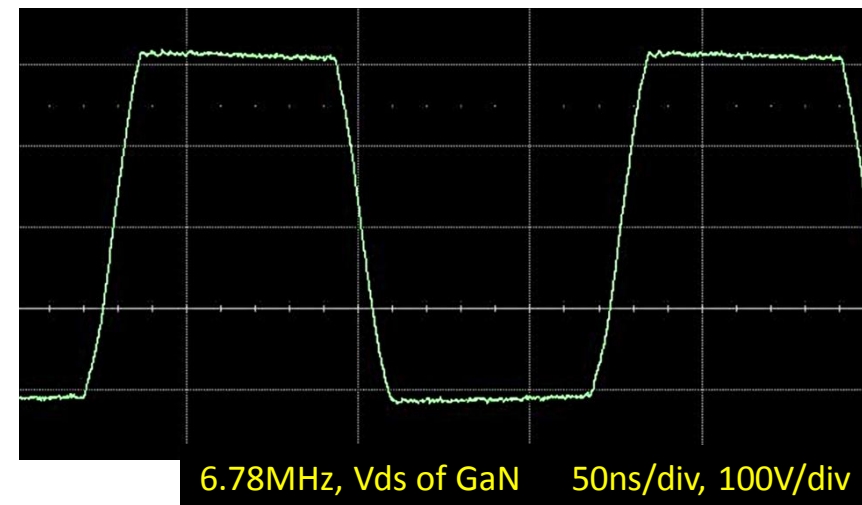


6 x 8 mm QFN



Single-Stage AirFuel Wireless Power Transmitter

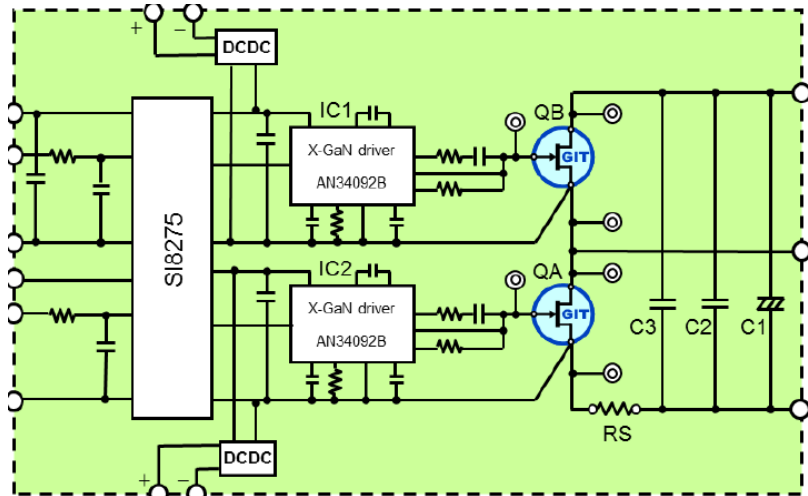
- GaN Single Stage has 10% higher efficiency AC input to RF output
- ZVS half-bridge with 2x NV6115 (650V, 500mOhm, 5x6 PQFN)
- Clean ZVS switching at 400V and 6.78MHz
- Si is limited to ~400kHz, due 10x higher RxQ, poor body diode





Complex Design → Made Simple

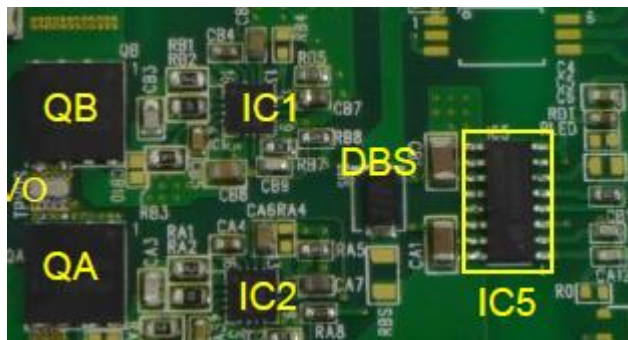
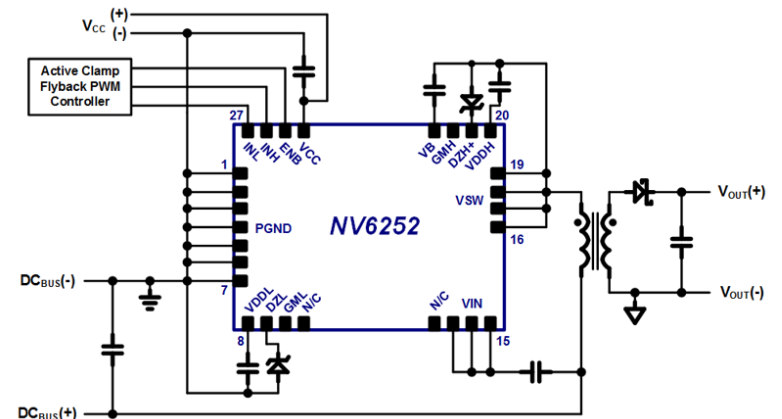
Half-Bridge *Discrete* GaN



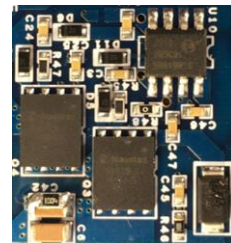
- 20x smaller PCB area
- 40+ fewer components
- Lower cost
- Robust & protected
- Simple
- Easy layout

Half-Bridge using 2x Single GaN Power ICs + isolator and bootstrap diode

Half-Bridge GaN Power IC



PCB Area: 24 x 42 ~ 1,000 mm²



PCB Area: 18 x 20 = 360 mm²

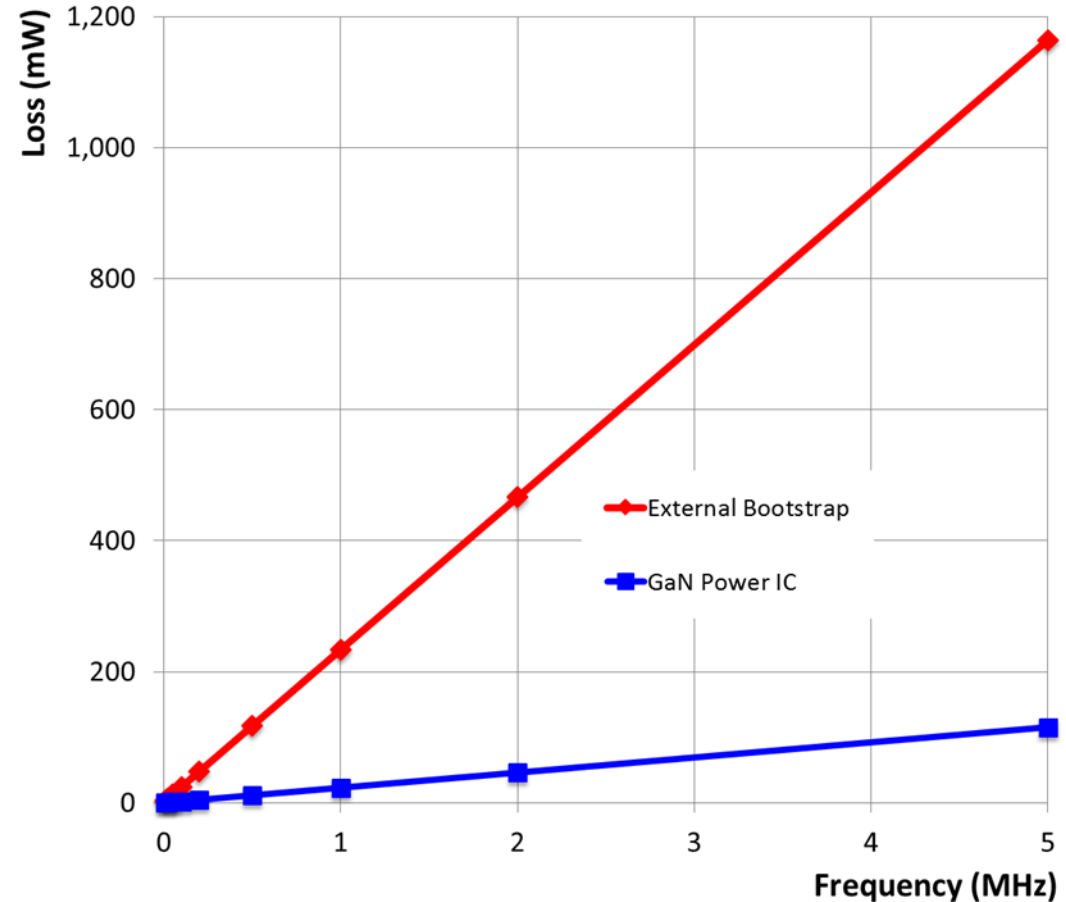


PCB Area: 6 x 8 = 48 mm²



Bootstrap Diode Integration Benefits:

- Avoids risk of dV/dt induced diode failure
- Eliminates diode recovery power loss
- Eliminates necessity of using SiC at high F_{sw}
- Saves cost, especially if SiC is required
- Charges bootstrap capacitor losslessly
- Assures full charge/voltage is delivered
- Eliminates lossy current limiting resistor
- Saves board space



$$\text{Bootstrap Diode Loss} = f(C_{\text{diode}}, I_r, Q_{rr}, F_{sw})$$

External diode ES1J (600 V, 1 A, $V_F = 1.7V$ at 1 A, SMA)

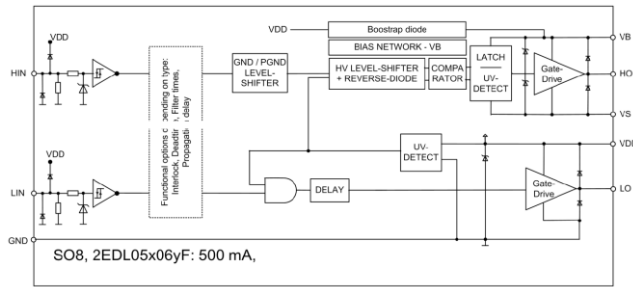


High-Frequency Level-Shift Candidates



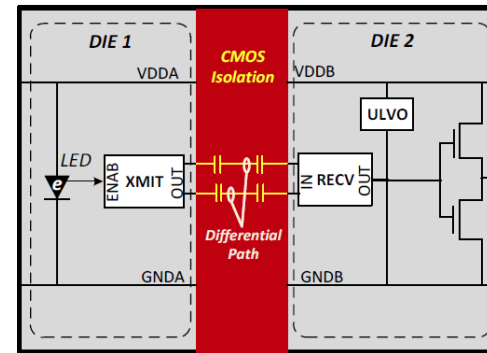
Silicon-On-Insulator (SOI)

e.g. IR2113, UCC21521



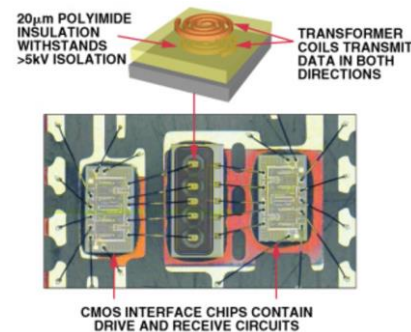
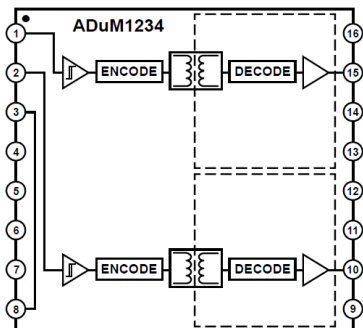
Capacitive-Coupled

e.g. Si8610



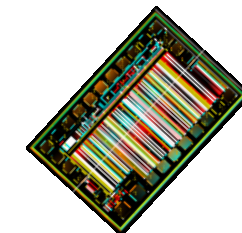
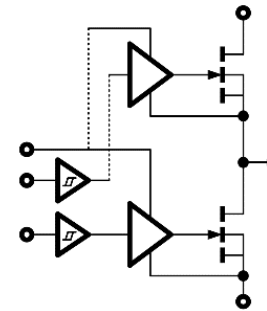
Inductive-Coupled

e.g. ADuM1234, ADuM3223, BM60210FV-C, 2ED020I06



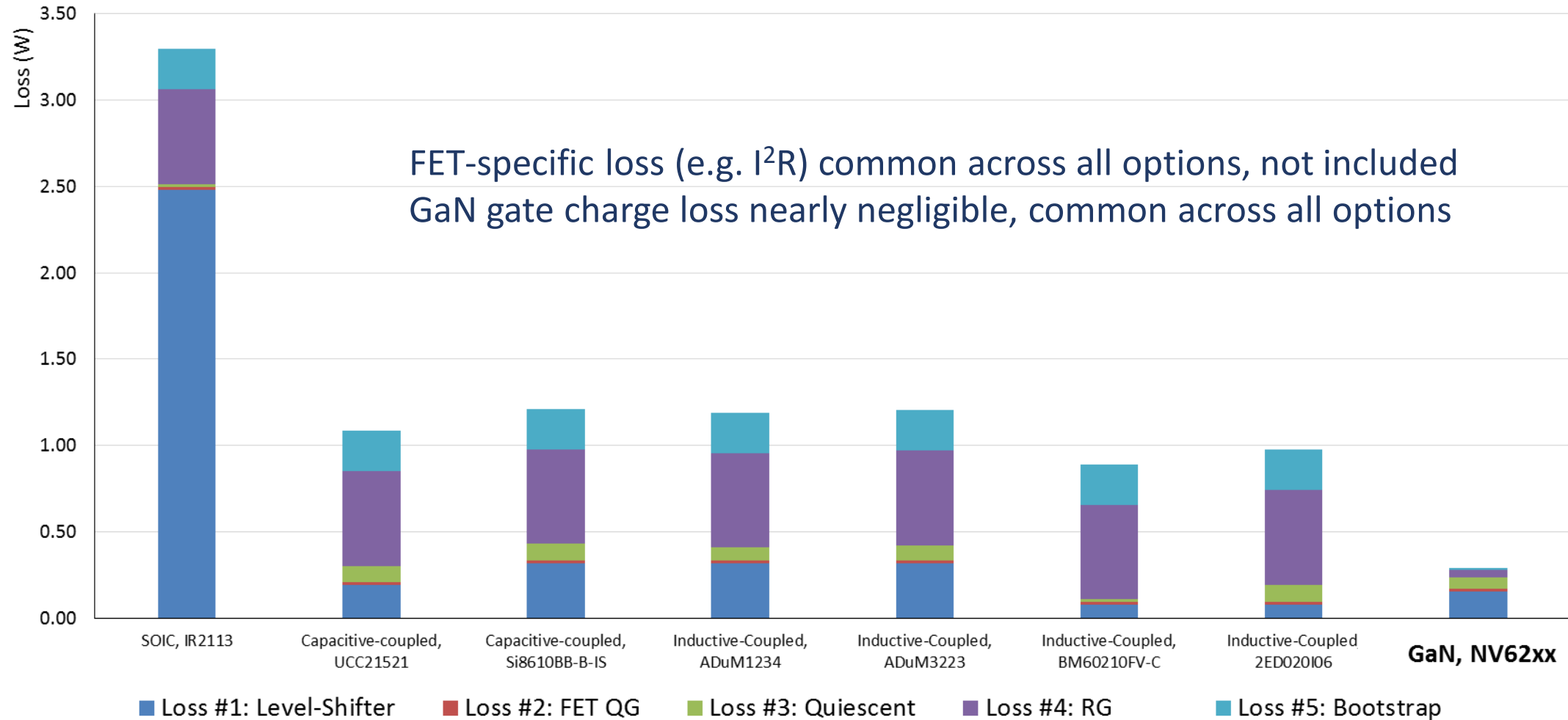
GaN Power IC

e.g. NV62xx





3x Lower Drive + Level Shift Loss, 1 MHz





The Power of GaN Power ICs

Driver Circuits

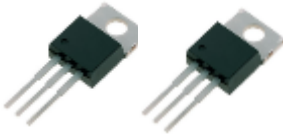
Power Devices

Passive Components

Switching Frequency

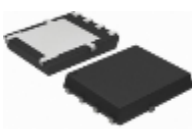
Energy Efficiency

Silicon



85-90%

Discrete GaN



88-92%

GaN Power ICs



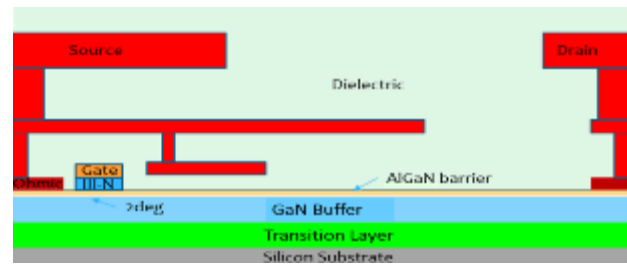
90-95%



Key Elements For New Adaptors

High Power Density Adaptors Needs

- GaN Power Device
- Higher Integration
- Advanced Magnetics
- High Frequency Controllers
- Soft Switching Topologies



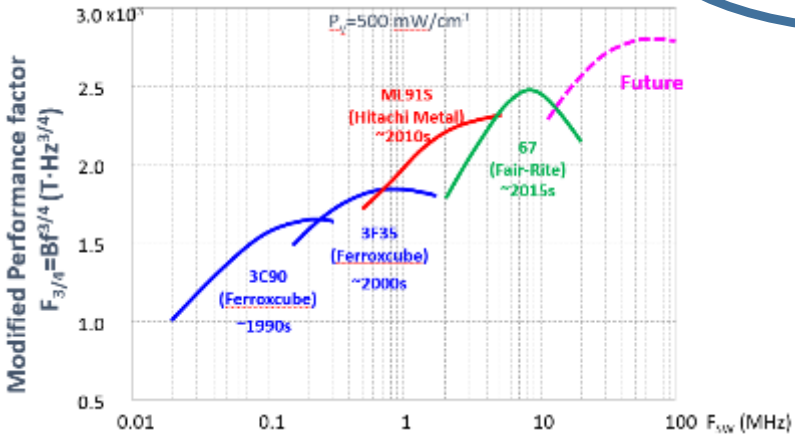
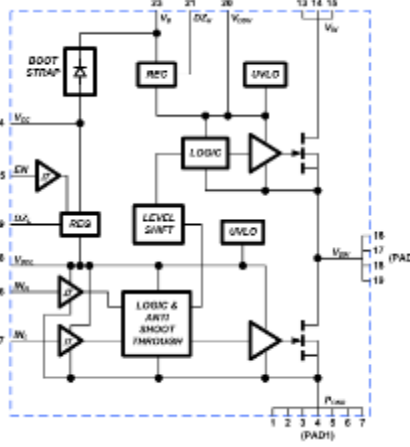
Higher Integration

GaN Power Device

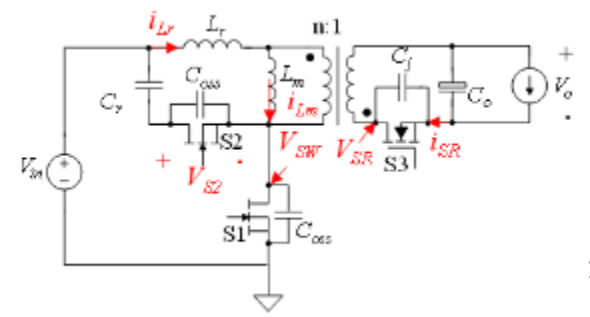
New Magnetics

New Control IC

New Topology

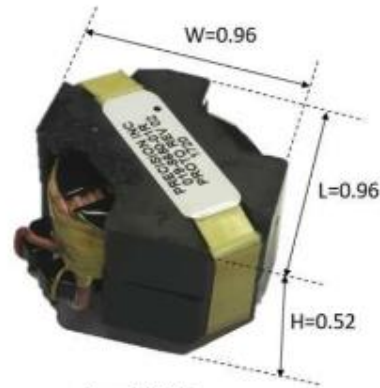


>500Khz Controllers are ready!

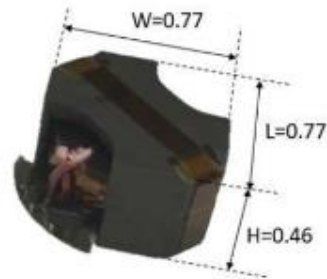




Reduced Magnetics Size @ 500kHz



F_{sw}=100kHz
RM10/ILP
0.48 in³

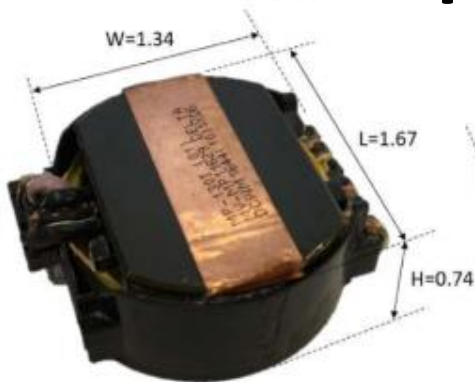


F_{sw}=200kHz
RM8/ILP
0.27 in³

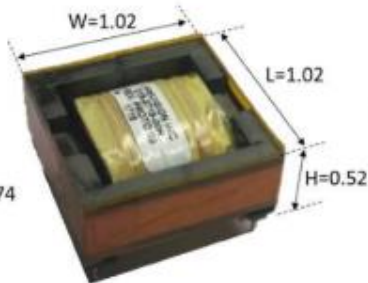
PFC Lm

$$L = \frac{V_{irms}^2 \cdot (V_o - \sqrt{2} \cdot V_{irms})}{2 \cdot f_{sw} \cdot P_i \cdot V_o}$$

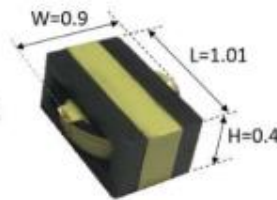
F_{sw} ↑ → L_m ↓ → Size ↓



F_{sw}=100kHz
PT40
1.66 in³



F_{sw}=300kHz
EFD25
0.54 in³



F_{sw}=500kHz
ER25
0.36 in³

LLC Lm

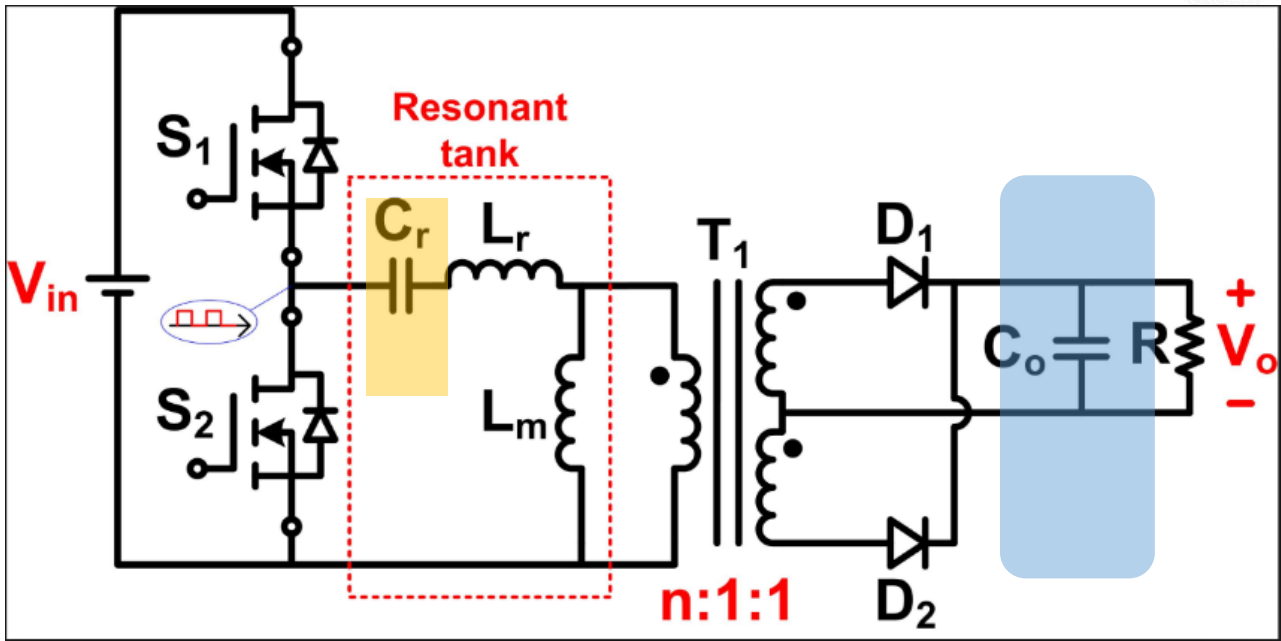
F_{sw} ↑ → L_r, C_r ↓ → L_m ↓ → Size ↓

GaN → C_{oss} ↓





Frequency Reduces Capacitor Size



Output Ripple = ESR Ripple + Cap Ripple
 ESR is dominant factor at high fsw

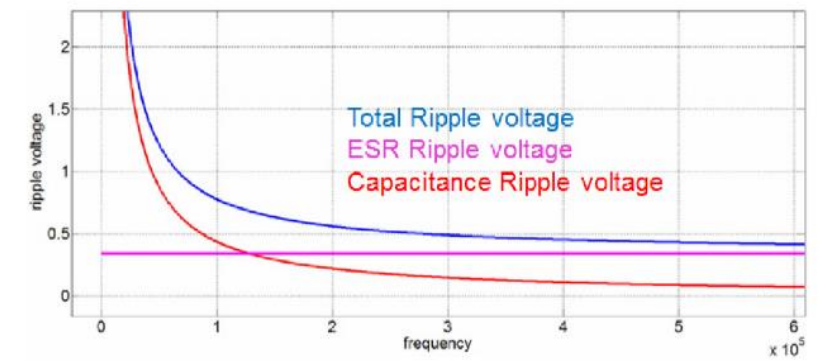


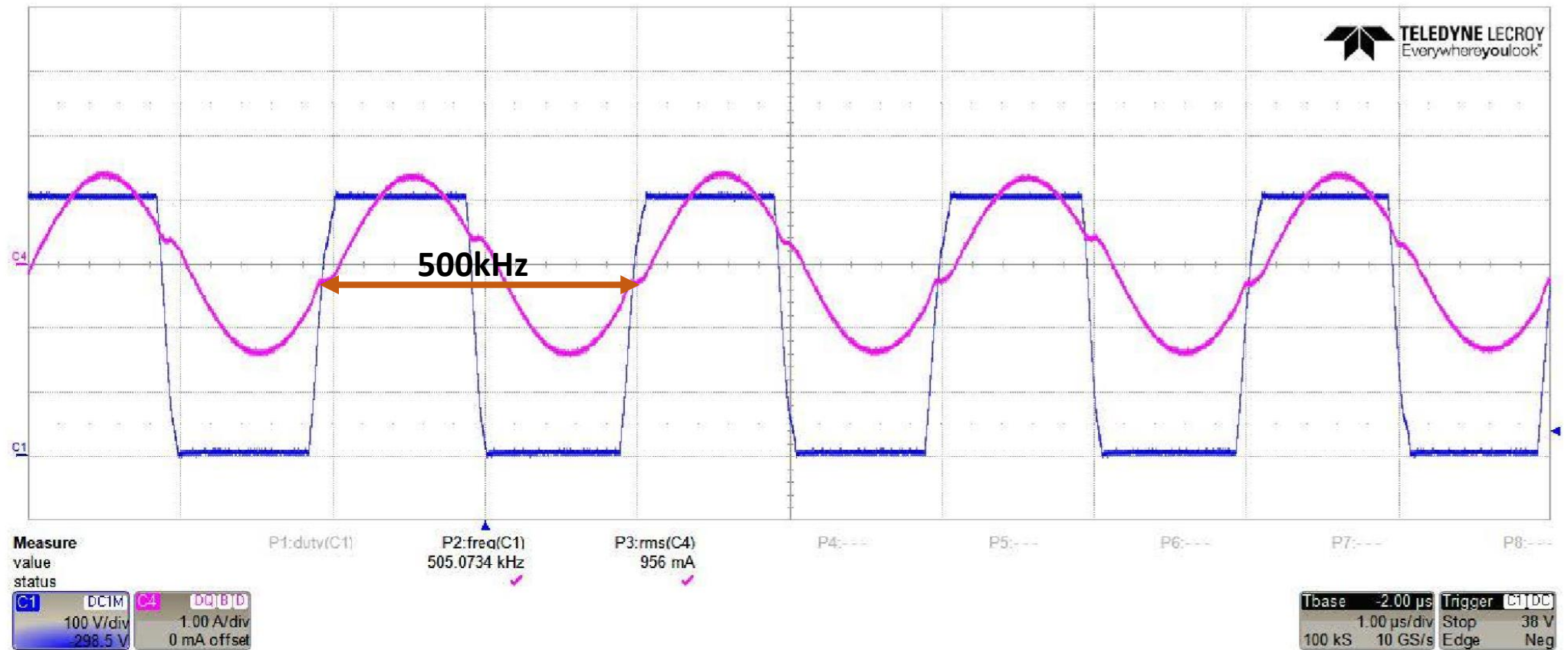
Fig. 4. Ripple voltage variation according to the switching frequency

“Design Considerations of Resonant Network and Transformer Magnetics for High Frequency LLC Resonant Converter”,

J Electr Eng Technol.2016; 11(2): 383-392

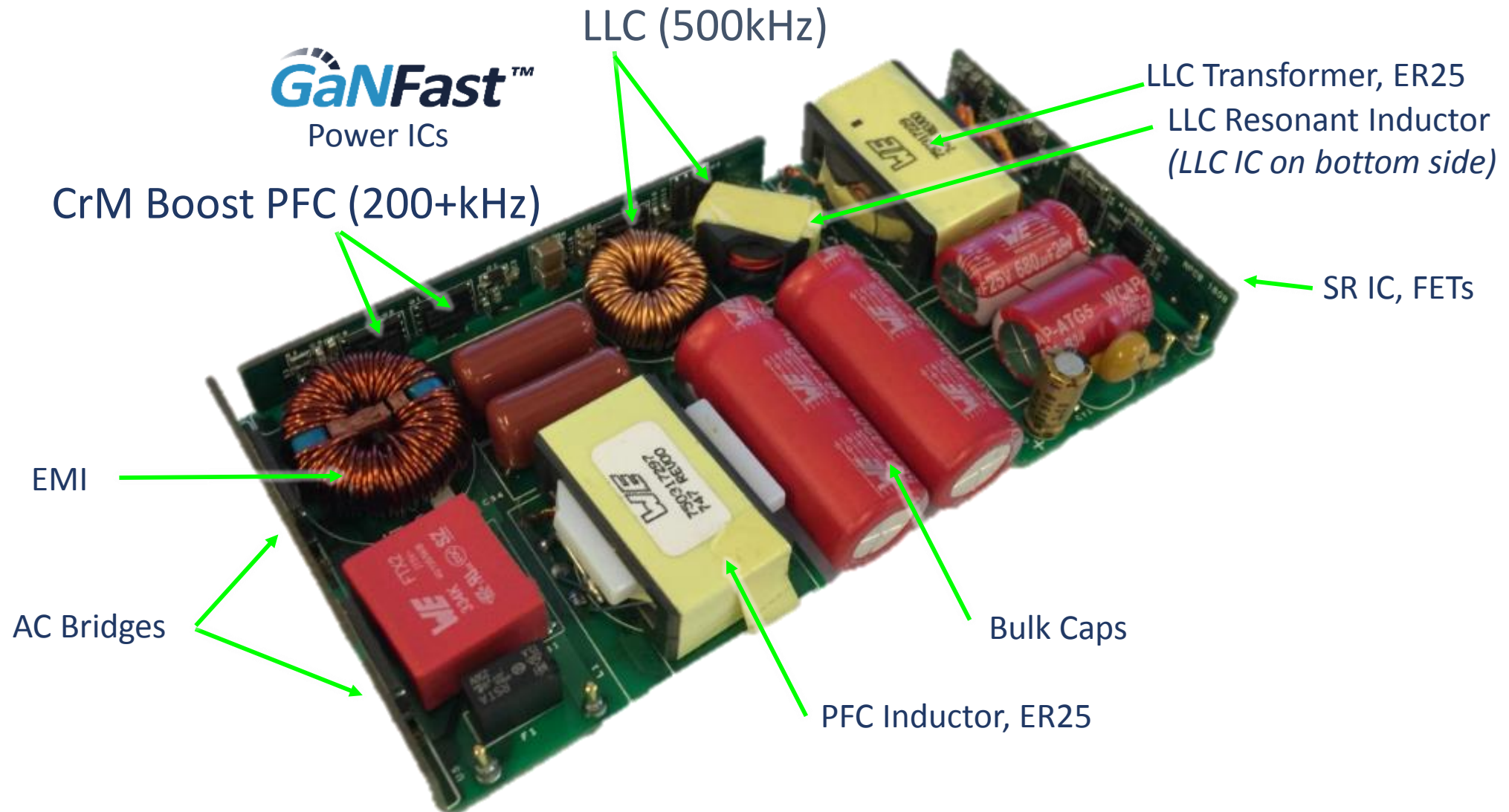


Switching Waveforms: DC-DC (LLC) Stage



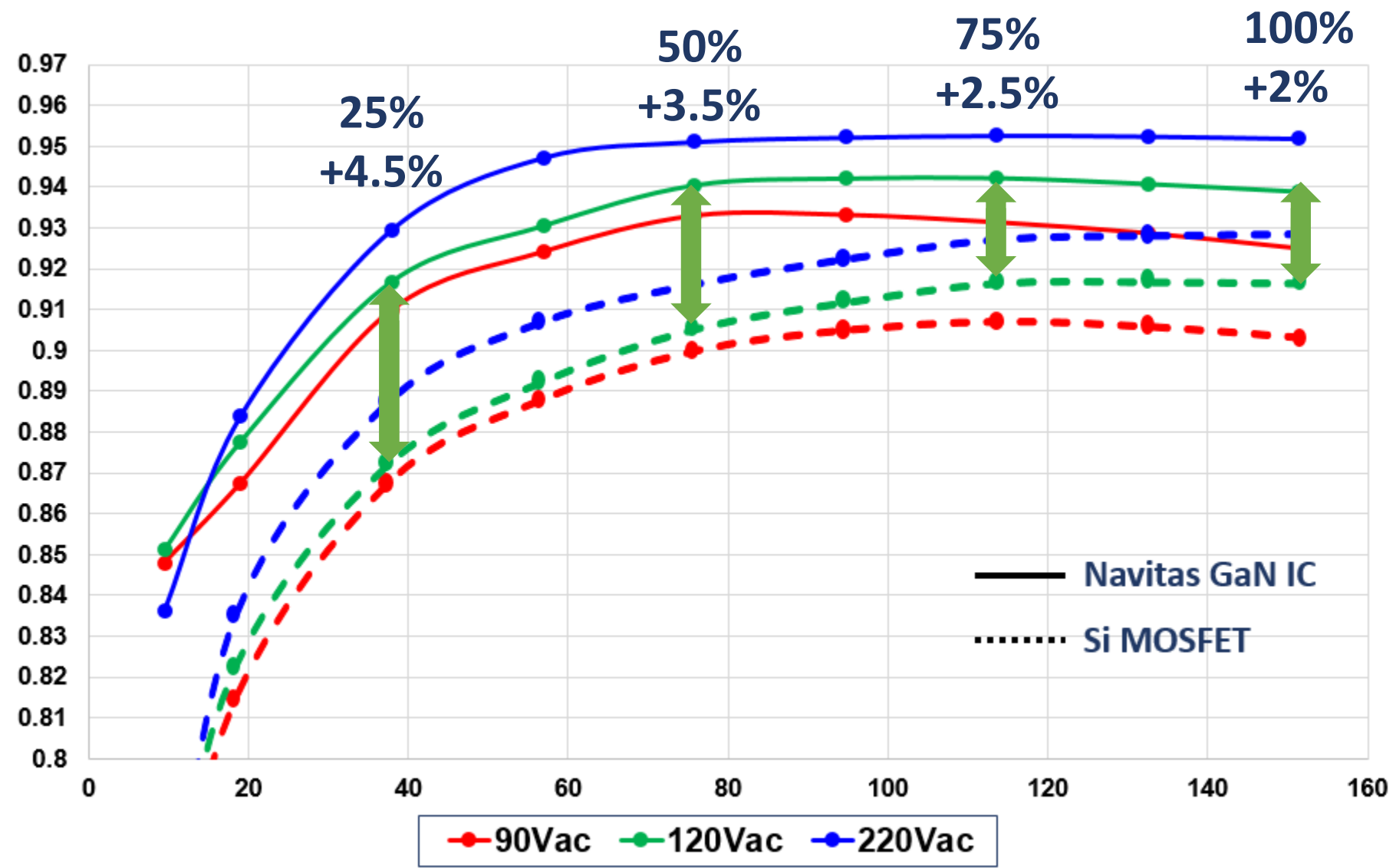


40W/in³, 95% efficient, 150W, 19V Adaptor





GaN Efficiency Outperforms Silicon





Let's go **GaNFast™**