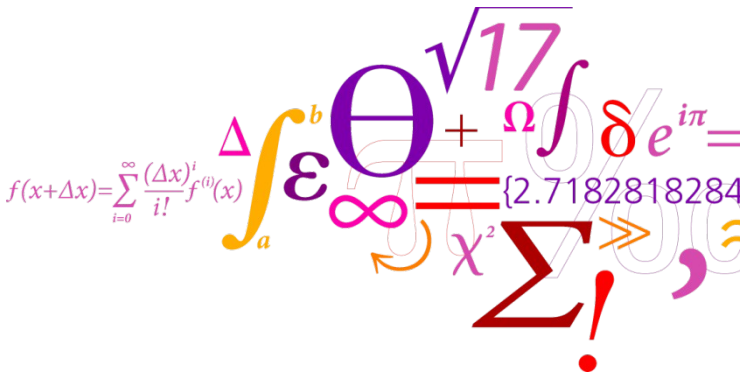
3D Microfabricated Air-core Inductors for Integrated Power Supply

Hoà Thanh Lê

DTU Danchip
National Center for Micro- and Nanofabrication

DTU Electrical Engineering
Department of Electrical Engineering

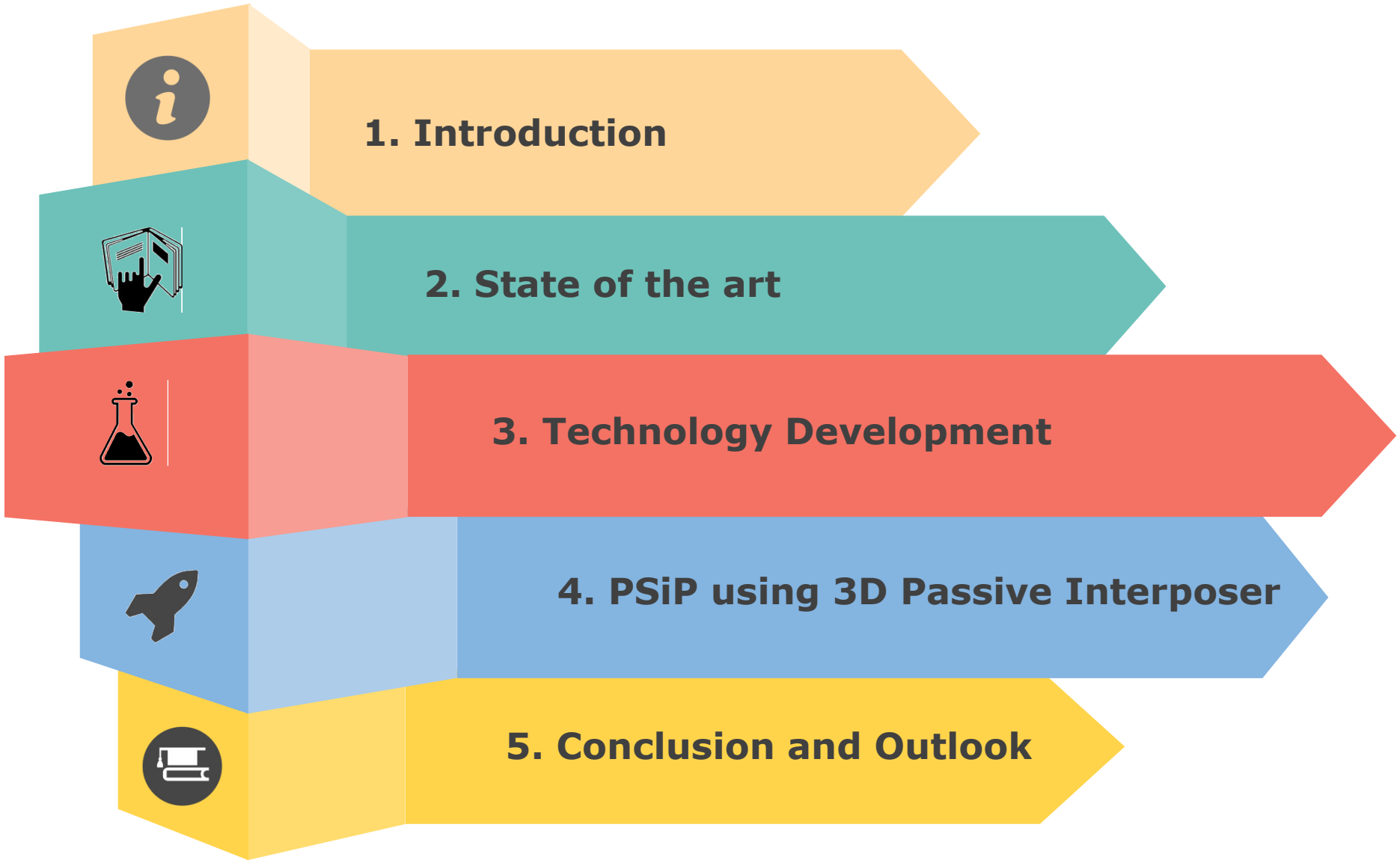


What is a power supply?

Want it to disappear?

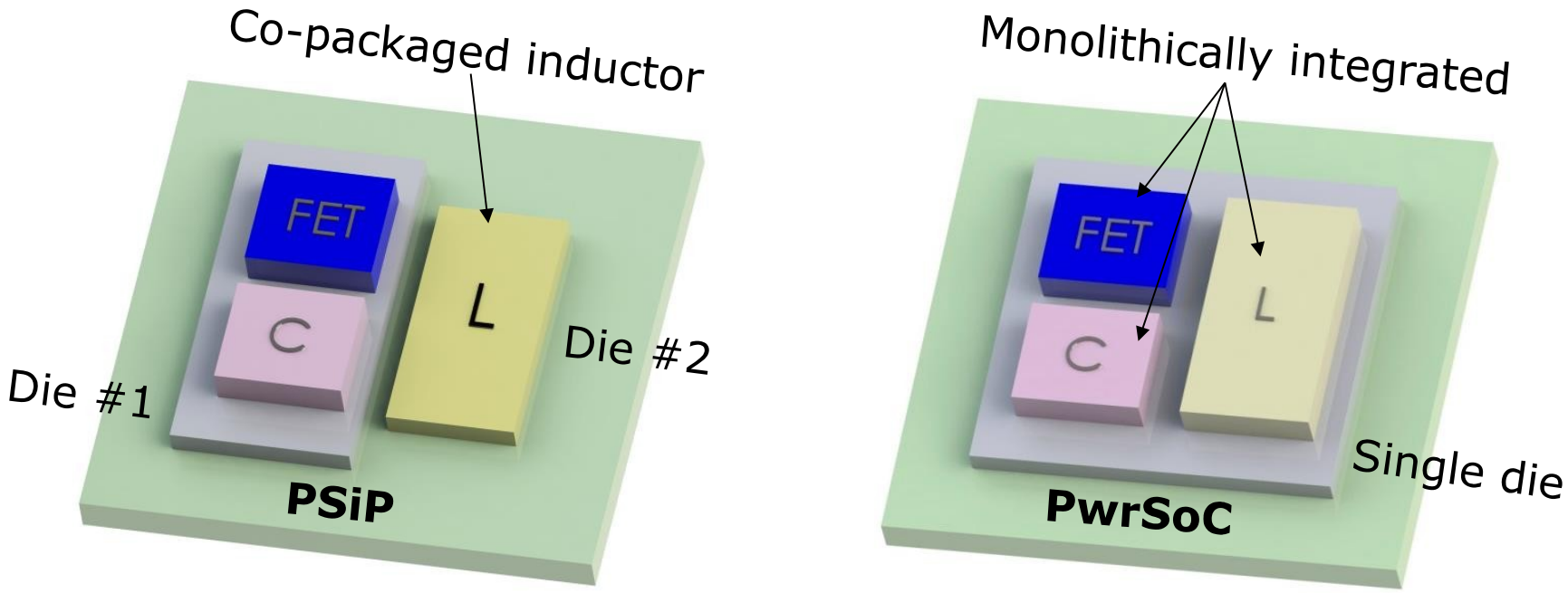
Integrated Power Supply

- Smaller, more functionalities
- Consume less energy
- Cheaper
- IoTs, LED lighting, etc.

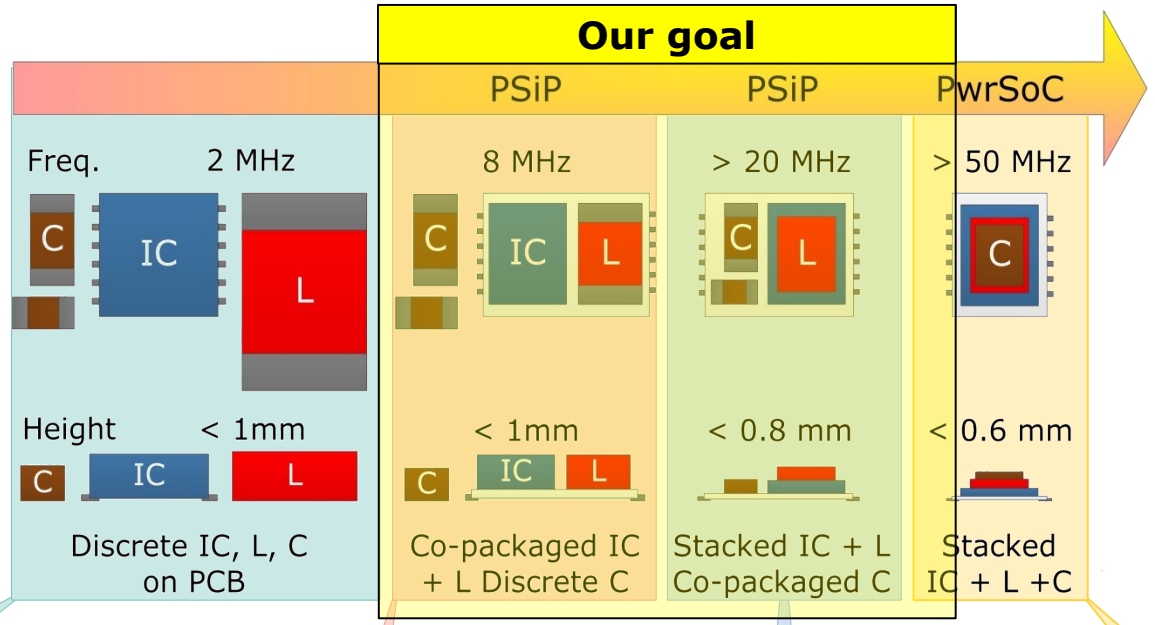

1. Introduction
2. State of the art
3. Technology Development
4. PSiP using 3D Passive Interposer
5. Conclusion and Outlook

Integrated power supplies

- Power Supply In Packaged (PSiP)
- Power Supply On Chip (PwrSoC)

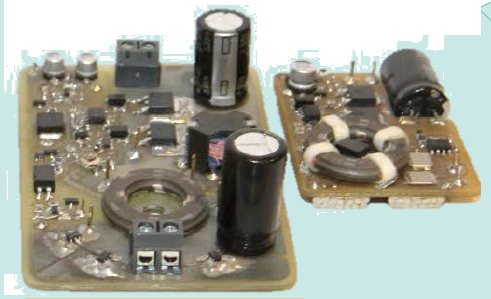


PwrSoC Evolution and State of the Art



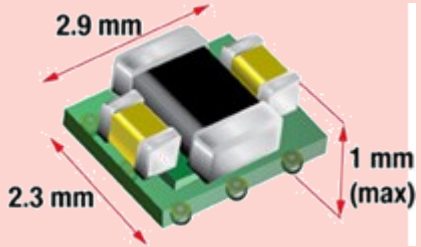
Frequency ↑↑

Size ↓↓



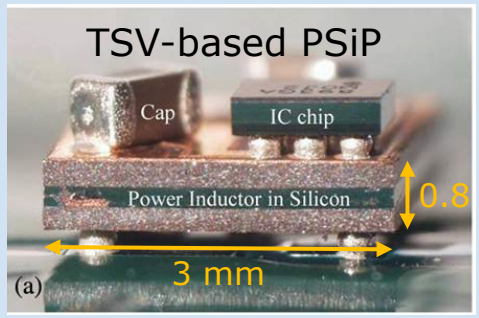
5 cm

Discrete 40W SMPS prototypes, DTU Elektro



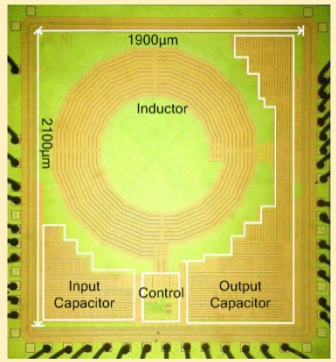
2.3-4.8 V to 1.8 V, 5.5 MHz, 90 %

TI product, TPS82671



3.6 V - 1.8 V, 1 W, 83 %

University of Florida, 2017



3.3 V – 2.5 V, 0.4 W, 180 MHz, 80.5 %

Fudan University, *2009*

Prof. Mathuna et al. 2013 , PwrSoC for more than Moore technologies

PwrSoC
Enabling Technologies

- Topologies
- Semiconductor
- Passive Device
- Packaging

"I want to develop the **world's smallest** power supply technology"

TinyPower

PwrSoC
Enabling Technologies

- Topologies
- Semiconductor
- Passive Device
- Packaging

"I want to develop the **world's smallest** power supply technology"

TinyPower

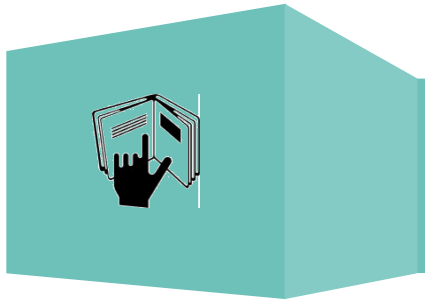
This talk

Microinductor & Packaging

PSiP technology

DC-DC converter

(VHF, 1-2 W, 5 - 12 V_{IN}, 3.3 - 5 V_{OUT}, $\eta > 80$ %)



2. State of the art

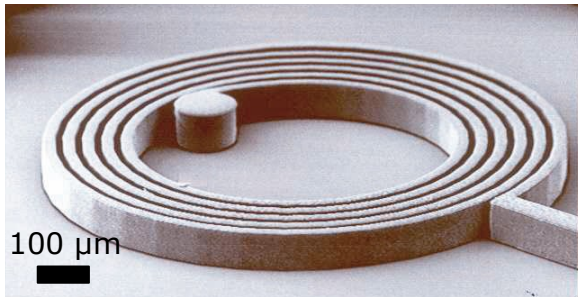
2.1 Microfabricated Inductor

2.2 Packaging Technology

2.3 Problems and Solutions

Winding structure

2D

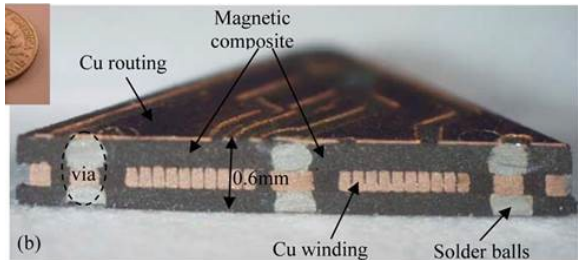


3D

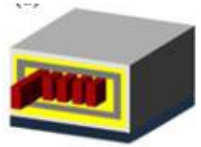
Kim et al. 2013, JMM

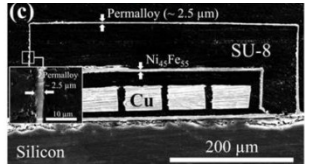
Core material

Powder

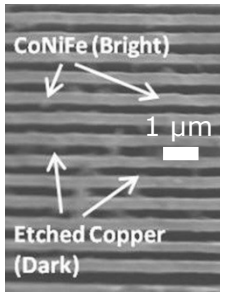


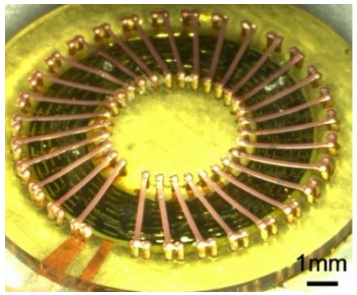
Thin film





Lamination

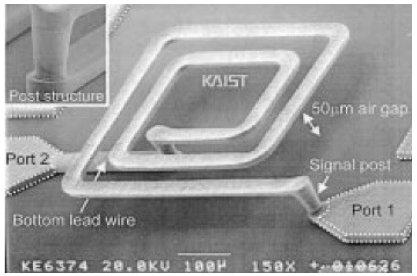




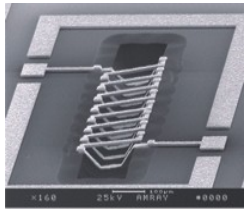
Wang et al. 2011, TPEL
Anthony et al. 2014, Micro. Eng.
Kim et al. 2013, JMM

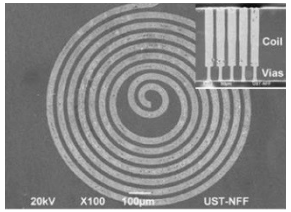
Fab. technology

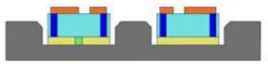
On-Si

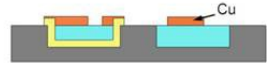


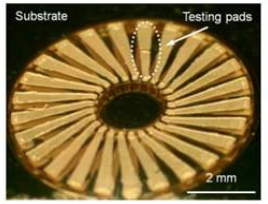
In-Si

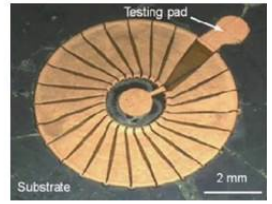




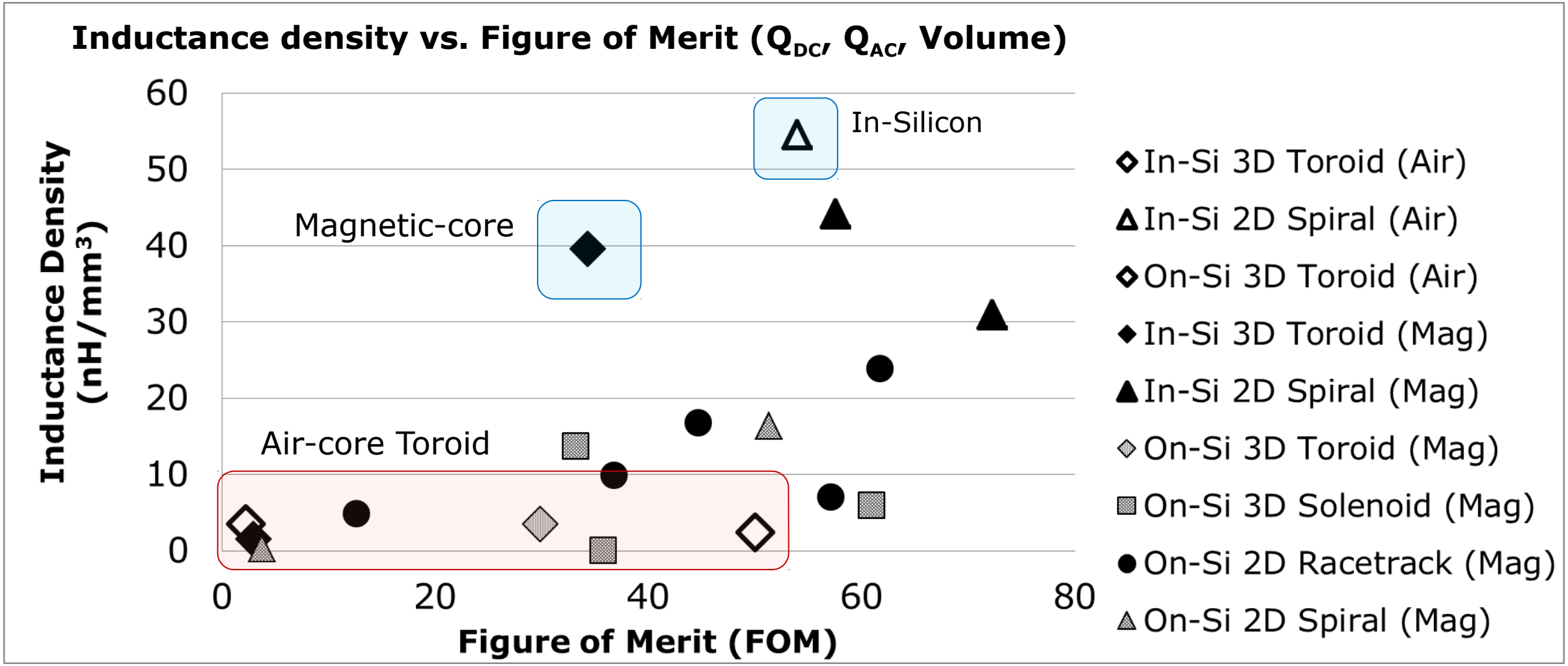




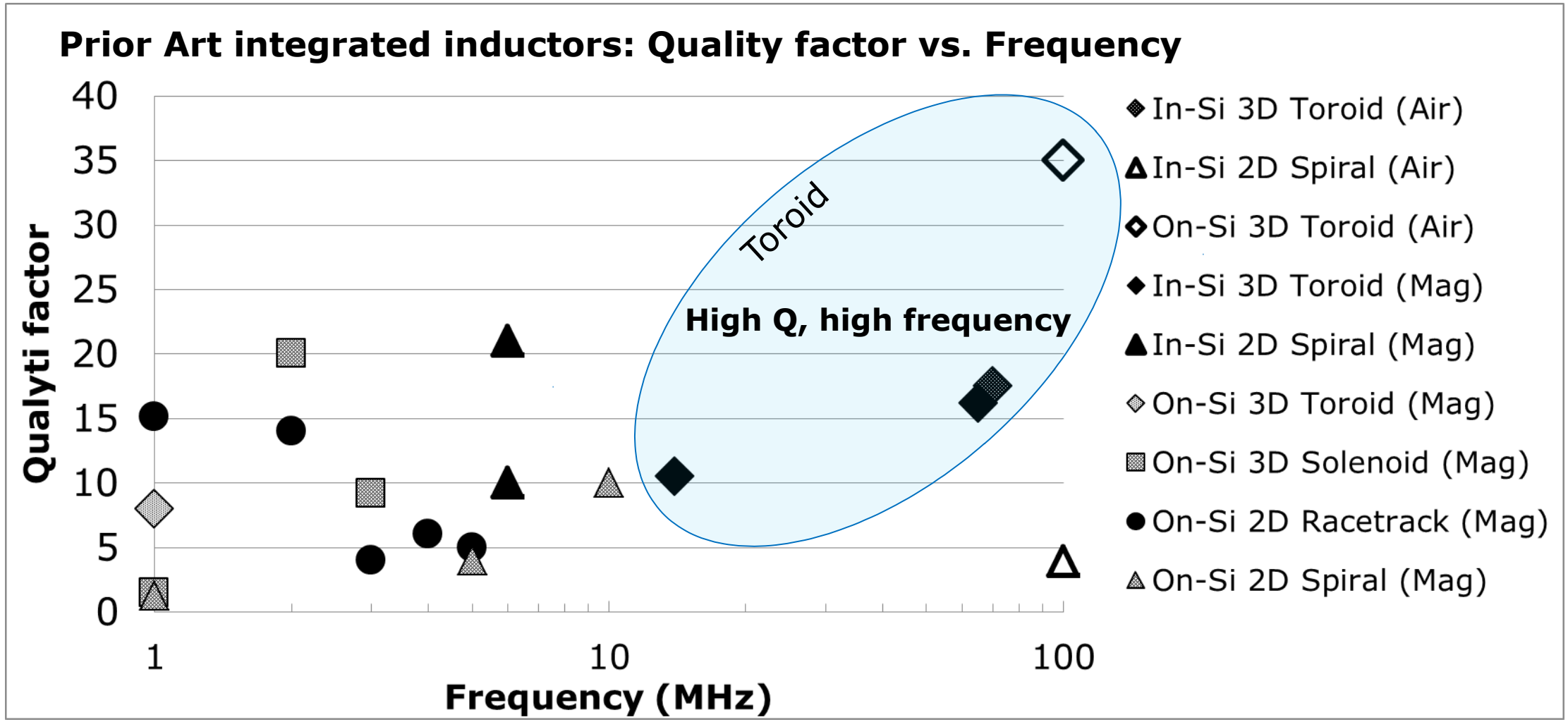




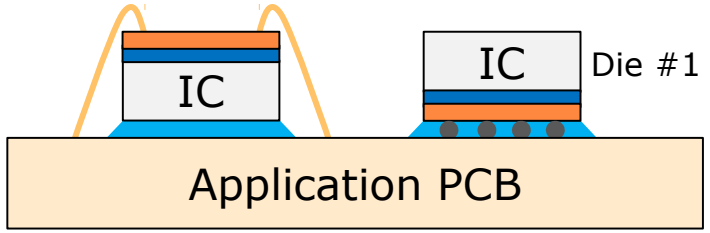
Wu et al. 2011, IEEE Elec. Device Let.
Wang et al. 2011, TPEL
Yu et al. 2013, JMEMS



$$\mathrm{FOM} = \frac{\sqrt{Q_{DC} \cdot Q_{AC}}}{\mathrm{Volume}} = \frac{\sqrt{L_{DC}/R_{DC} \cdot Q_{AC}}}{\mathrm{Volume}}$$

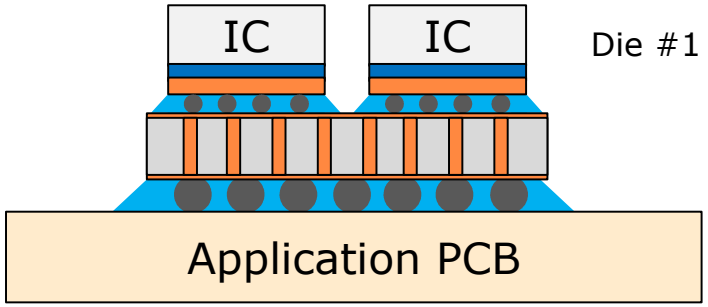

Prior Art integrated inductors: Quality factor vs. Frequency
Qualyti factor
40
35
30
25
20
15
10
5
0
1
10
100
Frequency (MHz)
Toroid
High Q, high frequency
In-Si 3D Toroid (Air)
In-Si 2D Spiral (Air)
On-Si 3D Toroid (Air)
In-Si 3D Toroid (Mag)
In-Si 2D Spiral (Mag)
On-Si 3D Toroid (Mag)
On-Si 3D Solenoid (Mag)
On-Si 2D Racetrack (Mag)
On-Si 2D Spiral (Mag)

2D



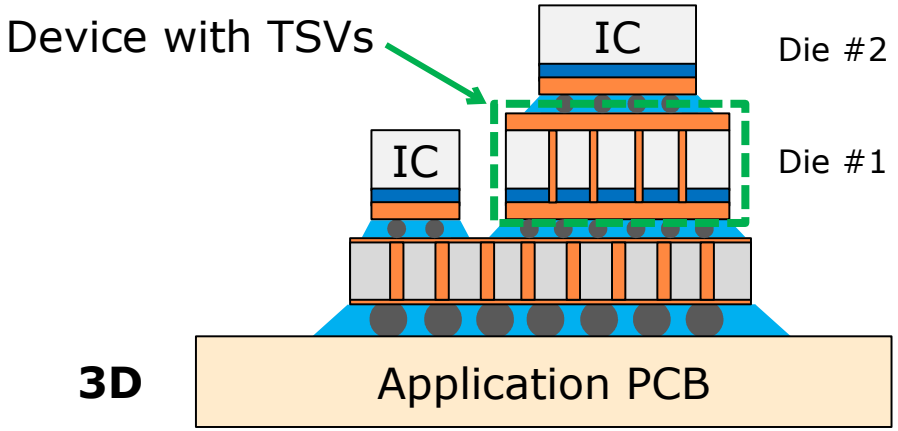
- Wire bond – high noise
- Flip-chip - shorter interconnects, less noise

2.5D



- TSV-based interposer
- Higher area density
- Thermal design is critical

3D



- Flip-chip bonding
- TSV-based IC (die #1)
- 3D stacking of multiple dies
- Thermal design is critical

- Lack of a TSV technology for 3D inductor and packaging
- CMOS-compatible for monolithic integration
- Toroidal inductor for high Q, high frequency, low EMI
- In-silicon inductors for low profile

Solutions?

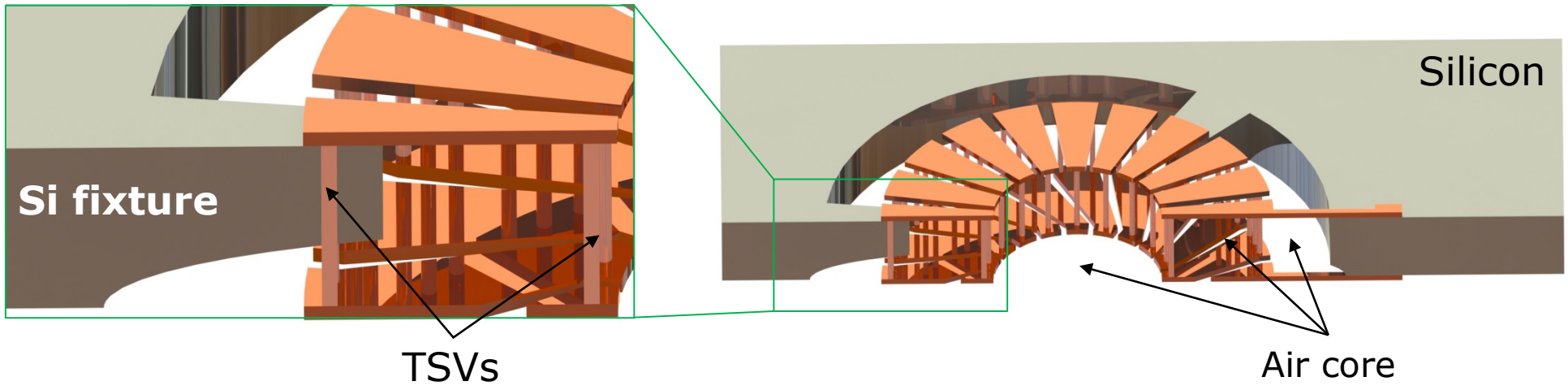
A novel design of 3D TSV air-core inductor

Features

- TSV-based inductor
- Free-standing windings without Si core
- Toroidal shape
- Hollow air core

Advantages

- ✓ In-silicon inductors, 3D packaging
- ✓ Low parasitic -> High Q, high frequency
- ✓ Low EMI with toroidal core
- ✓ Possibility for magnetic-core filling

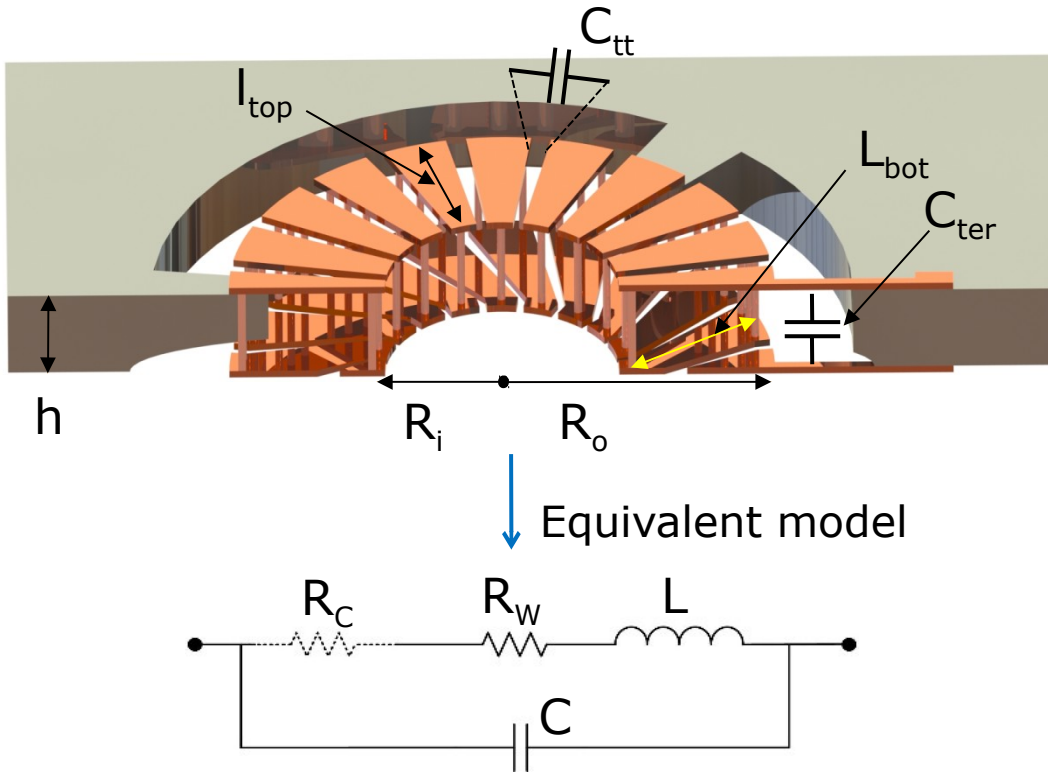


3. Technology Development

Analytical Modeling

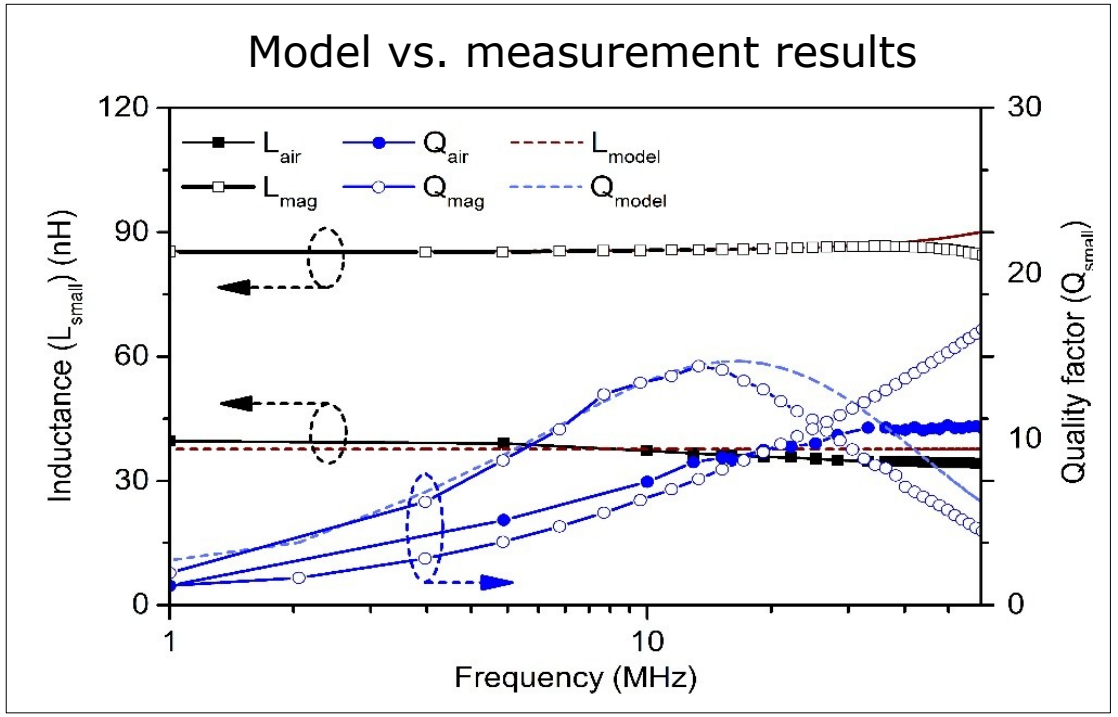
Inductor model

- predicts inductor's properties (L, R, C, Q)
- is based on an equivalent model
- accounts geometrical dimensions

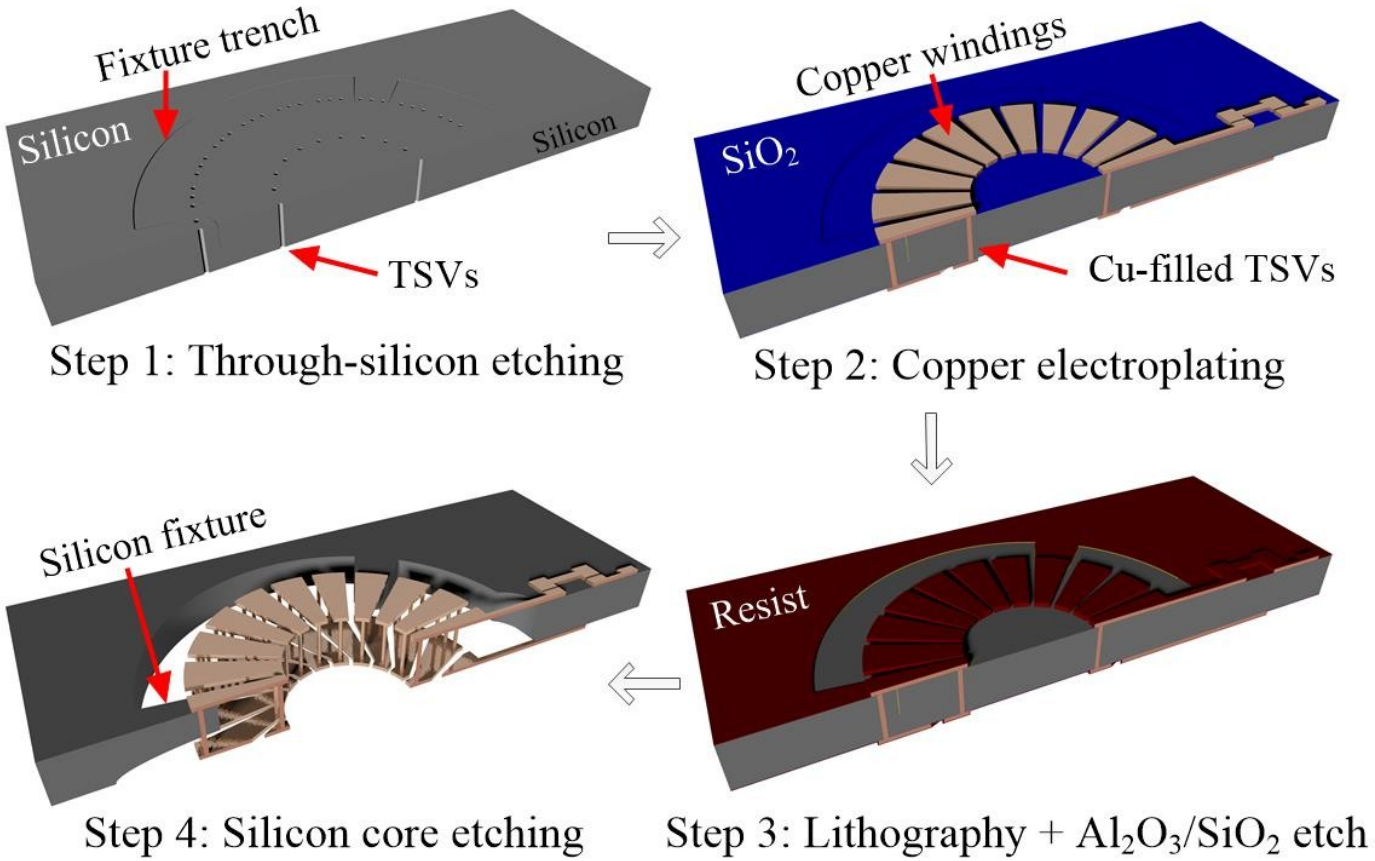


Model Accuracy for air-core inductor

- Inductance > 92.7 % (f < 66 MHz)
- Q > 90 % (f < 35 MHz)



Process 3D Animation



Step 1 is to create 50-µm-diameter TSVs in a 350-µm-thick wafer by deep reactive ion etching and atomic layer deposition.

Step 2 includes deposition of insulation layers 50 nm Al_2O_3 and 1.5 µm SiO_2, electroplating of copper in TSVs and top and bottom conductors, and copper wet etching to define the toroidal windings.

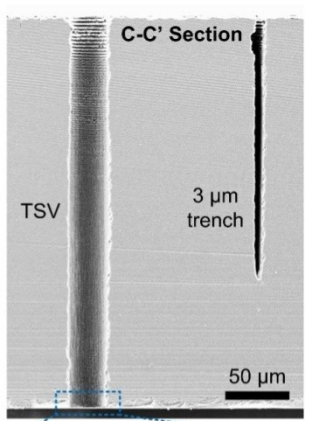
Step 3 starts with protecting Cu windings by Al_2O_3 followed by photolithography of spray-coated resist and wet etching using hydrofluoric acid.

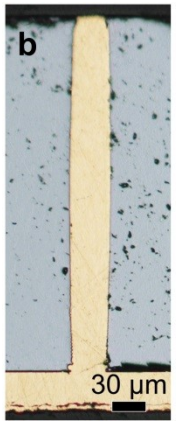
Step 4 is to etch the silicon core using dry ICP etching and release the suspended windings by wet etching and drying steps.

3D Animation is available at https://www.nature.com/articles/micronano201782

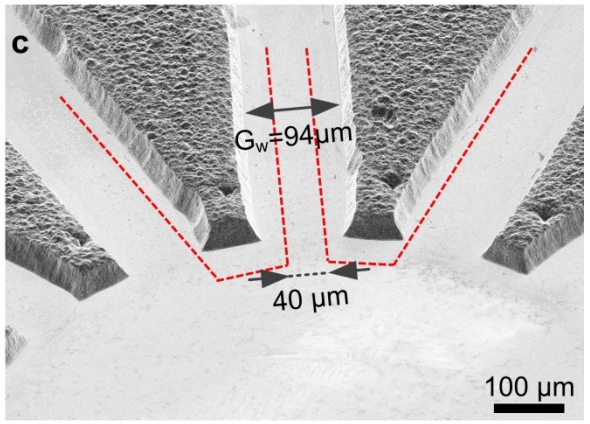
Fabrication Results at Important Steps

TSV Etching and Filling

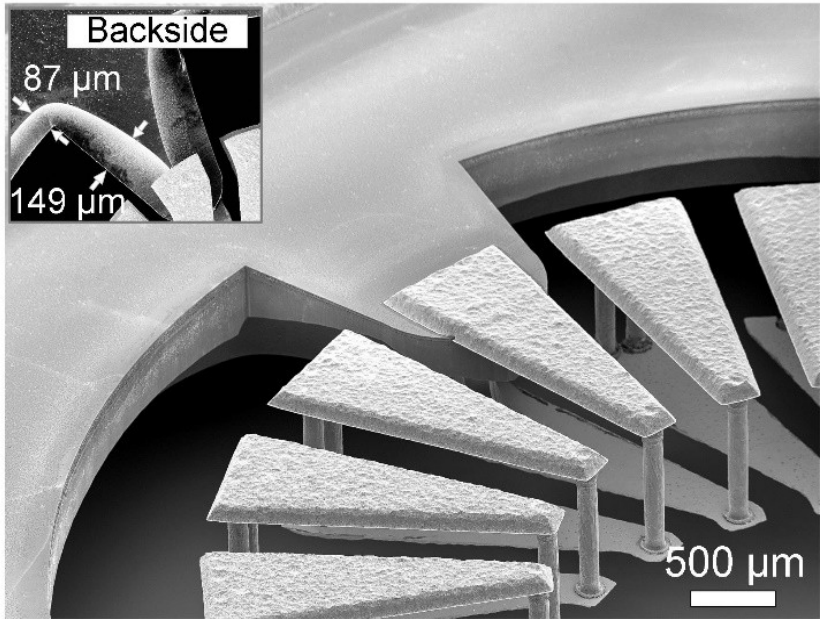




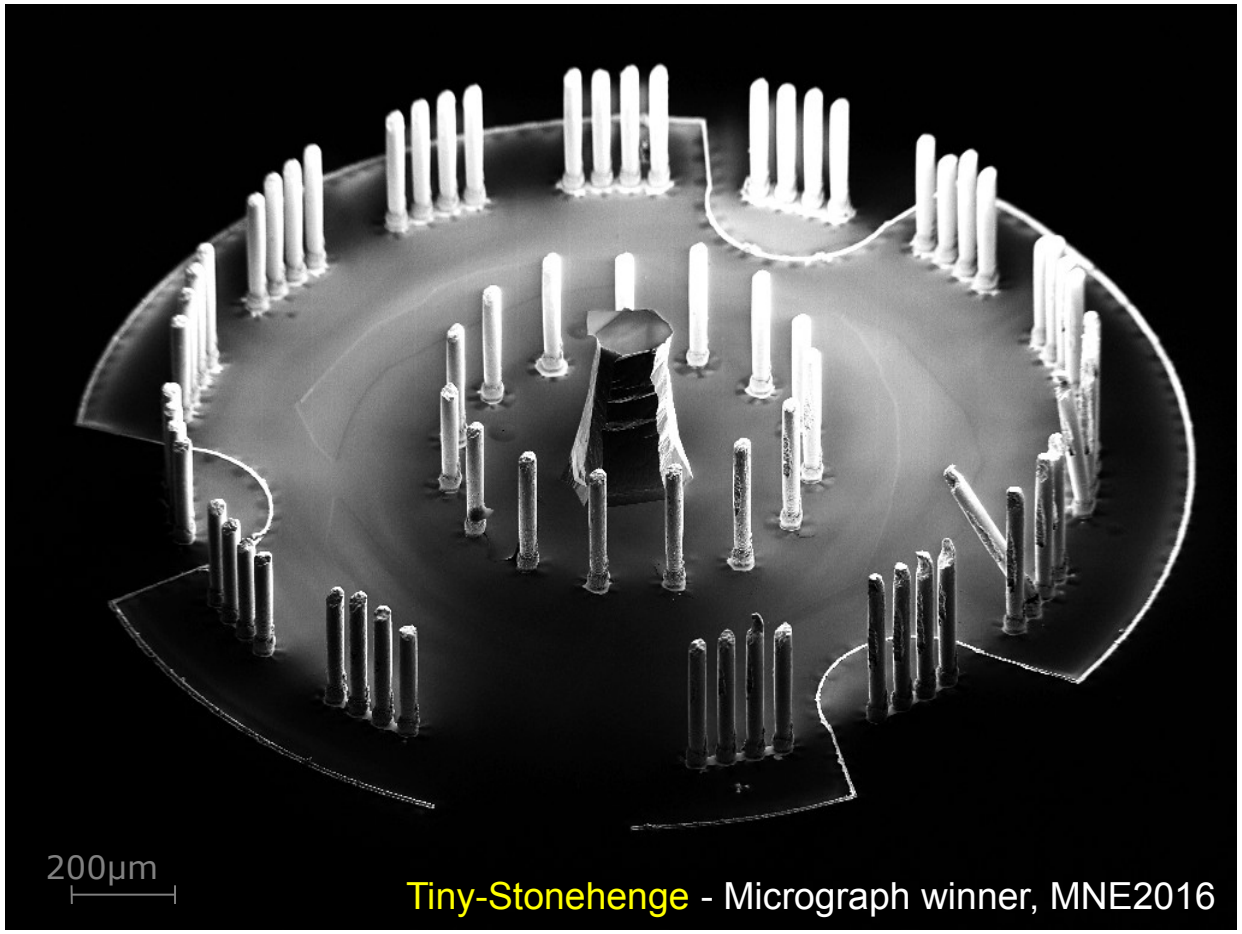
Winding patterning



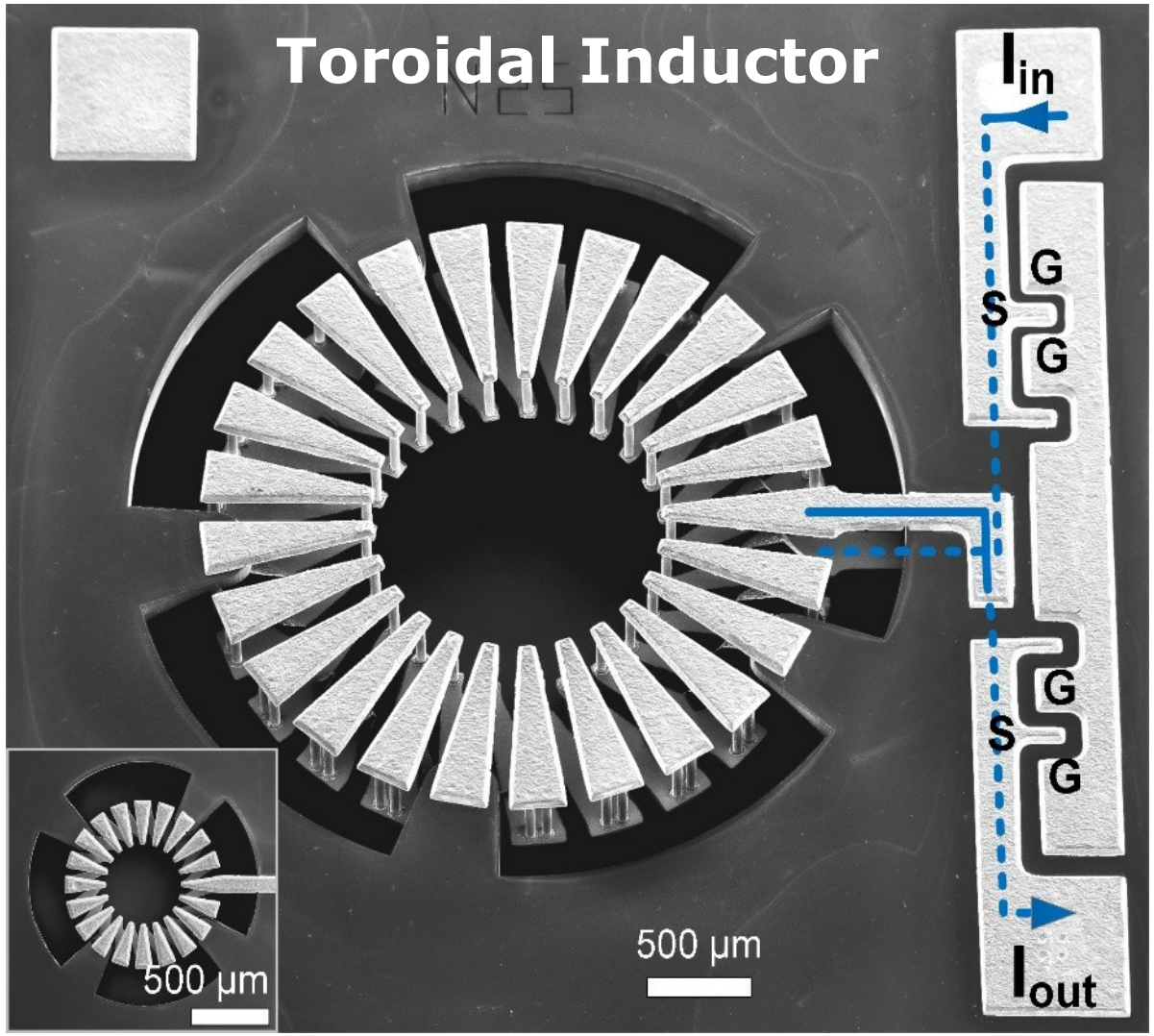
Si-core etching and releasing

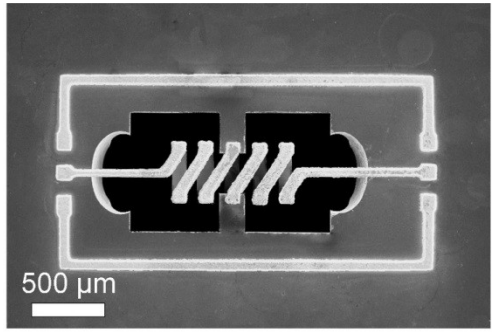


70 Cu-filled TSVs on a 15-turn toroidal inductor

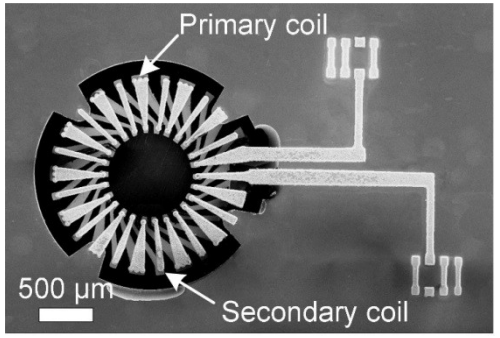


Fabrication Results



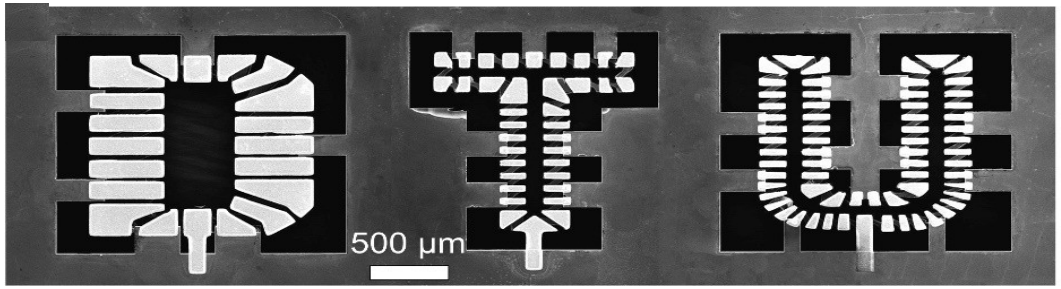


Solenoid



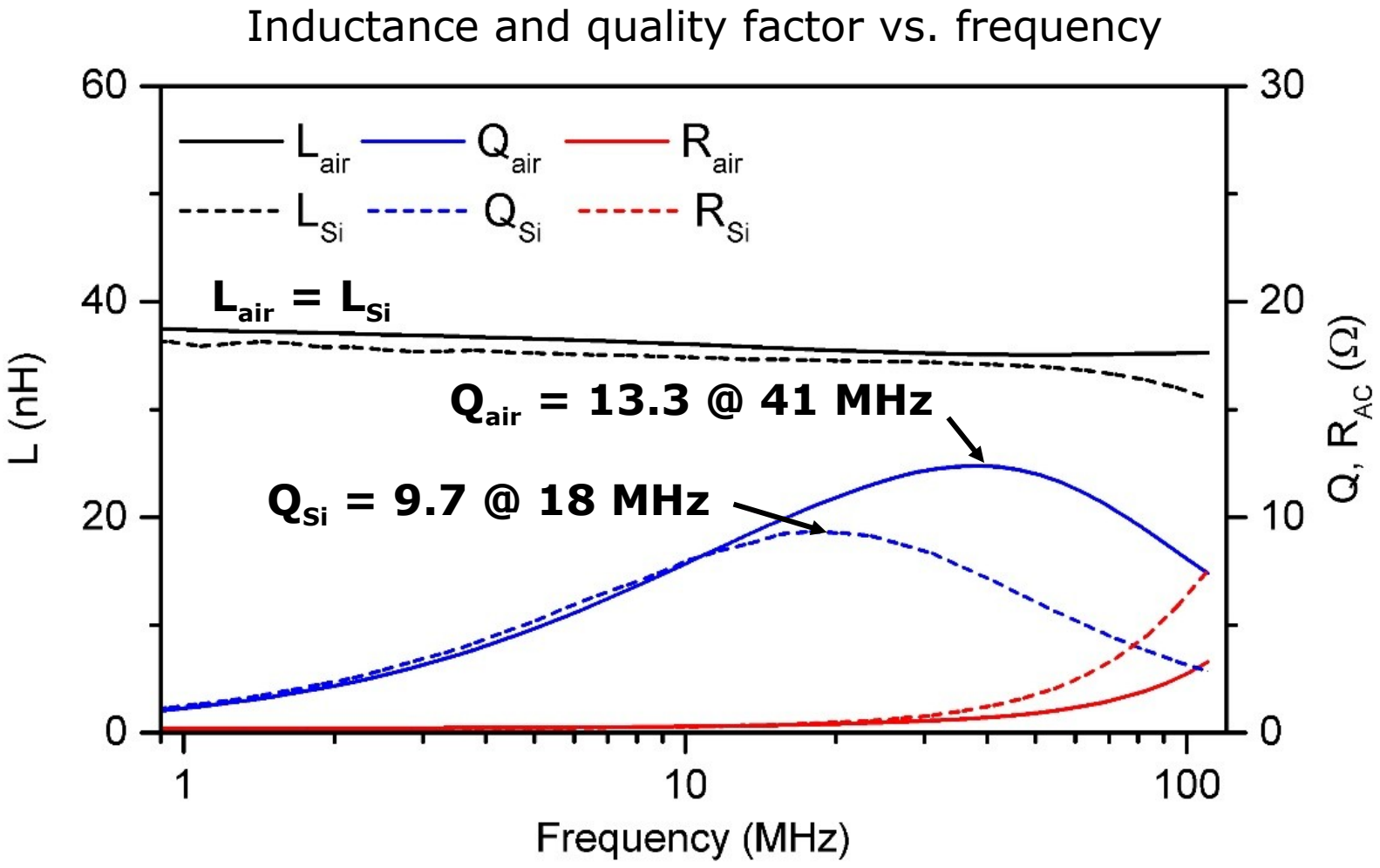
Transformer

DTU Inductor



Hoa Thanh le et al. 2018, Microsystems & Nanoengineering

Air-core vs. Silicon-core inductor

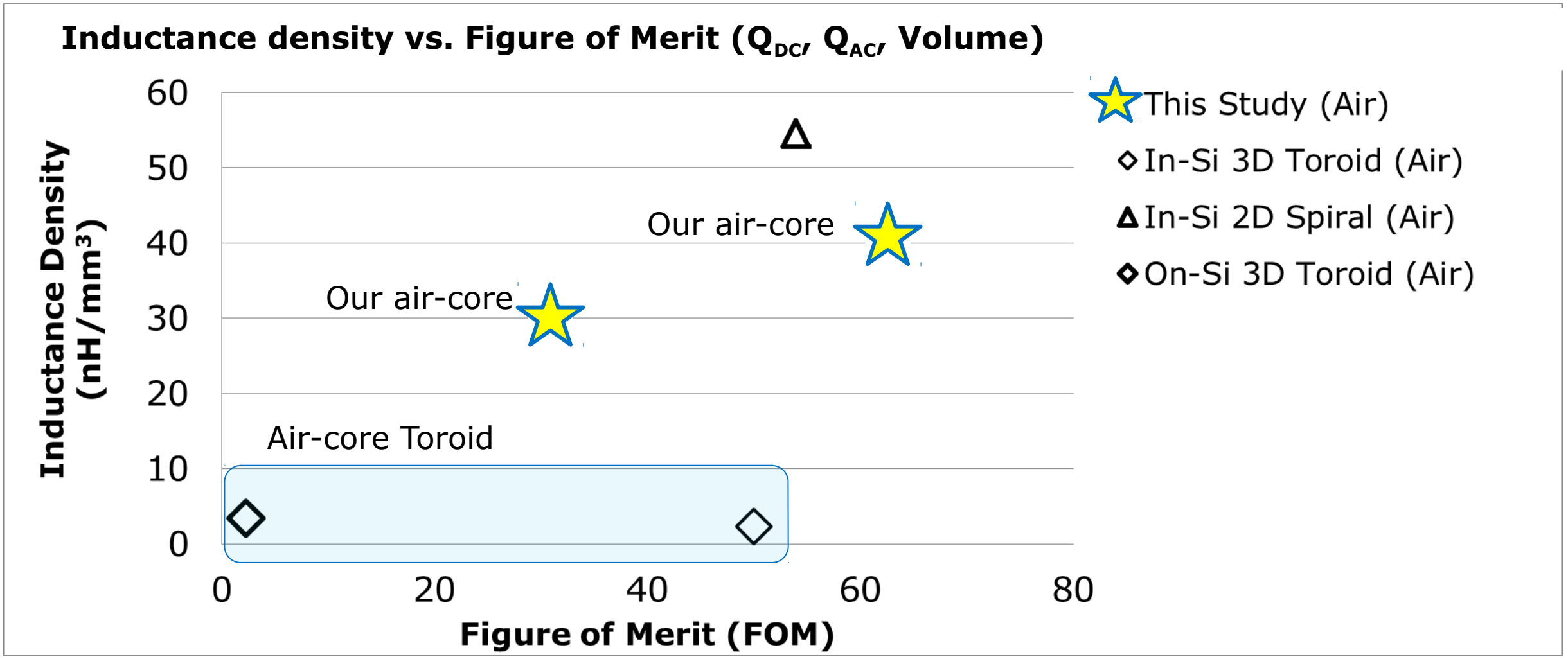


Removing the Si-core

- 3x less capacitance
- No substrate eddy-current loss

Highlights

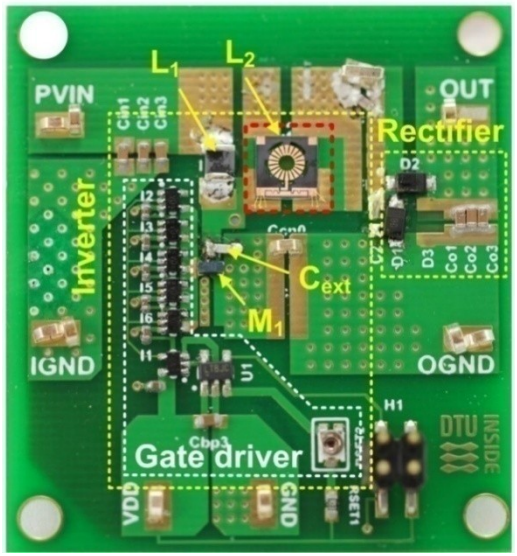
- Same inductance
- 40% higher Q
- 130% higher frequency



$$\mathrm{FOM} = \frac{\sqrt{Q_{DC} \cdot Q_{AC}}}{\mathrm{Volume}} = \frac{\sqrt{L_{DC}/R_{DC} \cdot Q_{AC}}}{\mathrm{Volume}}$$

Demonstrator 1 with Air-core Inductor

33 MHz ZVS Boost converter

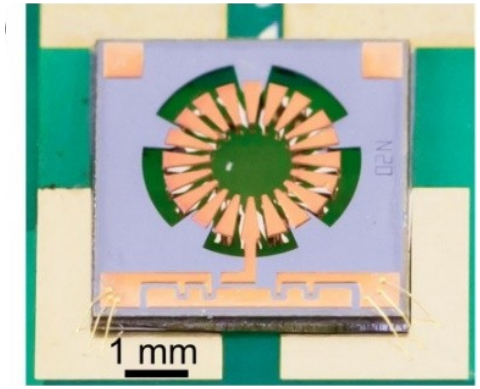


Inductor

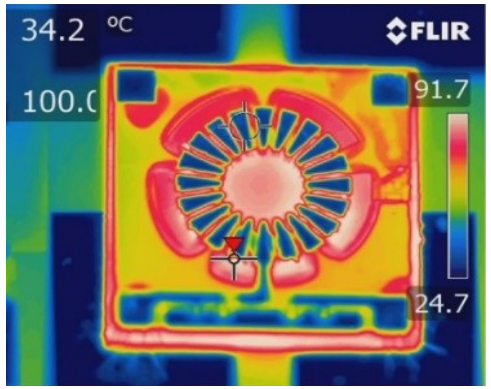
- carry 1 A of RMS current
- 0.98 W loss in inductor (winding loss)

Converter: 77% efficiency, 10 W output

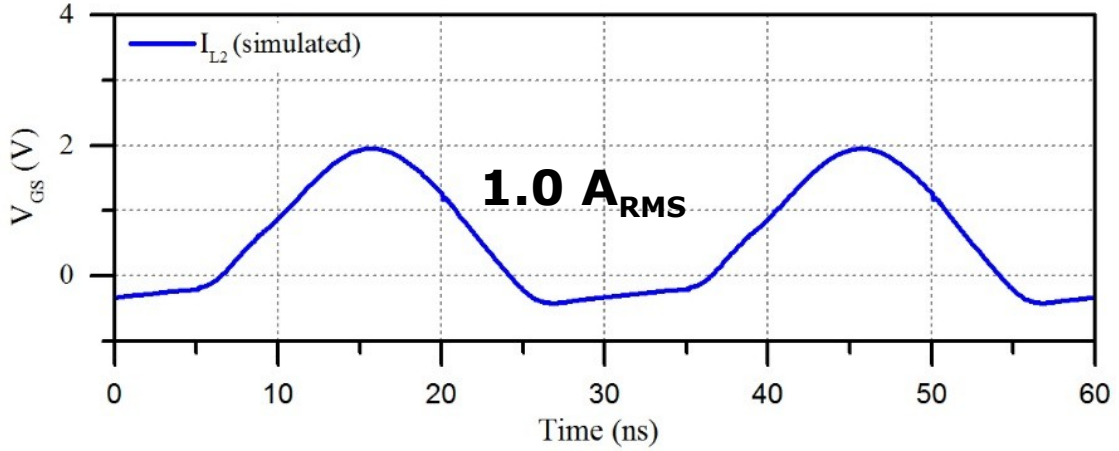
Air-core inductor



Thermal image



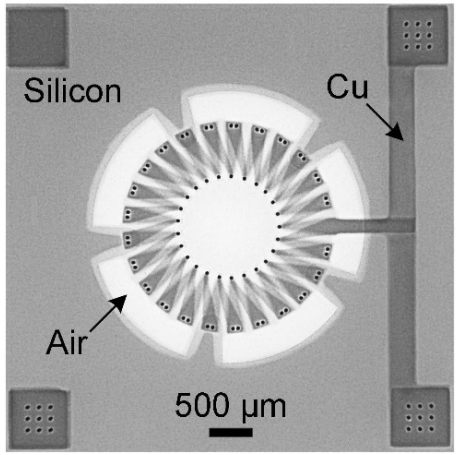
Simulated current waveform

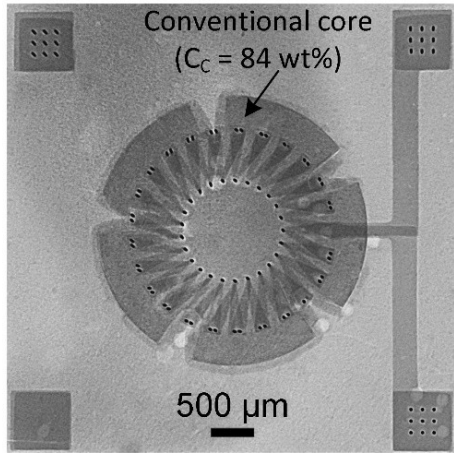


Hoa Thanh le et al. 2018, IEEE IESTPE

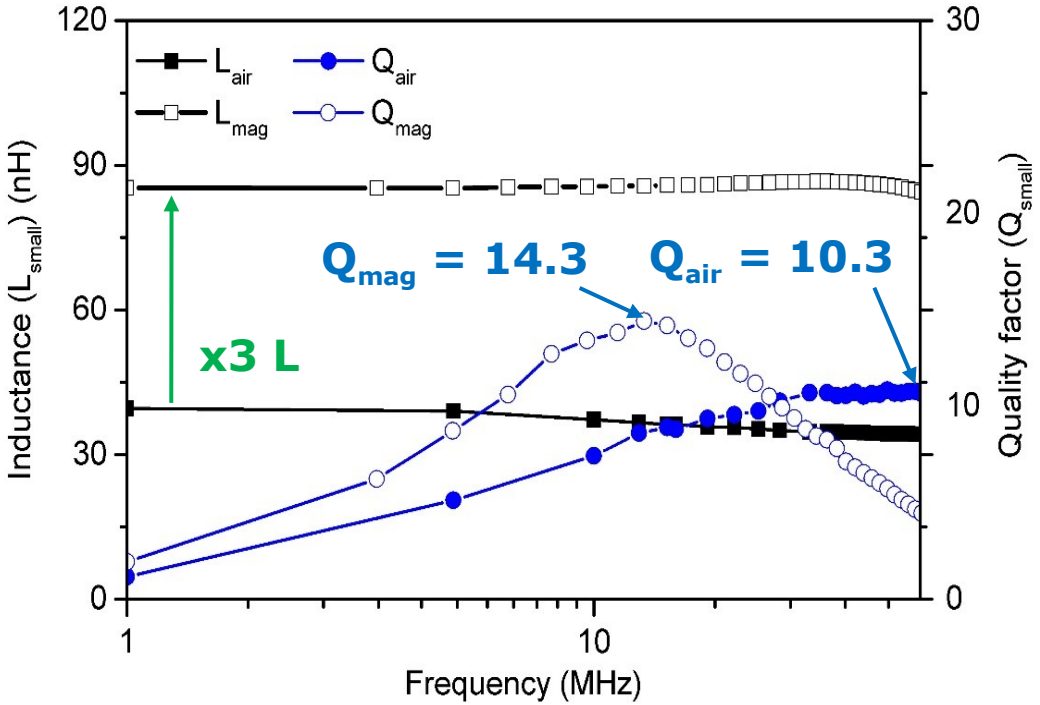
TSV Magnetic-core Inductors

Fabrication



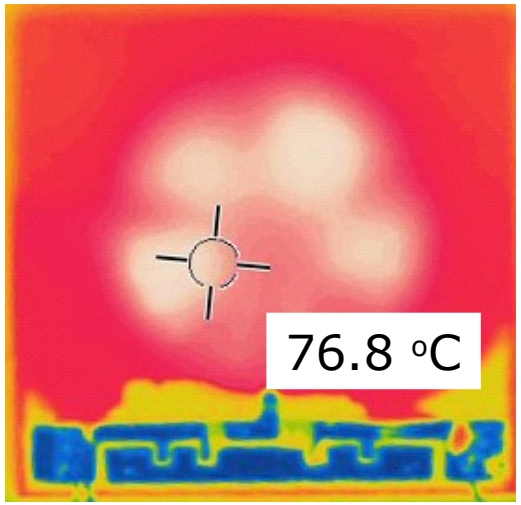


Modeling and Characterization



L and Q vs. Frequency

Converter testing



η = 76%, P_{out} = 2.5 W

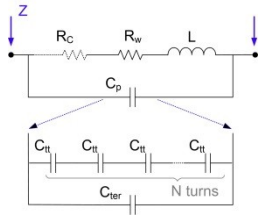
Inductor

- 0.5 A_{DC} + 0.86 A RMS
- 0.63 W loss

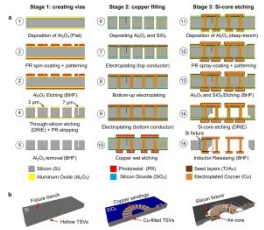
Hoa Thanh le et al. 2018, IEEE TPEL

Technology Development

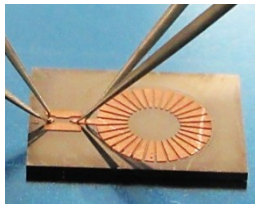
2.1 Inductor Design



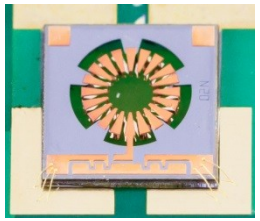
2.2 Fabrication Technology



2.3 Inductor Characterization



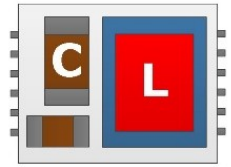
2.4 Converter Demonstration



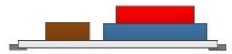
Power supply in package

PwrSiP

> 20 MHz



< 0.8 mm

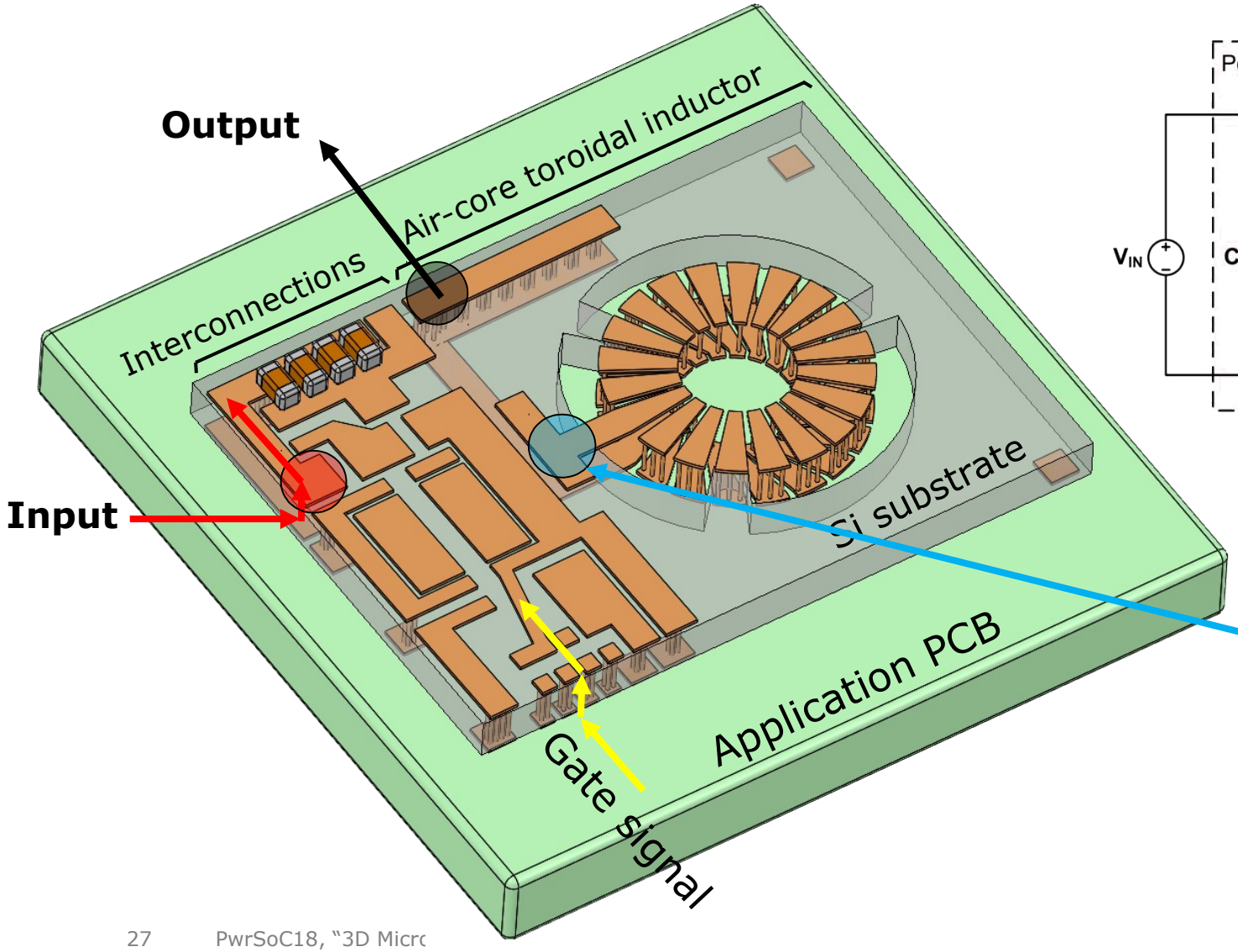


Stacked IC + L
Co-packaged C

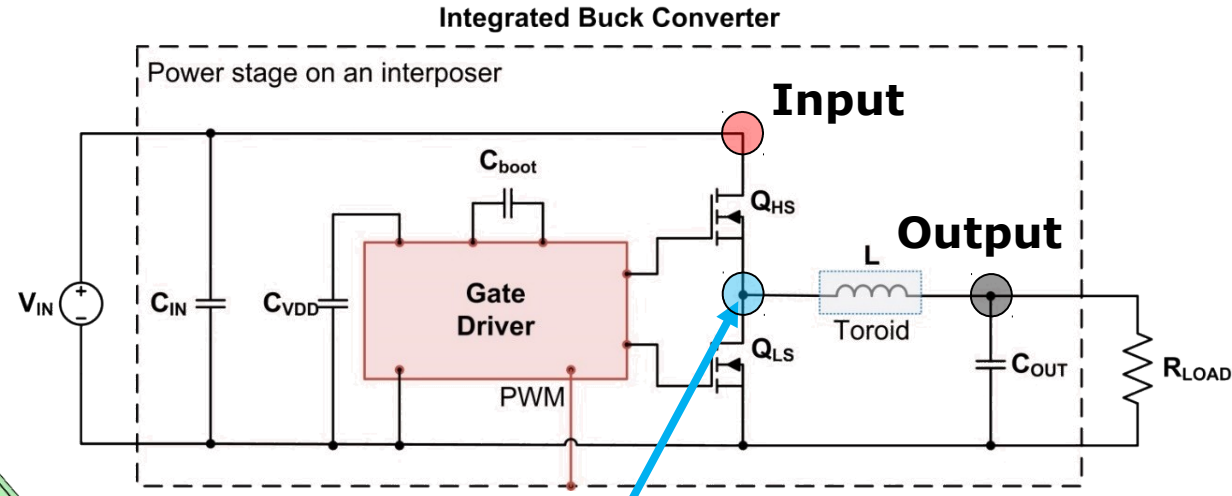
4. PSiP using 3D Passive Interposer

4.2 DC-DC PSiP Buck Idea

A DC-DC buck PSiP on application PCB



Schematic of a DC-DC buck PSiP

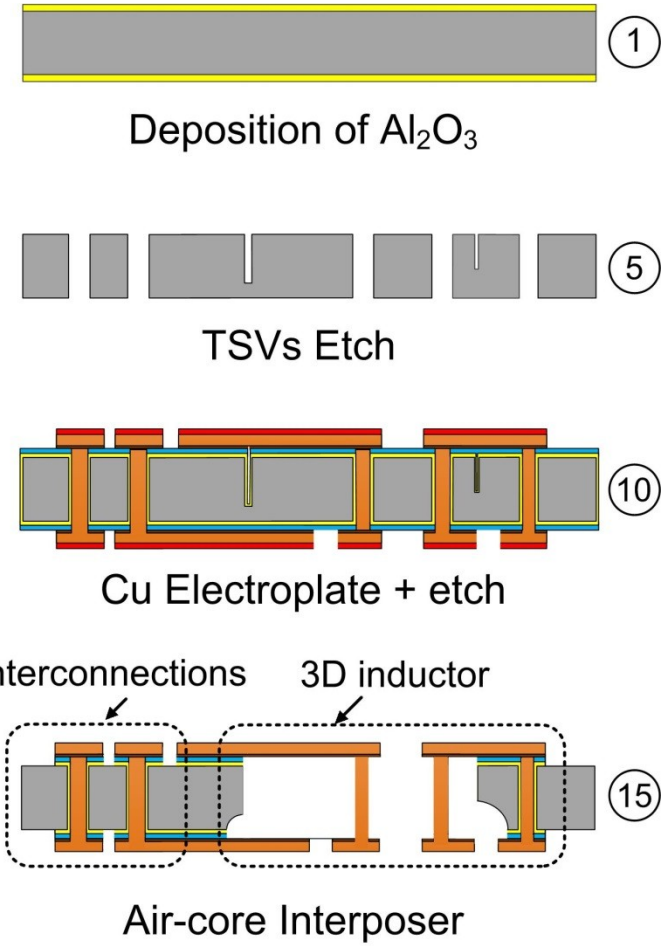


Switching node

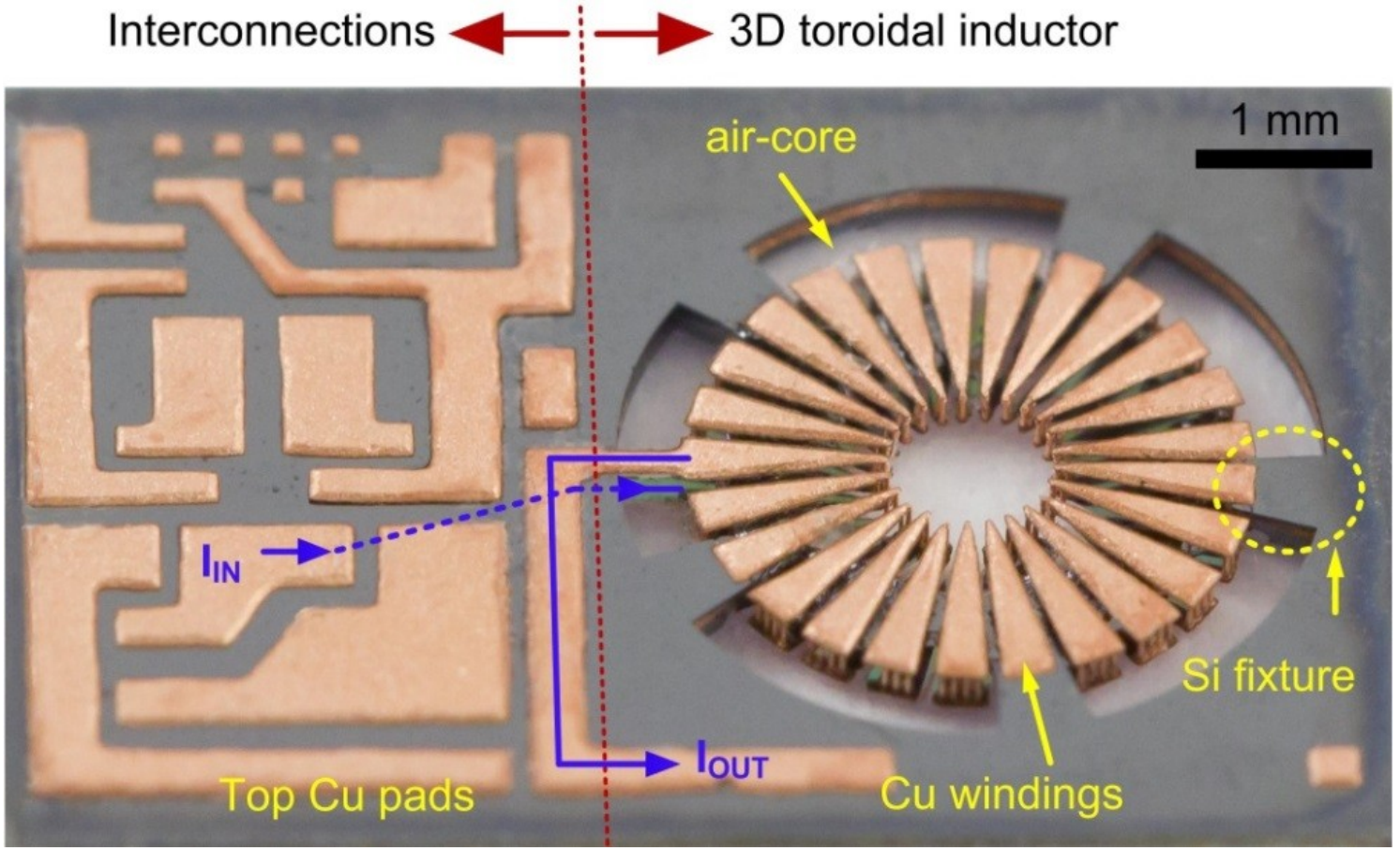
World's first PSiP using 3D passive interposer (2.2018)

4.2 PSiP Fabrication

Fabrication process flow

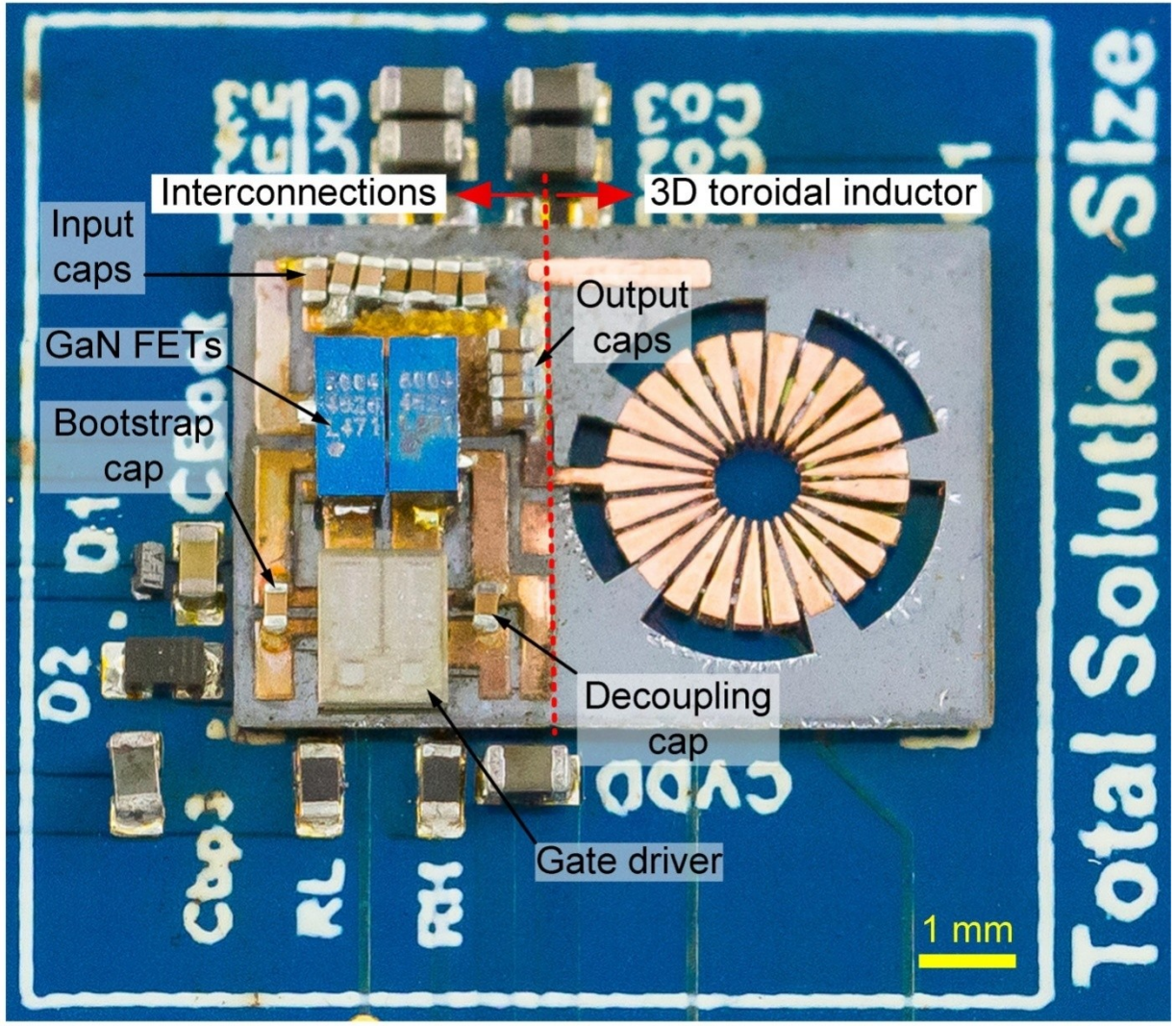


Fabricated 3D passive interposer



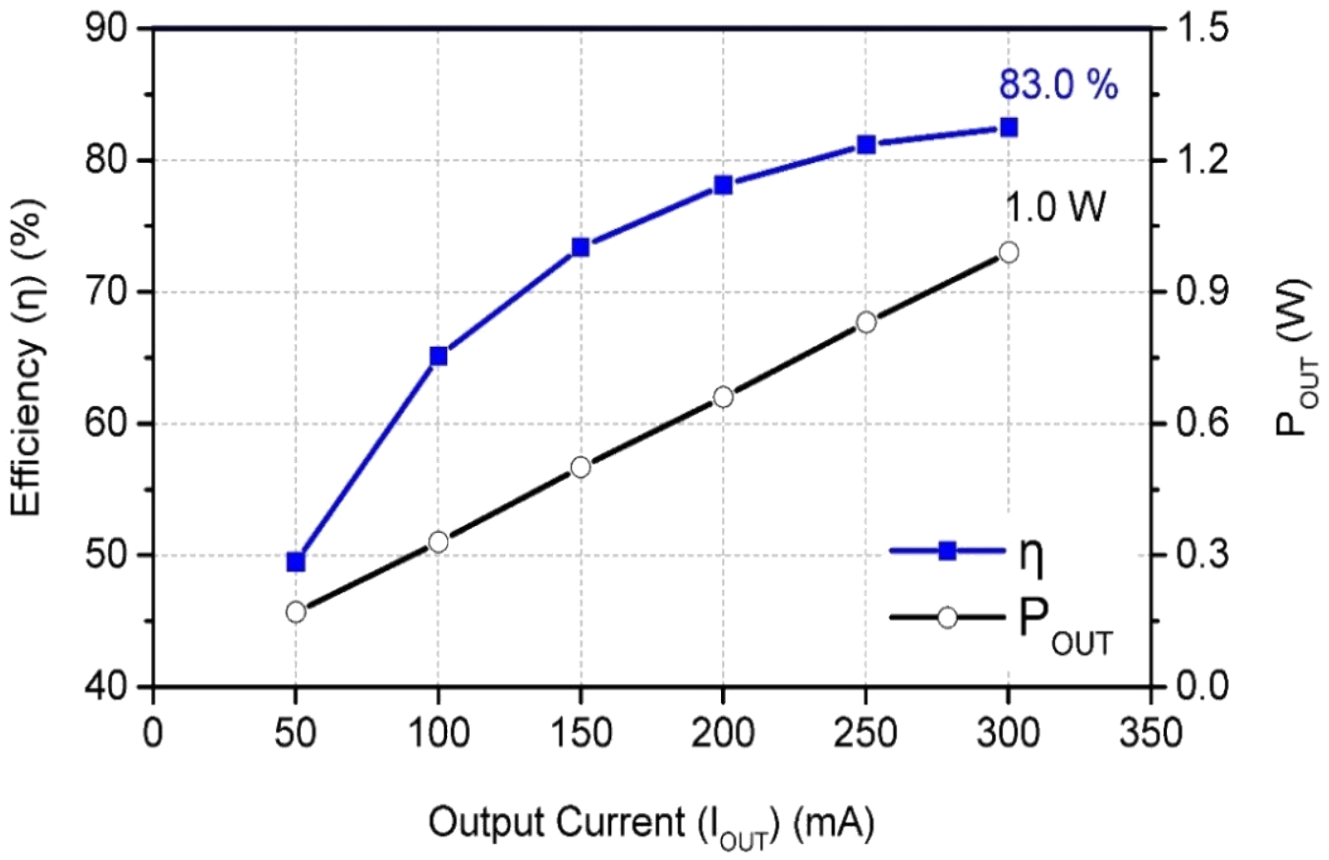
4.2 PSiP Assembly

Assembled PSiP with 2 GaN FETs, gate driver, 13 capacitors

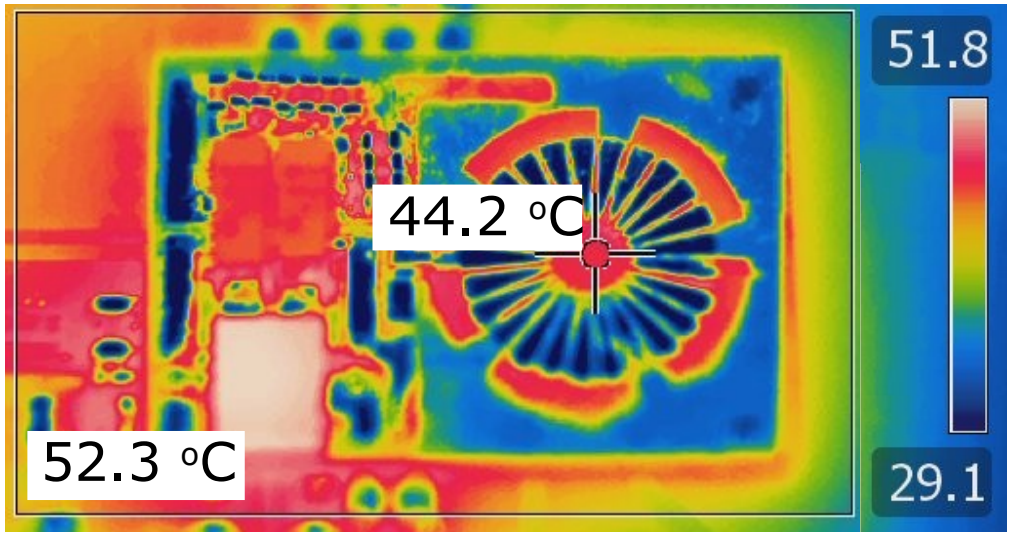


4.3 PSiP Testing

Efficiency and Output power vs. Output current

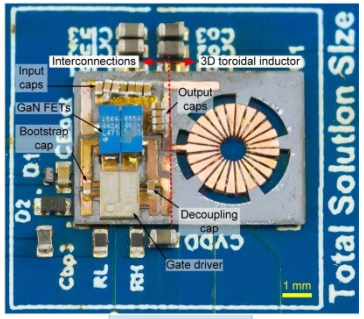


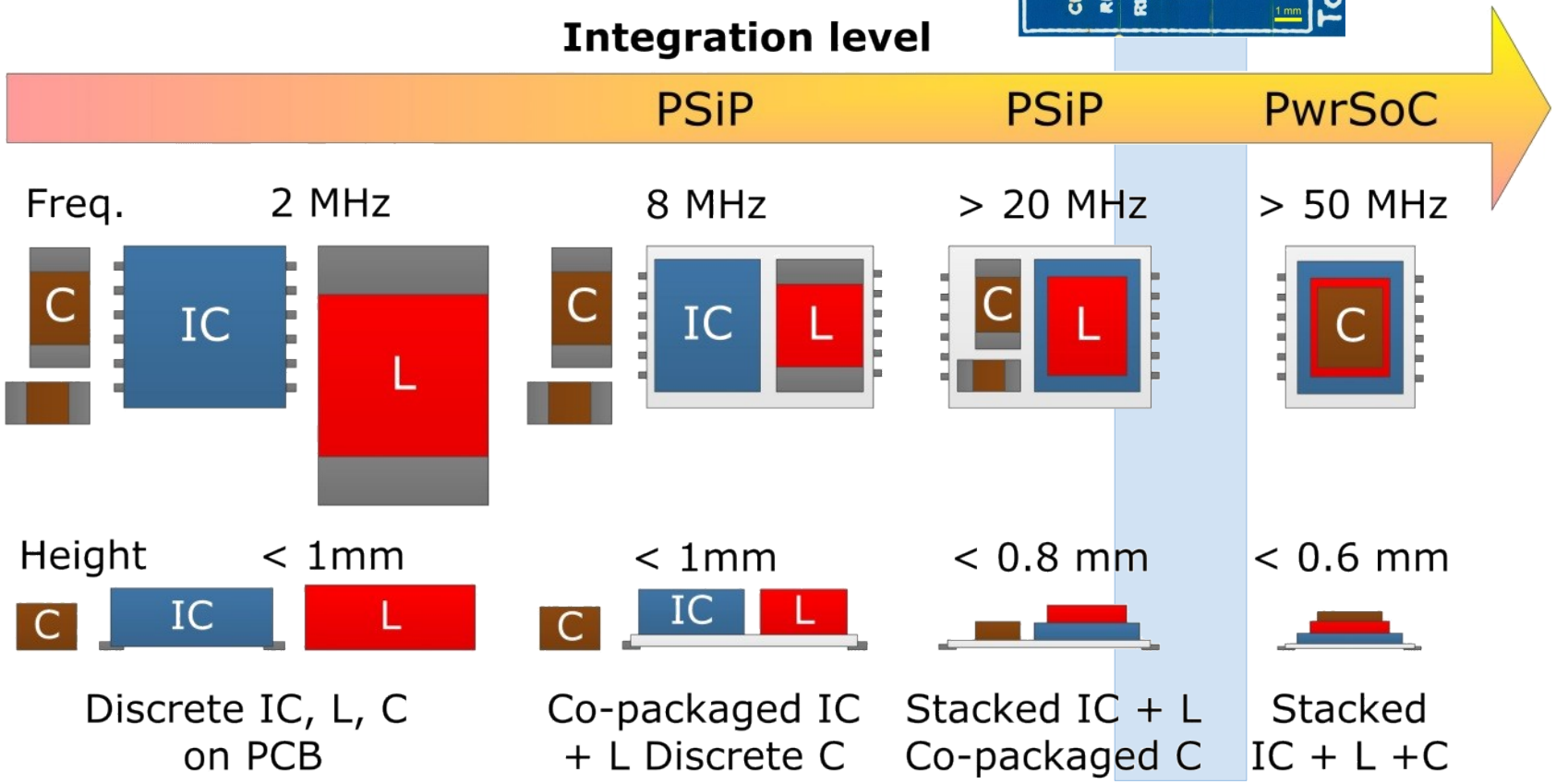
Thermal image of the inductor in PSiP at I_{OUT} = 0.3 A



4.4 PSiP Evaluation

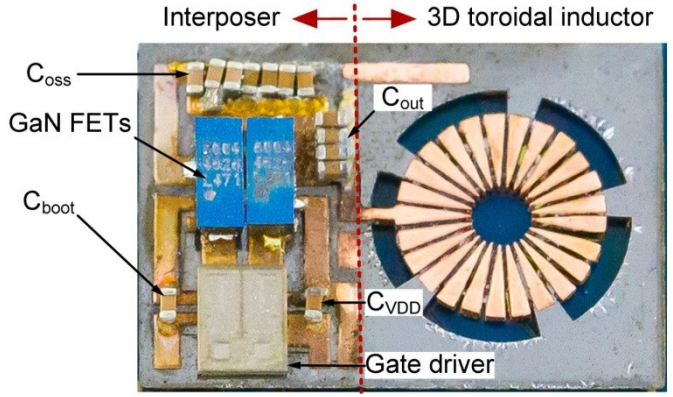
This study



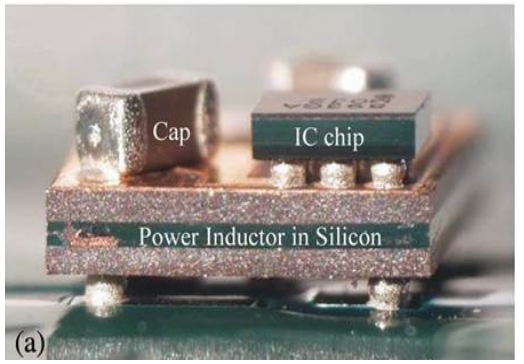


4.4 PSiP Evaluation

Parameters	This Study	Li et al. 2017
Size (cm)	0.4 x 0.8 x 0.**1**	0.3 x 0.3 x 0.18
V_{IN} (V)	3.5 – **8.5**	3.3
P_{OUT} (W)	1.15	1.0
P_D (W/cm³)	36	60
Efficiency (%)	83	83
f_{SW} (MHz)	22	6



This study

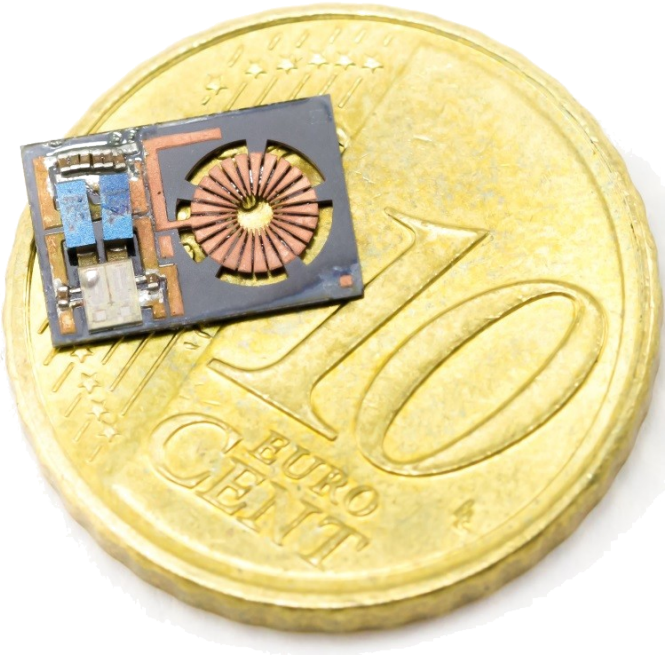


Li et al. 2017

5. Conclusion and Outlook

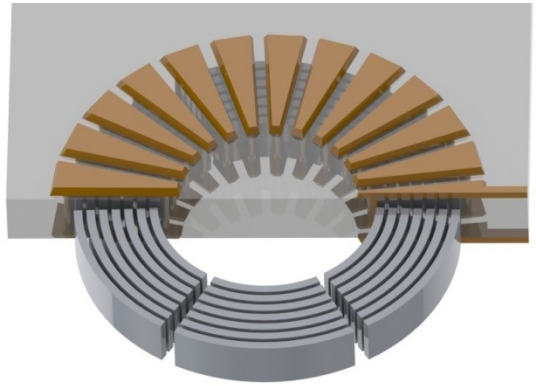
Conclusion

- 3D though-silicon vias (TSV) technology for inductor and packaging
- State-of-the-art inductor performance
- World's First PSiP using 3D Passive Interposer Low-profile, high-η

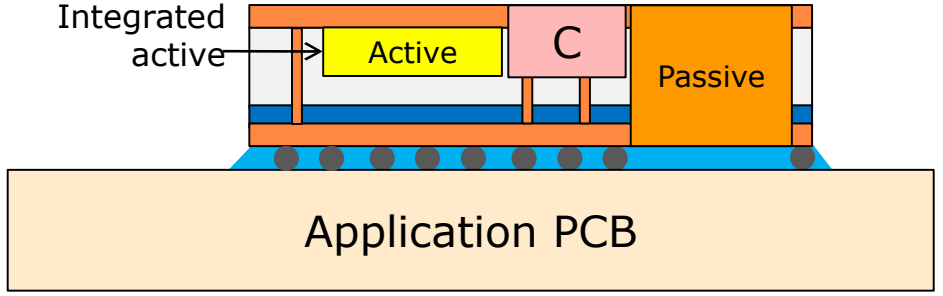


Future Development

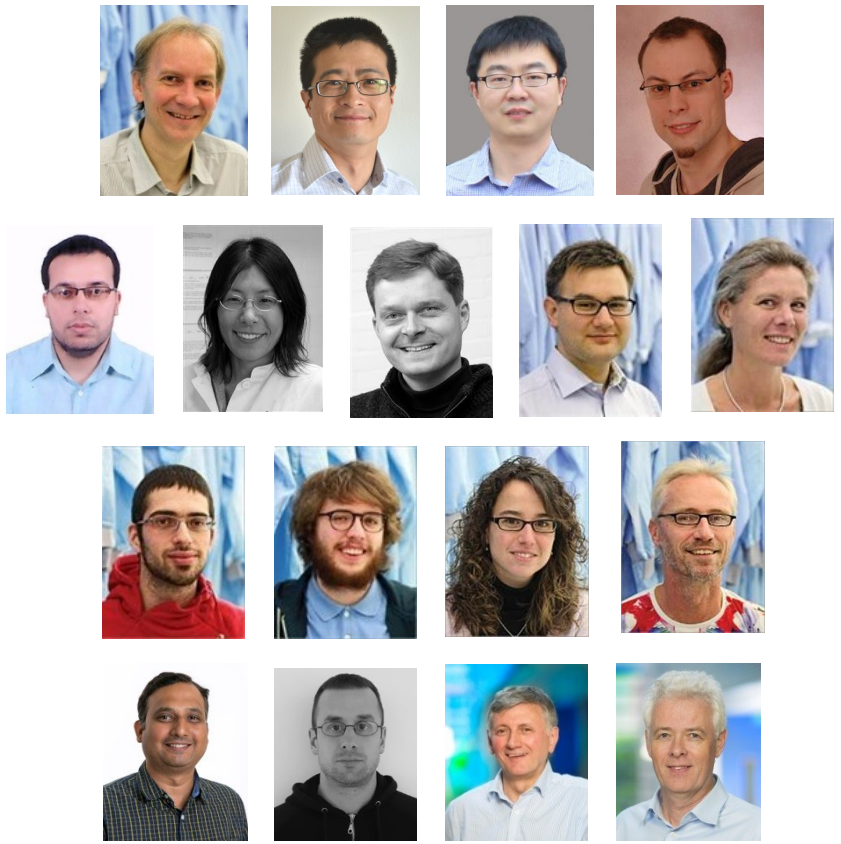
ALD laminated core



PwrSoC



5.4 Acknowledgement



DTU Danchip
National Center for Micro- and Nanofabrication

DTU Electrical Engineering
Department of Electrical Engineering

Tyndall National Institute
Institiúid Náisiúnta

IPU

noliac

Nordic Power Converters
Powering a brighter future™

SimpLight

niko

SERVODAN

Innovation Fund Denmark
RESEARCH, TECHNOLOGY & GROWTH