

# Integrated Gate Drive Transformers using laminated amorphous Co Zr Ta B magnetic core

Pranay Podder, Zoran Pavlovic, Joe O'Brien, Séamus O'Driscoll,  
Sean Cian Ó Mathúna, **Paul McCloskey**

Tyndall National Institute, University College Cork, Ireland.



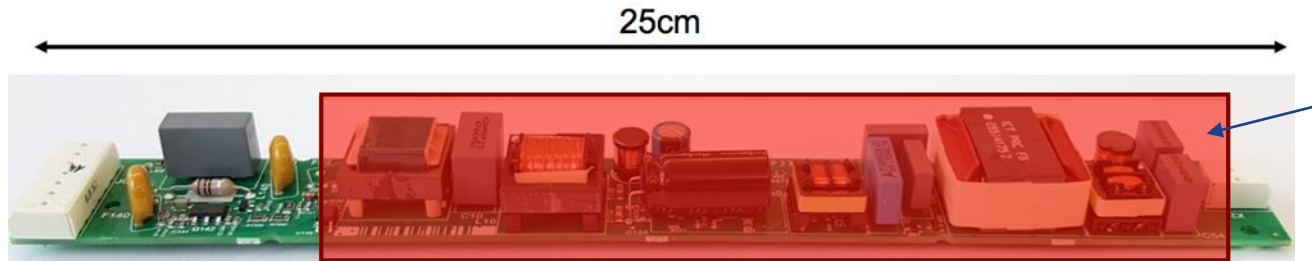
# Outline

- Background
- Construction of solenoid transformer
- Design
  - Specifications
  - Design parameters
  - Design space study using semi empirical equations
  - Finite Element modelling
- Fabrication of devices
- Electrical test
- Conclusions



# Background

## *Electrical Driver (Light Engine) for LED Lighting*



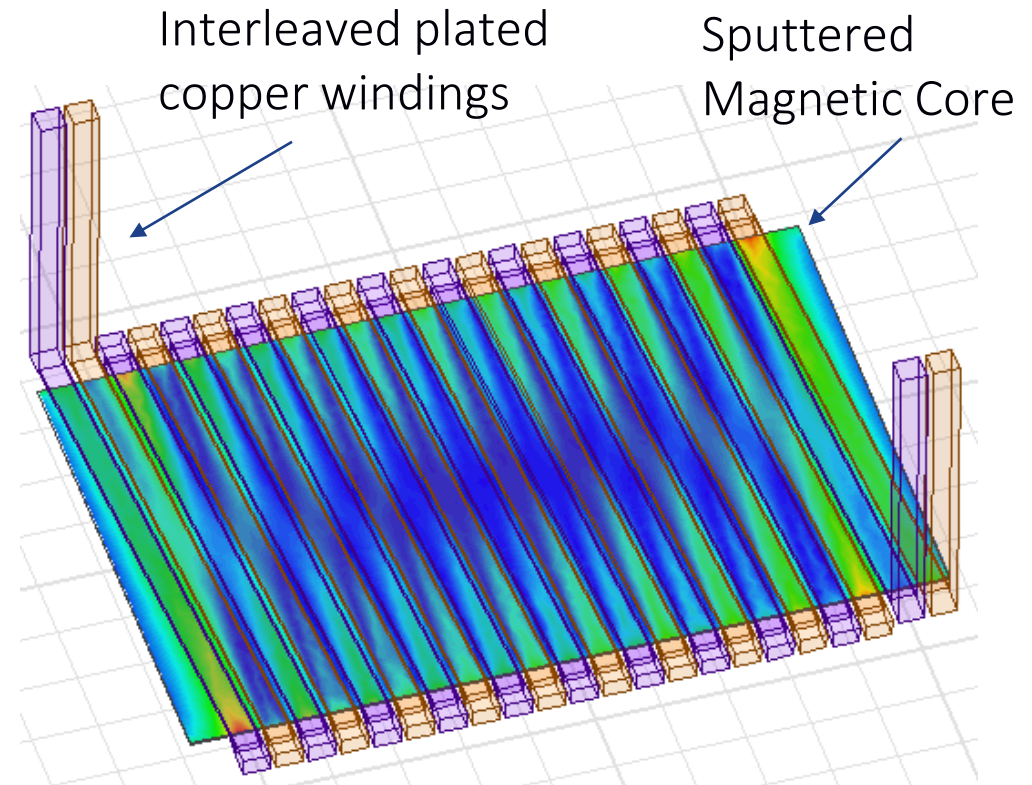
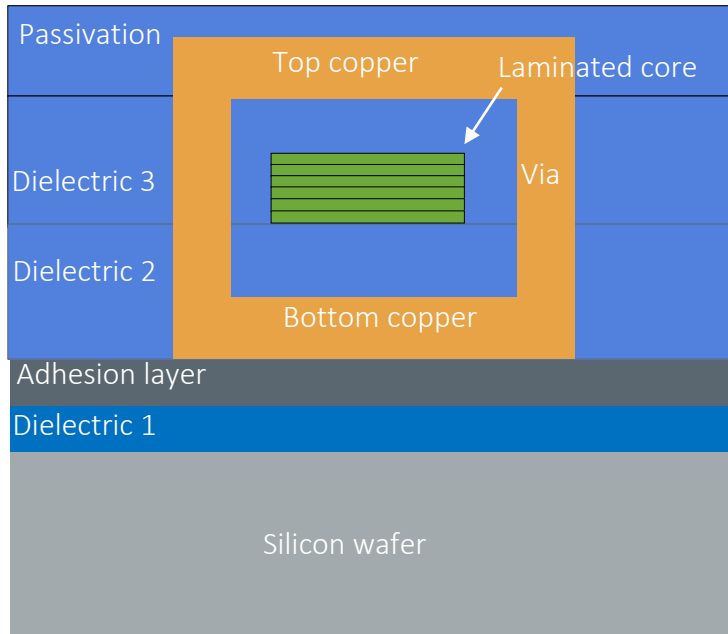
Passive  
components

75 W LED driver with a volume of 25 cm x 2 cm x 3 cm (150 cm<sup>3</sup>)

- Electrical driver
  - The **biggest bottleneck** for size, weight and cost reduction as well as reliability and energy efficiency improvement. **LEDLUM, “Tiny Light Engine for Large Scale LED Lighting”**, aims to address this challenge (funded under European Union’s Horizon 2020 programme)
- Strategy for improvement
  - High frequency power electronics
    - Reduction in passive component size => size and weight reduction
    - Elimination of electrolytic capacitors => life time improvement
  - Embedded active and passive components



# Micro-Transformer Construction

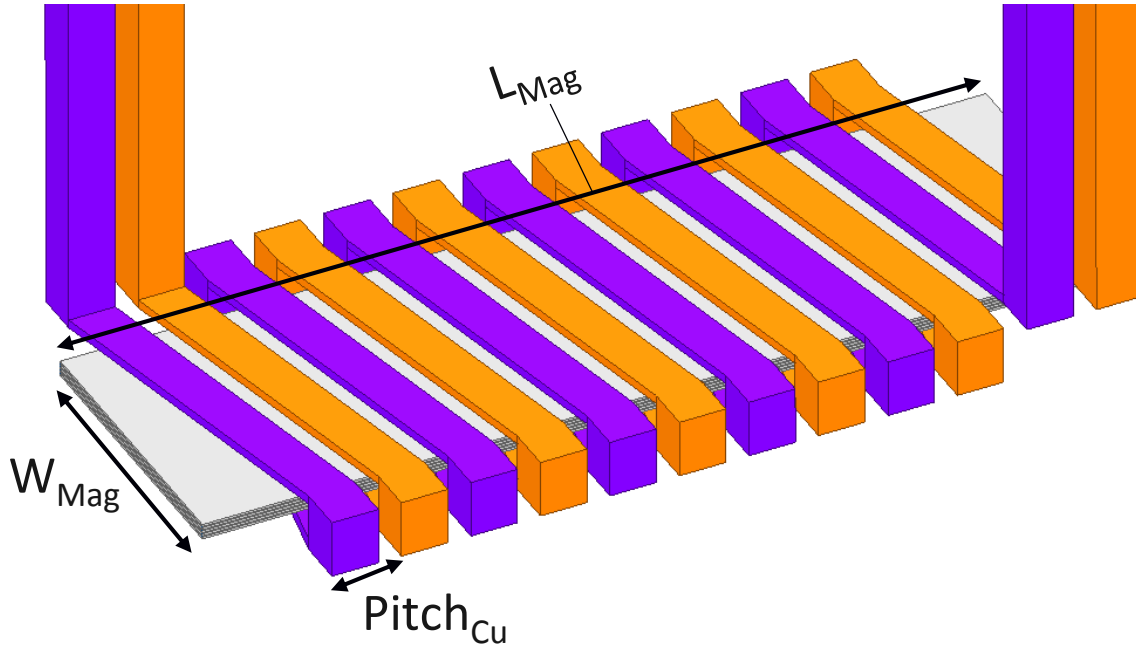


# Transformer specifications

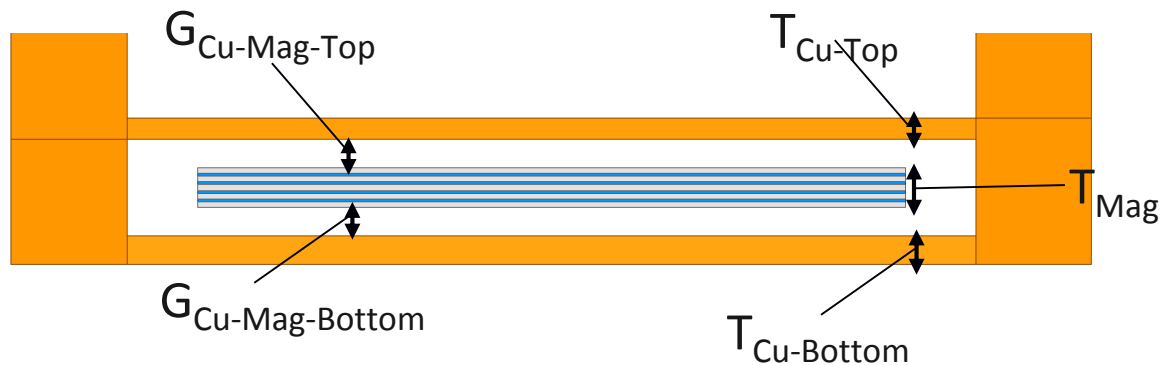
Integrated gate drive transformer

Parameter	Symbol	Value	Unit
Inductance per phase	L	300	nH
Peak to Peak current	$I_{pp}$	0.1	A
DC current	$I_{DC}$	0	A
Switching frequency	$f_{sw}$	15 - 20	MHz
Coupling factor		80% - 90%	

# Solenoid transformer design Parameters



Parameter	Symbol
Magnetic Core Length	$L_{Mag}$
Magnetic Core Width	$W_{Mag}$
Magnetic Core Thickness	$T_{Mag}$
Cu track pitch	$Pitch_{Cu}$
Cu track thickness	$T_{Cu}$
Vertical gap between Cu track and magnetic core	$G_{Cu-Mag}$



# Study of design space

- Study of design space is performed using modified analytical expressions of inductance and DCR.

$$L \approx \mu_0 \mu_{eff} N^2 \left( \frac{W_{Mag} T_{Mag}}{L_{Mag}} \right) \quad \text{Where, } \mu_{eff} = \frac{\mu_r}{1 + F_{Demag}(\mu_r - 1)} = \text{Effective permeability}$$

$$R_{DC} \approx 2N\rho_{Cu} \left[ \frac{L_{Cu}}{W_{Cu}T_{Cu}} + \frac{(T_{Cu} + H_{Via})}{W_{Via}^2} \right]$$

$\rho_{Cu}$  = Resistivity of Cu

$N$  = Number of turns

$F_{demag}$  = Demagnetization factor

- The parameters listed in the CONSTANT, INPUT VARIABLES and OUTPUT VARIABLES tables define the design space.

## INPUT VARIABLES

Parameters	Range
$I_{sat}$ [A]	0.5 – 0.7
$N_{turn}$	1 – 30
$W_{Cu}$ [ $\mu\text{m}$ ]	80 – 200
$W_{mag}$ [mm]	0.2 – 3.0

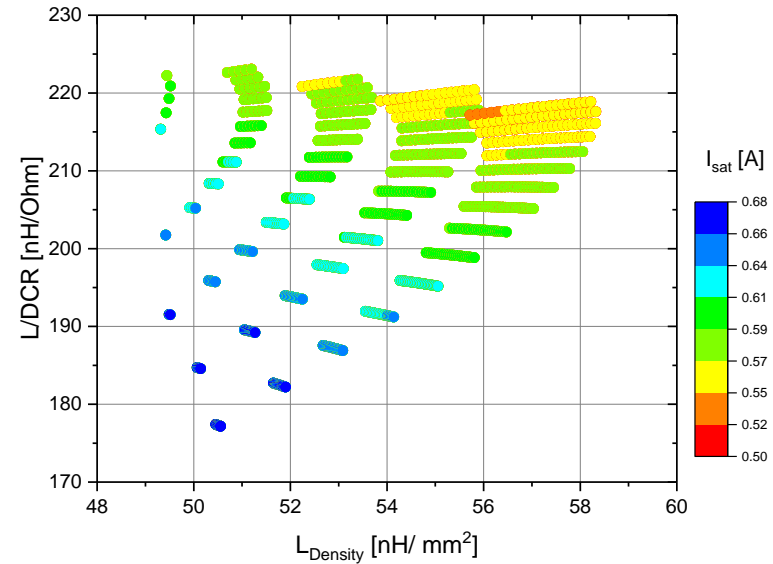
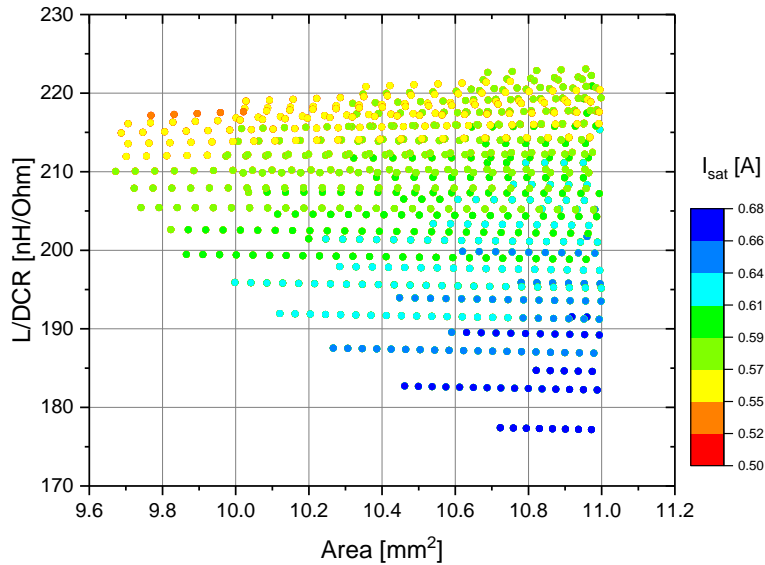
## OUTPUT VARIABLES

Parameters	Value $\pm$ tolerance
$L_{self}$ [nH]	300 $\pm$ 10%
Area [mm <sup>2</sup> ]	10 $\pm$ 20%
DCR [Ohm]	3 $\pm$ 50%
L/A [nH/mm <sup>2</sup> ]	50 $\pm$ 20%
$B_{max}$ [T]	< 1.1

## CONSTANTS

Parameters	Value
Frequency [MHz]	15 – 20
$\mu_r$	350
$\tan(\delta)$	0.1
$T_{mag}$ [ $\mu\text{m}$ ]	4.7
$T_{Cu}$ [ $\mu\text{m}$ ]	15
Pitch <sub>Cu</sub> [ $\mu\text{m}$ ]	100
$B_{sat}$ [T]	1.2

# Design space study

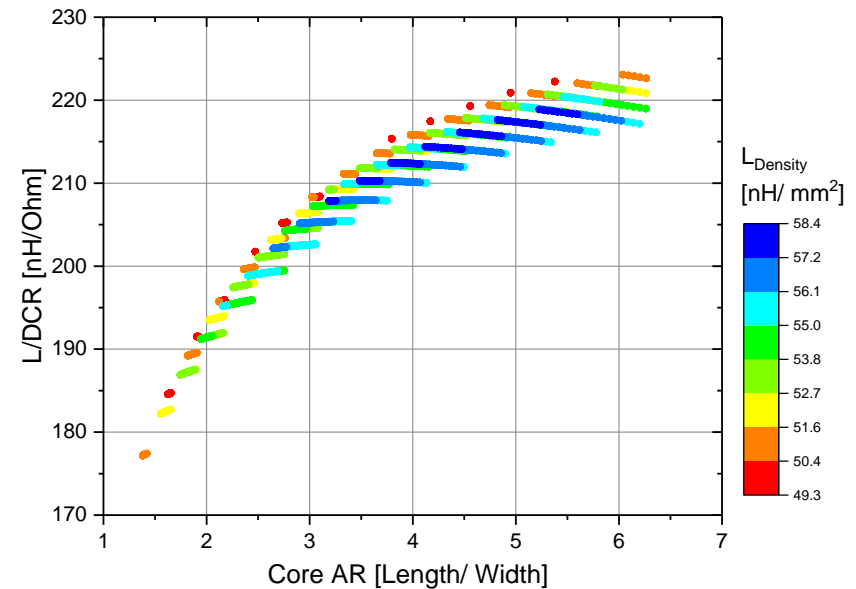
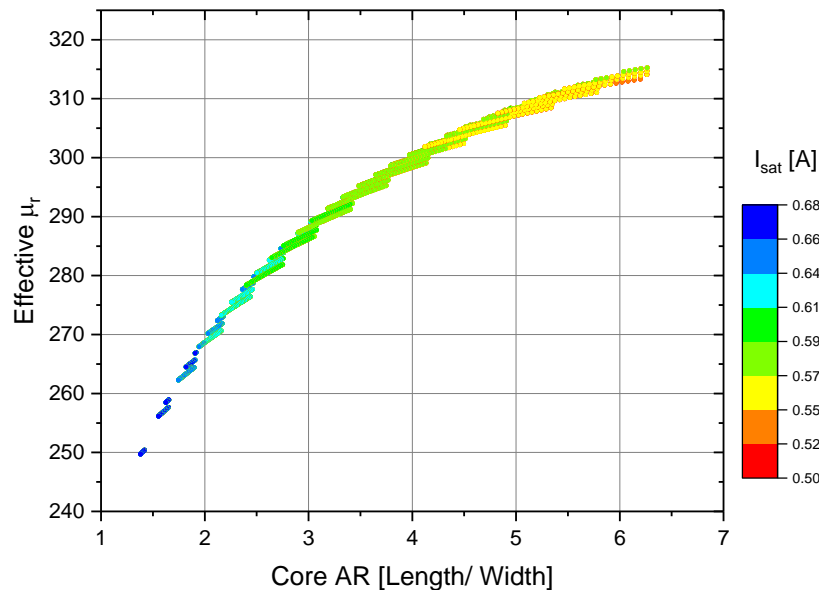


- Within a specified area, higher  $I_{sat}$  requirement leads to lower L/DCR.

- Higher  $I_{sat}$  requirement leads to lower L/DCR, as well as lower inductance density.



# Design space study

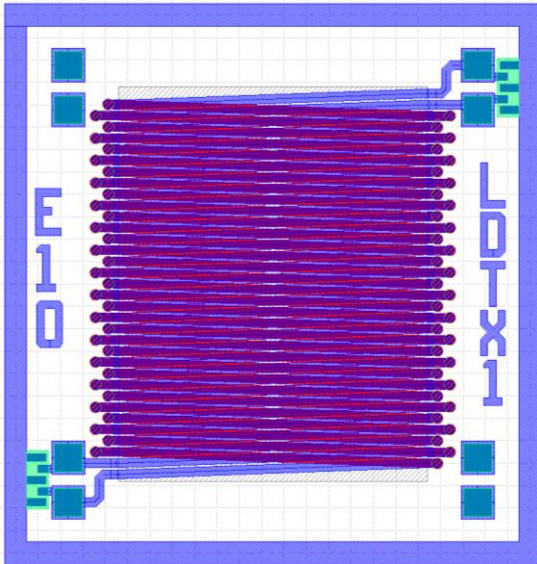


- Higher  $I_{sat}$  requirement leads to lower aspect ratio and lower effective permeability of the magnetic core.

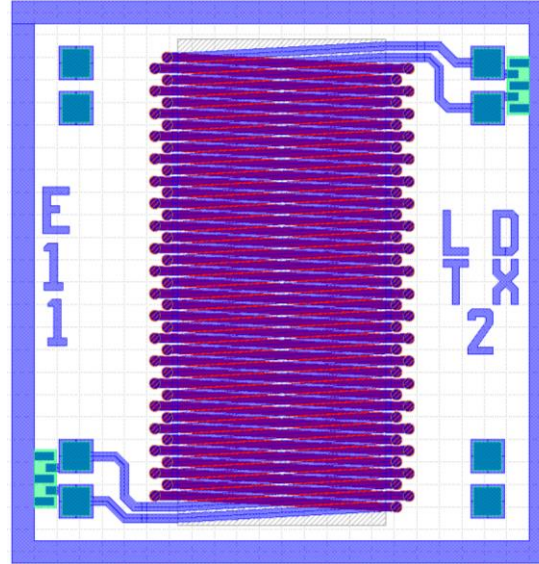
- Higher inductance density and L/DCR can be achieved by using a higher core aspect ratio.

# Transformer designs

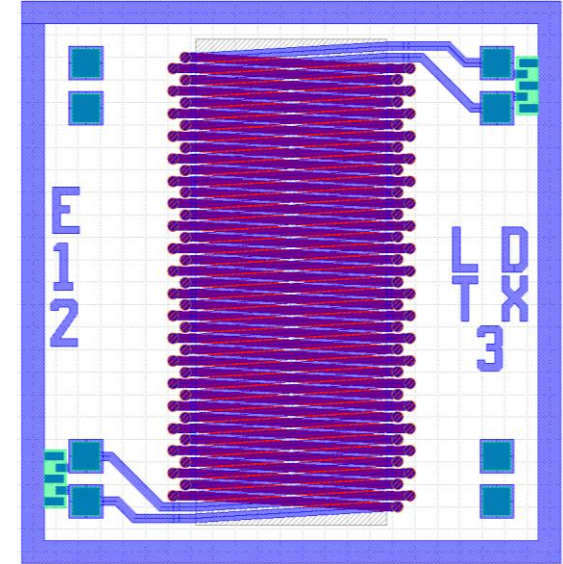
Design #1



Design #2



Design #3



Design #	Core Length	Core Width	Core Aspect Ratio ( $L_{Mag}/W_{Mag}$ )	Number of turns per winding
1	3520 $\mu\text{m}$	2760 $\mu\text{m}$	1.2	16.5
2	4325 $\mu\text{m}$	1850 $\mu\text{m}$	2.3	20.5
3	4325 $\mu\text{m}$	1700 $\mu\text{m}$	2.6	20.5

Top Copper

Bottom Copper

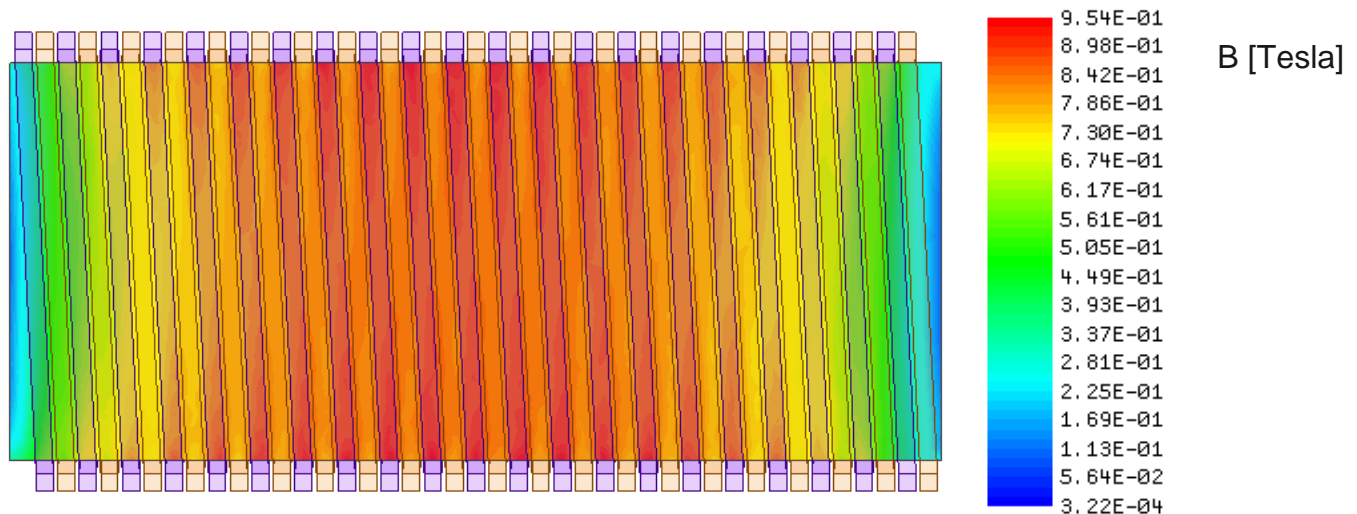
Passivation window

# Finite Element Simulation results for transformer designs

Parameters	Unit	Design #1	Design #2	Design #3
Core Aspect Ratio ( $L_{Mag}/W_{Mag}$ )	-	1.2	2.3	2.6
Inductance per phase @ $f_{SW}$	nH	350.2	303.2	281.4
DC Resistance per phase	Ohm	2.96	2.53	2.34
Equivalent Series Resistance (ESR) @ $f_{SW}$	Ohm	5.6	5.1	4.8
Coupling factor	%	86.2	90.1	90.2
$B_{Max}$ @ $I_{PP} = 0.1$ A	Tesla	0.22	0.25	0.28

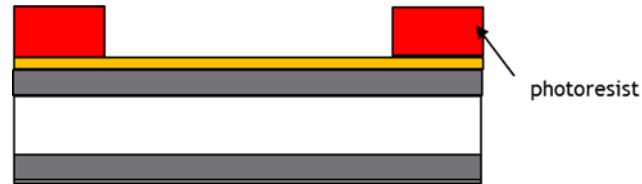
Current applied  
in one winding.

$$I_1 = 0.5 \text{ A}$$

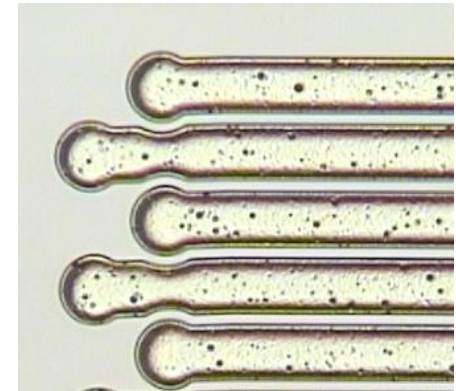
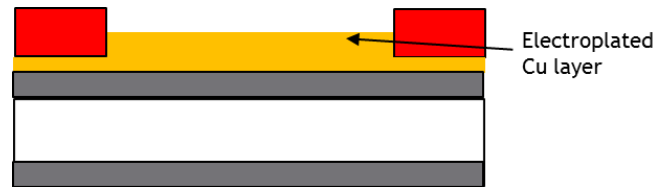


# Fabrication process

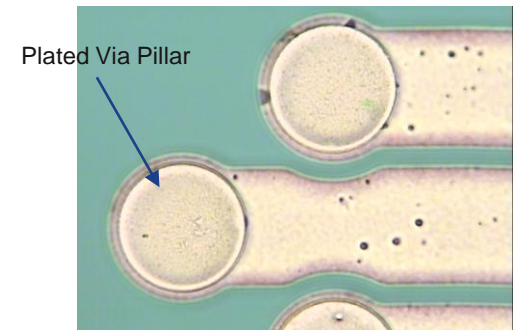
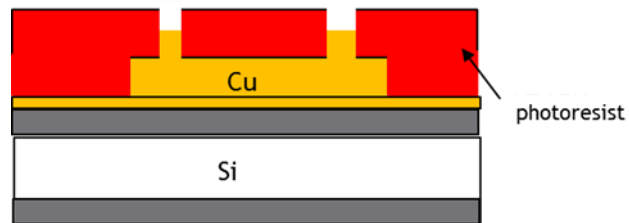
Spin-coating of photoresist and lithography for bottom Cu layer



Electroplate bottom coil layer.

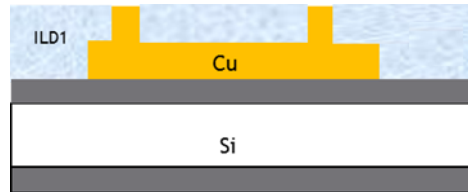


Via1 patterned and electroplated.

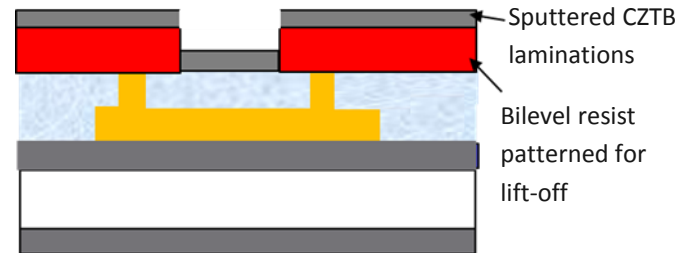


# Fabrication process

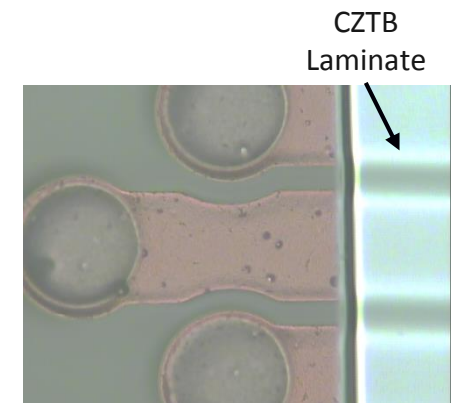
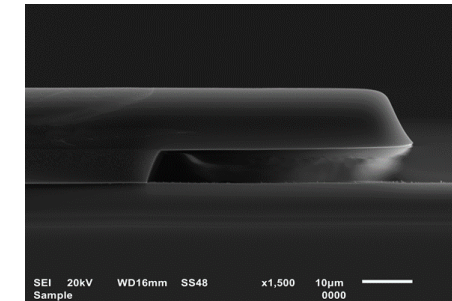
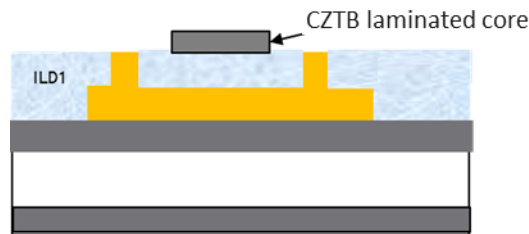
Strip photoresist, etch seed layer, and spin-on inter-layer dielectric (ILD)



CZTB core patterning by lift-off, and sputter deposition of CZTB laminated core.

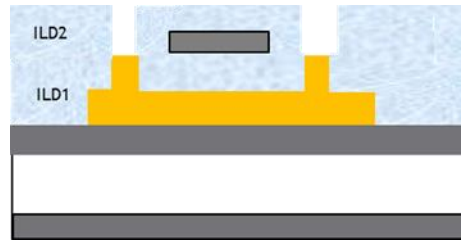


CZTB laminated core patterned by lift-off, photoresist stripped.

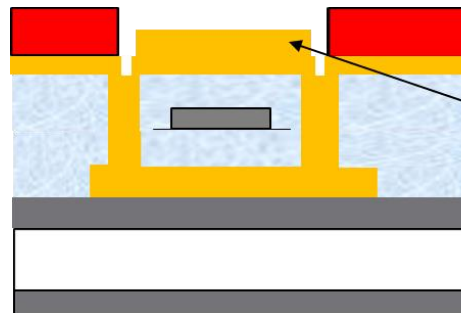


# Fabrication process

Spin-on inter-layer dielectric (ILD2) . Pattern to expose via tops.

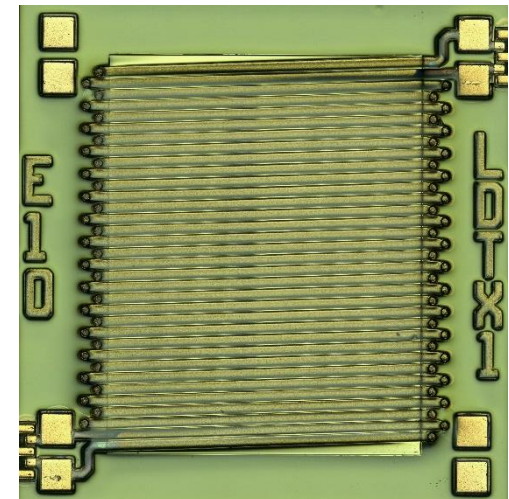
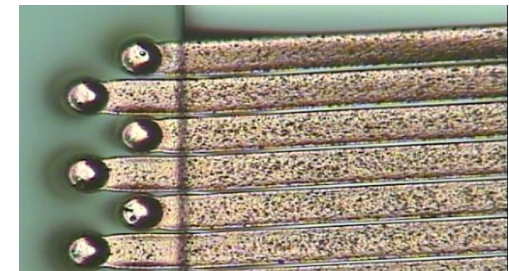
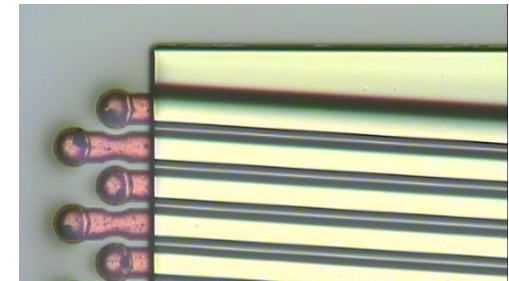
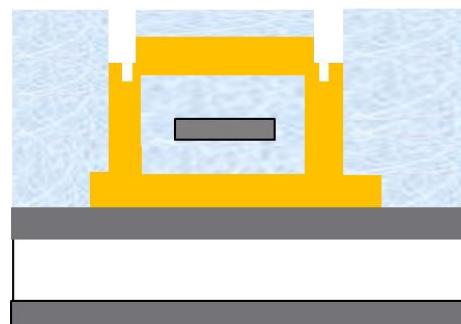


Sputter top Cu seed layer, pattern vias and top Cu tracks, electroplate vias and top Cu tracks.

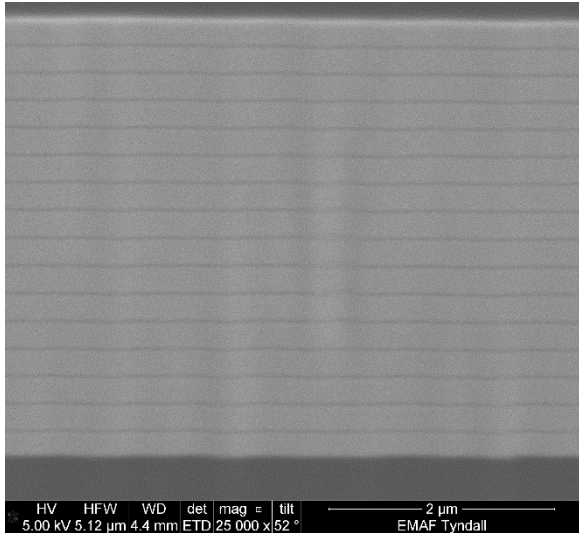


Electroplated top Cu tracks

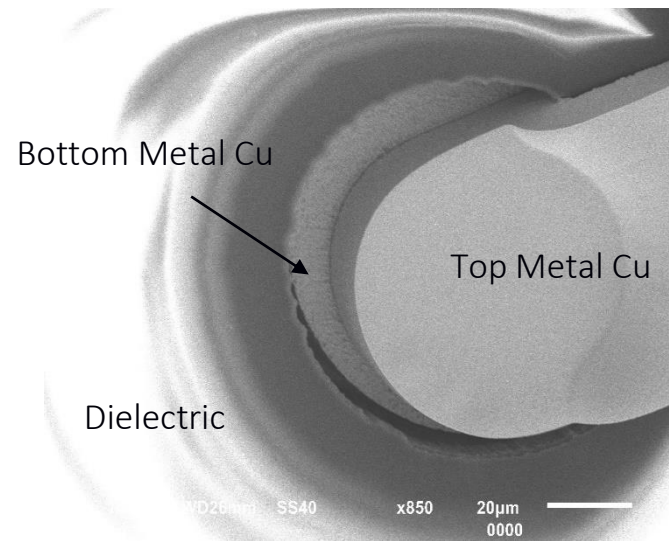
Strip resist, etch top Cu seed layer. Spin on passivation and open contact pads.



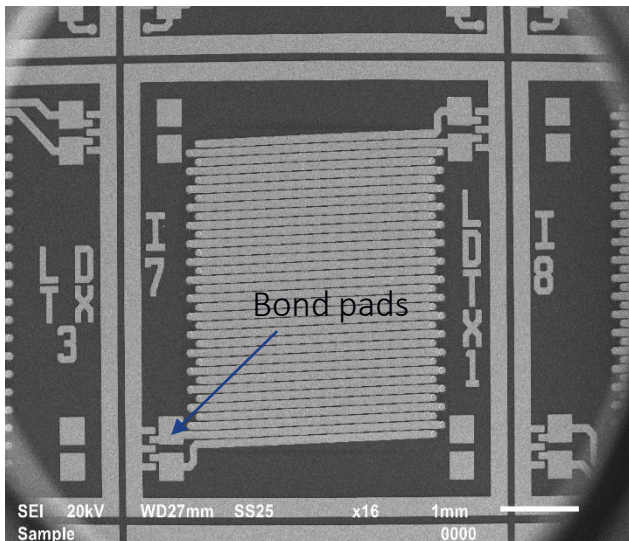
# Fabrication of devices



Laminated magnetic core



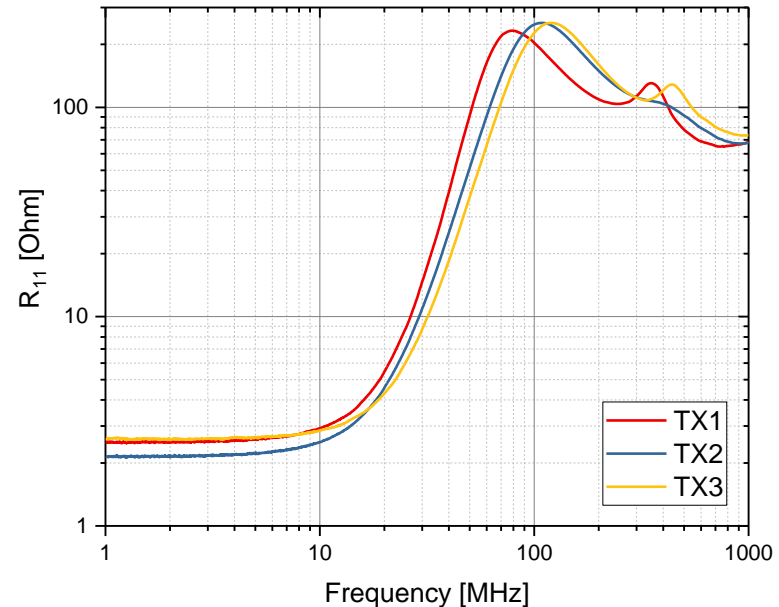
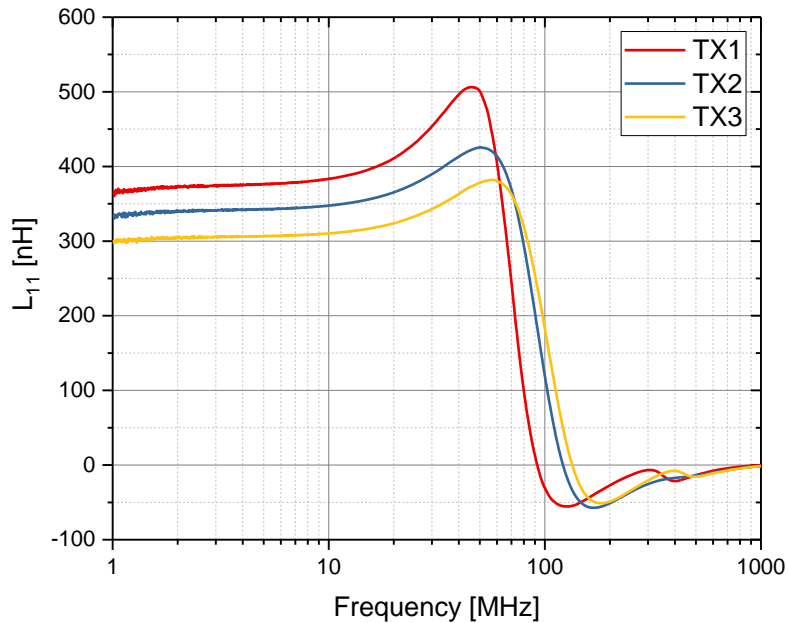
Top copper to bottom copper connection



Devices prior to final passivation



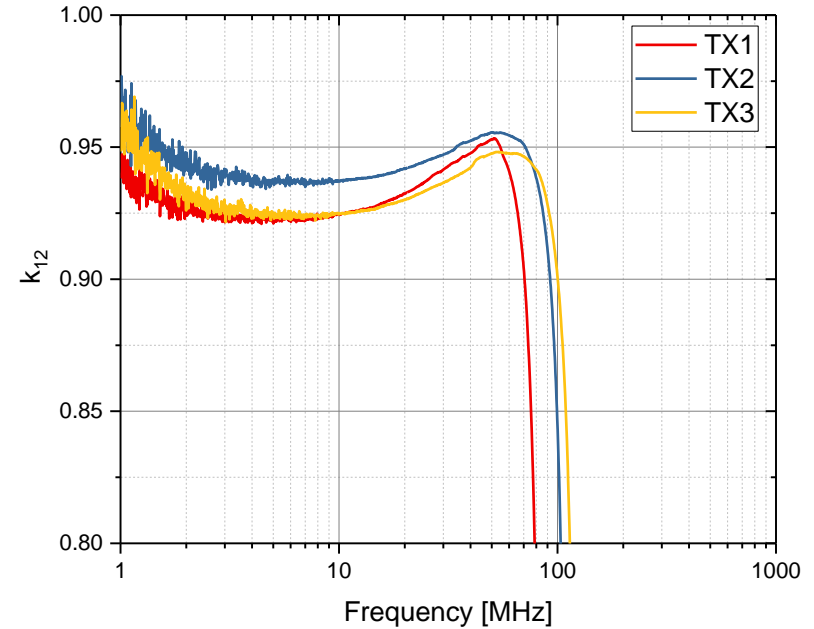
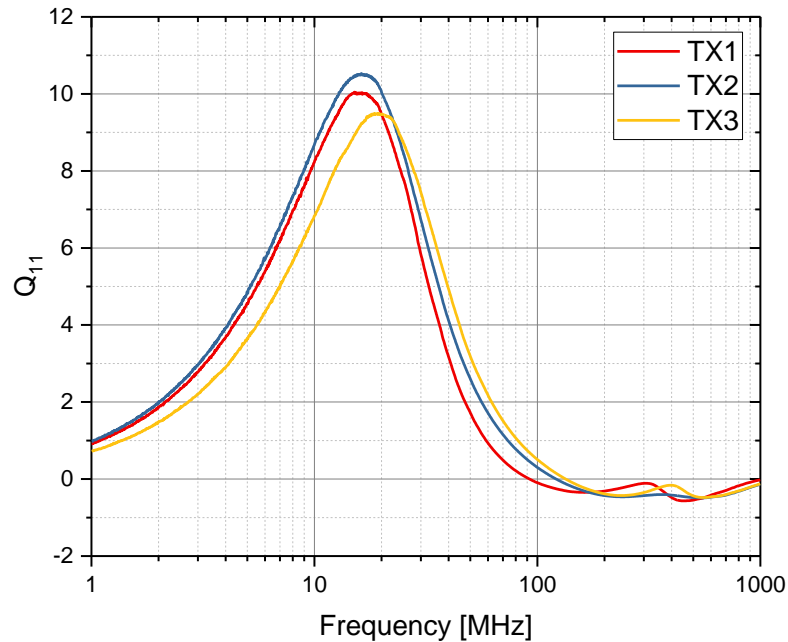
# Small signal S-parameter measurement



- Resonance due to parasitic capacitance occurring at >85 MHz
- TX1 has lowest aspect ratio and highest core width => highest  $L_{11}$
- TX1 has largest core volume and highest loss



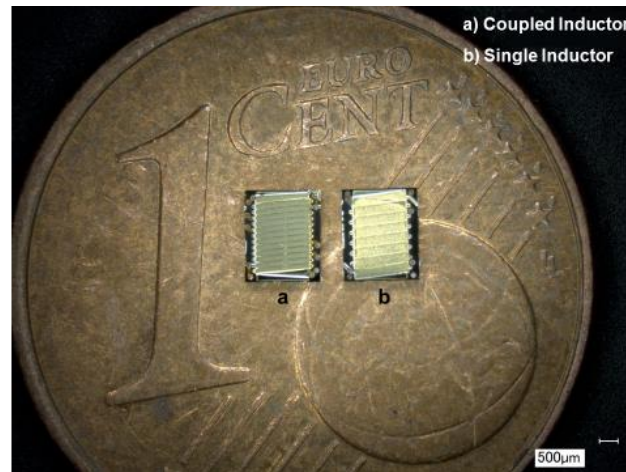
# Small signal S-parameter measurement



- Maximum Q occurring between 15 to 20 MHz
- Coupling factor  $> 0.925$

# Other application areas

- This fabrication process has also been used to magnetic devices for use in Point-of-Load (POL) converter applications
- Pranay Podder et al, “Electrical Characterisation of Thin Film CZTB Solenoid Inductors for PwrSiP” poster at PwrSoc 18
  - Targeting  $\sim 30$  MHz operation
  - Single and coupled inductors
  - Designed for high Q
  - Measured device Q  $\sim 24$  at  $\sim 30$  MHz.



# Conclusions

- Thin film laminated CZTB gate drive transformer fabricated and characterised
- Electrical properties suitable for application with frequencies 15-20 MHz
- BEOL compatible planar solenoid transformer with thickness  $< 60 \mu\text{m}$



# Acknowledgements

- Work carried out in LEDLUM, “Tiny Light Engine for Large Scale LED Lighting”
- This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 731466.





**Tyndall National Institute,**  
Lee Maltings,  
Dyke Parade,  
Cork,  
Ireland.  
T12 R5CP

t: +353 21 490 4177

e: [info@tyndall.ie](mailto:info@tyndall.ie)

[tyndall.ie](http://tyndall.ie)