

MEDIATEK

Signal and Power Integrity Analysis of INFO Interconnect for Networking Application

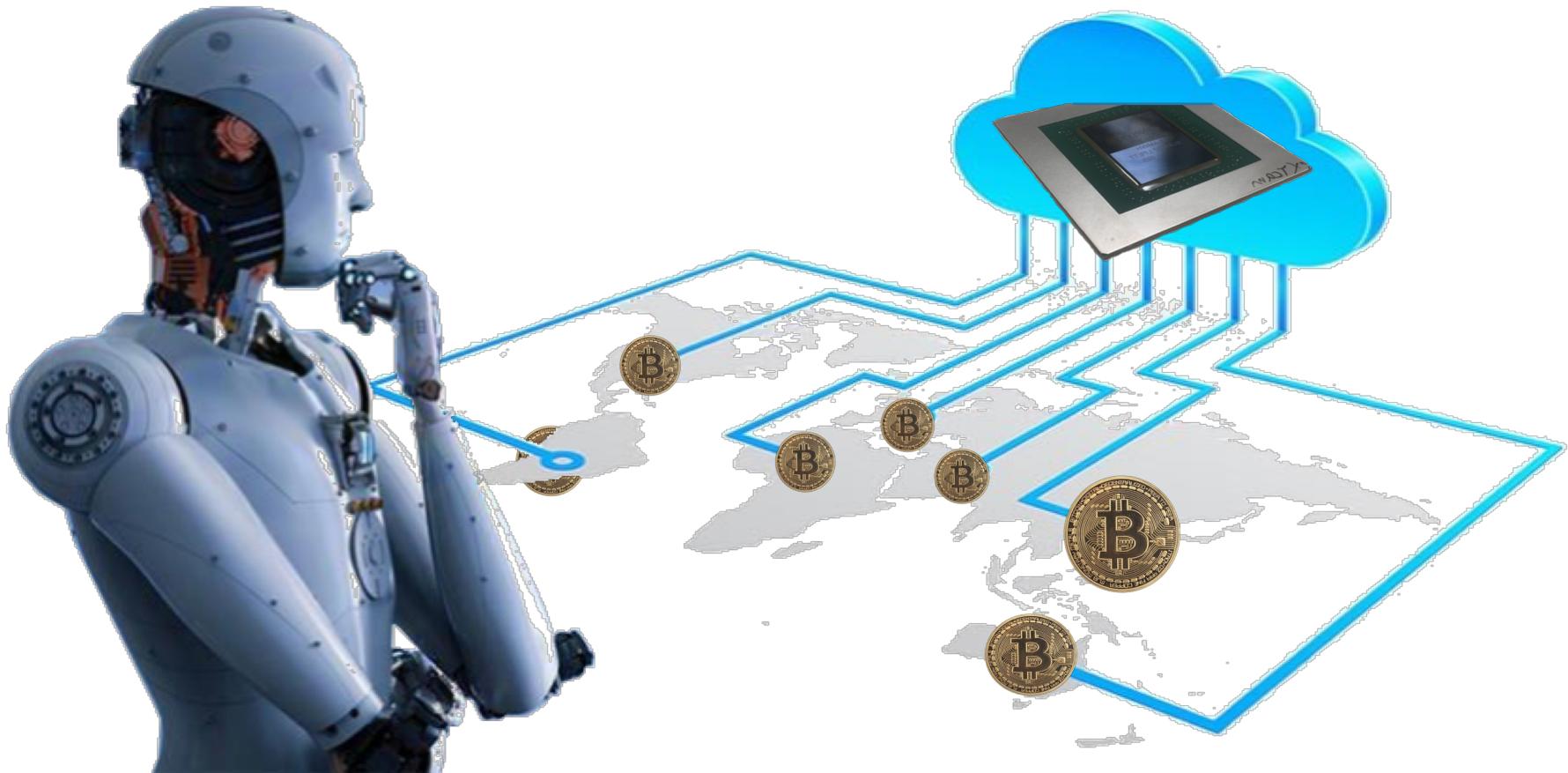
Paul, Po-Hao Chang
MediaTek Inc.



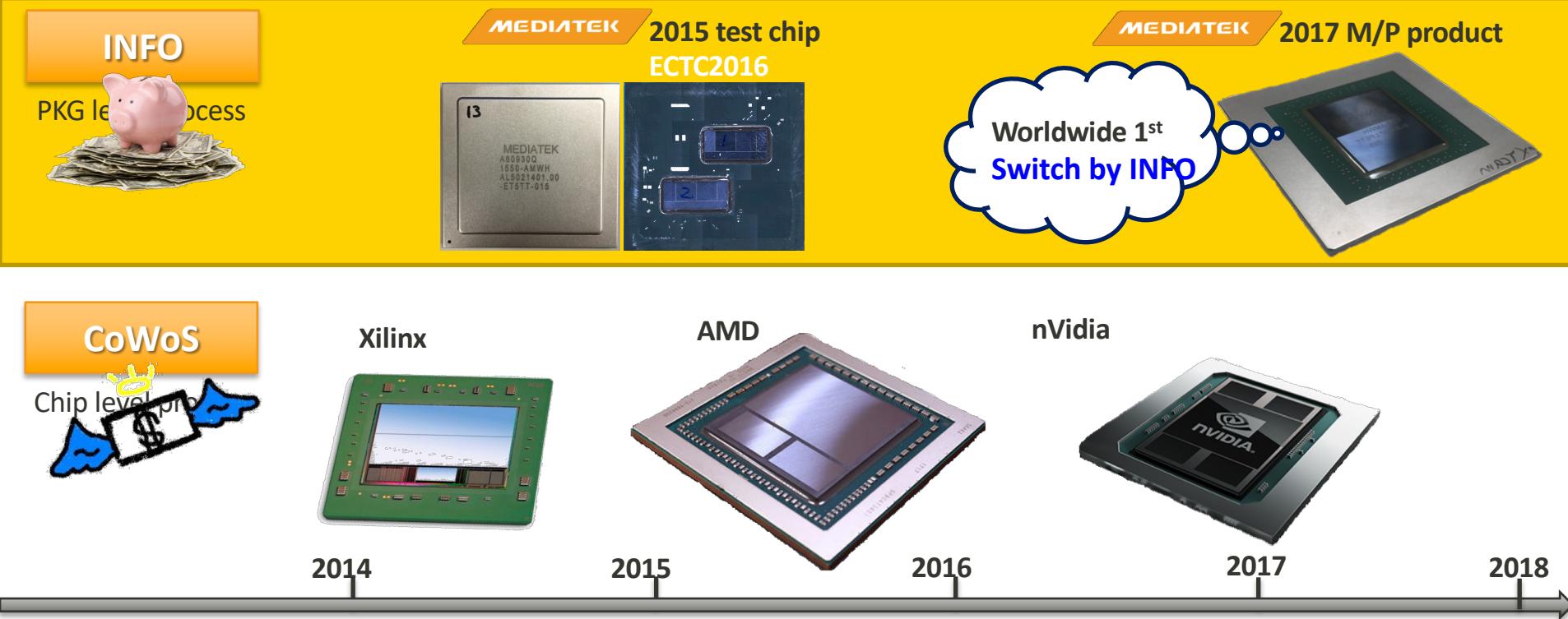
Outline

- Preface
- Design Challenges and Solutions
- Silicon Verification
- Conclusion

Motivation: Industry 4.0



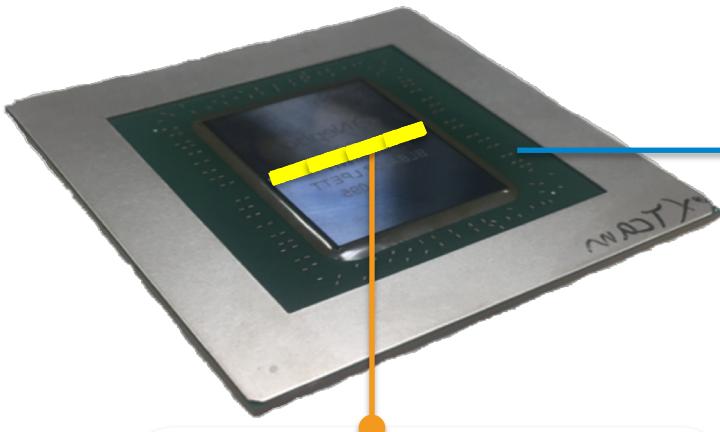
Why InFO ?



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Design Challenges (PI)

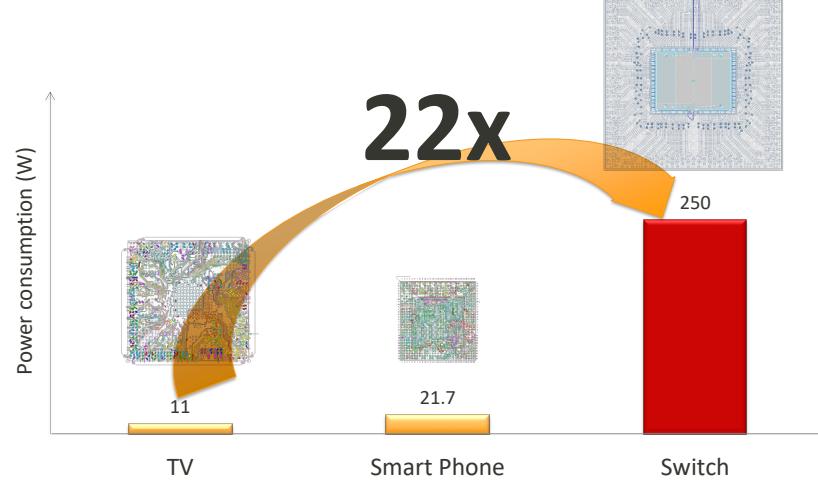


SI design

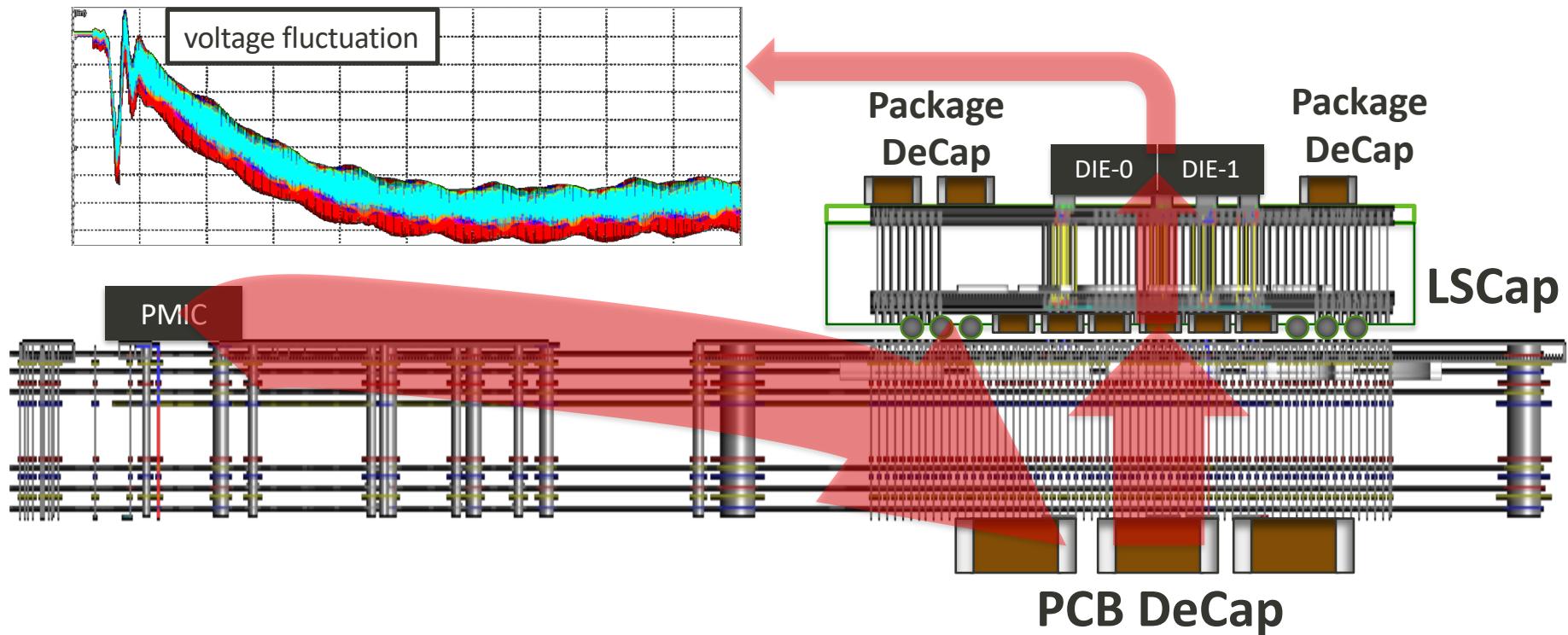
- 2268 DQ within 22000um
- Cross-talk reduction
- Trace length investigate

PI design

- PDN optimization w/ 250W
- Shortest path w/o PKG Cap.
- 2268 DQ SSO noise control



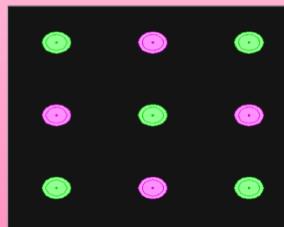
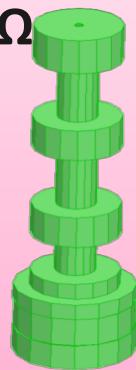
Charging Path



INFO PDN: VIA Structure

Traditional VIA:

R:11mΩ



DC R

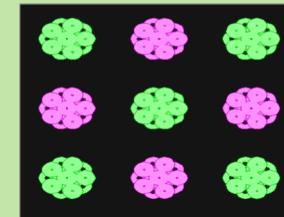
/4

Density

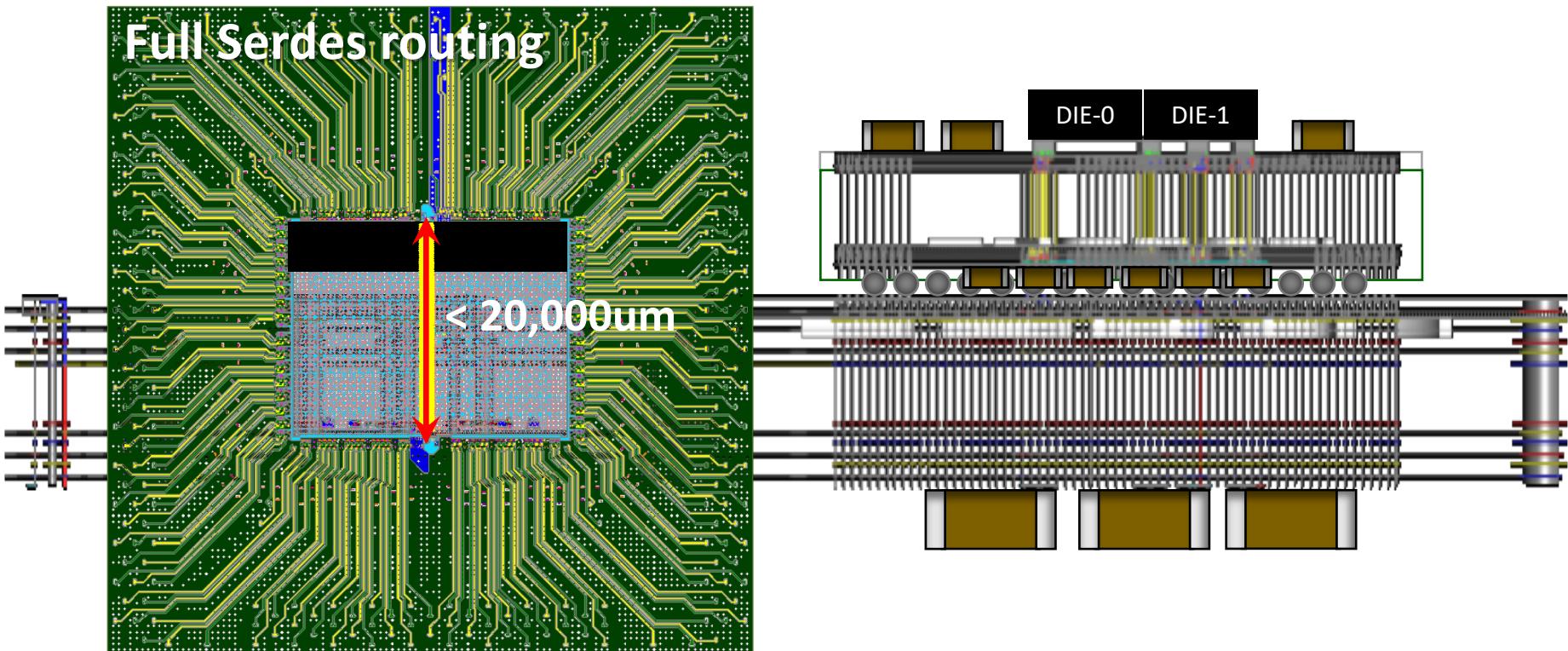
5X

New INFO VIA pattern :

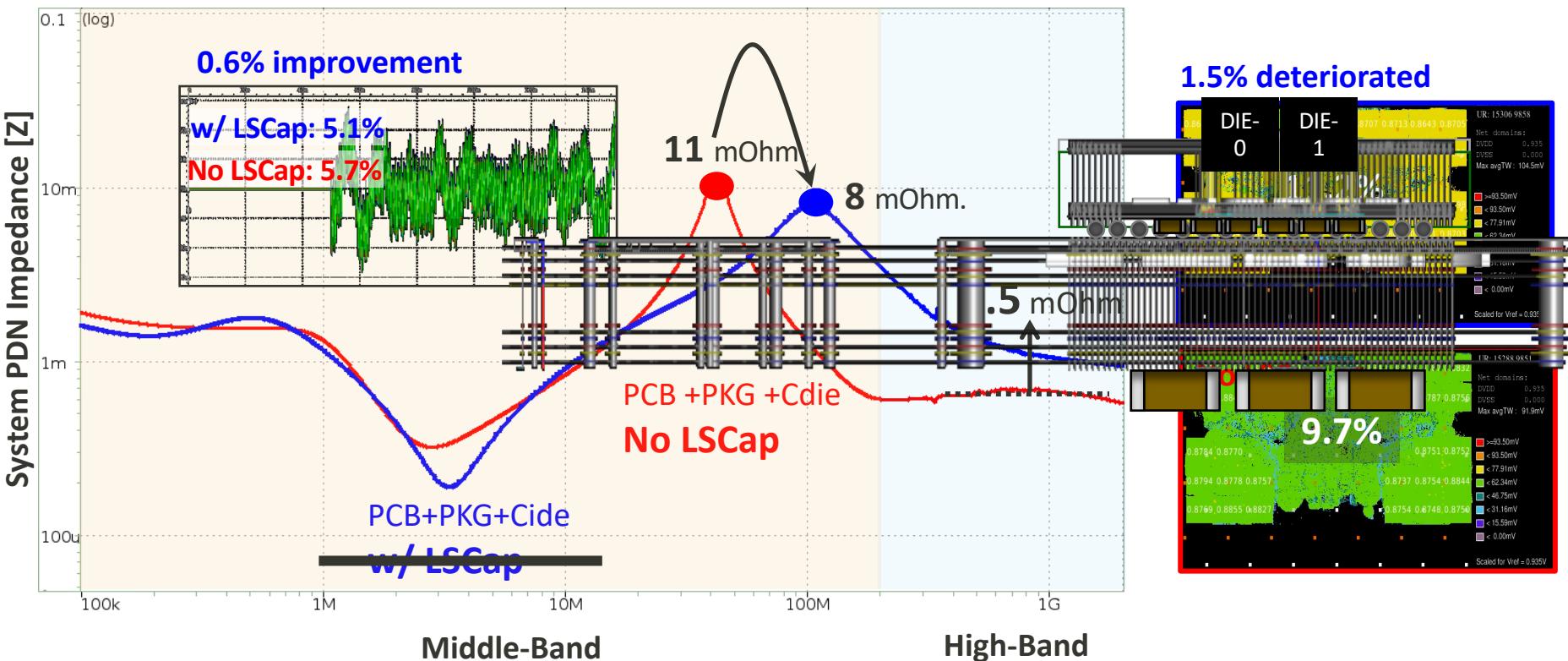
R:3mΩ



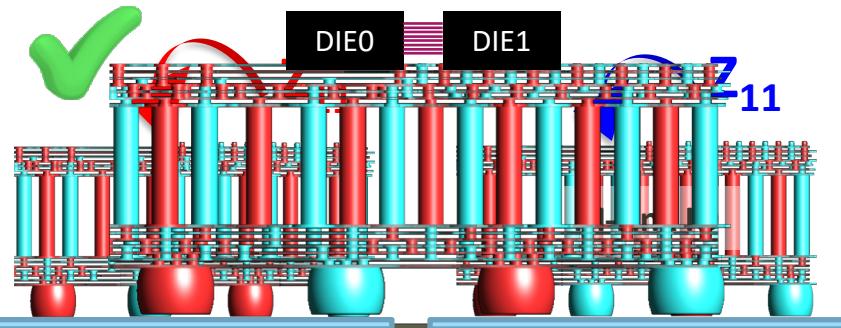
DeCAP Placement Strategy



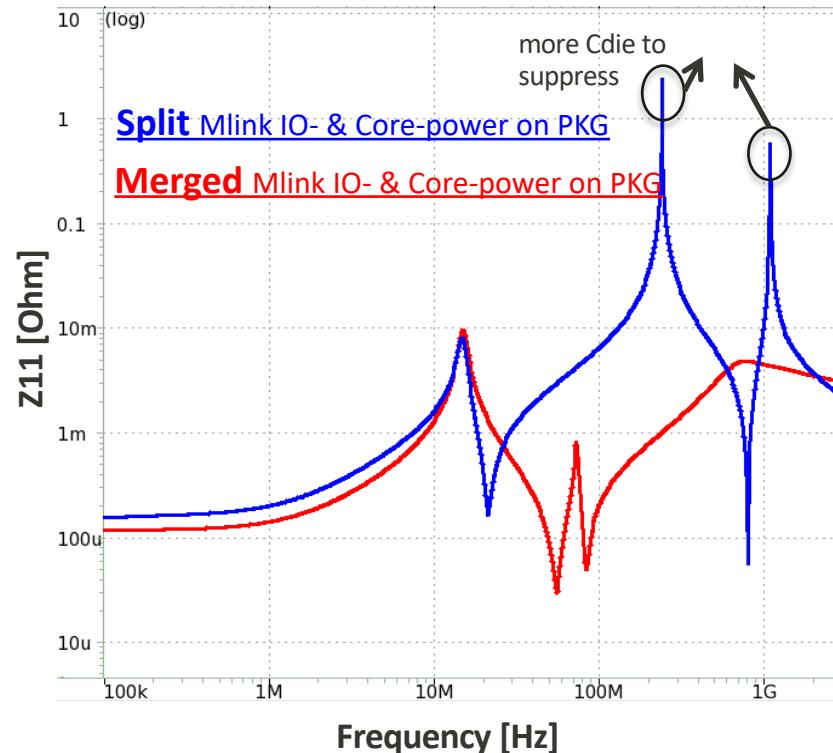
PKG LSCap



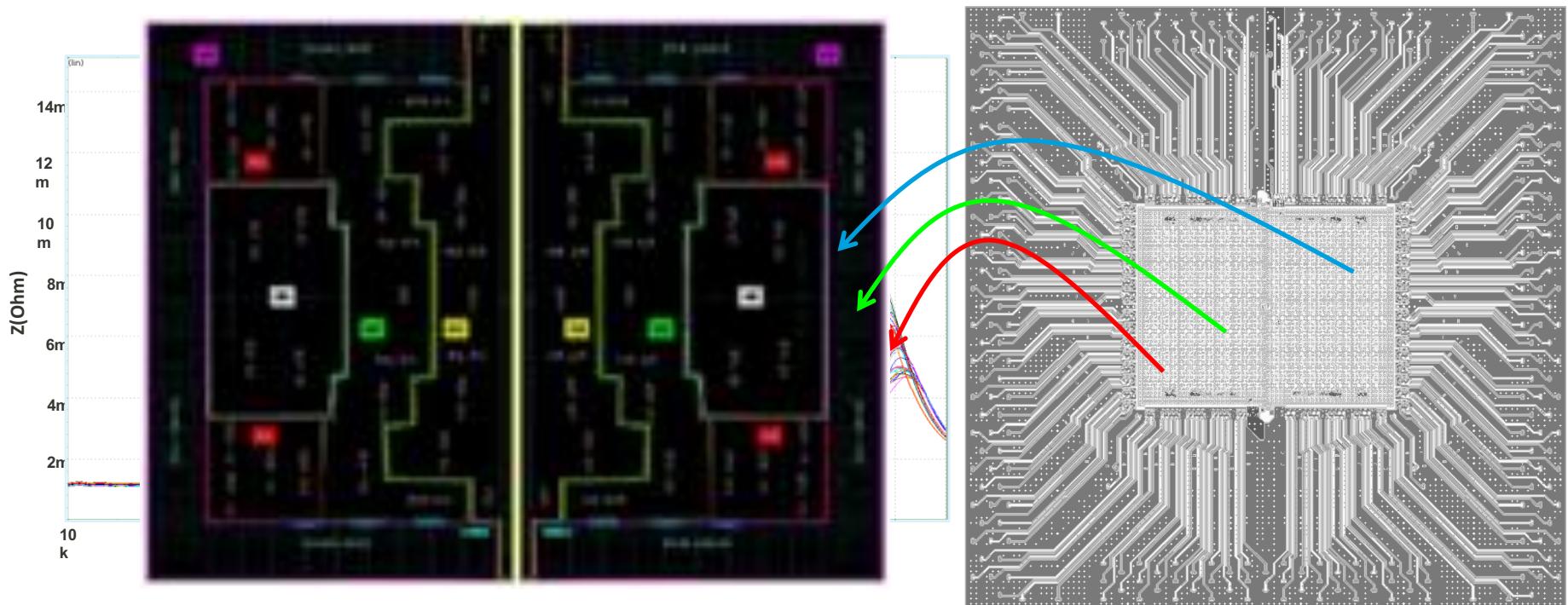
PKG PDN Organization



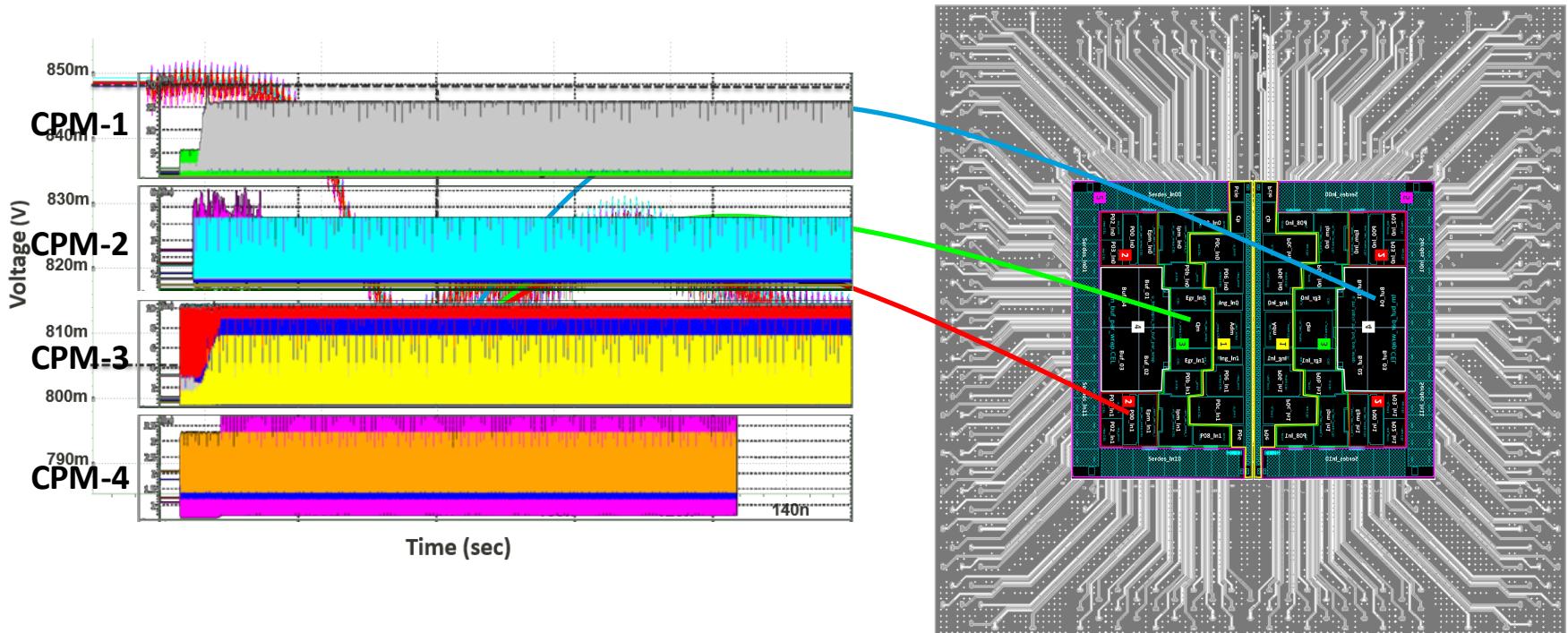
	Merged Solution	Split Solution
Pros	<ul style="list-style-type: none">Complete Core-power planeBetter INFO domain DCR & ACLNo need LSCap to improve INFO PDN	<ul style="list-style-type: none">Core-power noise not couple to M-Link
Cons	<ul style="list-style-type: none">Additional Core-power noise couple from core domain	<ul style="list-style-type: none">Layout design complexity



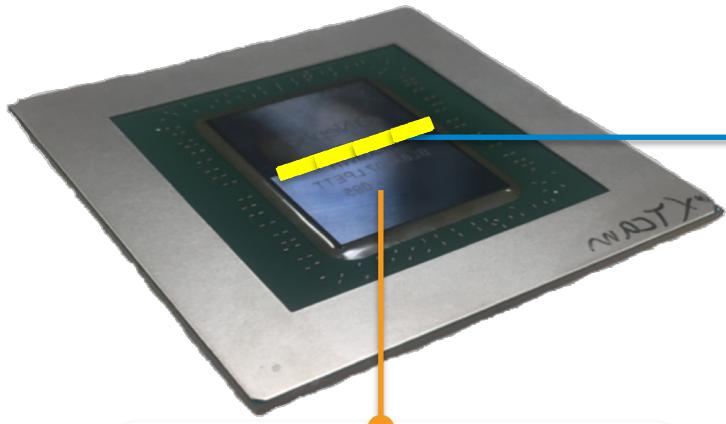
System PDN Modeling



System IR Drop



Design Challenges (SI)

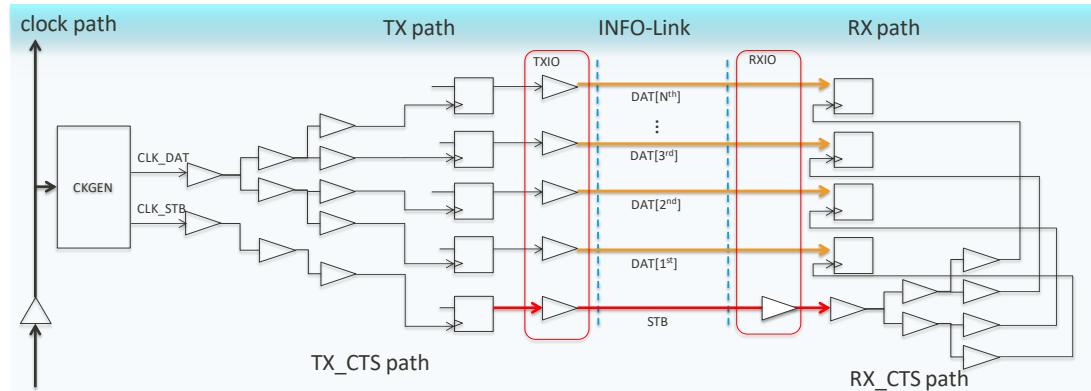


SI design

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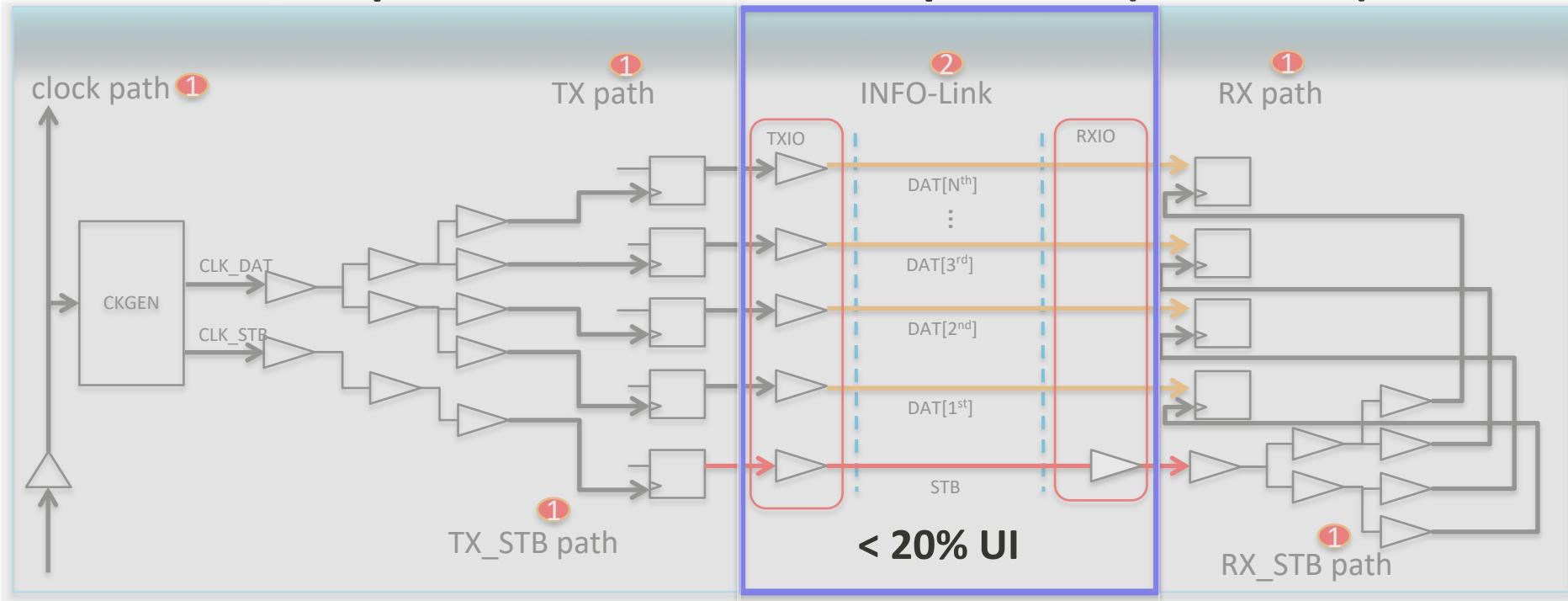
PI design

- PDN optimization w/ 250W
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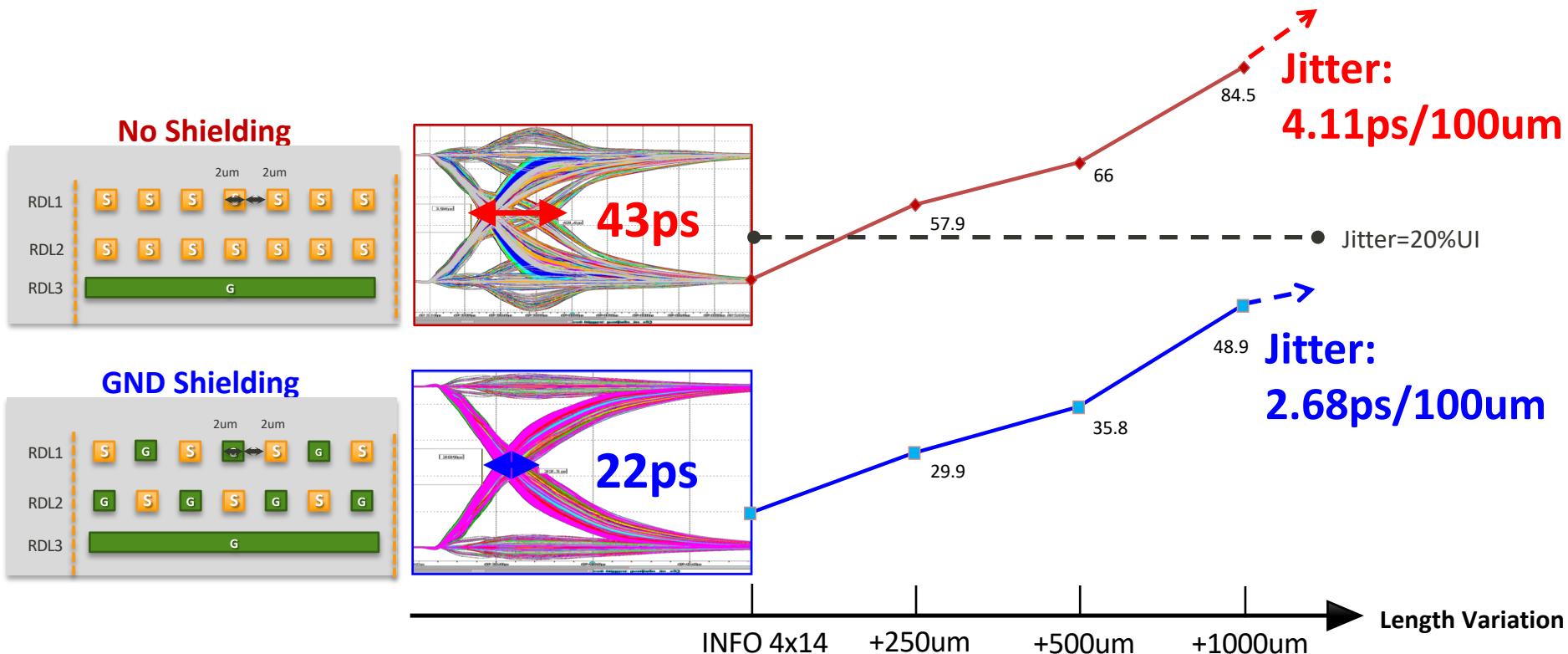


M-Link Circuit Block Diagram

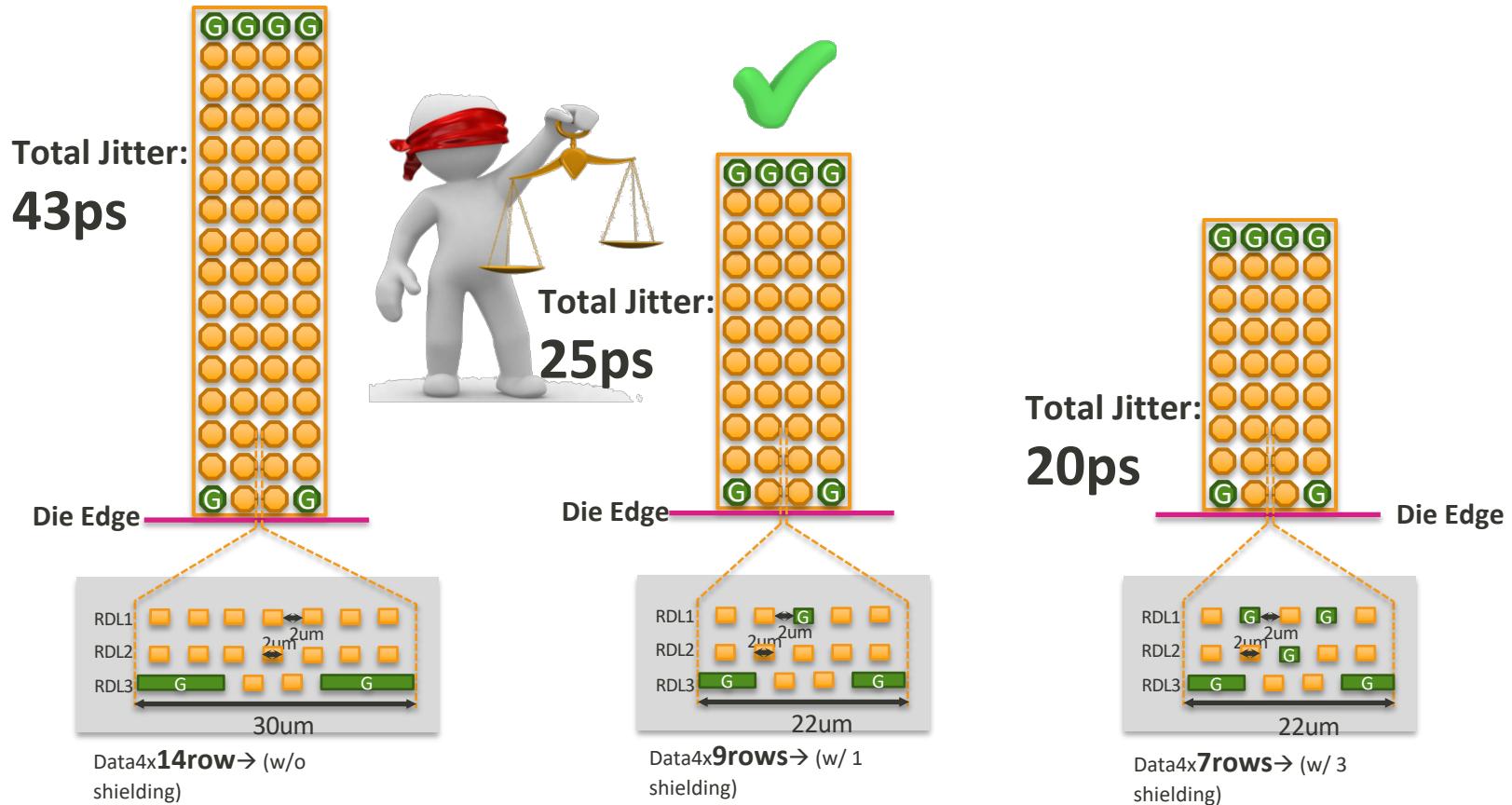
M-Link → ① Chip level circuit + ② Off-Chip carrier (INFO-Link)



Extreme INFO Topologies



INFO Bump Tile Combination

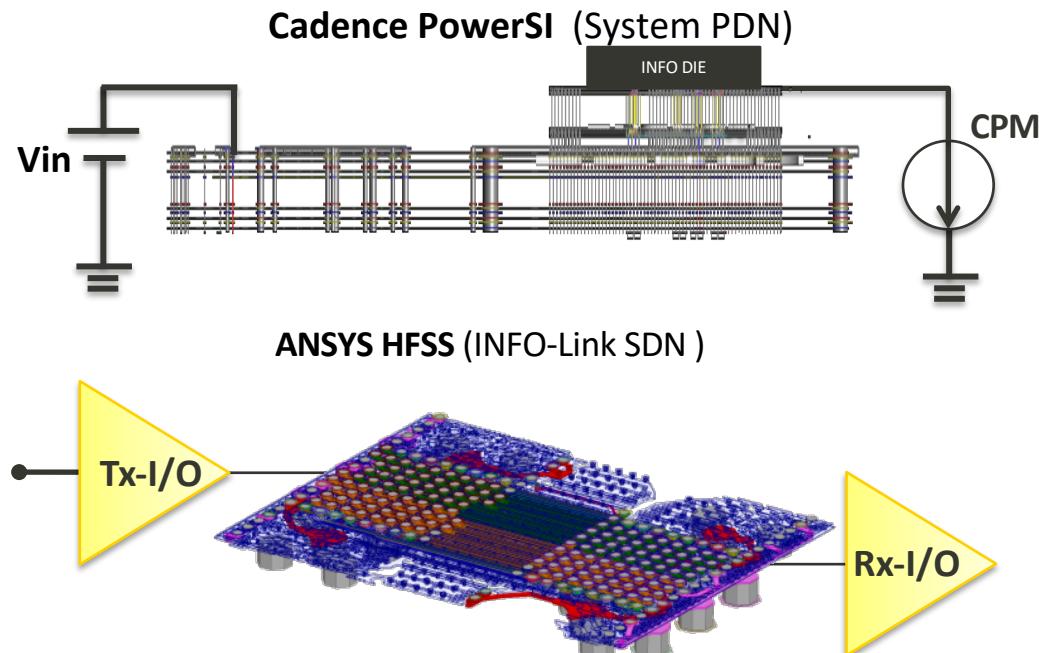


Outline

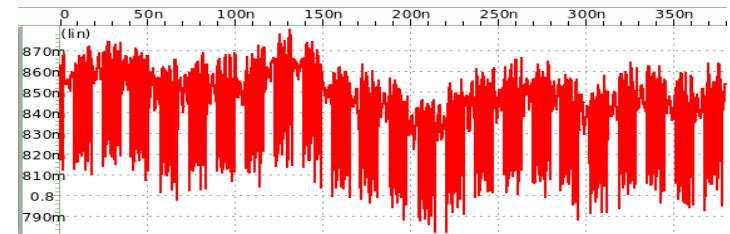
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SI/PI Co-Simulation

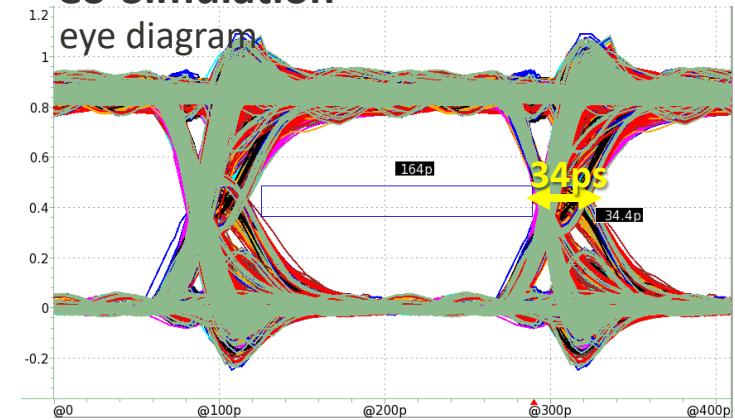
Configuration



Power noise (Core noise and INFO SSO)



Co-Simulation
eye diagram



Silicon Verification

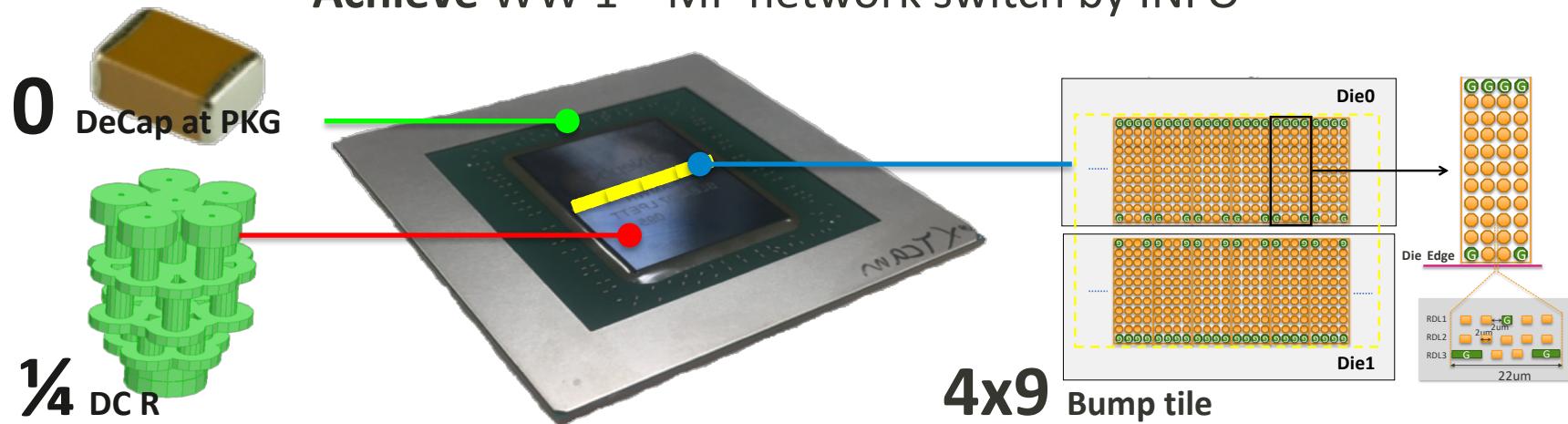
M-Link Jitter			
Condition	Worst Simulation (250W)	Heavy load Measurement (186W)	Light load Measurement (76W)
Circuit level (Jitter)	60ps	79ps	60ps
INFO-Link SI/PI (Jitter)	34ps		
Pass window (UI-Jitter)	133ps (58%UI)	148ps (62.5% UI)	167ps (70.0% UI)

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Conclusion

Achieve WW 1st MP network switch by INFO



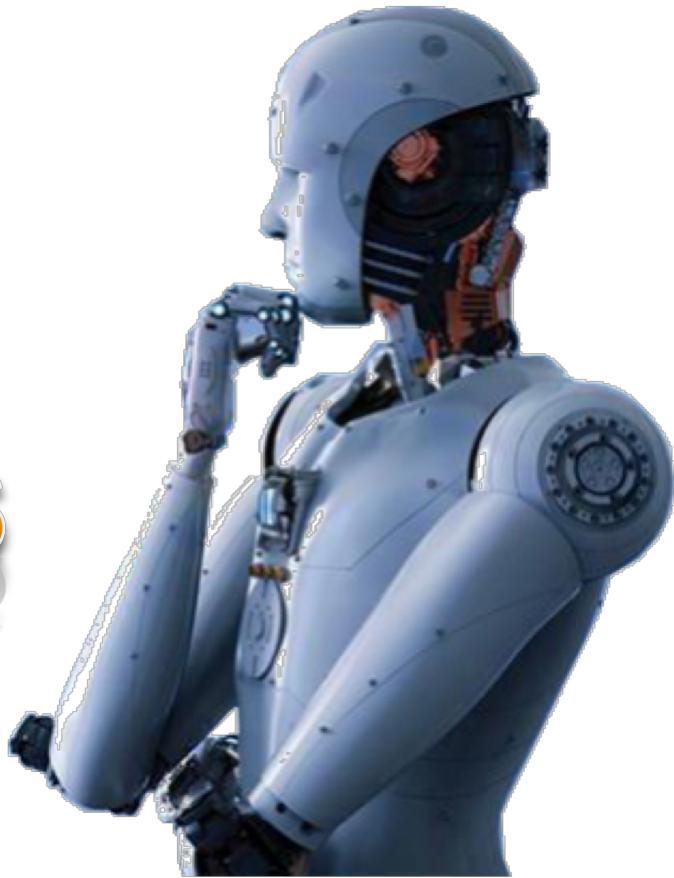
Achieve 250W System power requirement

1. package design with 0 capacitor
2. INFO VIA design reduces the impedance by 1/4
3. Merged PDN w/ System-IR drop around 5.22%

Achieve 6.4Tb System BW requirement

1. The INFO bump tile in 4x9 with one ground shielding
2. Total jitter in 34ps is satisfied with 20% UI budgeting specification

Any
Questions





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everyday genius