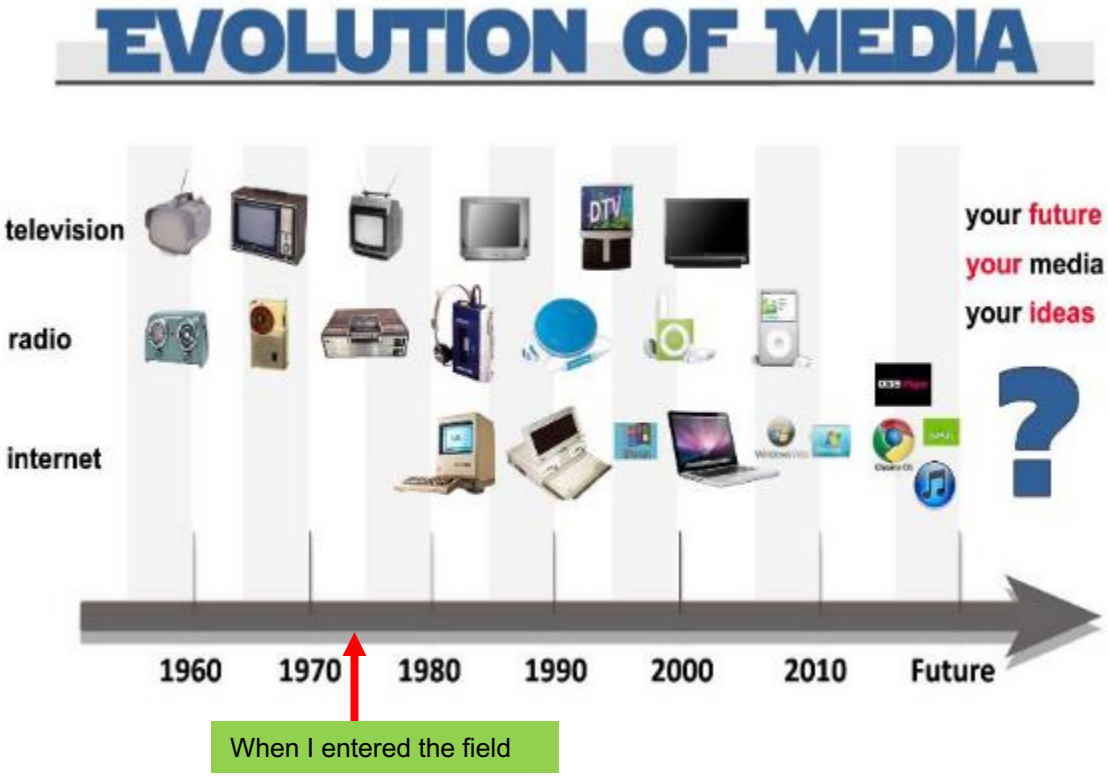
100Mhz .13u Buck in a SIP *evolution* to IVR – “Merckx”

…personal
…portable
…connected

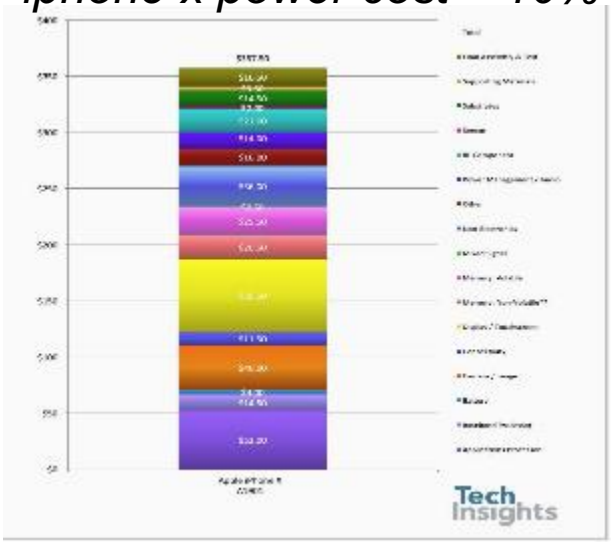
Agenda 100Mhz Buck Evolution To PWRsoc

- **Progress Towards Power Supply on Chip or SIP**
- Scaling Impact and Process Selection (Optimizing PPAC)
- Progress on Discrete Inductors and Capacitors
- Introducing Merckx – Stage 2 SIP
- 100Mhz Results Efficiency, DVS Load step and settling
- Stage 1 and Stage 2 architectures and Simulation Results
- Roadmap ongoing Development

Evolution of Products and Power Delivery



iphone x power cost ~ 10%



iphone x cpu power board area ~30%

High Efficiency Power Delivery is one of the few opportunities to save cost, area, battery life and thermal – *higher frequency operation required*

Evolution of VR Technology [1]

Progress Being Made

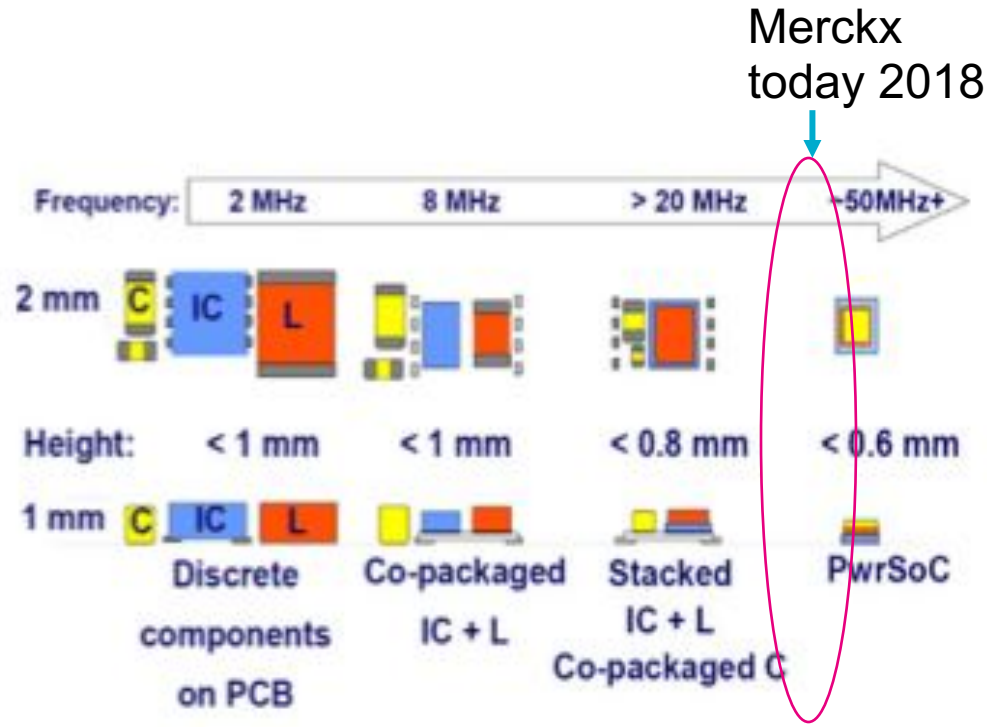


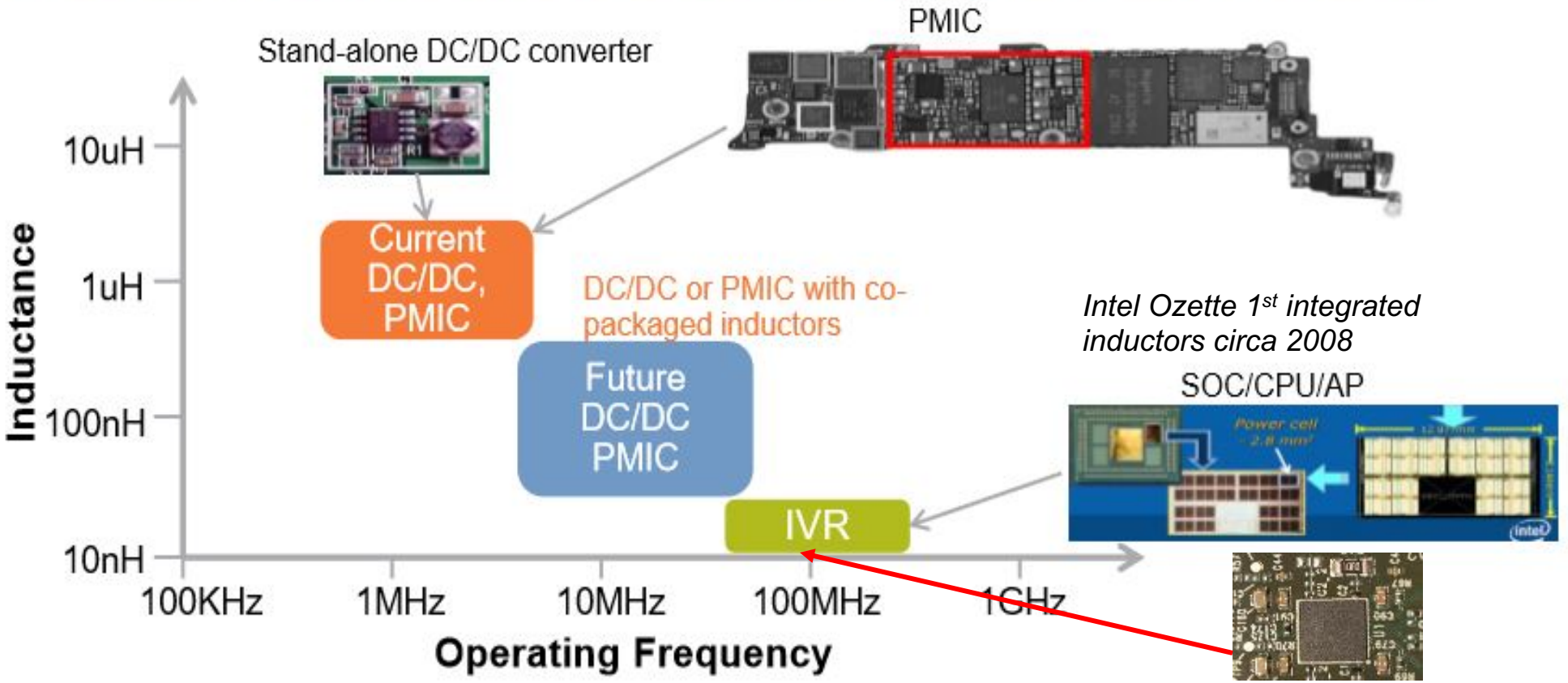
Fig. 3. Vision for evolution of PwrSoC technology.

Where we are now – 2018 Integrated inductor products eminent -2019

The Size and Value of the ondie inductor will dictate Die Size present technology for 1 amp saturation is ~ .5MM Area. Beyond 55 nM, smaller die will not allow Integrated Inductors.

Review of Integrated Magnetics for Power Supply on Chip (PwrSoC) Cian ´O Math ´ una, Senior Member, IEEE, Ningning Wang, Santosh Kulkarni, and Saibal Ro IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 11, NOVEMBER 2012 4799

Reducing the area used for power conversion



Intel Ozette 1st integrated inductors circa 2008

Merckx SIP 2018
(Inductors and Capacitors Inside Package)

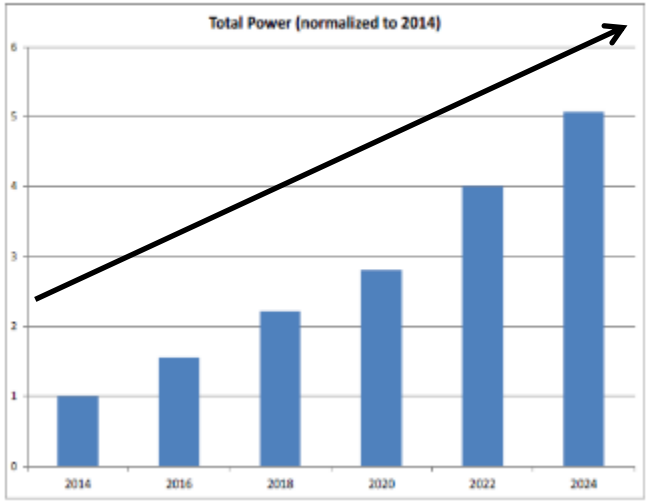
- SUMMIT technology focus is on DC/DC and PMIC

Motivation Why run a buck at ~100MHz?

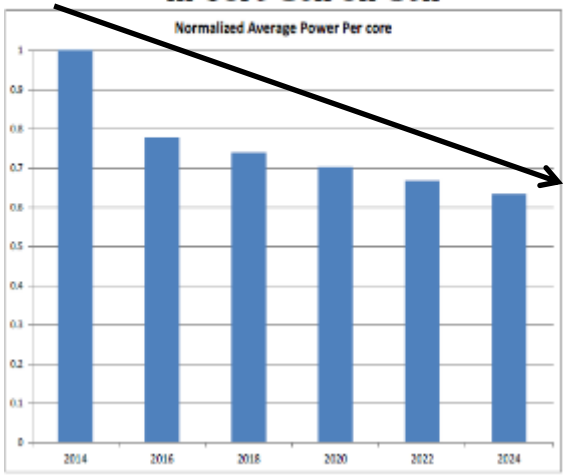
Can't fight physics…

- Architecture changes in cores cannot change physics
  - The demand for increased CPU performance Gen on Gen drives power up
  - To counteract this, per-core power consumption must decrease – each core must become more efficient
  - The PMIC must help with this – CPU core architecture cannot do it alone
  - # of Cores on SOC Increasing – Fine Grain Power Management Required.
  - To get smaller and fewer components need to go faster (area ~ switching Frequency)

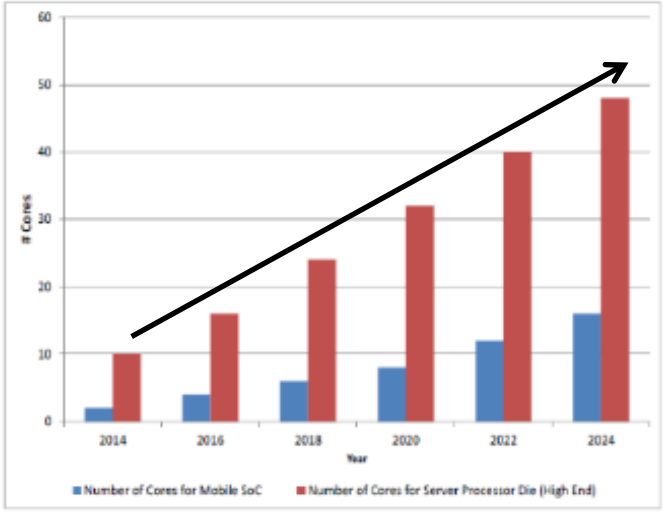
Max Power Gen on Gen



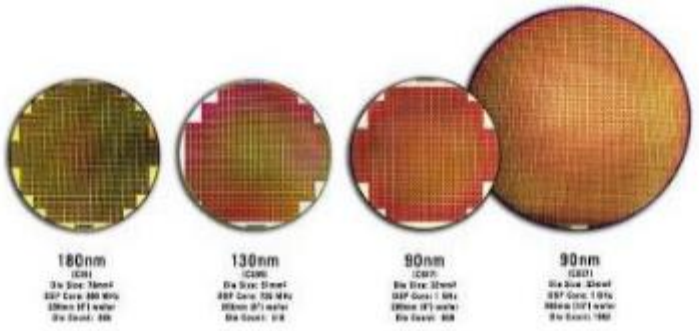
Power Required to stay flat in Core Gen on Gen



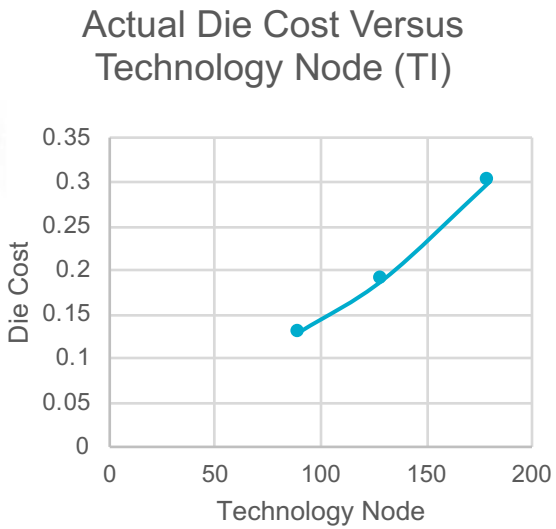
# of Cores on SOC over Time

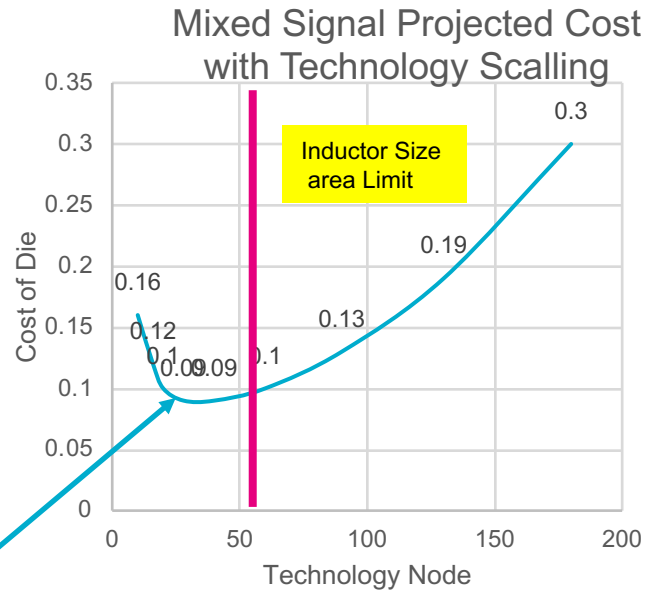


Why Consider .13u Versus Deep Sub Micron



Cost Going up in Deep Submicron technologies





Minimum cost Point ~ 28nM

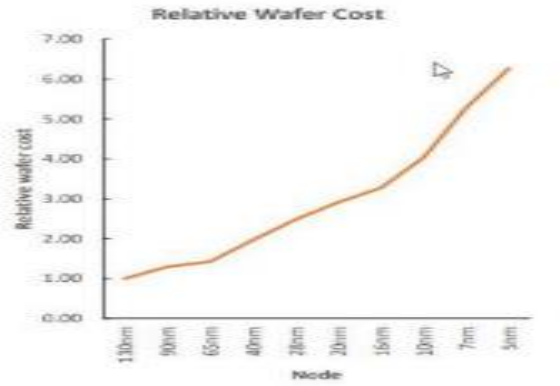
Projection by Jim Doyle

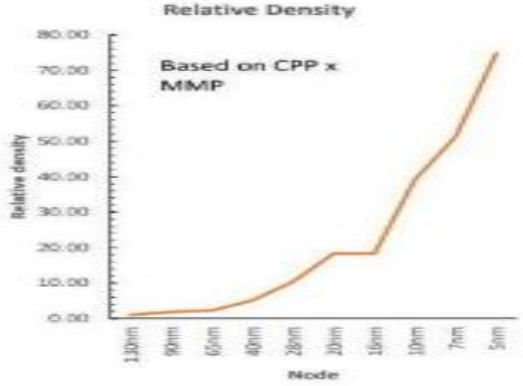
Technology Node (nM)	Die Size MM2	DSP Clock (Mhz)	# of Die	Cost per Die $
180	78	300	336	0.3
130	51	720	518	0.19
90	32	1000	826	0.13
8 Inch wafer costs / $1000				

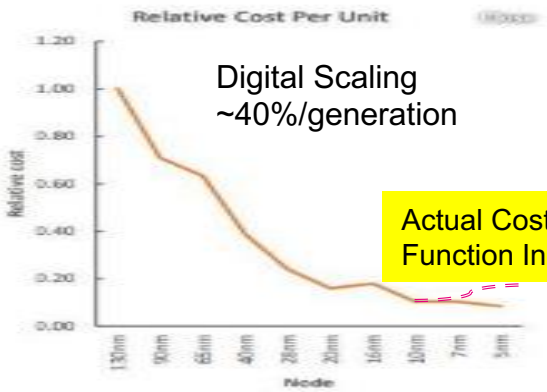
Economies of CMOS Scaling

Dr. Hans Stork Senior Vice President, and CTO Texas Instrument 2004

Relative Cost versus Analog Scaling (10% Analog Scaling/Technology Node)







Actual Cost per Function Increasing

The scaling of MOSFETs, Moore's law, and ITRS 2014

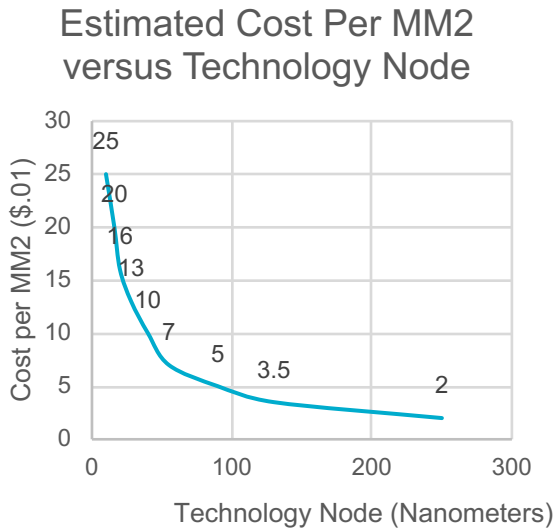


Figure 1

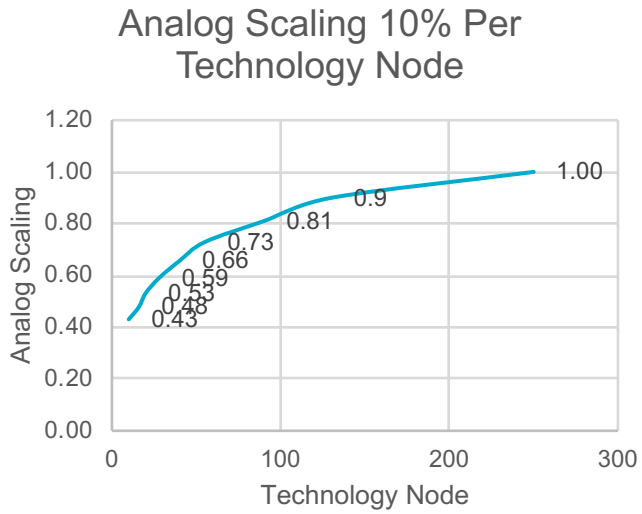
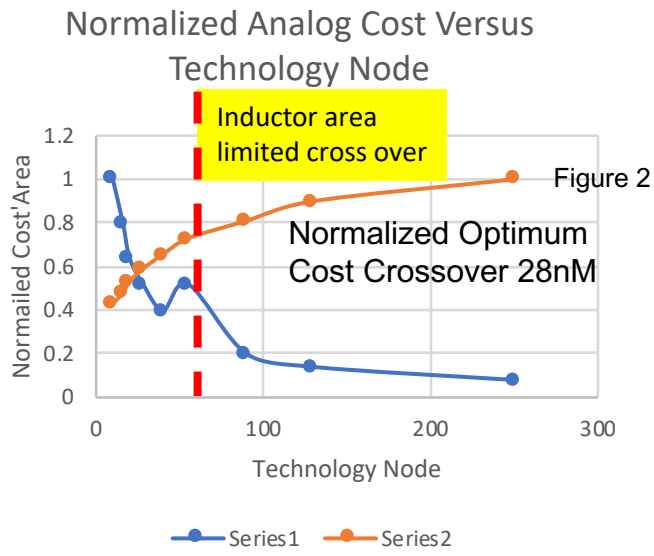


Figure 2



Projections by Jim Doyle based on publish results

Capacitor Technology

Miniaturized Passives for SiP

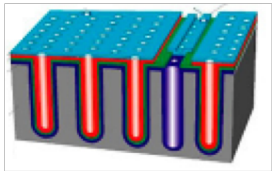
Silicon caps offer significant improvements in electrical performance and reduced foot print, but at a higher per-unit cost.

Reduced ESL in Si-Caps can directly impact voltage droop (~30% improvement) for LSC configurations.

MLCC

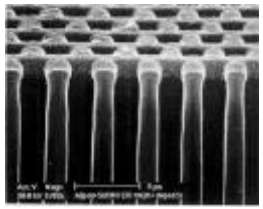
Size: 0402 (0.1mm)
Target Value: 220nF
Derating: 2x
ESL: ~150pH
Cost: ~ $0.01

Silicon Caps
(discrete)



Size: 0402 (0.1mm Thick)
Target Value: 2 x 220nF
Derating: 1x
ESL: ~50pH
Cost: ~$0.05

Silicon Caps
(integrated)



Size: ~1µF/mm^2
Target Value: 220nF
Derating: 1x
ESL: ~10pH
Cost: TBD

Inductor Technology (Challenging)

Miniaturized Passives for SiP

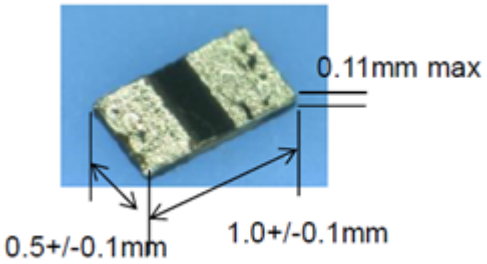
Low DCR coils is key to maintaining high efficiency with high-frequency VRs

LSC connected coils are the “best” option today, with integrated coils (on-die / in-package) becoming available in the near future.

Discrete Coils
(stage-1)

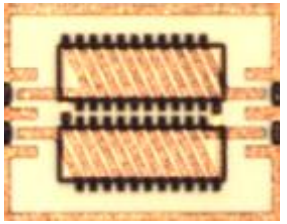
Size: 1206 (<1mm)
Target Value: ~20µF
I_{SAT}: >3A
DCR: <20mΩ

LSC Coils
(stage-2)



Size: 0402 (0.1mm – 0.2mm)
Target Value: ~5nH
I_{SAT}: ~3A
DCR: 20mΩ - 50mΩ

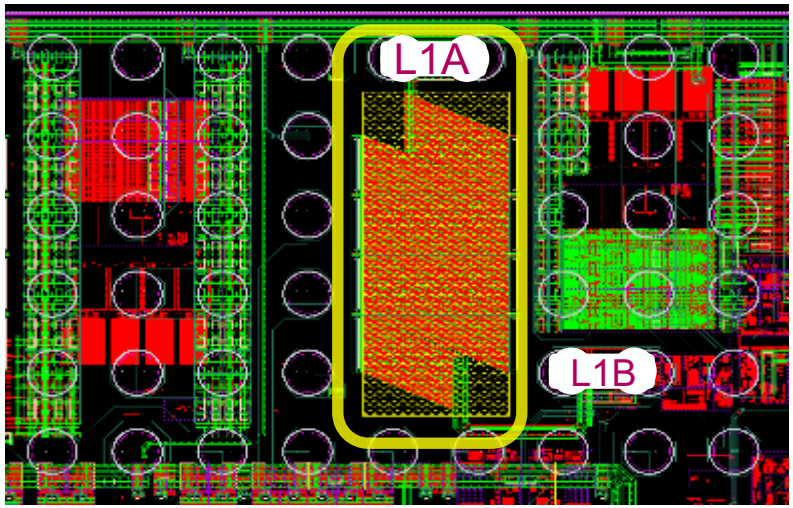
Integrated Coils
(stage-2)

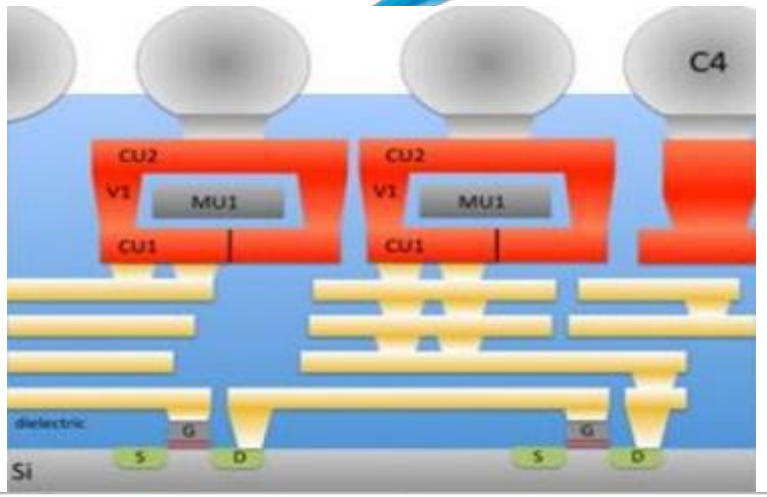


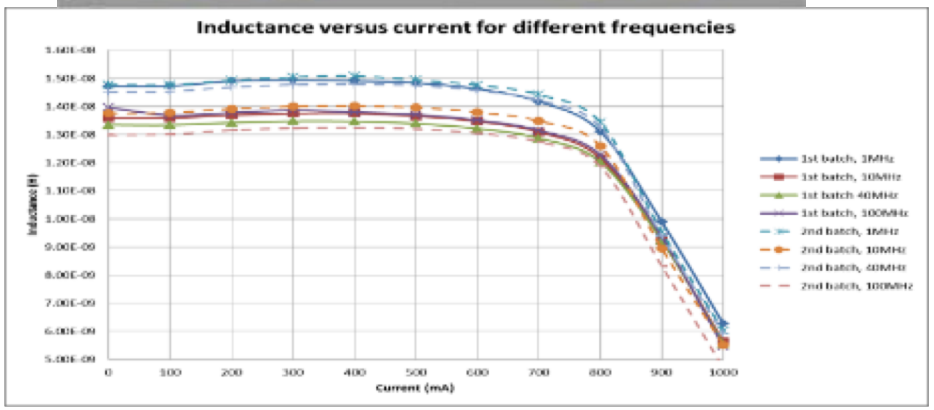
Size: ~300nH/mm^2
Target Value: ~5nH
I_{SAT}: 1A (uncoupled)
DCR: 20mΩ - 50mΩ

1st Generation “Tesla” 10nH integrated inductor with Magnetics circa 2016

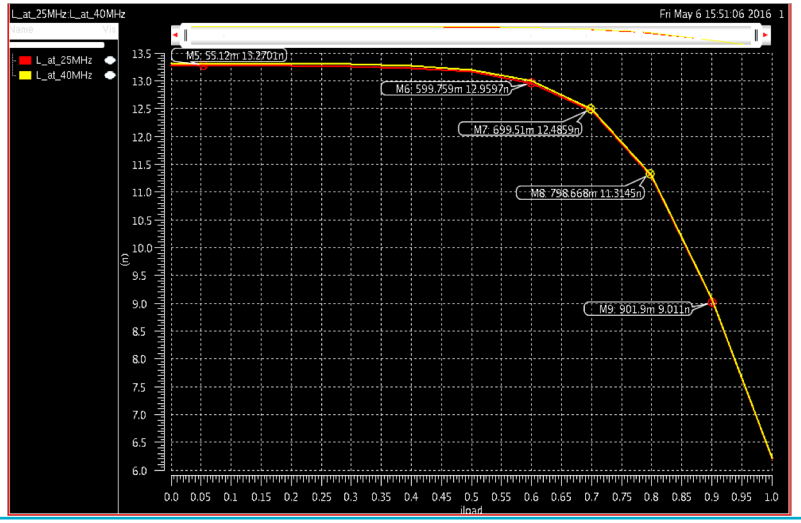
Inductor area 2MM x 1MM







Measured Results in Good agreement with Model



1st & 2nd silicon results (measured on different sites, equipment, test jig)
10% inductance reduction at ~800mA (Isat)

Integrated Inductor with Magnetics on a Production Chip (Industry 1st)

Why Consider an Older Co-package Technology versus Deeper Submicron Integration.

Decision to integrate Power or Not to integrate on SOC?

- Lower Total system Cost
  - KGD Know Good Die Improves System Cost.
  - 20% fewer components
  - 40% Total Board area (stage 2 inductors replace with on chip solution)

- Performance
  - Fast DVS 25-30% Longer battery Life (ref. Intel). Now available on .13u process
  - Wide Bandwidth (10Mhz) eliminates 2nd and 3rd Droop
  - Efficiency improved with asymmetric device availability .13u/55nM

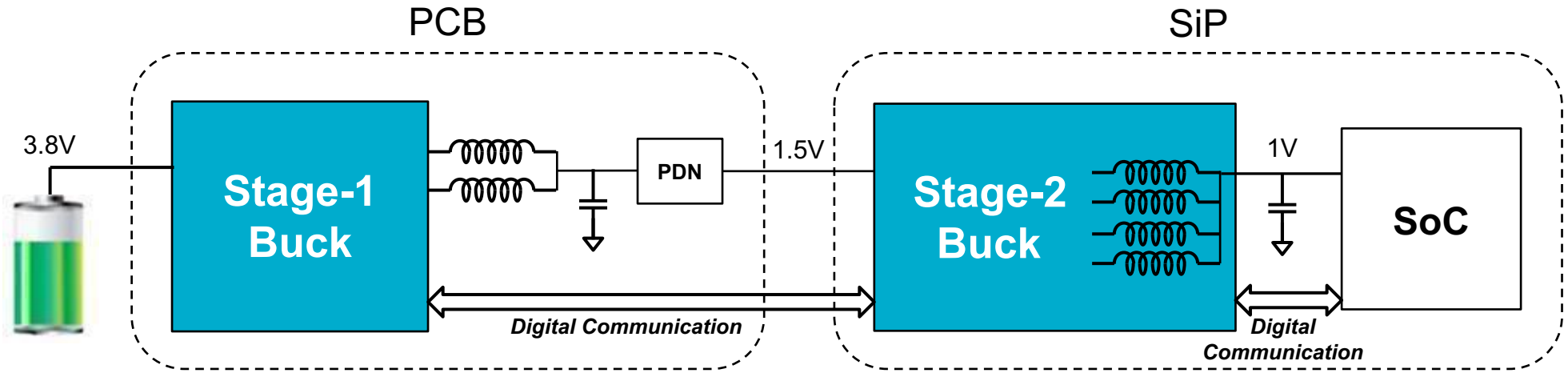
- Additional Benefits
  - Thermal Balancing moving IVR away from Core
  - Improved SOA due to larger feature silicon (.13uBCD).
  - Improved Rout-ability (Less package congestion due to ondie versus in Package Inductors)
  - More Available Ground and Supply Balls due to internal in-package conversion Ratio
  - Integrated Inductors will not fit in the shadow of deep submicron technologies

Dual-Stage Buck Architecture

PMIC-outside -of-SOC Package (SIP)

Dual-stage buck system

- Stage-1 pre-regulator typically remains with main system PMIC
- Stage-2 high-frequency buck is in-package with SoC
- Dual-stage system is optimized for target SoC load profile



- Target f_{sw} < 5MHz
- Target efficiency ~96%
- Low accuracy, high efficiency, low bandwidth, low power modes
- External magnetics

Target f_{sw} > 50MHz (78Mz)

Target efficiency ~90%

High accuracy, high efficiency, wide bandwidth, high-speed droop mitigation

On-die or in-package magnetics

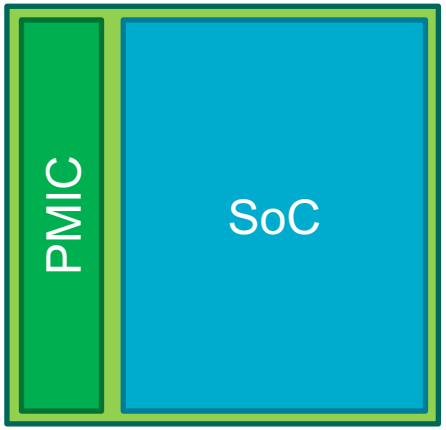
Co-Packaged With Customer Silicon Option

PMIC-in-Package (co Package)

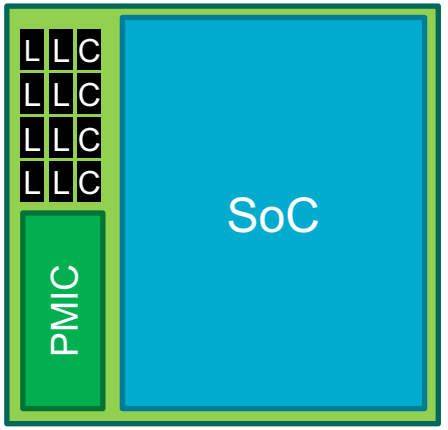
"PMIC-in-Package" is enabled by high-frequency, dual-stage voltage regulators

Use miniaturized (0402), in-package, or on-die inductors and capacitors.

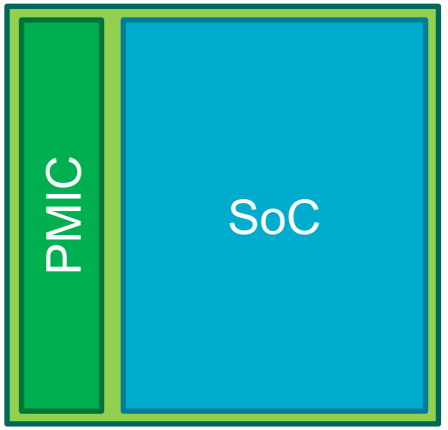
Option #1:
Land-Side Connect (LSC)



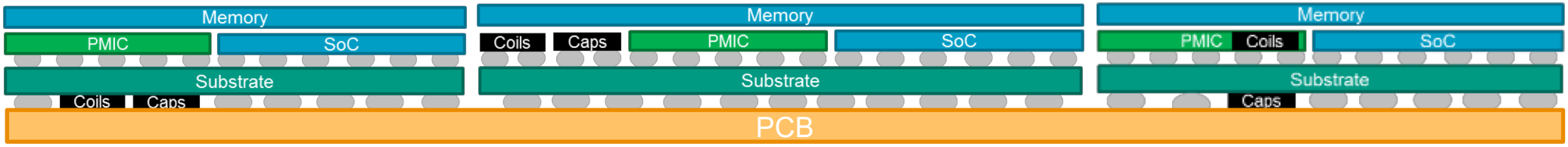
Option #2:
Die-Side Connect



Option #3:
On-die Integration

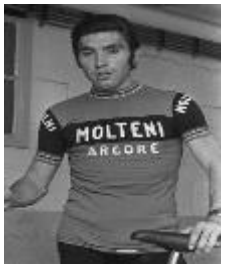


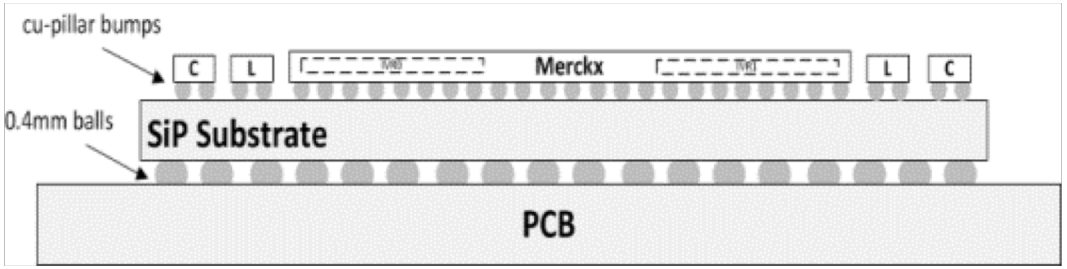
Merckx Proposal



Merckx Stage 2 SiP Package Option

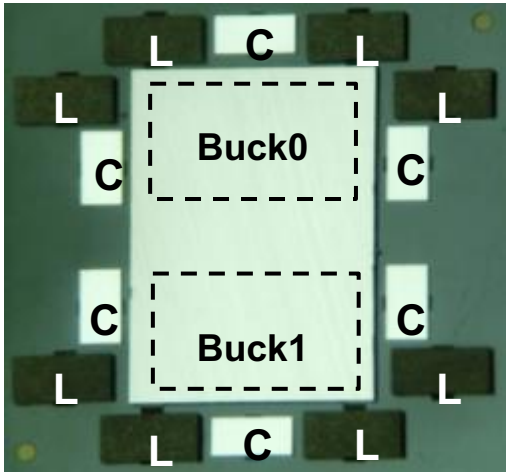
Chip named in honor of Eddy Merckx winner Tour de France 1974

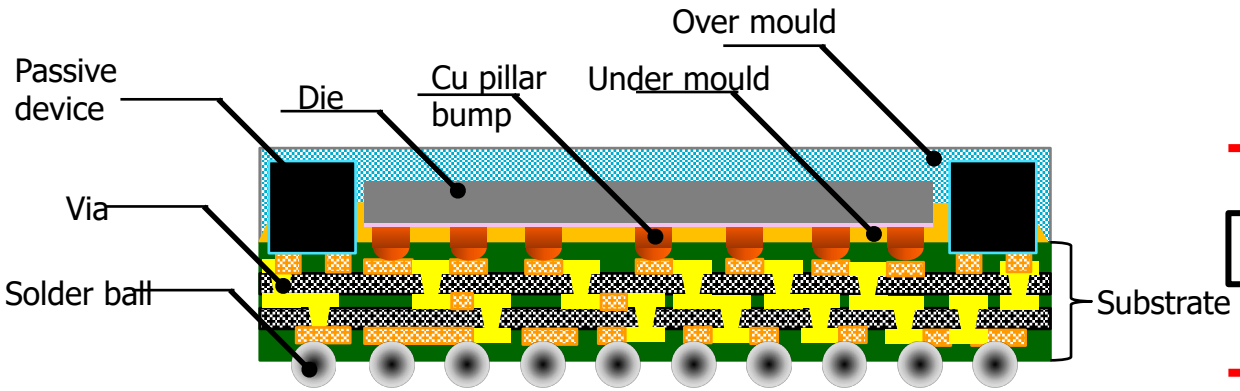


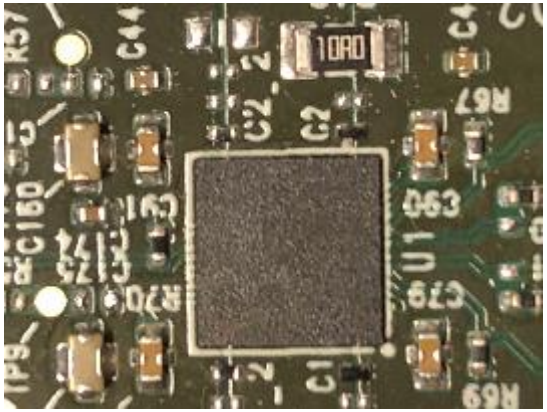


- Merckx Die – 3mm x 4.5mm
- Inductors – muRata, 5.6nH, 0.6mm x 1.2mm
- Output Capacitor – IPDiA, 200nF, 0.5mm x 1.0mm
- Input Capacitor (2x) – IPDiA, 50nF, 0.3mm x 0.6mm

6.4mm







Merkx on Demo Board

Merckx Thermal Considerations

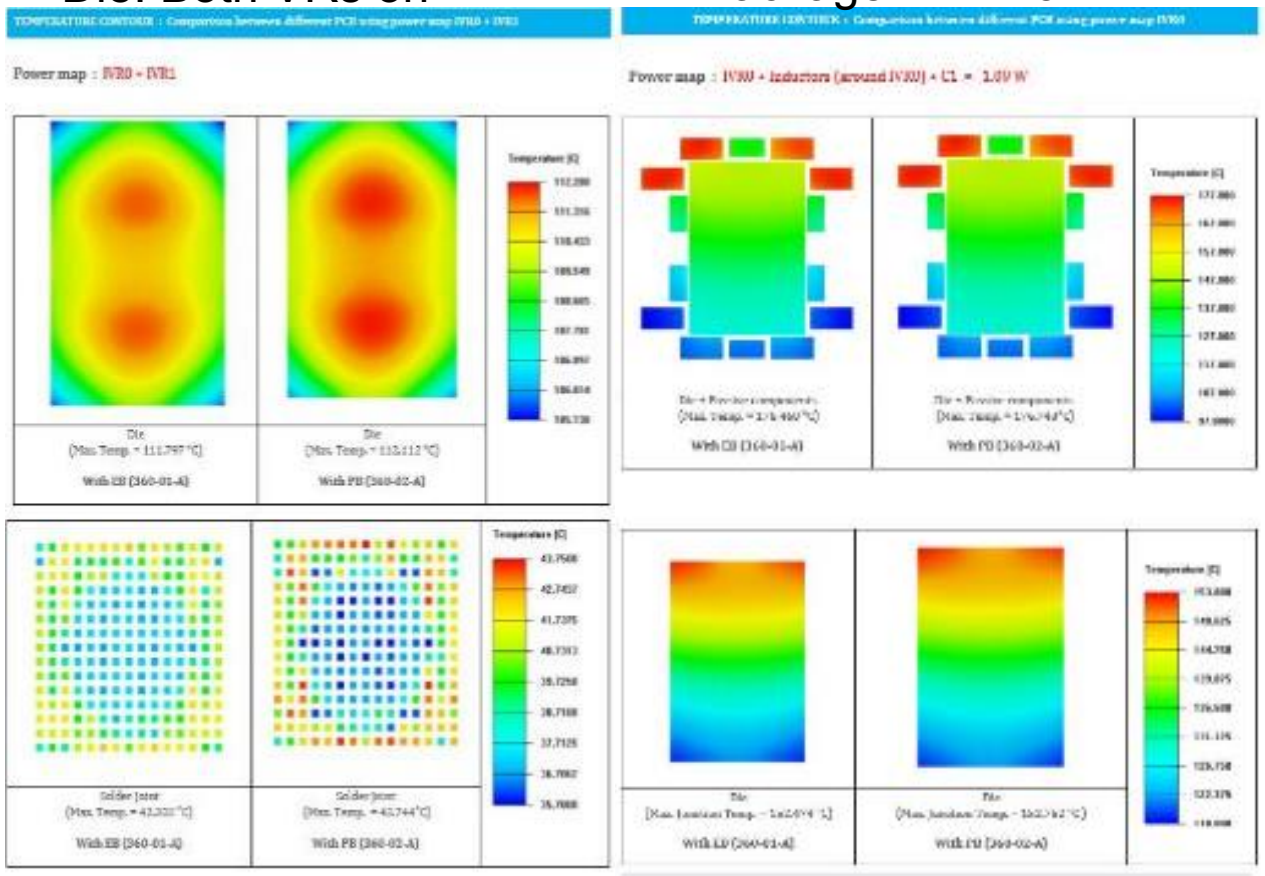
Assumptions

- Maximum load power ~8 Watts (1 volt output Load =8 amps; 4 amps/VR)
- Efficiency ~ 87%

- Merckx SIP Volume ~ 20mm^3 which is a power density of .4 watts per mm^3 or ~ 400 watts per cm3.
- Temperature rise of package is rated at degrees C rise per watt ~70C rise per watt for SIP.
- If we assume 70C Rise is acceptable @ absolute maximum power (8 amps) assuming 87% efficiency power delivered 8 watts then ~1 watt dissipated in SIP. Note: Typical Operating power is less (complete thermal report available).

Die: Both VRs on

Package: 1 VR on



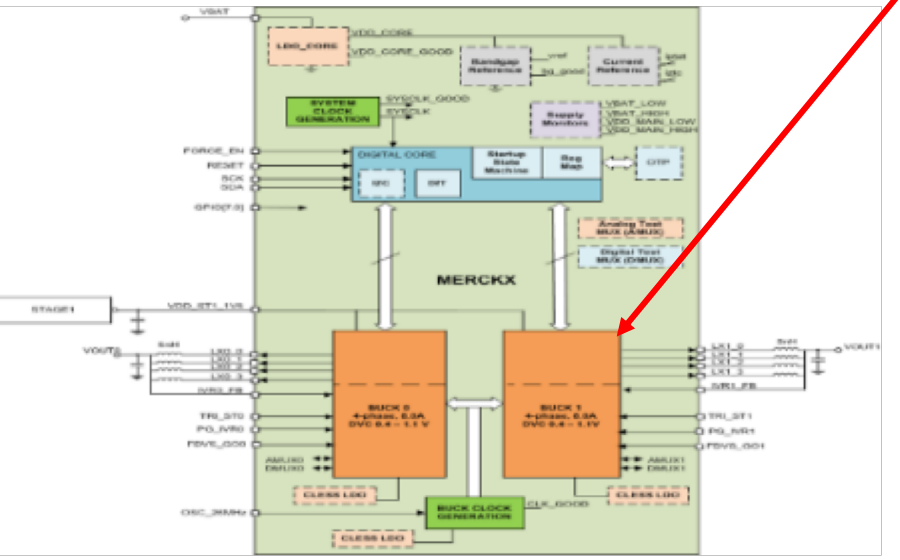
- Note: SIP distributes power away from SOC cores as opposed to Integrated solution

Vision: Merckx Gen1 SIP-> Gen2 IVR

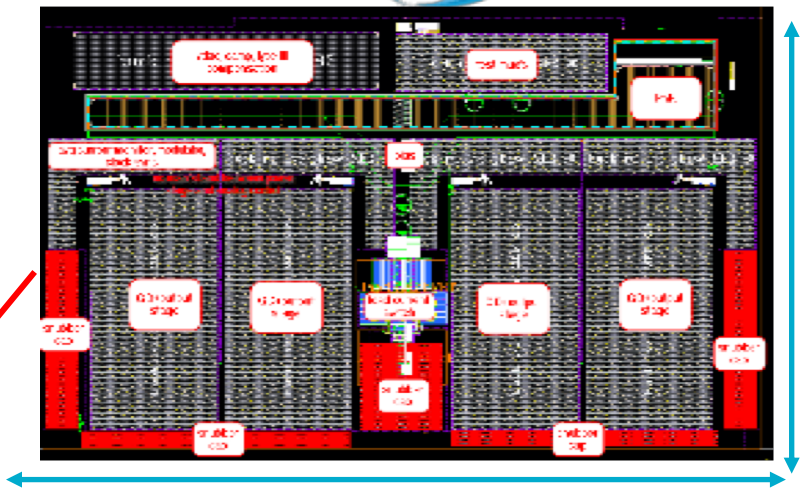
Features with Block Diagram

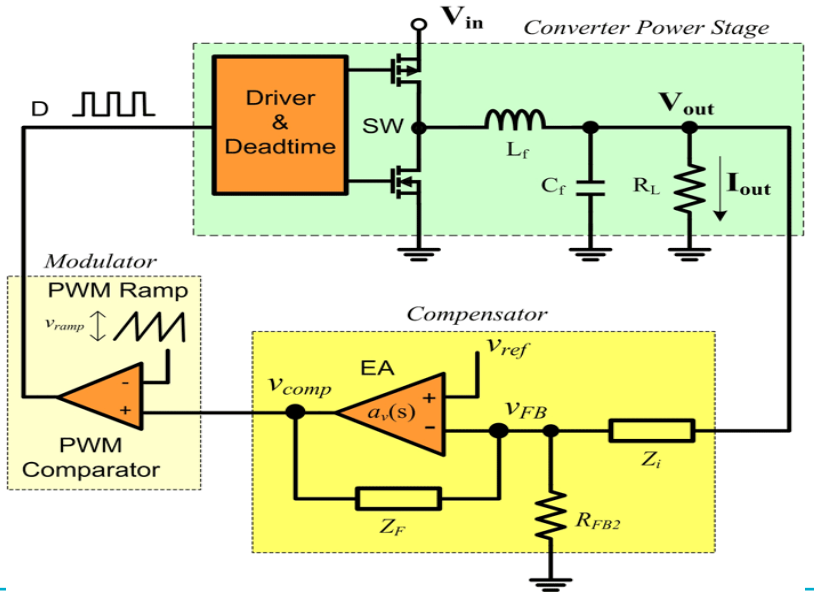
Key Features:

- 2 IVRs >4 amps each
- SIP with Discretes (.8MM Height)
- Fast DVS > 1V/uS
- Bandwidth > 10Mhz
- Resolution 9 Bits
- Output Range .4v- 1.1V
- Low Cost .13u Technology



Normalized to 4 Amps Output
(2 VRs with 4 amps each)

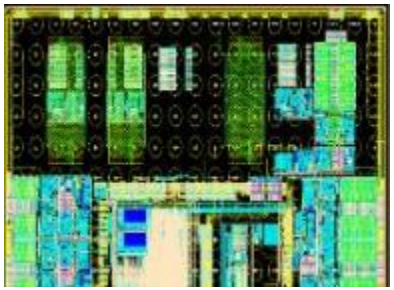




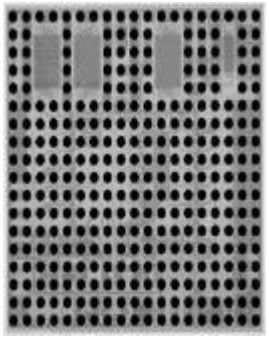
Conventional Type3 Voltage Mode Multiphase

1st Generation onDie Magnetic Inductor WLCSP circa 2016 Output stage .13uBCD

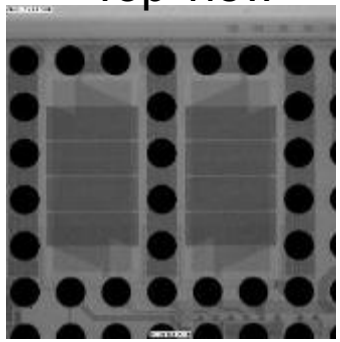
- *2 Driver/Inductor stages - side by side to test coupling*
  - *Substrate coupling*
  - *Cross coupling*
- *Outcome very little interference.*



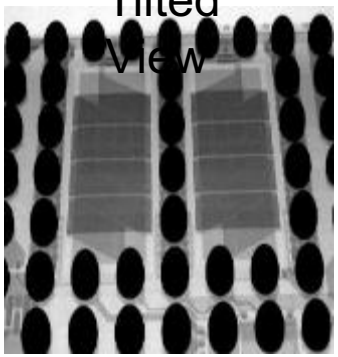
Overview (Balls Pitch .4MM)



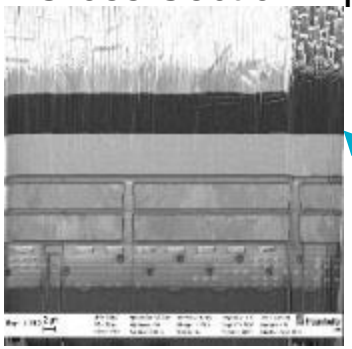
Top view



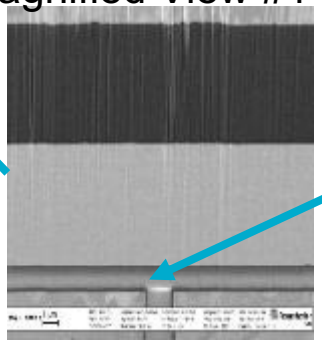
Tilted View



SEM Cross Section



Magnified View #1



Magnified View #2

1.5V->1V 1-Phase 30Mhz @500mA

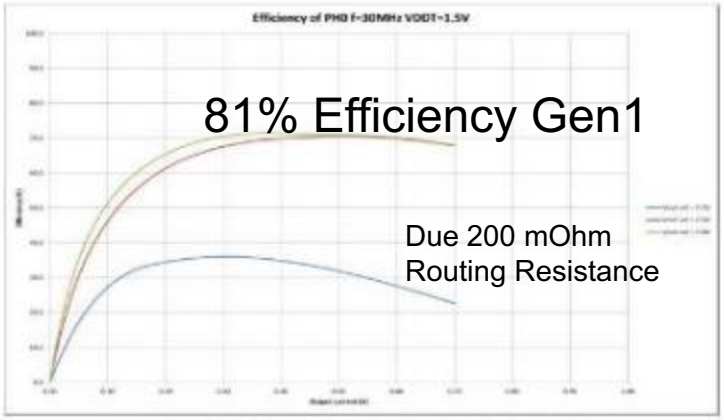


Figure 6: Efficiency of PH0, frequency 30MHz, VDDT 1.5V

Tesla - Industry 1st Integrated Inductors on a production VR Chip 10NH inductor (1MM x 1.5MM) circa 2016.

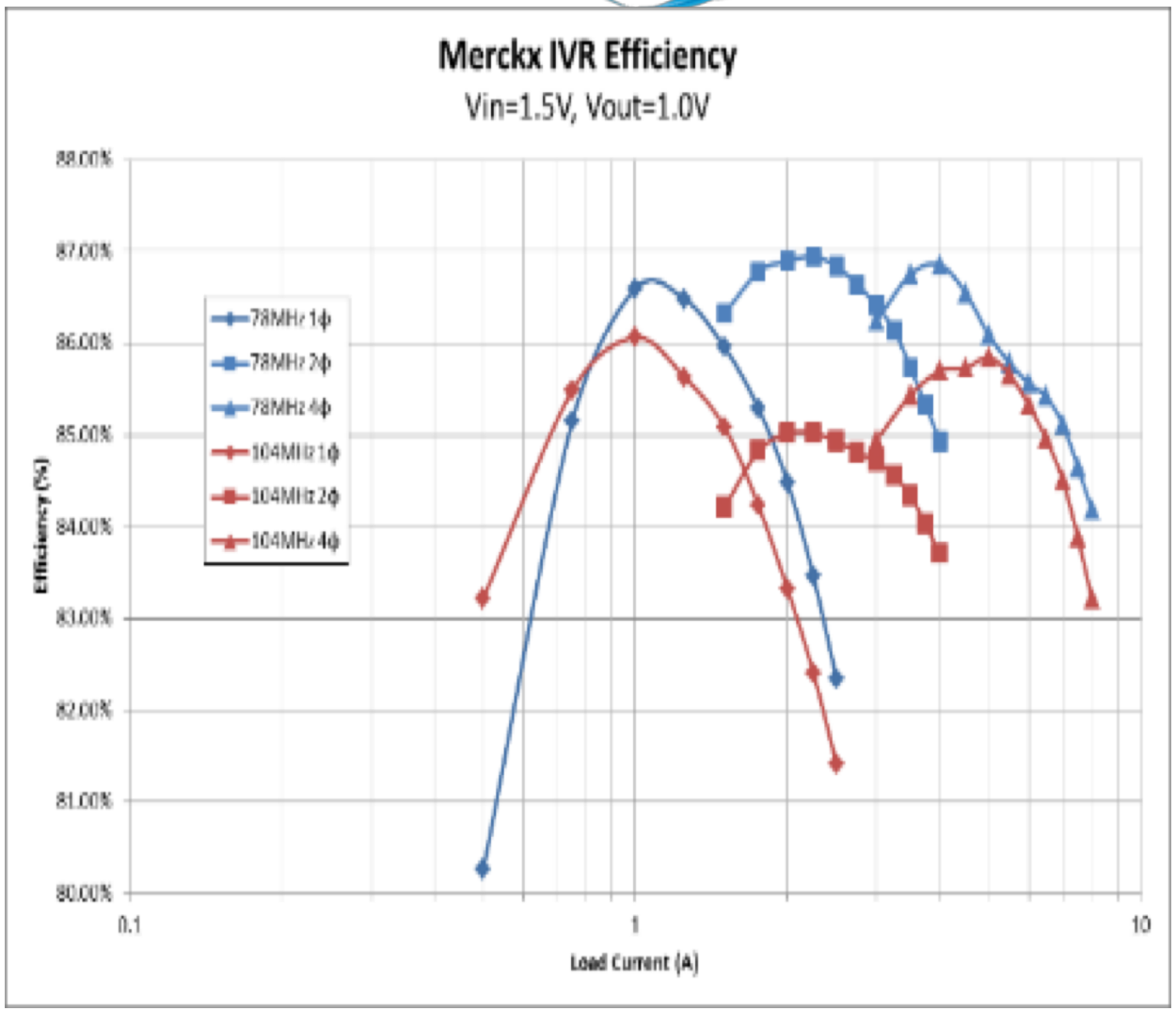
Results: Merckx Measured efficiency

Simplified efficiency analysis

- $P_{loss}(DC) = I^2R = 2^2 * (21m\Omega + 10m\Omega) = 124mW$
- $P_{loss}(AC) = \sim 50mW$ (taken from muRata data
- $P_{loss}(total) = \sim 174mW$
- Overall Efficiency Estimate:

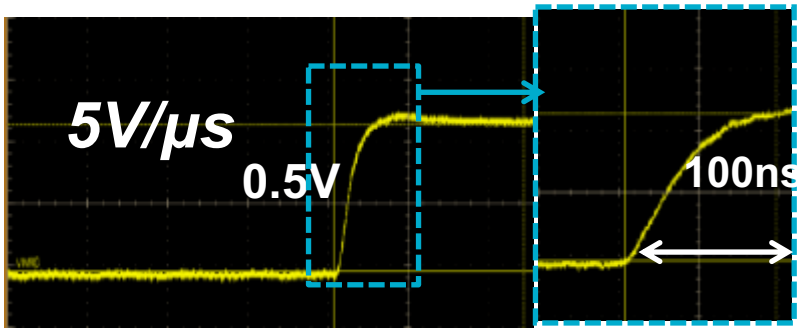
$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$
$$= \frac{P_{out}}{P_{out} + (P_{Loss\_L} + P_{Loss\_SW})}$$
$$= \frac{2W}{2W + 174mW + 89mW} = 88.4\%$$

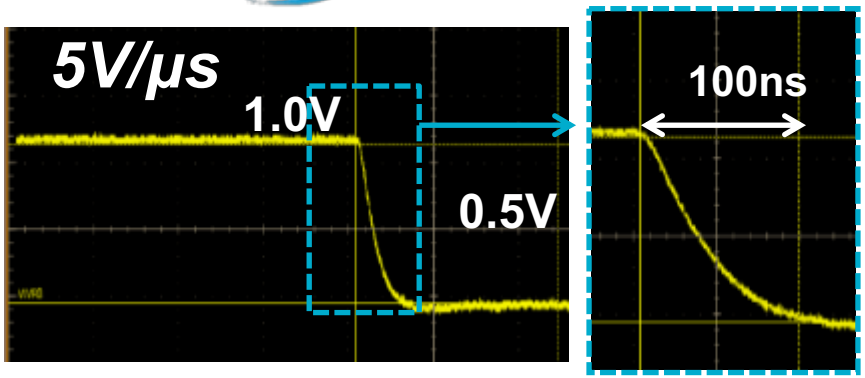
- 89mW switching losses is in line with our efficiency simulations.
- *Key to high efficiency is a low loss inductor.*



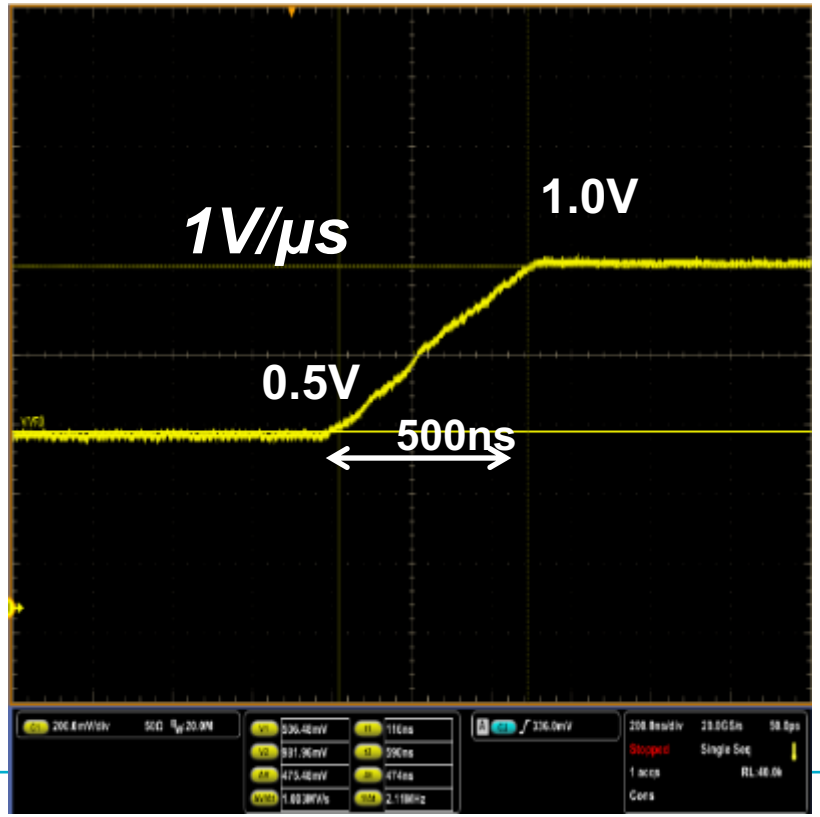
Results: Fast DVS Rise/Fall

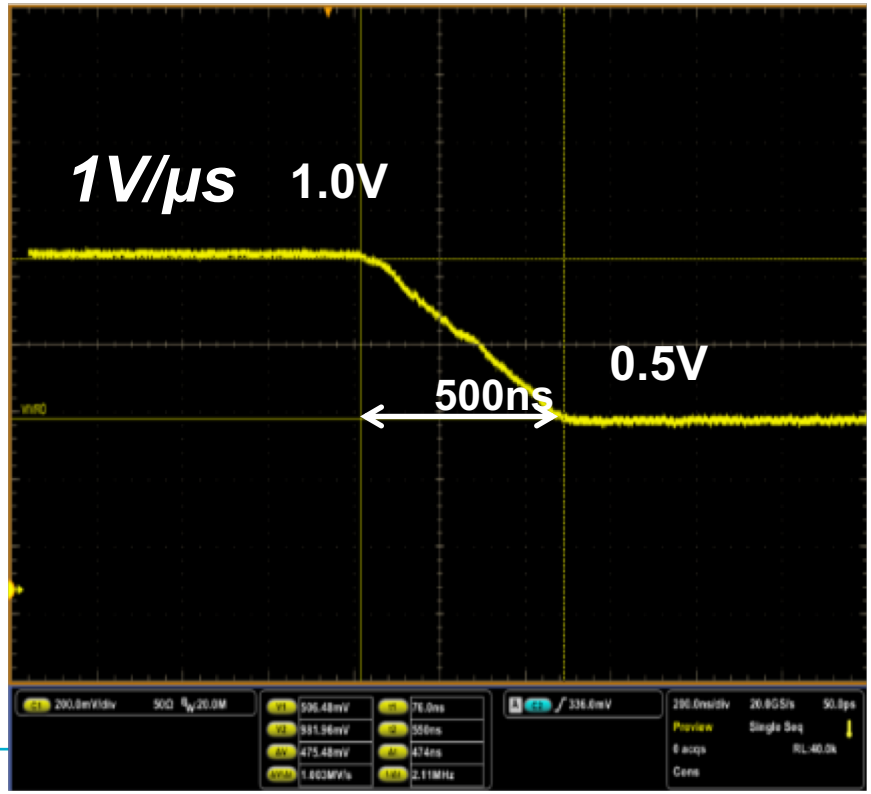
VDAC Step Response
0.5V → 1.0V
1.0V →0.5V
4ϕ, 4A Load





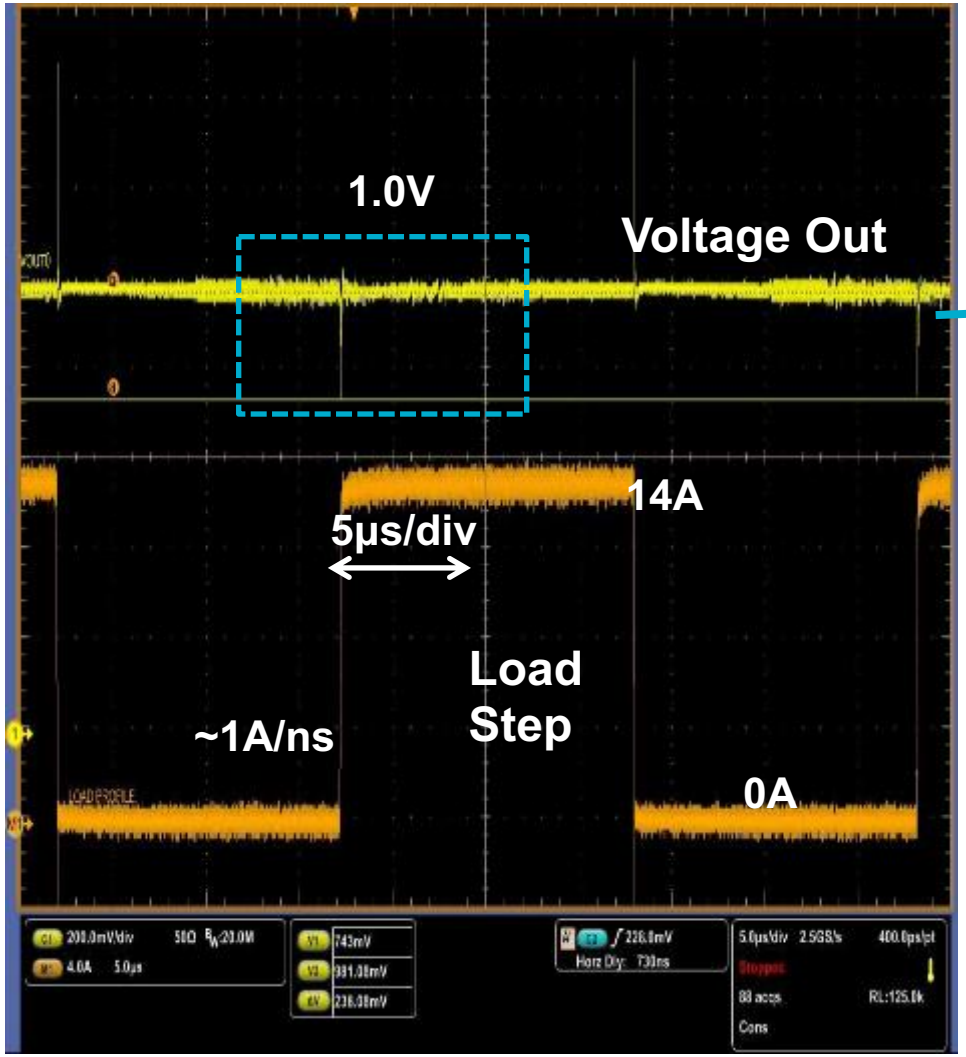
Controlled FDVS
0.5V → 1.0V
1.0V → 0.5V
4ϕ, 4A Load

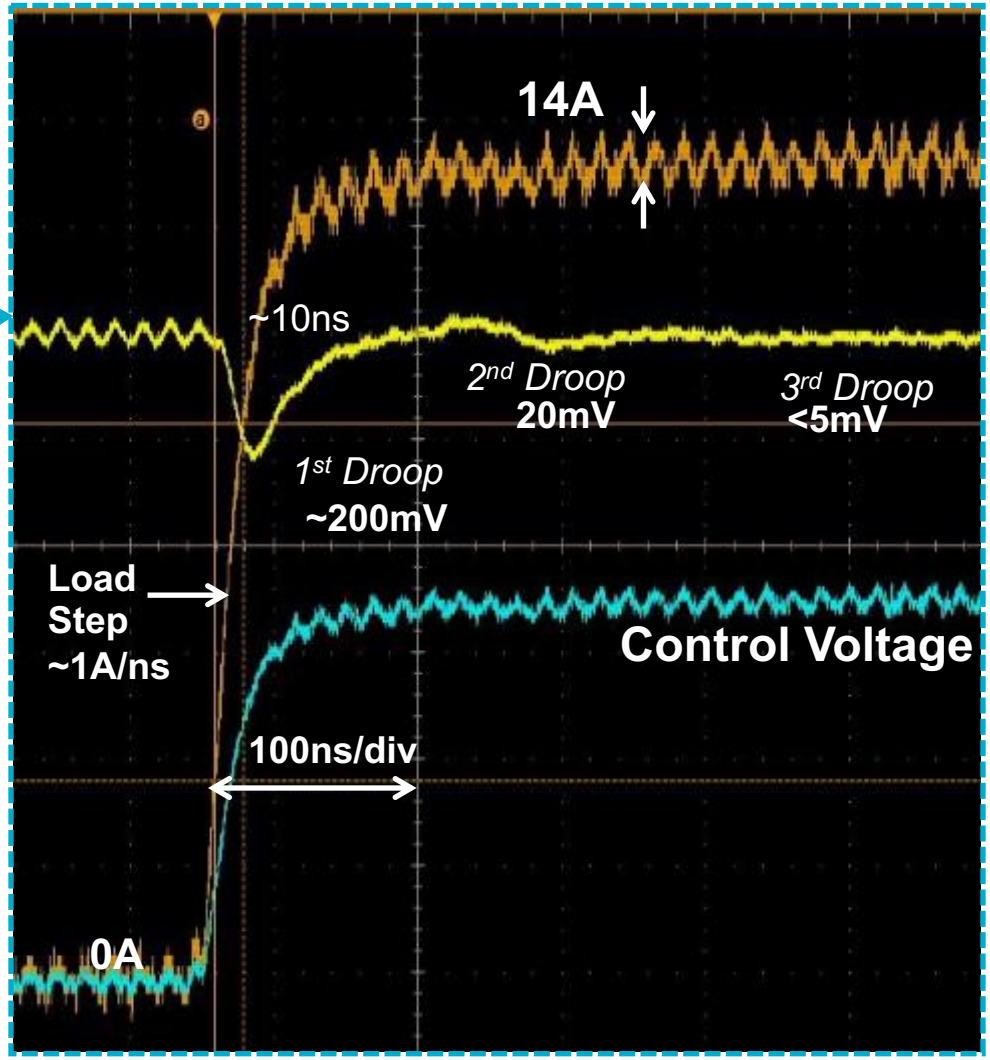




Results: Load Step/Transient Response

4ϕ, 0A → 14A, ~1A/ns





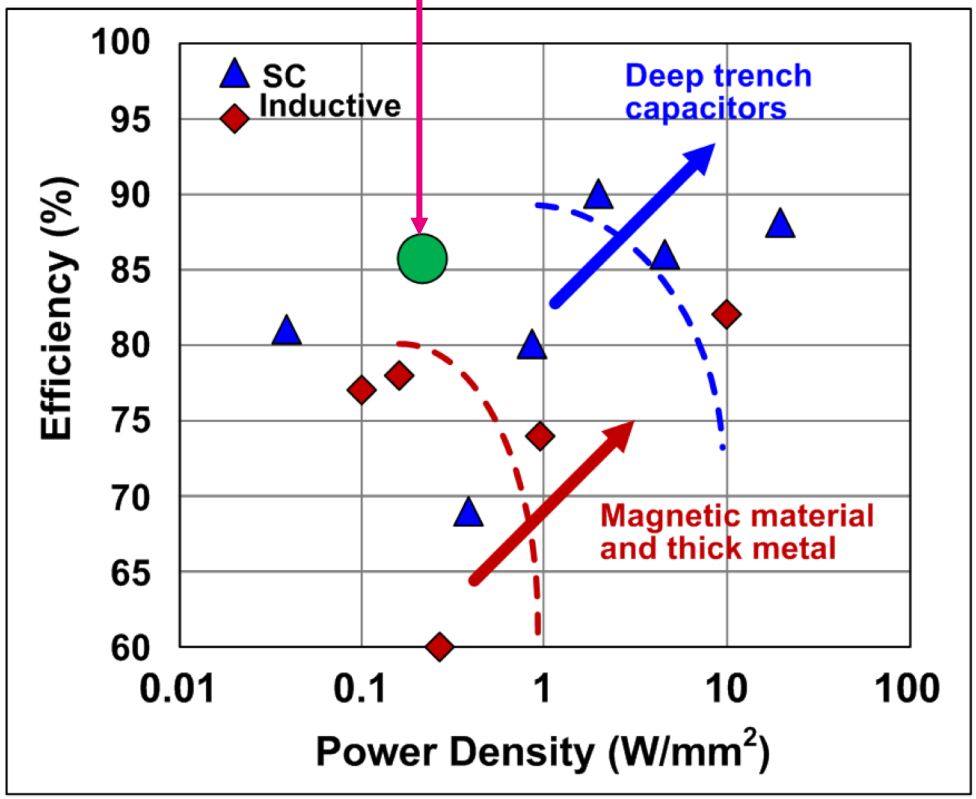
Summary of Achieved Results:

Merckx Results Achieved on 1st Silicon

Parameter	min	nom	max	Unit	Comments
Input Voltage	1.35	1.5	1.65	V	
Output Voltage Range	0.4		1.1	V	
Output Voltage Resolution		2.35		mV	VDAC LSB
Frequency Range	52	78	104	MHz	higher and lower frequencies are possible
Load Current Range	0.5		8	A	higher and lower possible at reduced efficiency
Efficiency @78MHz		87		%	Peak efficiency @ 1A, 2A, 4A
Efficiency @104MHz		86		%	Peak efficiency @ 1A, 2A, 4A
FDVS (Fast Dynamic Voltage Scaling)			5	V/µs	4ϕ, 4A Load
Closed Loop Bandwidth		10		MHz	Estimated from transient response
Line Regulation		6.6		mV/V	4ϕ, 4A Load, Vout=0.75V, Vin=1.35V-1.65V
Load Regulation		0.27		mV/A	4ϕ, Vout=0.75V, Vin=1.5V, Load=2A-8A

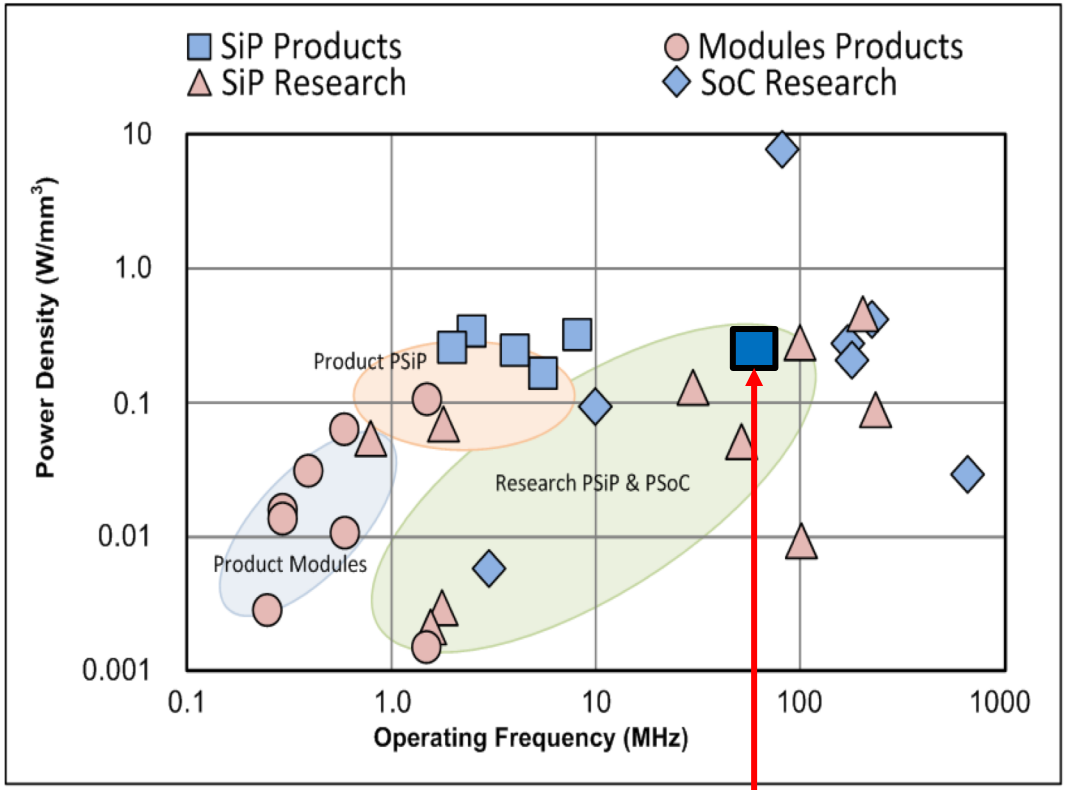
Merckx Power Density (.4 watt/mm^3) [1]

Merckx ~8 watts in **20MM3**



The Road to Fully Integrated DC–DC Conversion via the Switched-Capacitor Approach
Seth R. Sanders, *Fellow, IEEE*, Elad Alon, *Senior Member, IEEE*, Hanh-Phuc Le, *Student Member, IEEE*, Michael D. Seeman, *Member, IEEE*, Mervin John, and Vincent W. Ng, *Member, IEEE*

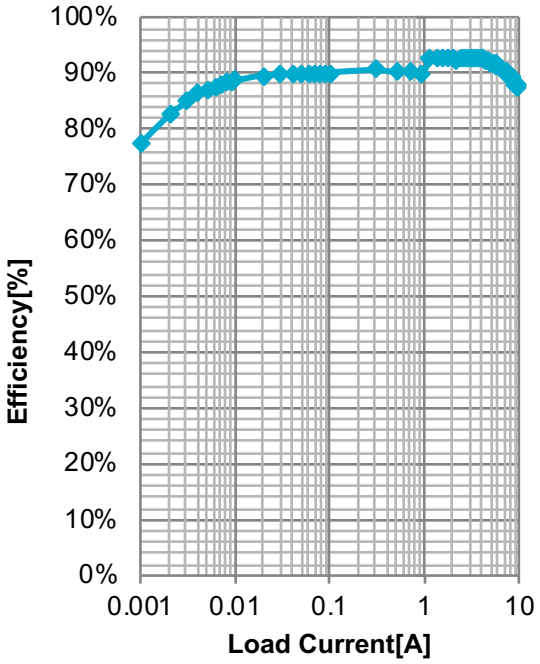
Review of Integrated Magnetics for Power Supply on Chip (PwrSoC) Cian ´O Math ´una, Senior Member, IEEE, Ningning Wang, Santosh Kulkarni IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 11, NOVEMBER 2012 4799

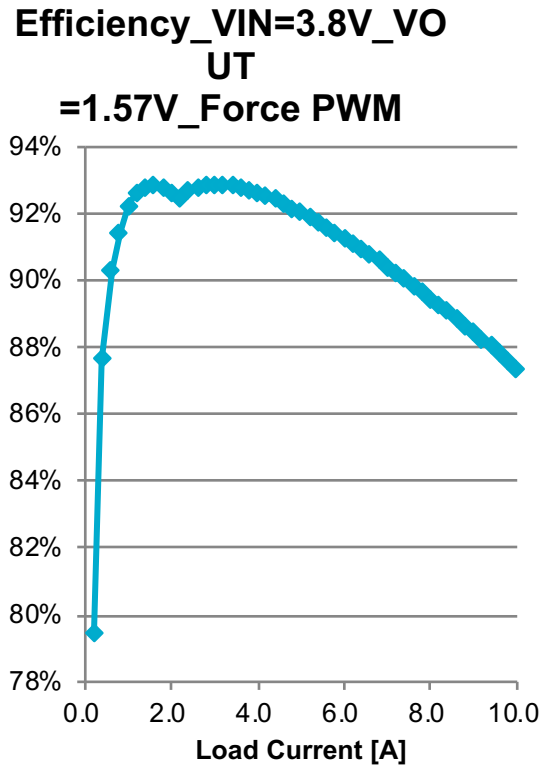


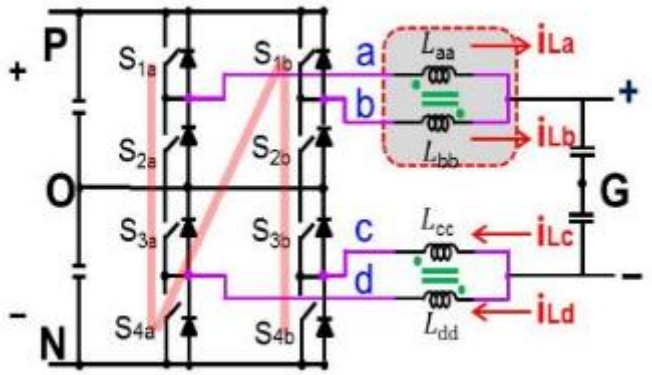
Merckx ~8 watts in **20MM3 (78Mhz)**

Dialog's Gen1 Stage 1 Juno+ Efficiency Results – Ongoing Development

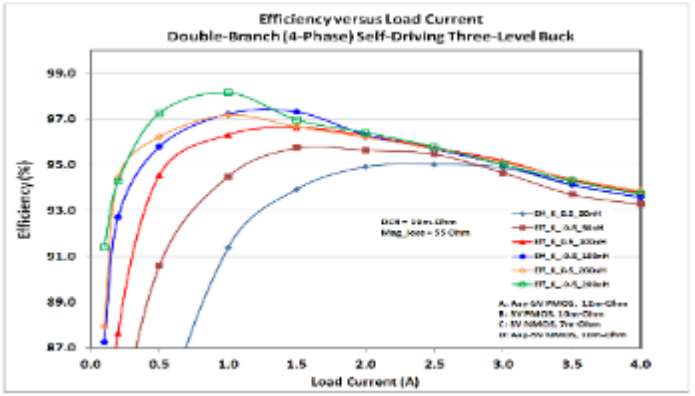
Available in production now ..see demo table







Alternate Stage 1 Architectures:
3 Level Coupled Buck [7,8, 9]

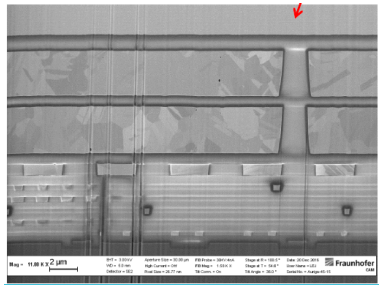


DA9214A available in High Volume Production today… 3 level development continuing goal to achieve > 95% efficiency + smaller inductor

https://www.dialog-semiconductor.com/sites/default/files/da9213-14-15_datasheet_2v2.pdf

DIALOG INTEGRATED BUCK ROADMAP

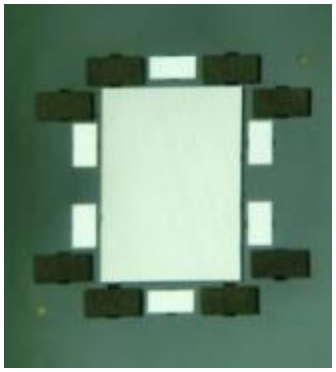
2016



TESLA

Technology demonstrator
Establish foundations
Develop models
Build knowledge

2018



MERCKX

Prototype Product
Functional regulator
Product quality IP
Full performance

Max. current- 8A
Peak eff.- 87%
Freq- 50-100MHz

2019

MERCKX2

First Product
Fully featured IP
Integrated 1st stage
Improved performance

Max. current- 8A
Freq- 50-100MHz

2019

INTEGRATED MAGNETICS

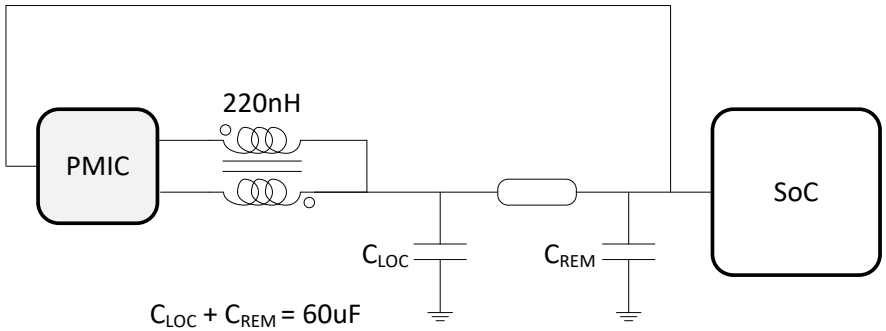
First Products
Standalone DCDC
Dialog standard IP
Ready for integration into ASIC PMU

Conclusion:

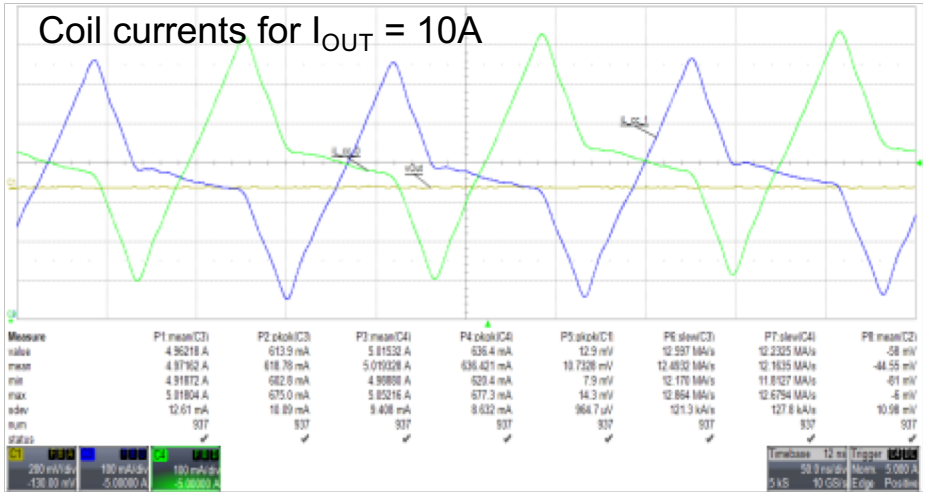
- Significant progress being made in realizing PWRsoc in commercial production based on new available discrete components and improvement in IC process devices and architectures.
- A IVR SIP developed and tested for stage 2 in a .13uBCD process which is very competitive in performance, price, system area (PPAC) with alternative packaging methods proposed.
- Multiple methods of including IVR solutions including co package stage 1 and stage 2 approach (same process) proposed with significant advantages over a single stage approach simulated and in development (ref Roadmap).
- Demo available for further discussions with interested potential customers.

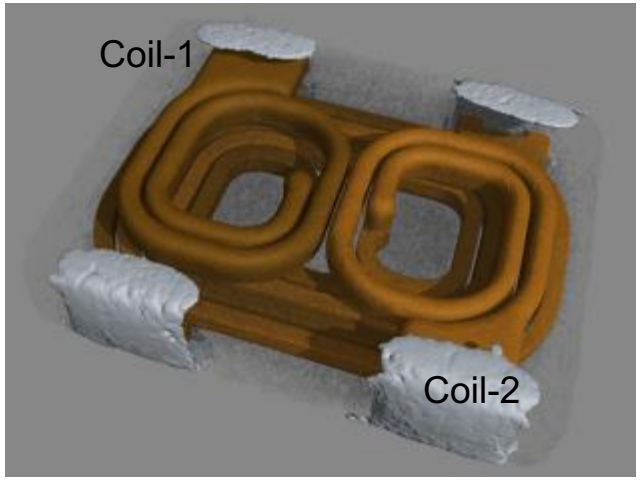
Other Options -15A buck for SoC in16.4mm^2

Stelvio is a prototype dual-phase buck converter with coupled-coils



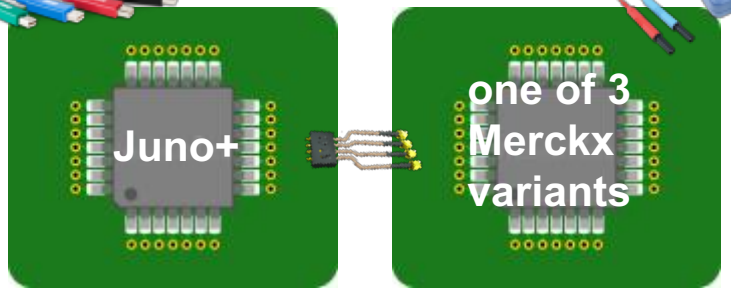
Parameter	Value
V_{IN}	2.3 - 4.9 V
V_{OUT}	0.5 – 1.2 V
Switching Frequency	6 - 9 MHz
Max I_{OUT} DC	15 A
Max I_{OUT} Pulsed	25 A for 25% duty cycle
Buck+BOM	16.4 mm^2





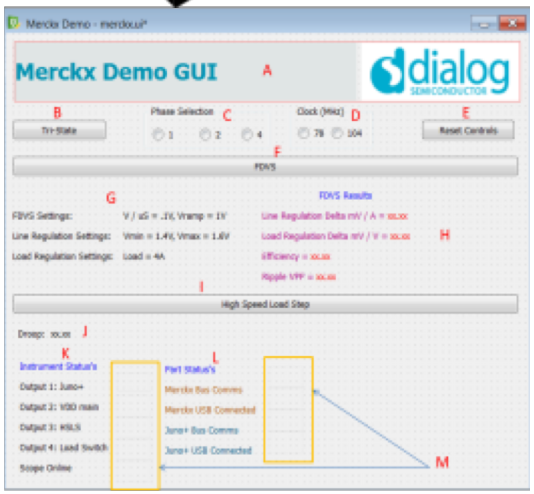
Merckx Demo Setup (see @ Dialog Demo Table)

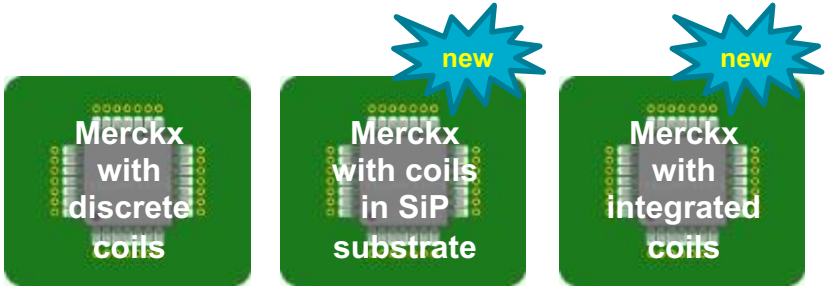
Configuration



Juno+ Demo PCB
(can be bypassed)

Merckx Eval PCB
with on-board Load Step
with on-board CLK source





- FDVS
- Vdroop
- Efficiency
- Ripple
- Line Reg
- Load Reg

Design challenges for realizing Integrated coils (Aircore vs Magnetics)

Basic defining Equations:

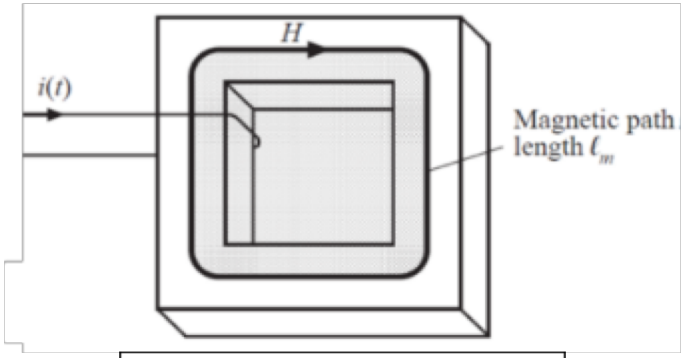
Energy stored/Volume= $2^{*}\frac{1}{2}B_{pk}H_{pk}$

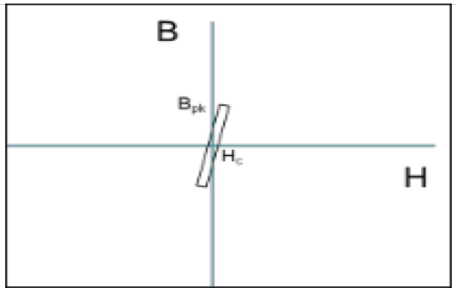
Using Ampere's Law, Energy/volume= $\mu\frac{N^2.I_{max}^2}{l_m}$

Core loss/volume- area inside the loop= $2 * B_{pk} * H_c$

Using Ampere's law, Core loss/vol = $2 * \frac{\mu.N.I_{max}}{l_m} * H_c$

Saturation current, $I_{sat} = \frac{B_{sat}.l_m}{\mu.N}$

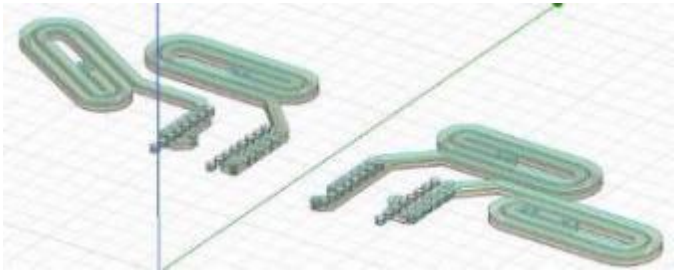




Integrated Coil takeaway-

- ***Silicon processing technology limited the volume of the magnetic core, copper deposited***
- ***Require smaller inductance to benefit for silicon processing which requires higher operating frequency***
- ***Use of thin film cores with higher μ, Isat suited for integrated coils, but also have higher losses***
- ***Design challenge for integrated coils- balancing μeff to achieve inductance, versus current handling & losses(Isat).***

Alternative to Integrated Magnetics -> On Die Aircore ~3nH Q~6 @ 100Mhz



Included on Merckx Gen2 in Fab

References

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[8] A Fully Integrated Battery-Connected Switched-Capacitor 4:1 Voltage Regulator with 70% Peak Efficiency Using Bottom-Plate Charge Recycling Tao Tong, Xuan Zhang, Wonyoung Kim, David Brooks, Gu-Yeon Wei School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, U.S.A E-mail: taotong@seas.harvard.edu

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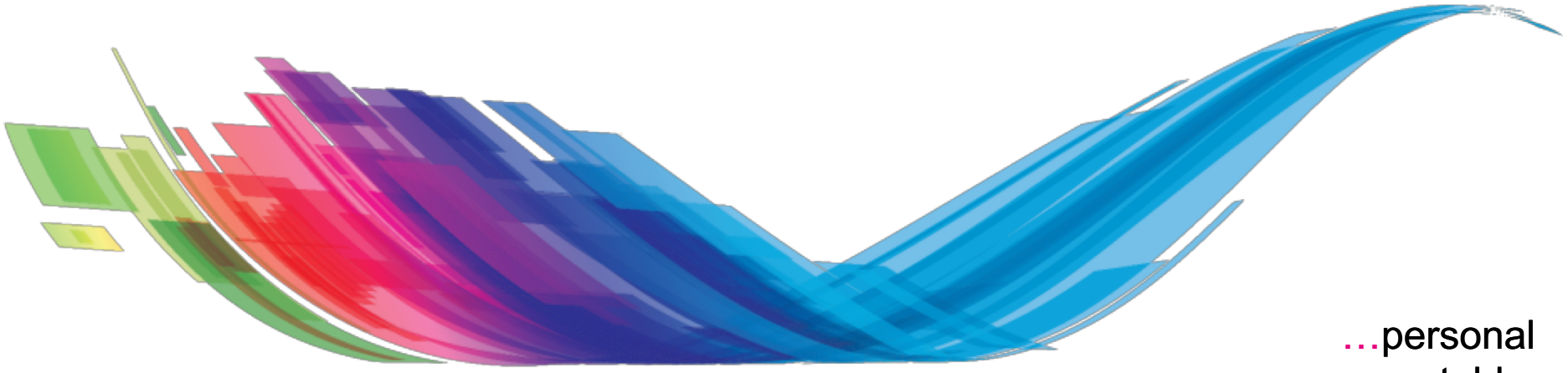

…personal
…portable
…connected