Using Time-Based Control Techniques for Active Rectification

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Introduction

- Achieving high efficiency very high frequency (VHF) is problematic.
- Diodes capable of handling high currents at VHF is sparse.
- To achieve **higher efficiencies** and **higher power densities** ways for implementing **active rectification** is necessary.
- Here we propose two solutions to active rectification:
  - **Phase Locked Loops (PLL)** control
  - **Delay Locked Loops (DLL)** control

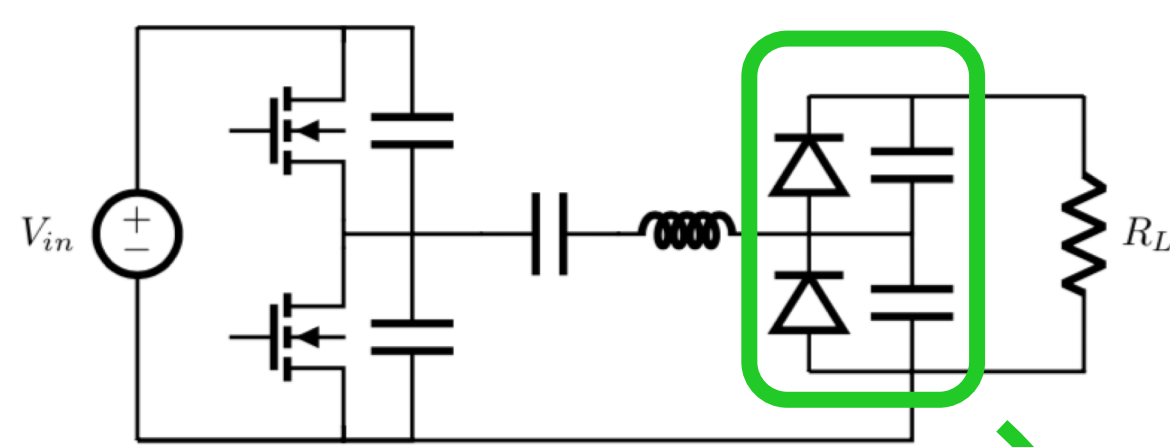|	Benefits	Challenges
PLL	• Stable Frequency generation • Wide bandwidth	• Locking time > 7-10 cycles. • Requires stability analysis
DLL	• Inherently stable • Operational after 1 cycle.	• High level of tuning and timing

Full Power Converter

Fig 1. Class DE Converter

Class DE Active Rectifier
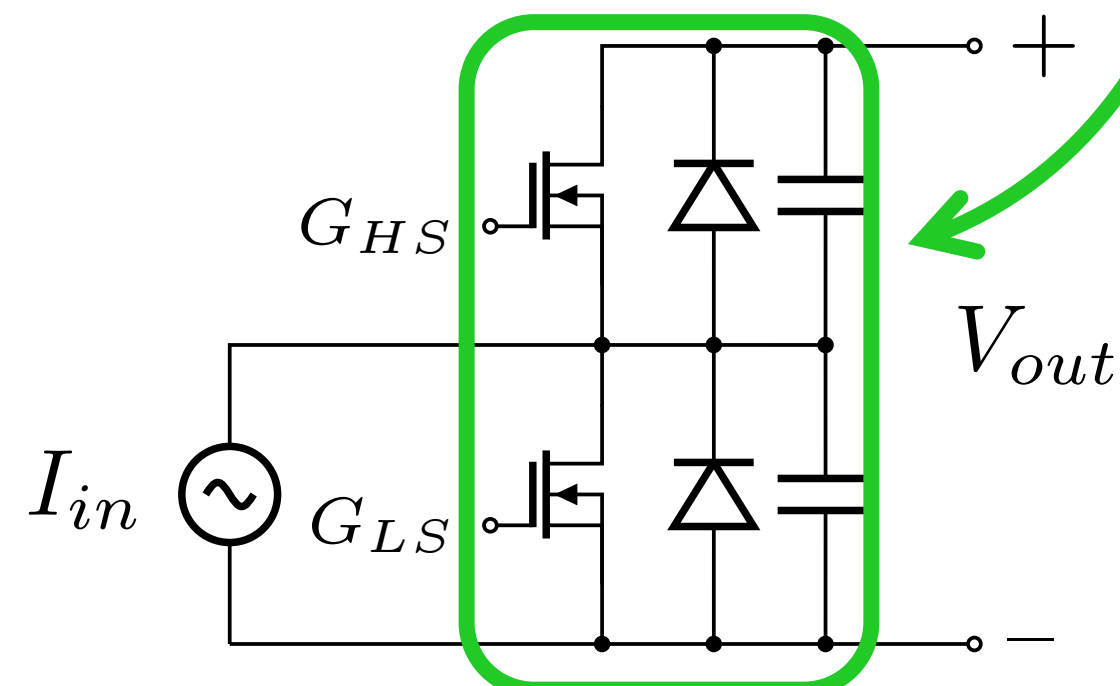
Example of an active rectification **Solution**

Fig 2. Class DE Rectifier
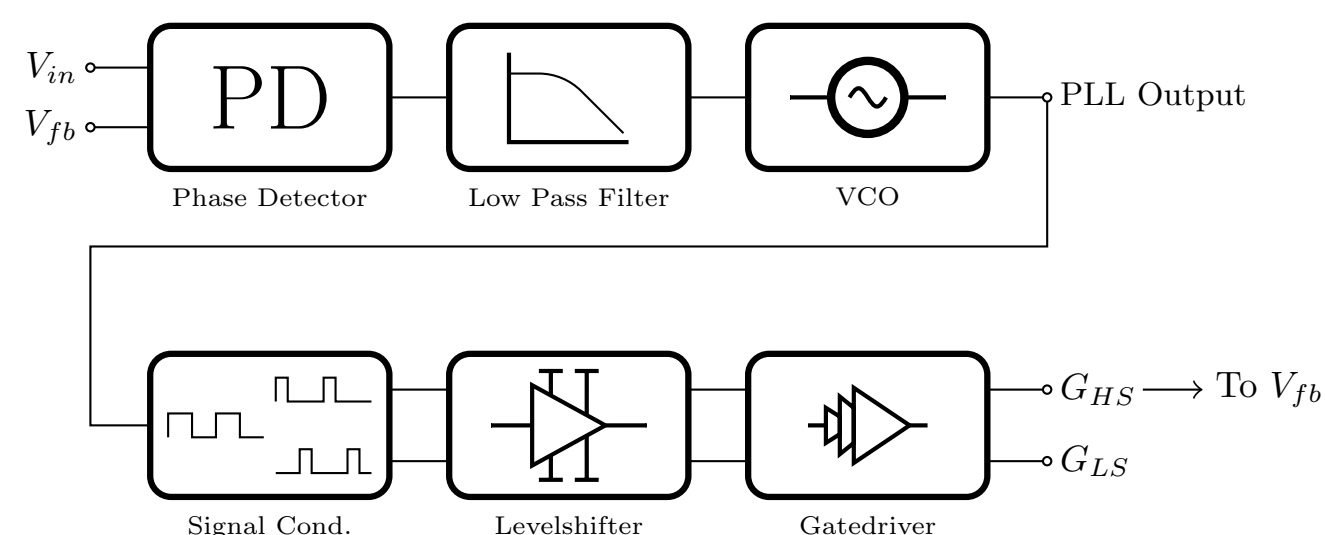
Active Rectification with Phase Locked Loop
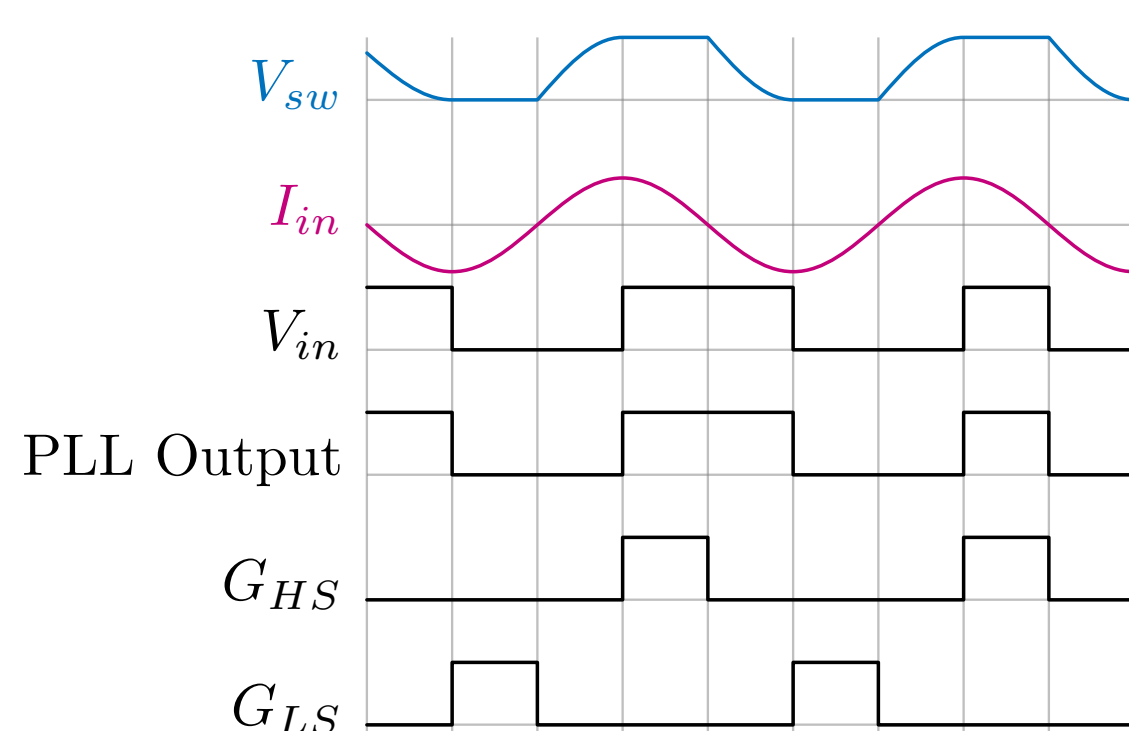

Fig 3. Active Rect. Using PLL concept

Fig 4. Waveforms when PLL is locked
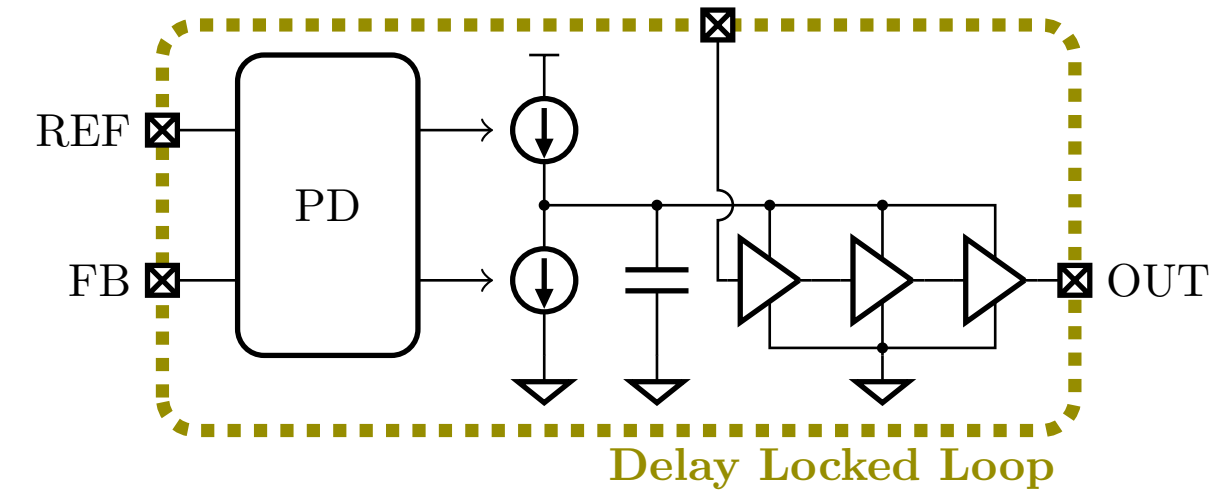
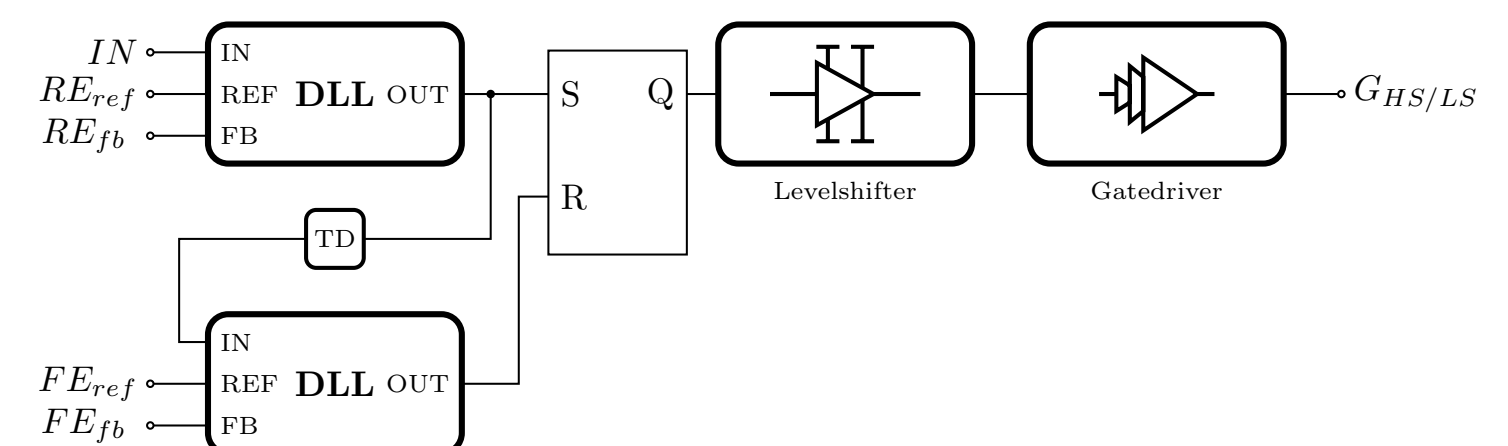## Active Rectification with Delay Locked Loop

Fig 5. Delay Locked Loop

Fig 6. Active Rect. Using DLL concept
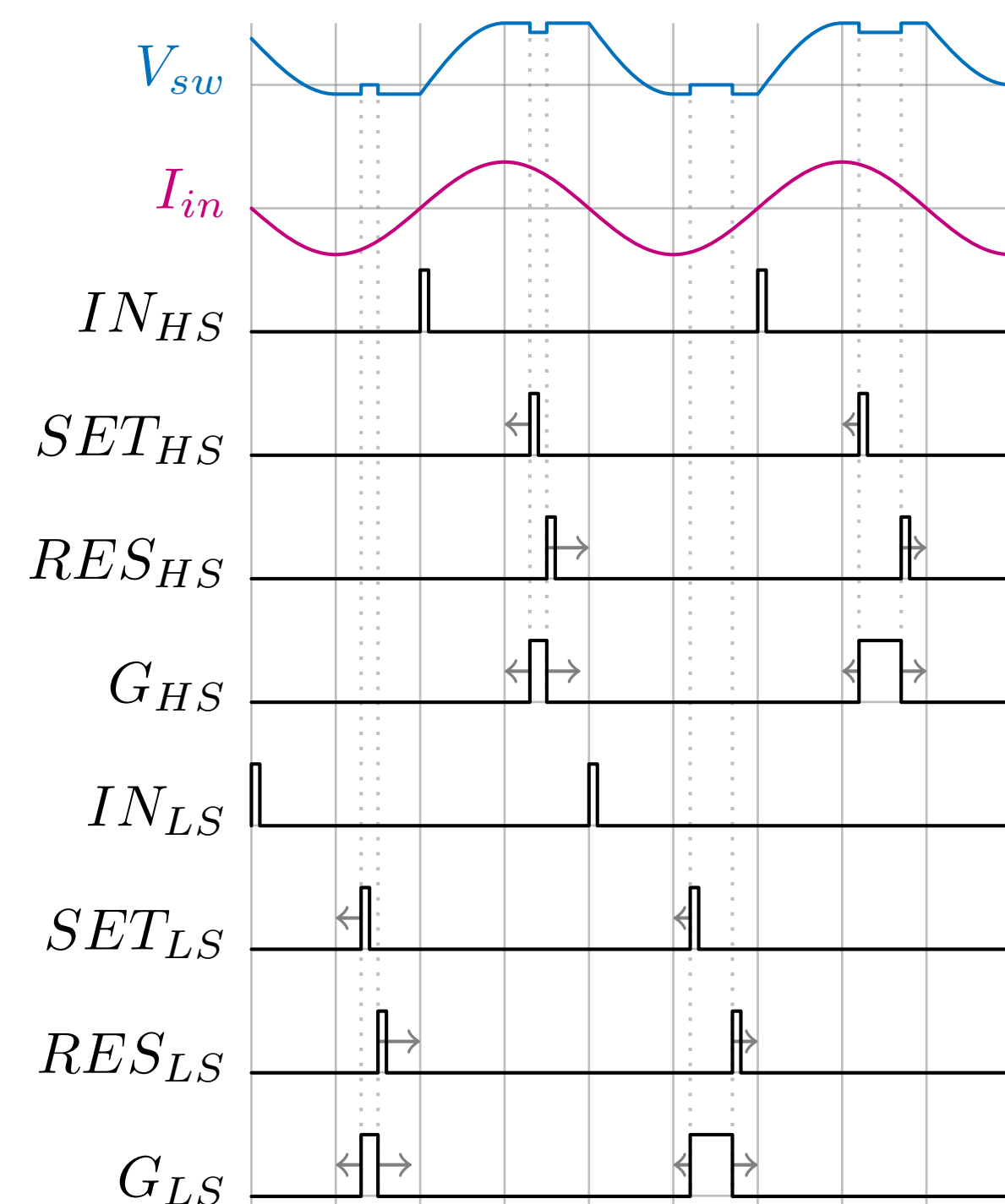

Fig 7. Waveforms when DLL is operational
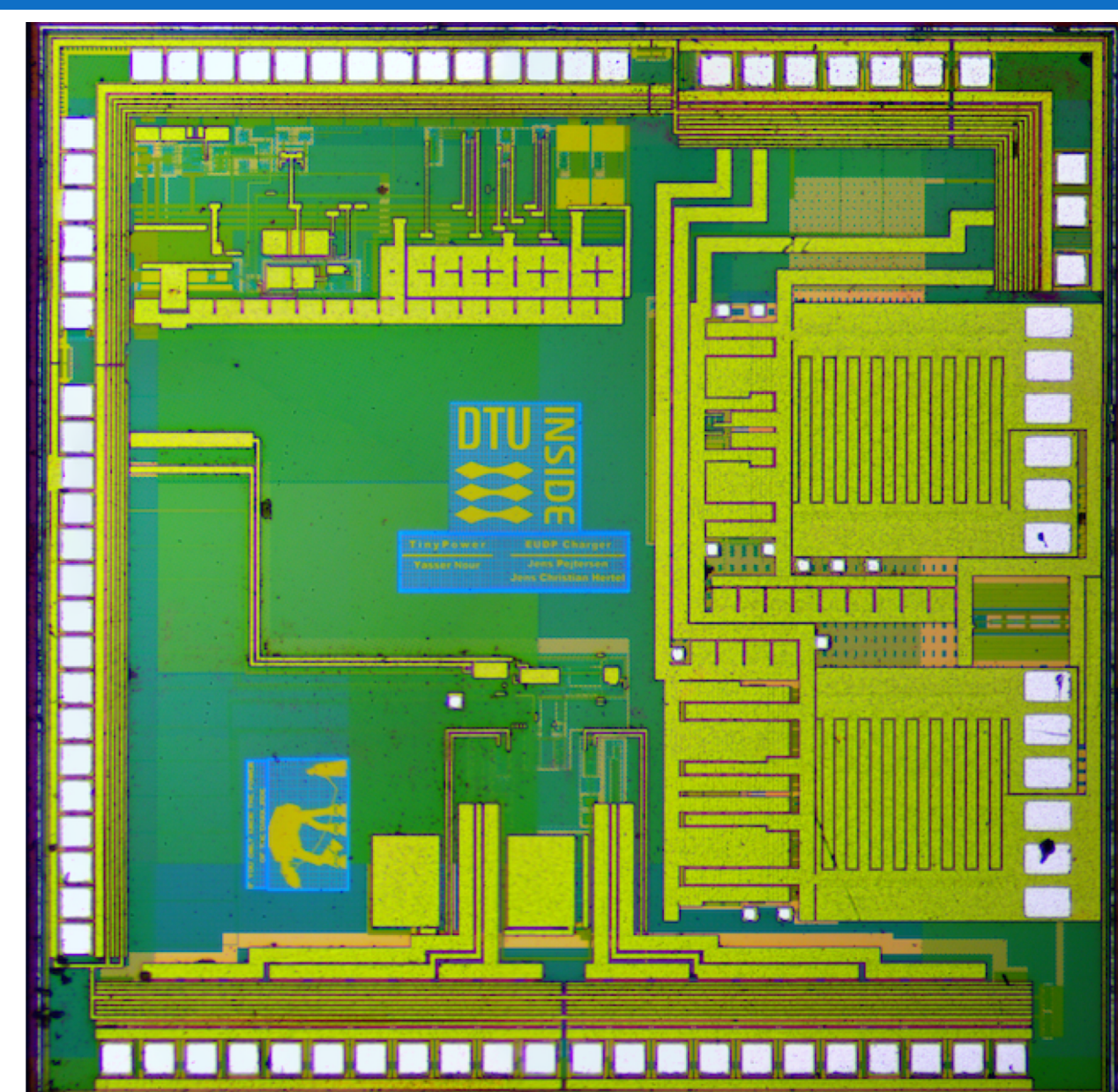
Implementation

Fig 8. Chip photograph

Key Contributions

- **Fully integrable** CMOS technology
- Eliminating need for **High Power Diodes in VHF**
- Ensuring **Soft Switching** of rectifying FETs

Acknowledgement