Spike Noise Cancelling Circuit for Switched Capacitor DC-DC Converter Mounting MLCCs on CMOS die

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INTRODUCTION

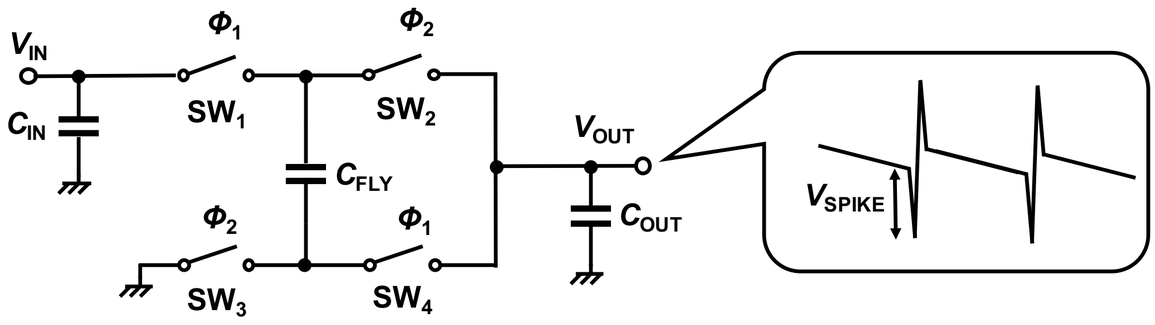


Fig.1 Circuit schematic of 1/2 SC DC-DC converter and definition of spike noise voltage (V_{SPIKE}).

- In the previous work [1], the switched capacitor (SC) DC-DC converter mounting four 100-nF 0402 (0.4mm x 0.2mm x 0.2mm) multilayer ceramic chip capacitors (MLCCs) on 180-nm CMOS die was presented for integrated voltage regulators and achieved the efficiency of 92.9% at the output power density of 62mW/mm^2.
- When the SC DC-DC converter is scaled down from 180-nm CMOS to 65-nm CMOS with the same MLCCs, the increase of the spike noise caused by the parasitic inductance of MLCCs is observed due to the increasing di/dt of power transistors.

PROPOSED CIRCUIT

- To solve the problem, a new spike noise cancelling circuit, where each power transistor is divided into two transistors with large and small gate width in parallel and the switching timing of the small transistor is delayed than the large transistor, is proposed

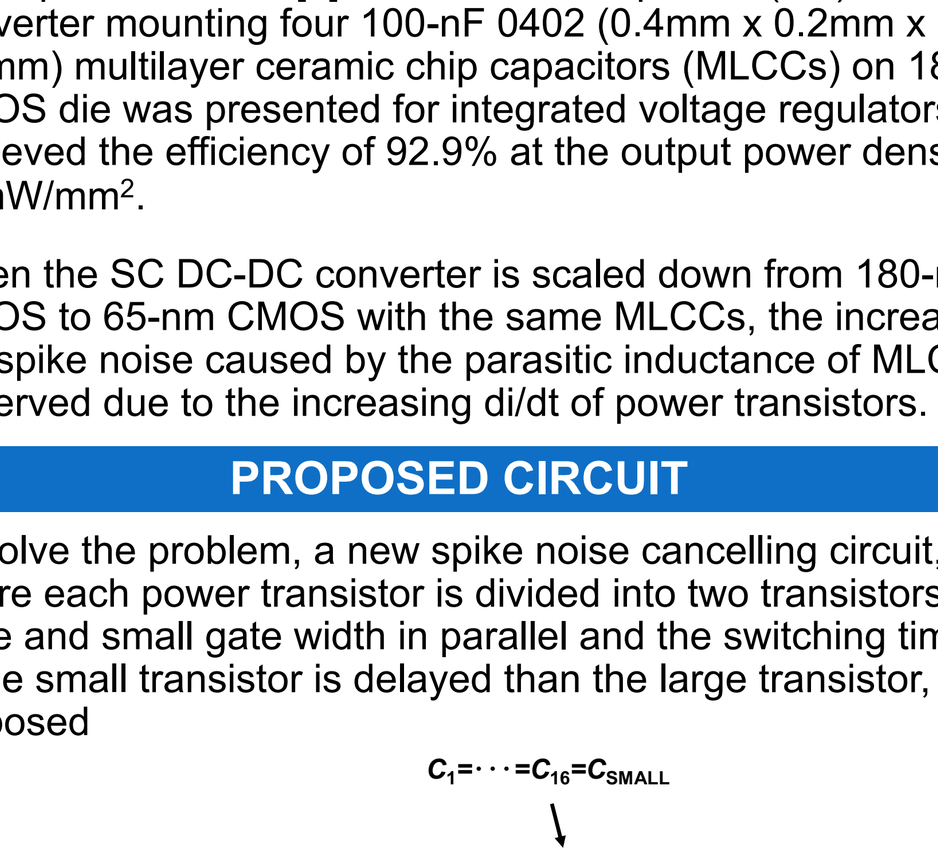


Fig.2 Implementation of SW_3 in Fig. 1. (a) Initial and (b) conventional design [2]. (c) Proposed spike noise cancelling circuit.

CONTRIBUTIONS

- The proposed spike noise cancelling circuit reduces the spike noise from 103mV to less than 10mV in the measurement of the 2-V input 1/2 SC DC-DC converter in 65-nm CMOS.

SIMULATION RESULTS

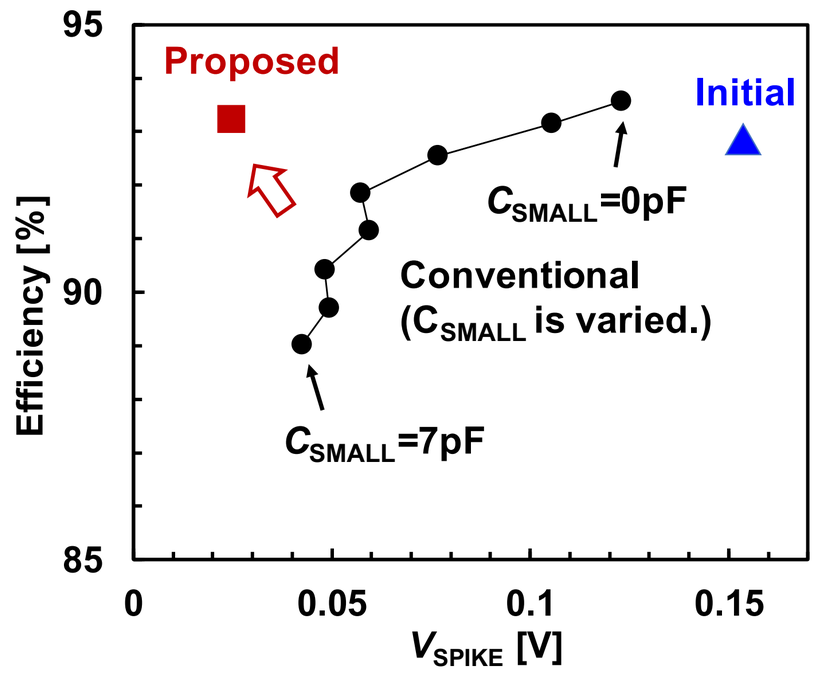


Fig.3 Simulated efficiency vs. V_{SPIKE} of different converter mounting converters in Fig. 2.

- Fig. 3 show the SPICE-simulated efficiency vs. V_{SPIKE} of the different SC DC-DC converters in Fig. 2.

EXPERIMENTAL REULTS

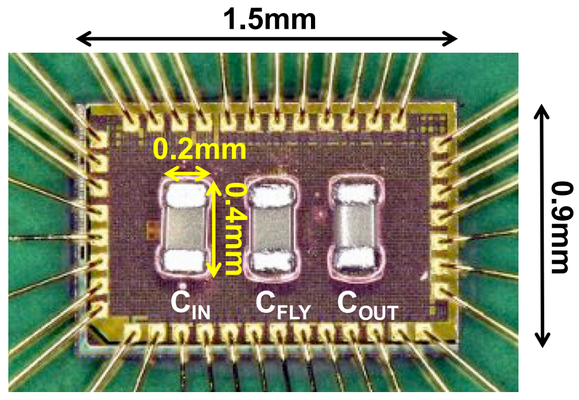
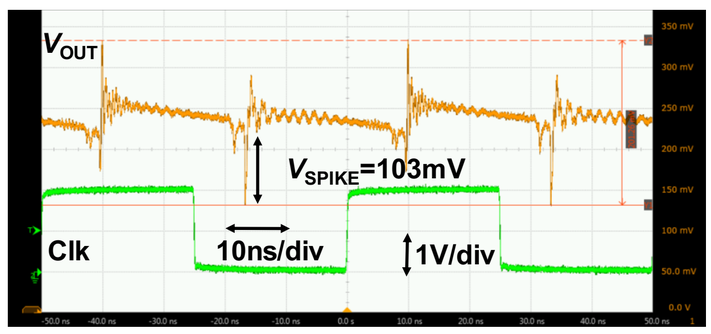
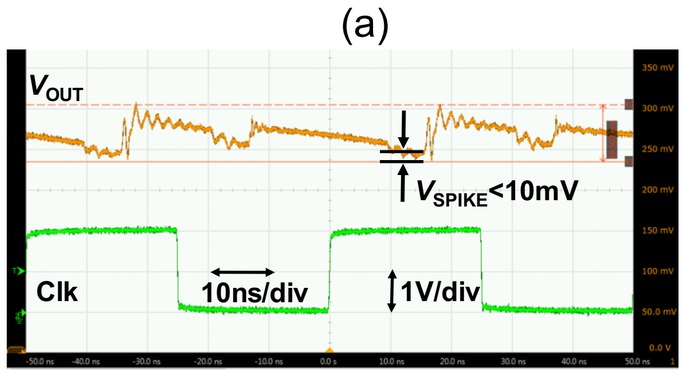


Fig.4 Fabricated 2-V input 1/2 SC DC-DC converter mounting three 100-nF 0402 MLCCs on 65-nm CMOS.



(a)



(b)

Fig.5 Measured waveforms of SC DC-DC converter with initial design (Fig. 2 (a)) and proposed design (Fig. 2 (c)).

- Figs. 5 (a) and (b) show the measured waveforms of V_{OUT} and the 20-MHz clock signal of the 2-V input 1/2 SC DC-DC converters with the initial design (Fig. 2 (a)) and the proposed design (Fig. 2 (c)), respectively. The output current is 300mA.

REFERENCES

[1] T. Sai, Y. Yamauchi, H. Kando, T. Funaki, T. Sakurai, and M. Takamiya, “2/3 and 1/2 Reconfigurable Switched Capacitor DC-DC Converter with 92.9% Efficiency at 62mW/mm² Using Driver Amplitude Doubler,” IEEE Transactions on Circuits and Systems II: Express Briefs (Early Access).

[2] J. Liu, et al., “Slew-Rate Controlled Output Stages for Switching DC-DC Converters,” IEEE, ICICDT, pp. 1-4, 2011.