International Workshop on Power Supply On Chip (PwrSoC) 2016

Ring-Shaped Multiphase Switched-Capacitor DC-DC Converters

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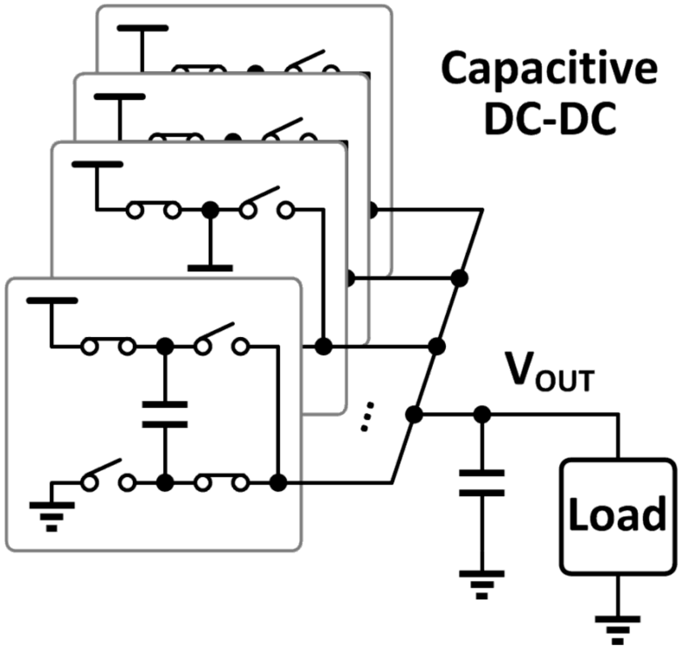
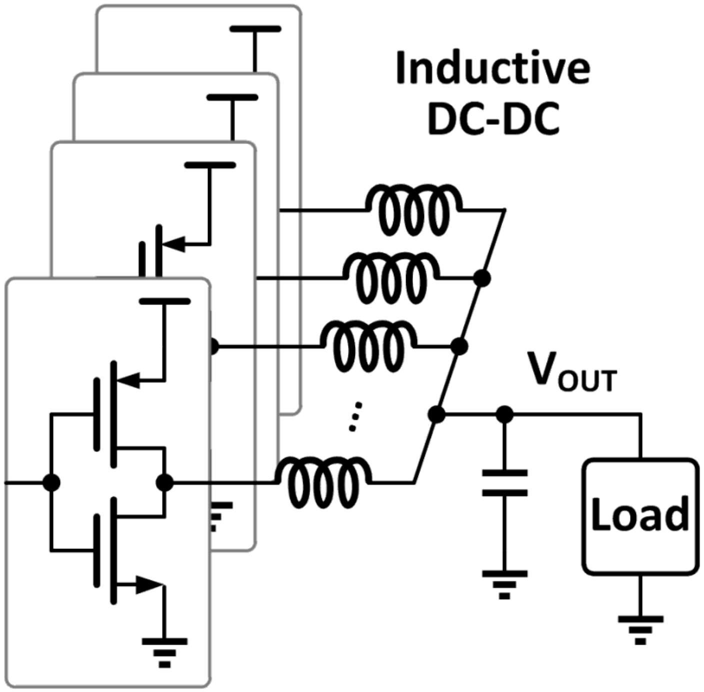
Outline

- Motivations of the DC-DC Converter-Ring
- Discussion on Unity Gain bandwidth Extension
- Layout-Oriented Converter-Ring Design
- Measurement Results
- Extended Possible Solutions
- Conclusions

Multi-Interleaving-Phase DC-DC Converters

- Reduce output voltage ripple
- Reduce input current ripple



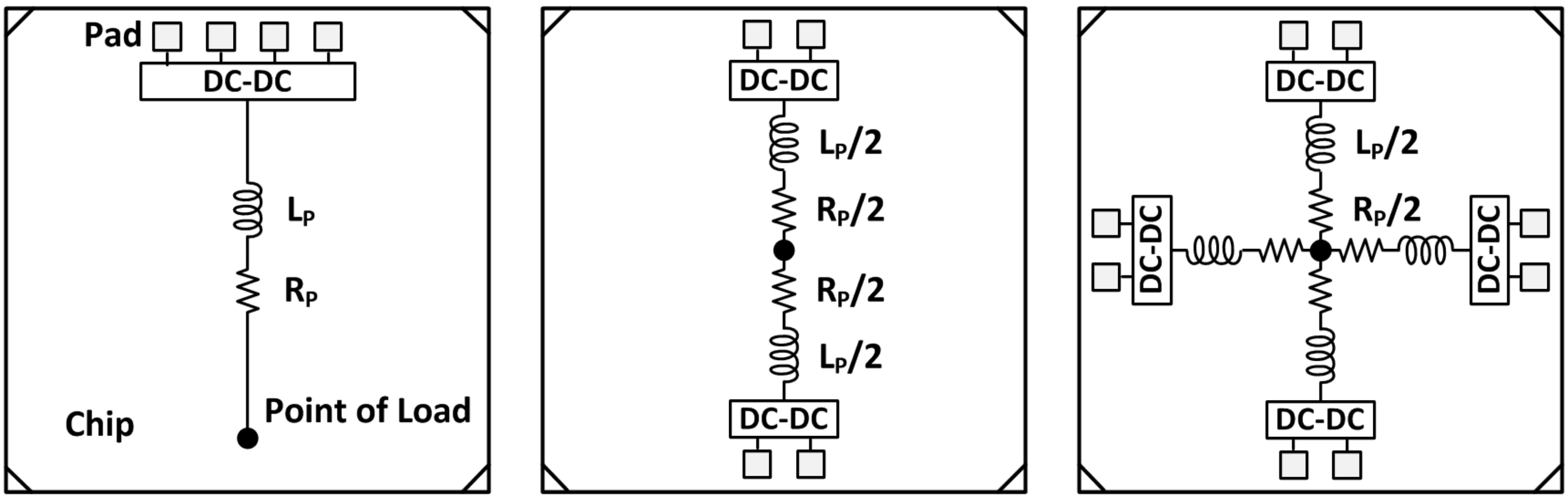


✓ Fully-on-chip, multi-phase
x Efficiency (like linear regulator)
✓ First-order power stage

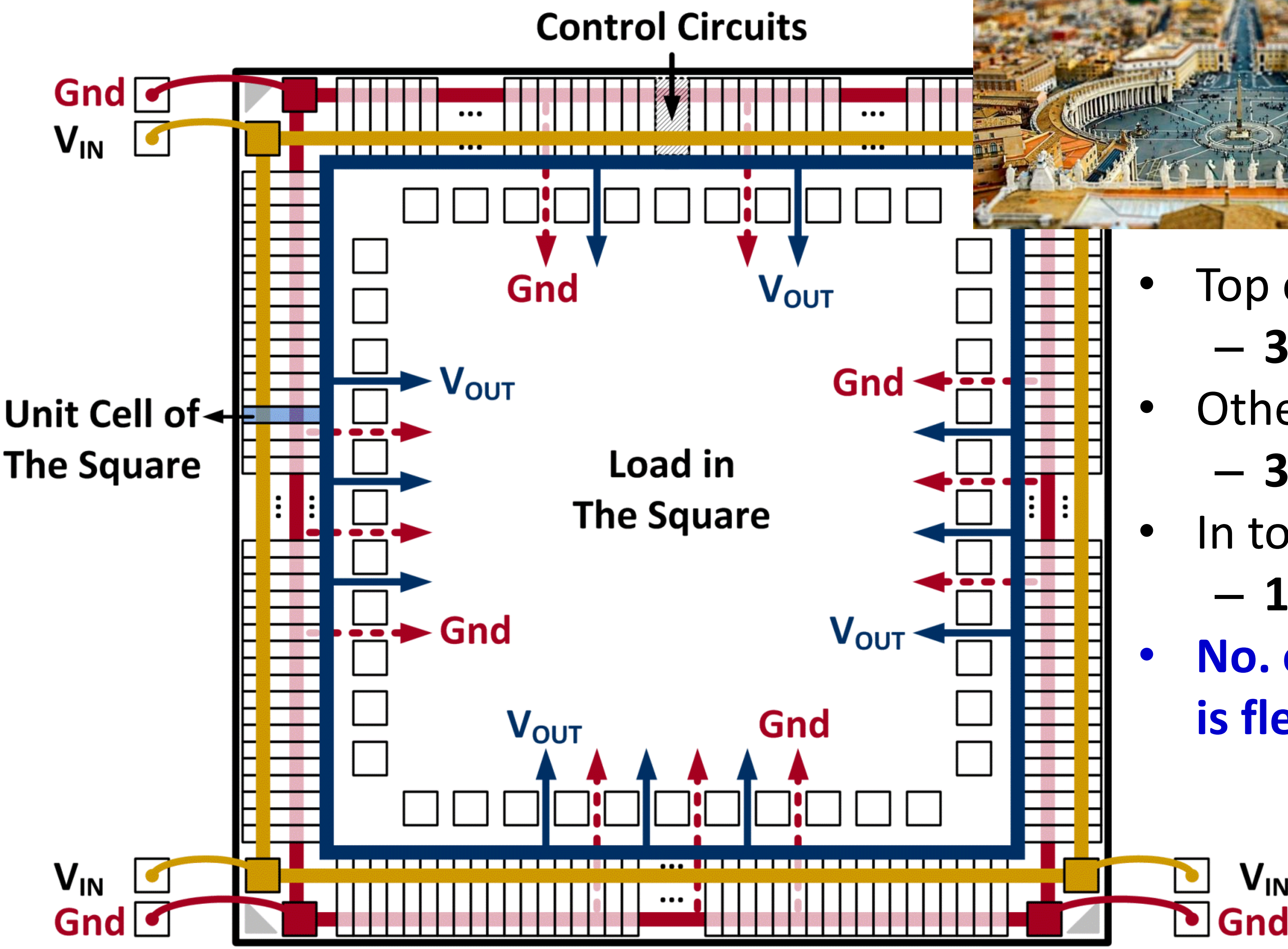
x One *L* for each phase
✓ Efficiency (ideally 100%)
– *LC* second-order filter

On-Chip IR Drops and d*I*/d*t* Variations

- On-chip power delivery suffers from IR drops and supply variations.
- Supplying the load from all directions can significantly alleviate such problem.

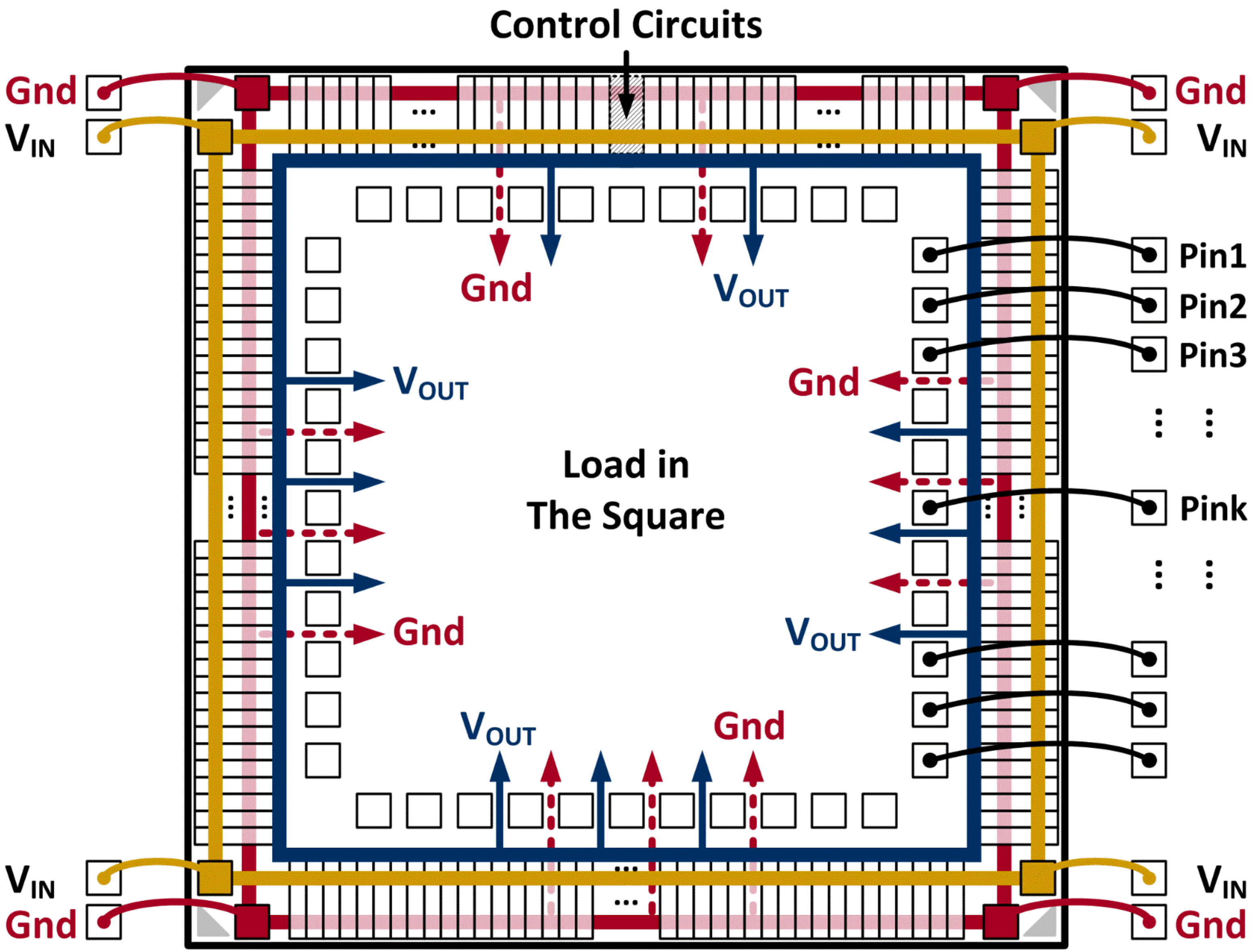


Conceptual Layout of the Converter-Ring



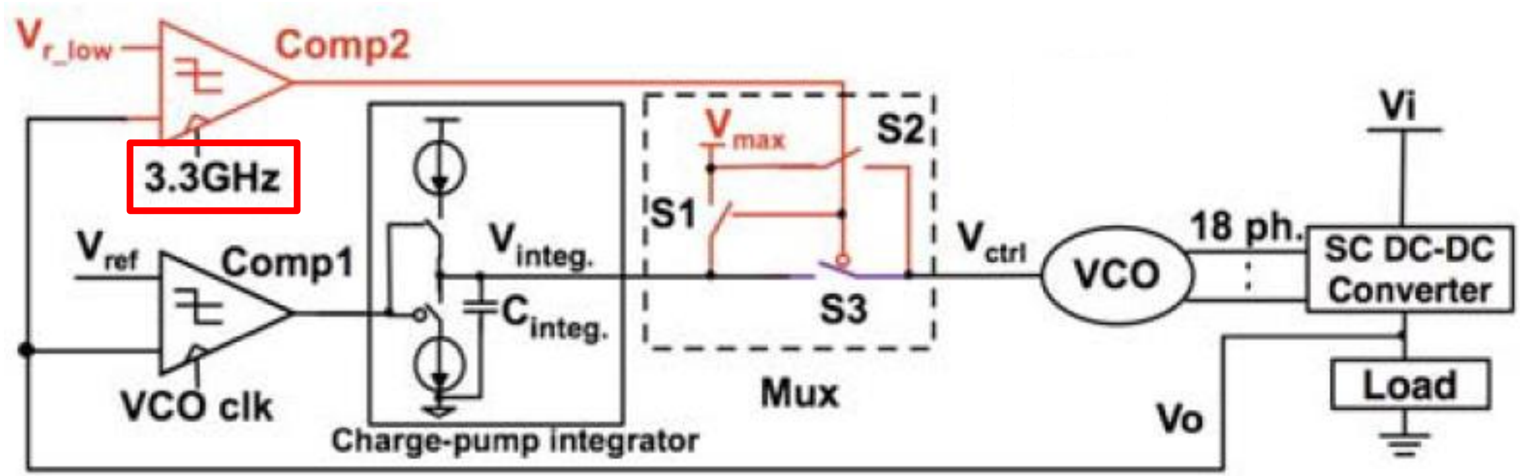
- Top edge:
  - **30** Phases
- Other 3 edges:
  - **31** Phases
- In total:
  - **123** Phases
- **No. of Phase is flexible.**

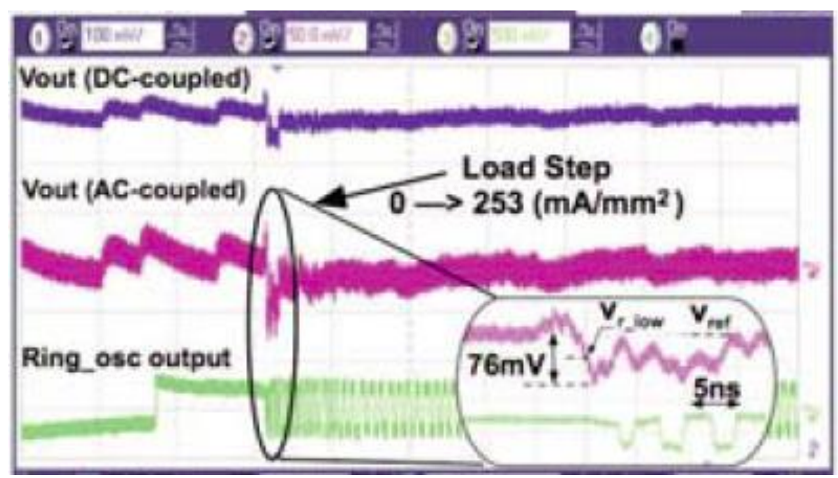
Conceptual Bonding Diagram



Prior Art Achieving Fast Transient

- Achieved fast transient response with additional 3.3GHz Clock.

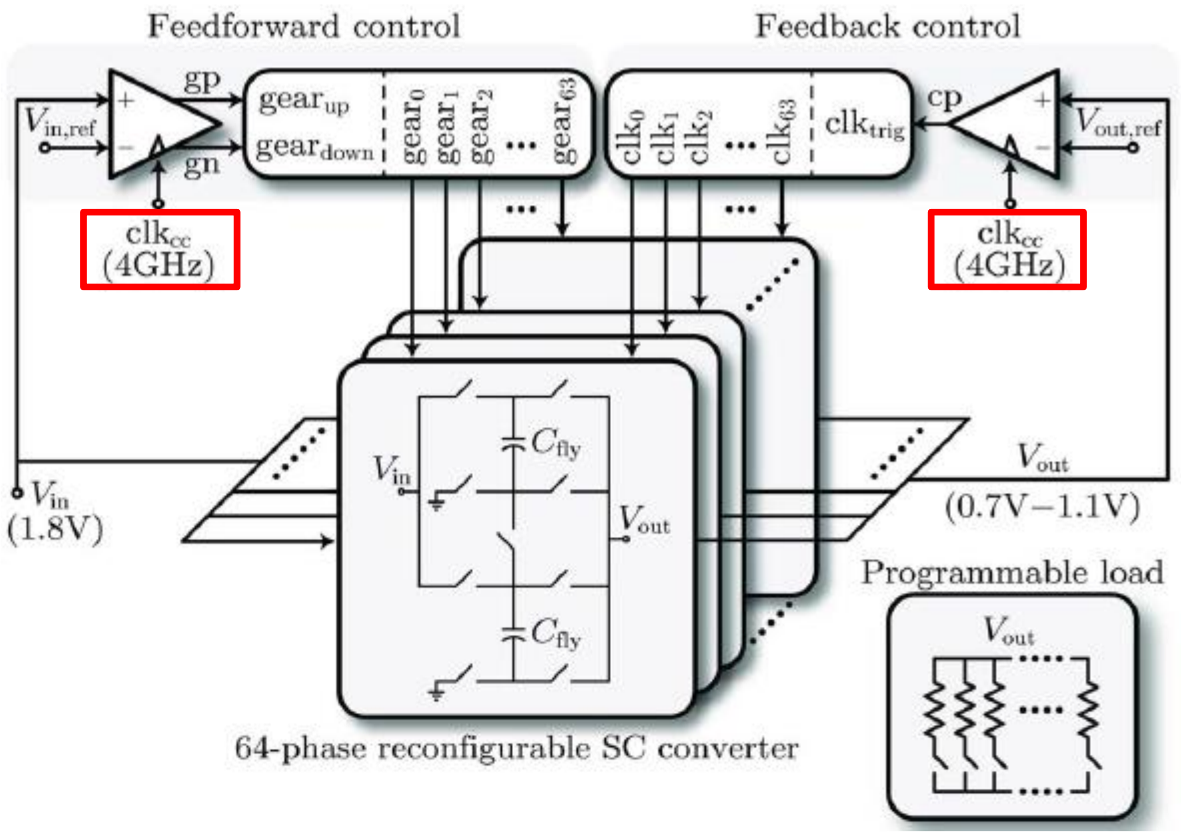


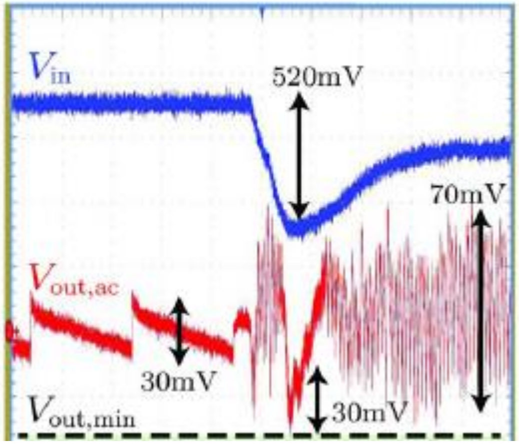


H.-P. Le, et al., ISSCC, 2013

Prior Art Achieving Fast Transient

- Achieved fast transient response with 4GHz Clock and feedforward control.

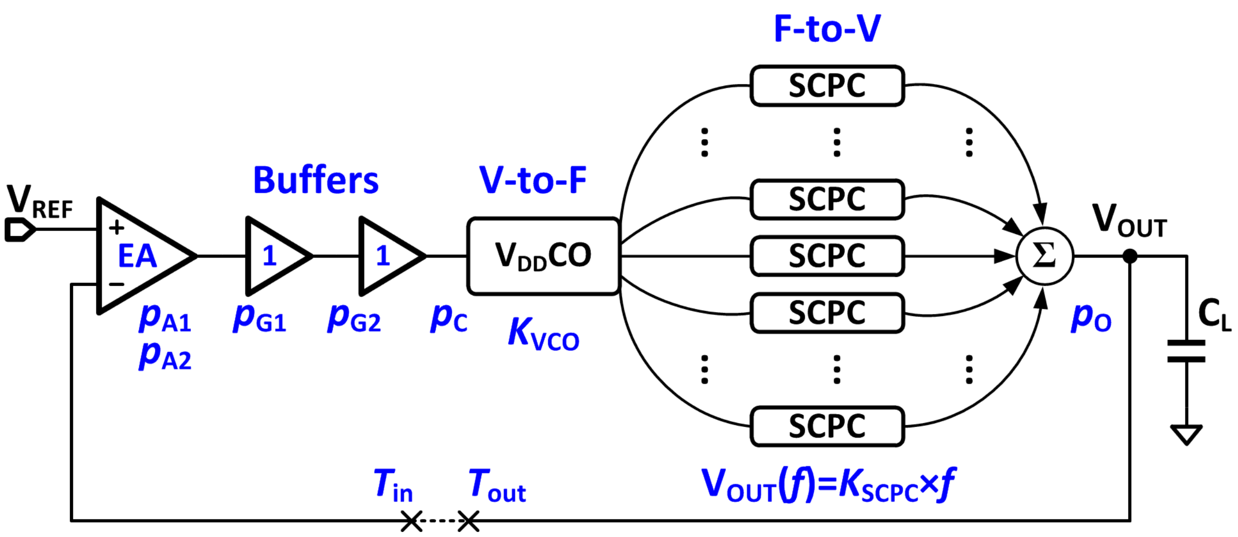




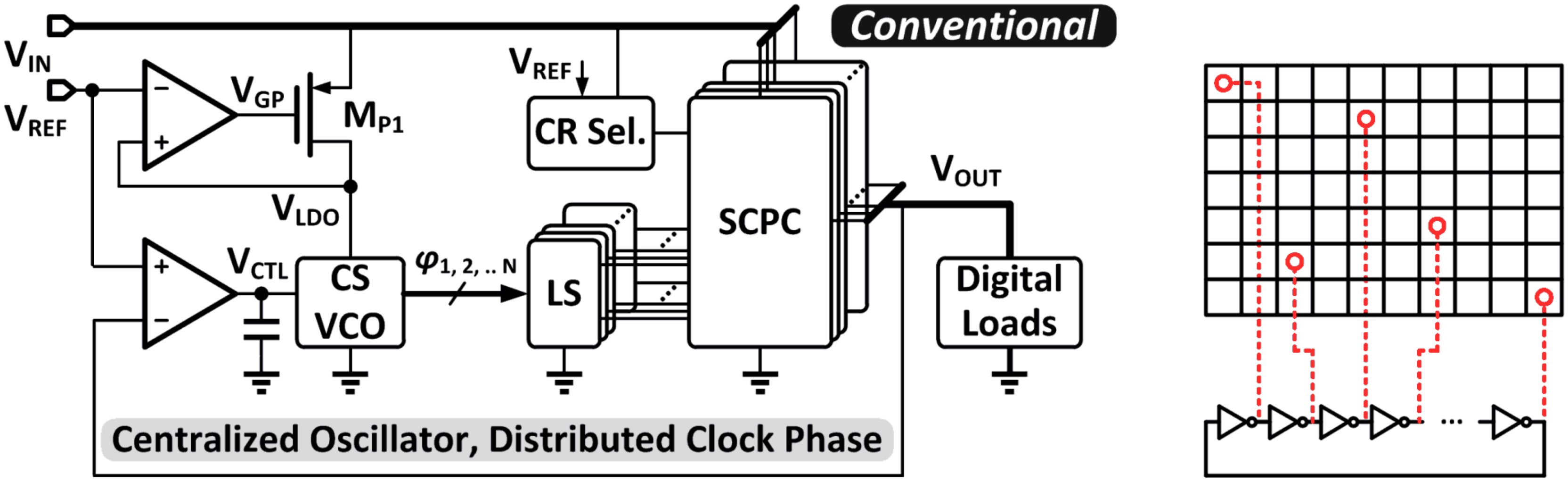
T. M. Andersen, et al., ISSCC, 2015

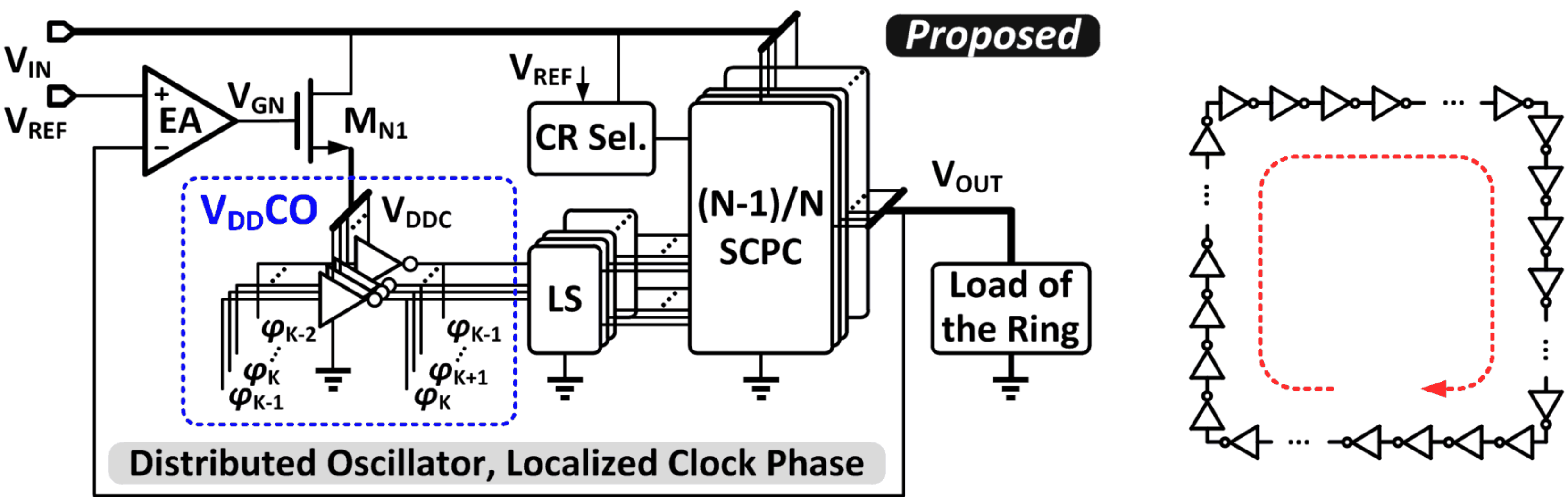
Unity Gain Frequency (UGF) Extension

- Using the following configurations for the switched-capacitor power converter (SCPC) for UGF extension:
  - Set the dominant pole at V_{OUT},
  - Employ a high speed error amplifier (EA),
  - Tune the oscillator frequency through its supply (V_{DD}CO).



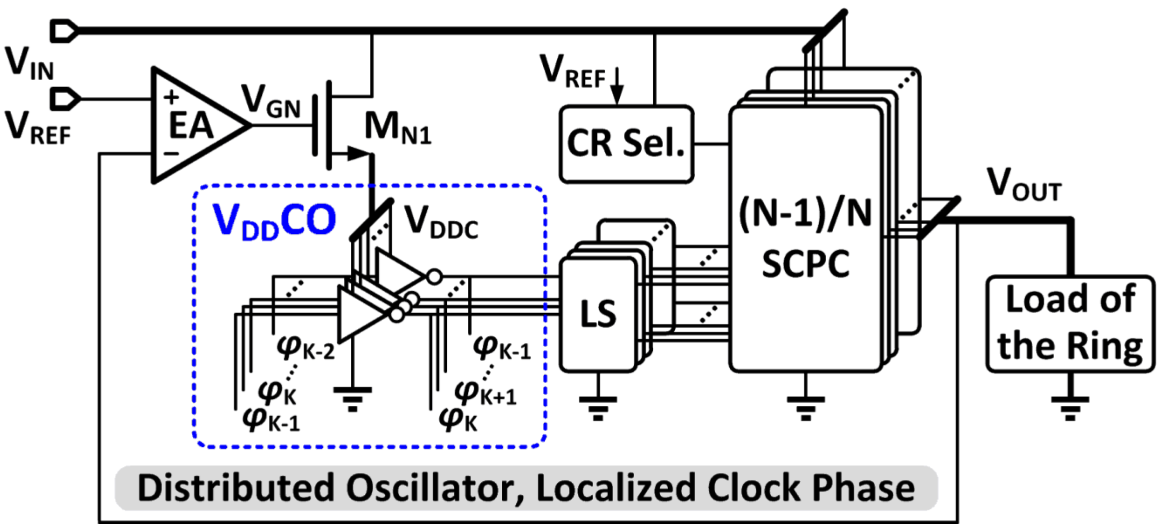
Proposed System Architecture





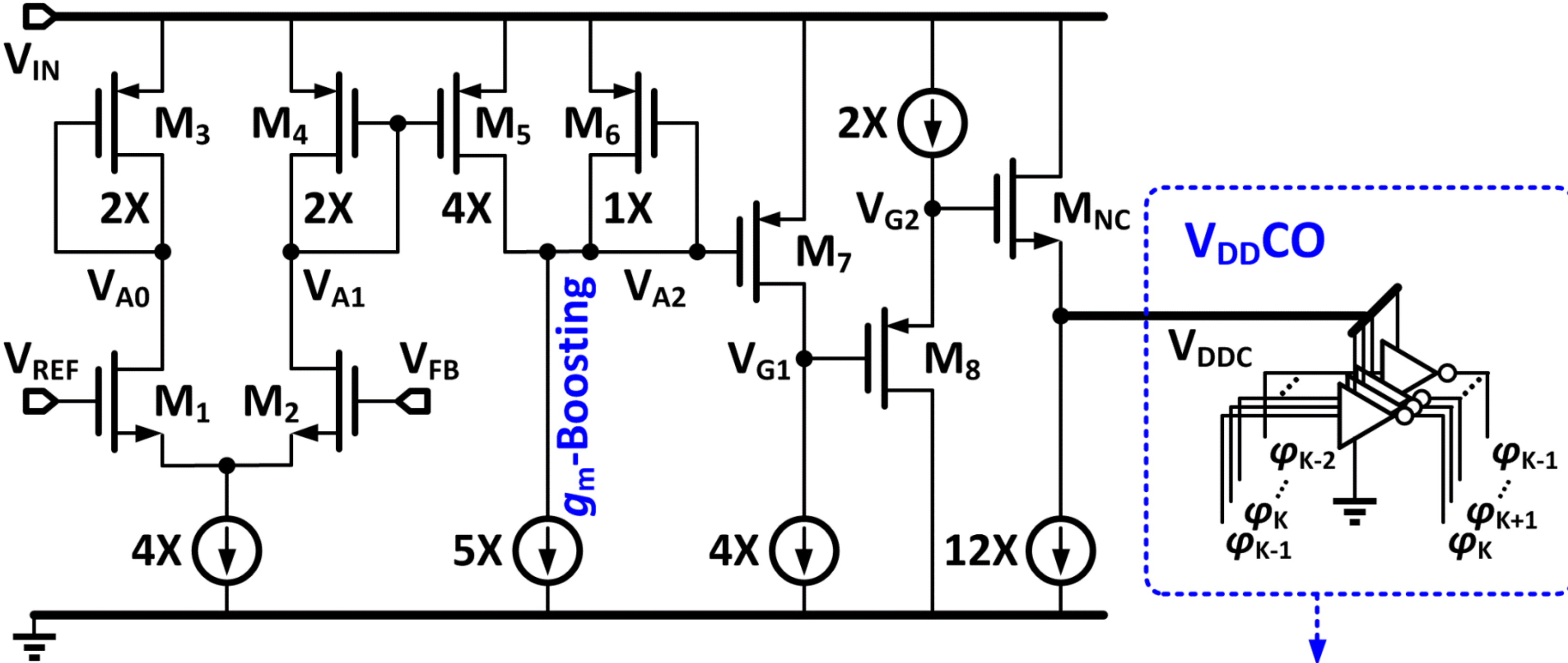
Pseudo-Continuous-Time SCPC

- Increasing the phase number also enables the control-loop to response at every fraction of the switching period (T), which is T/123 in our case.
- The discrete-time SCPC approaches a pseudo-continuous-time power stage. Thus, UGF of the control-loop could be designed to be higher than the switching frequency of the SCPC.

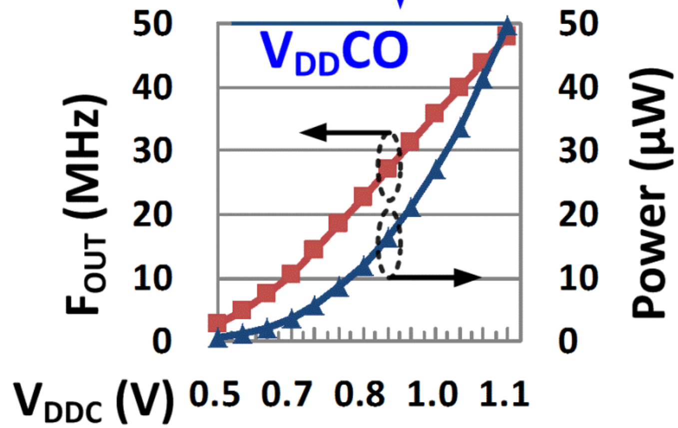


Achieve fast response without using additional GHz clock.

Error Amplifier and V_{DD} Controlled Oscillator

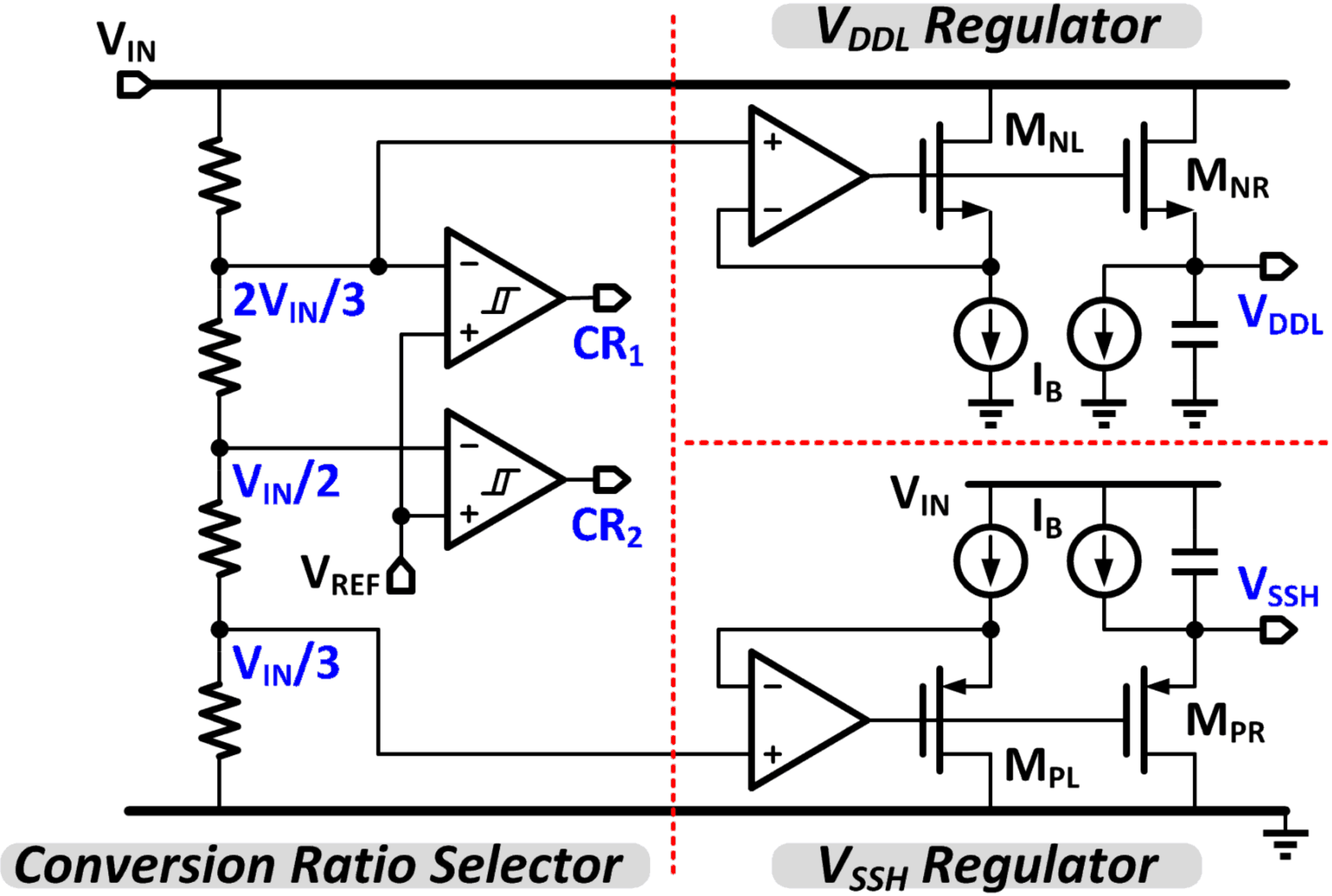


$$A_{EA} = \frac{g_{m2}}{g_{m4}} \cdot \frac{g_{m5}}{g_{m6}} \cdot g_{m7} r_{o7} \cdot A_8 \cdot A_{NC}$$
$$\approx 8 \cdot g_{m2} r_{o7}$$



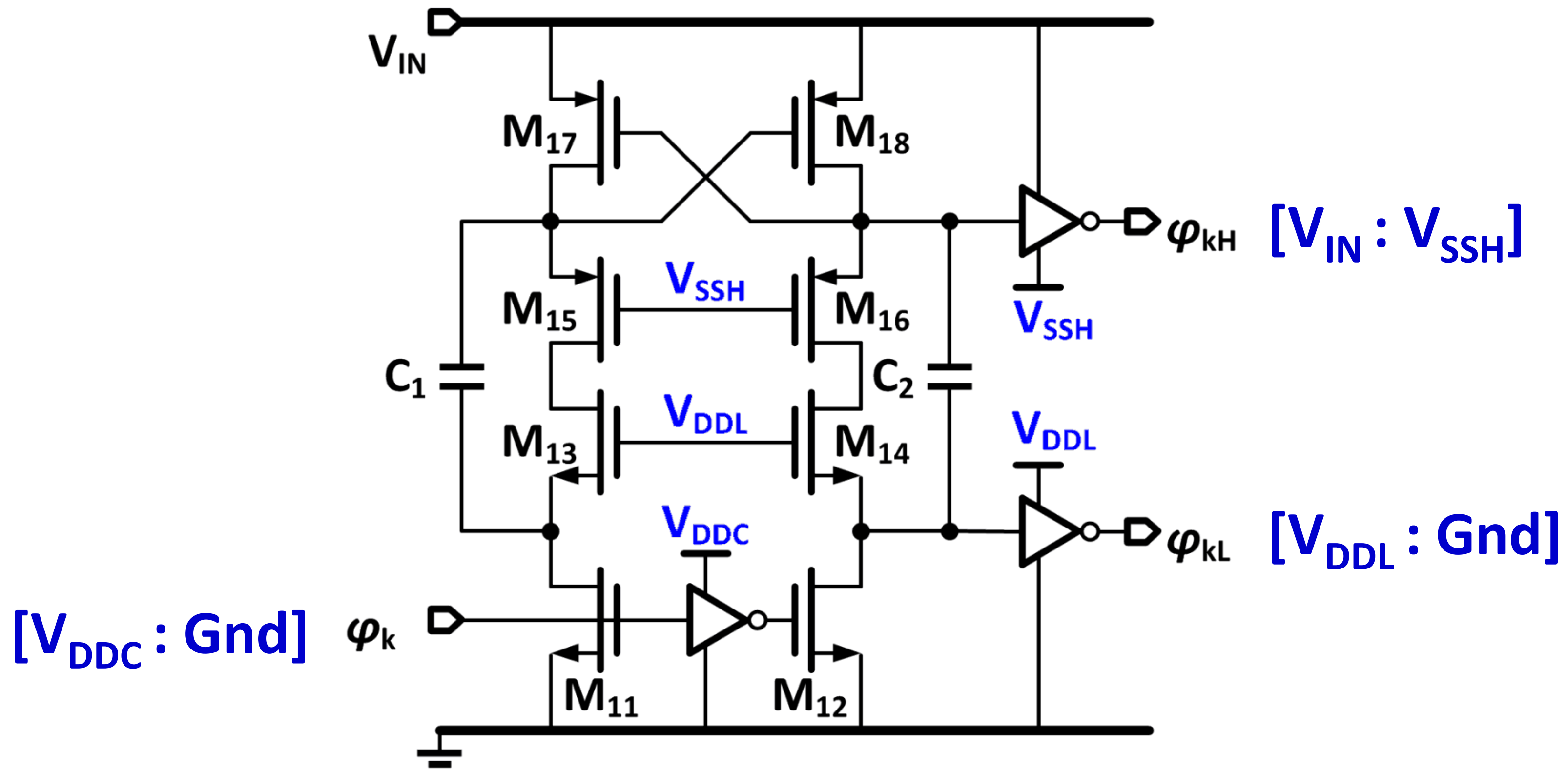
Internal Rails for Low Voltage Devices

- Voltage domain [V_{IN} : V_{SSH}] = [V_{IN} : $V_{IN}/3$]
- Voltage domain [V_{DDL} : Gnd] = [$2V_{IN}/3$: Gnd]
- V_{IN}: 1.6V to 2.2V



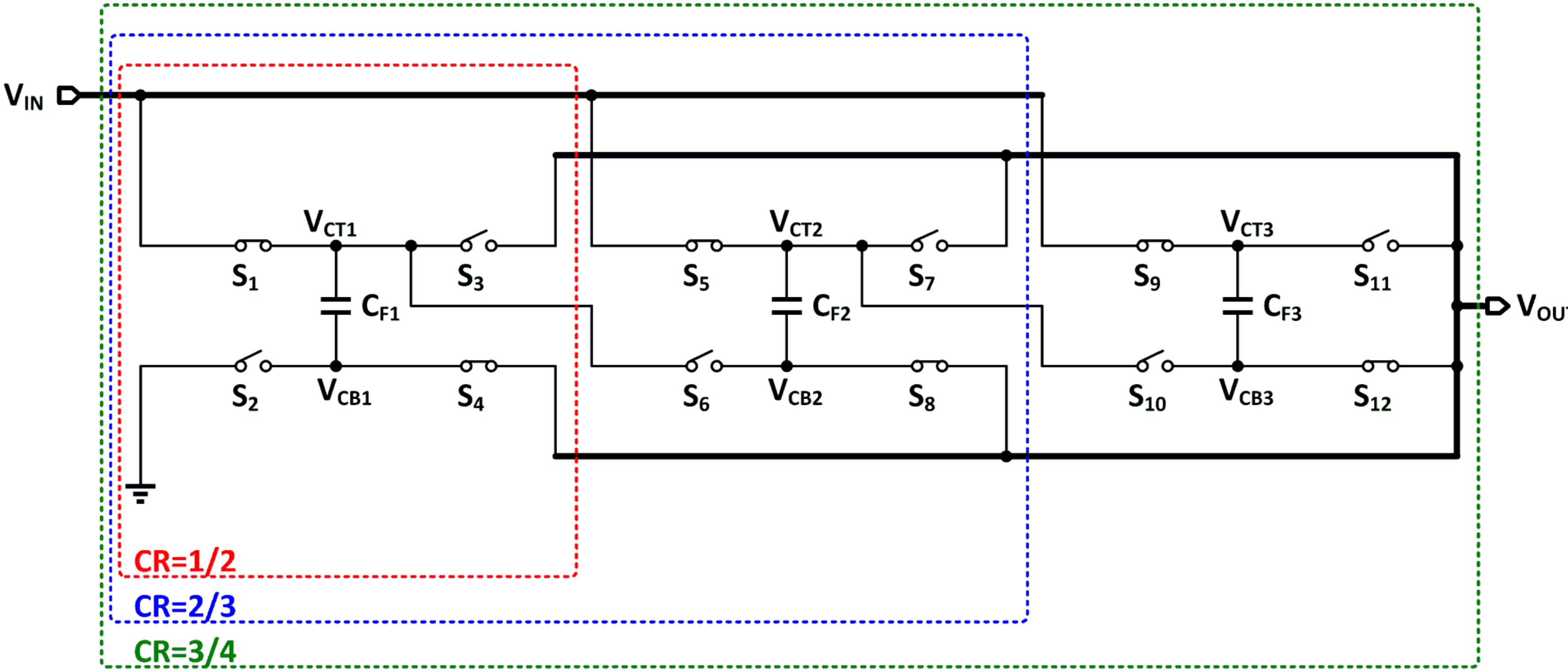
Level Shifter (LS)

- Effectively convert the input signal from the **[V_{DDC} : Gnd]** domain to the domains of **[V_{IN} : V_{SSH}]** and **[V_{DDL} : Gnd]**, simultaneously, through one single conversion.

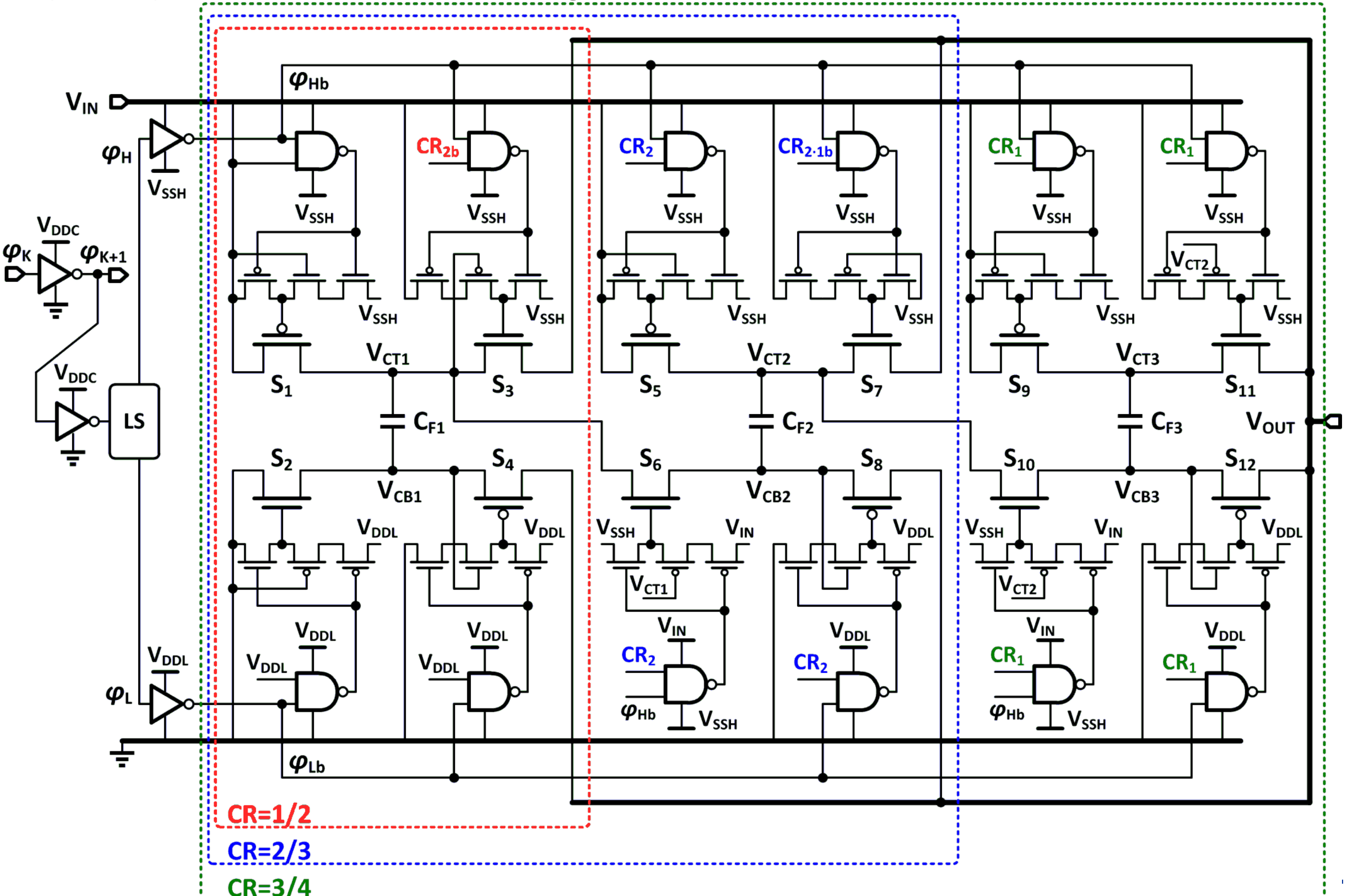


(N-1)/N Switched-Capacitor Power Converter

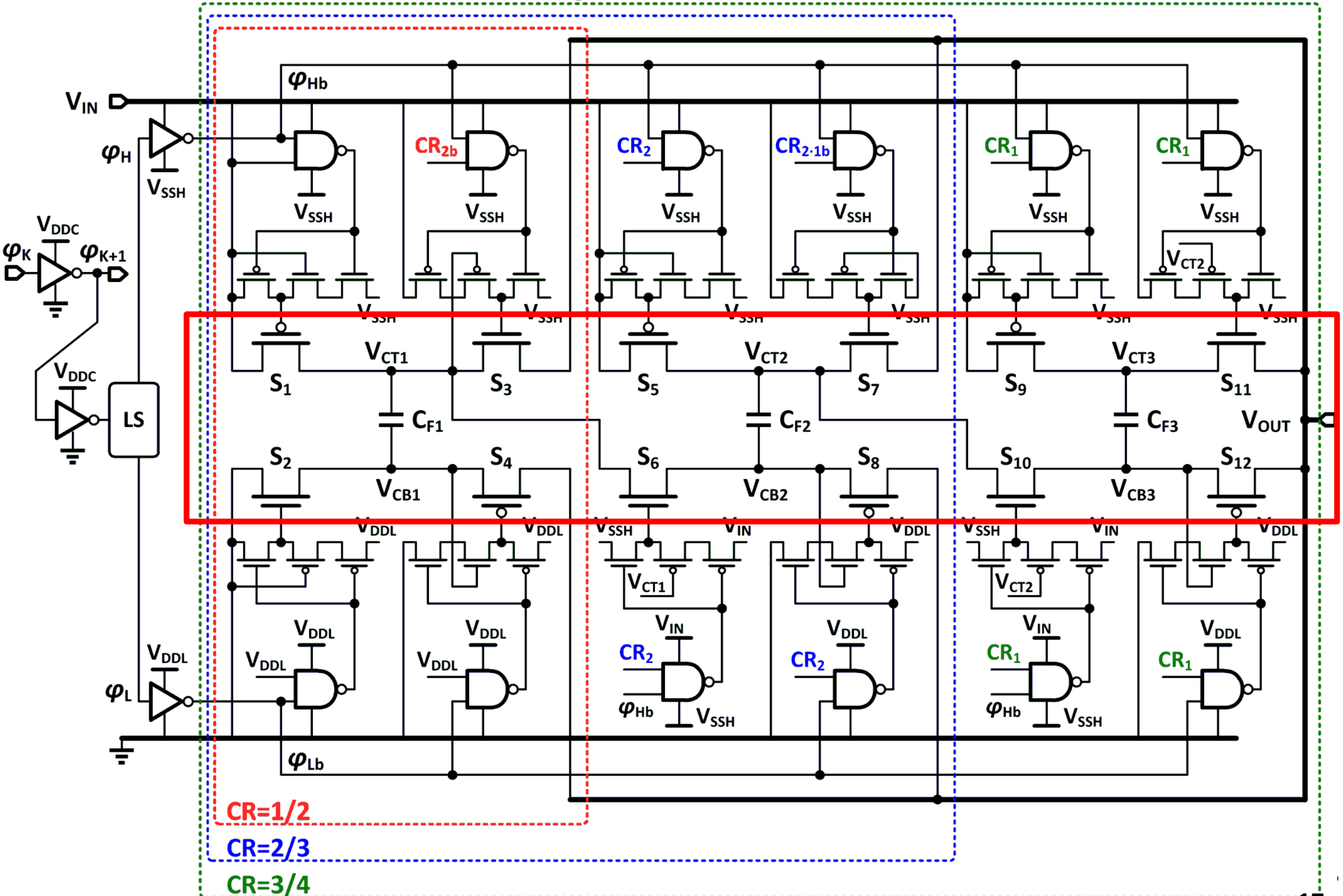
- The conversion ratio (CR) can be reconfigured into 1/2, 2/3, 3/4.



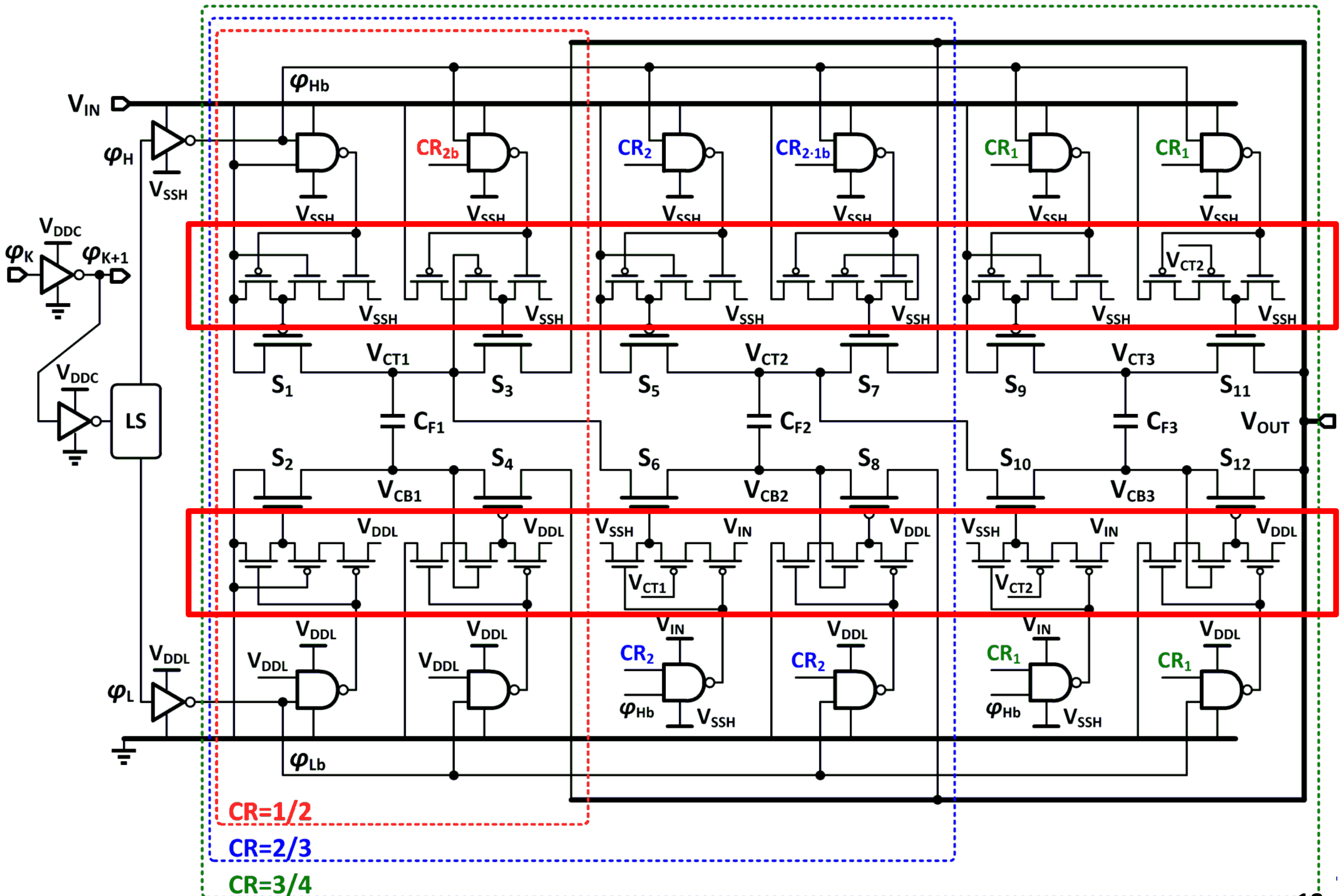
(N-1)/N Switched-Capacitor Power Converter



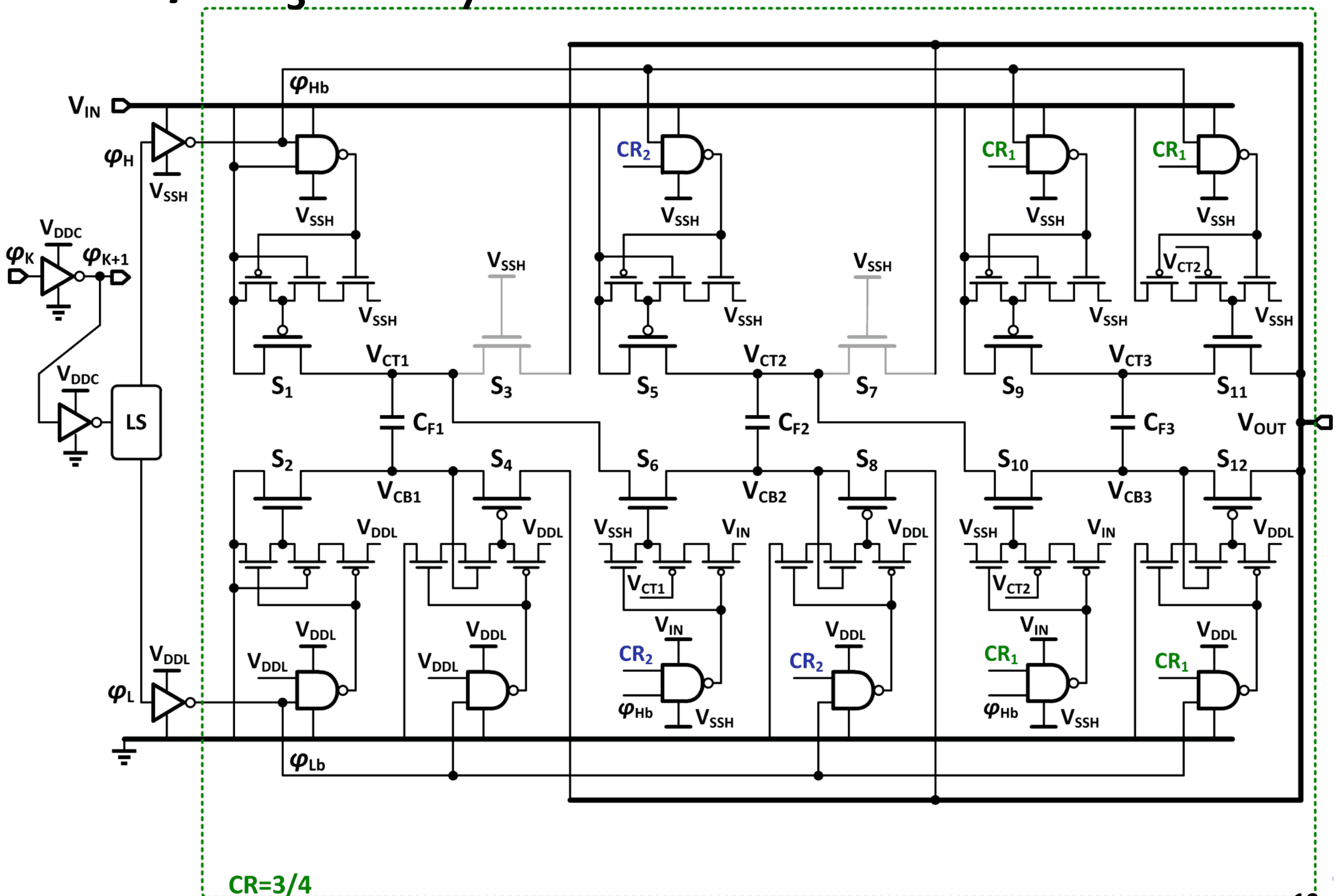
12 Switches and 3 Capacitors for Each Unit Cell



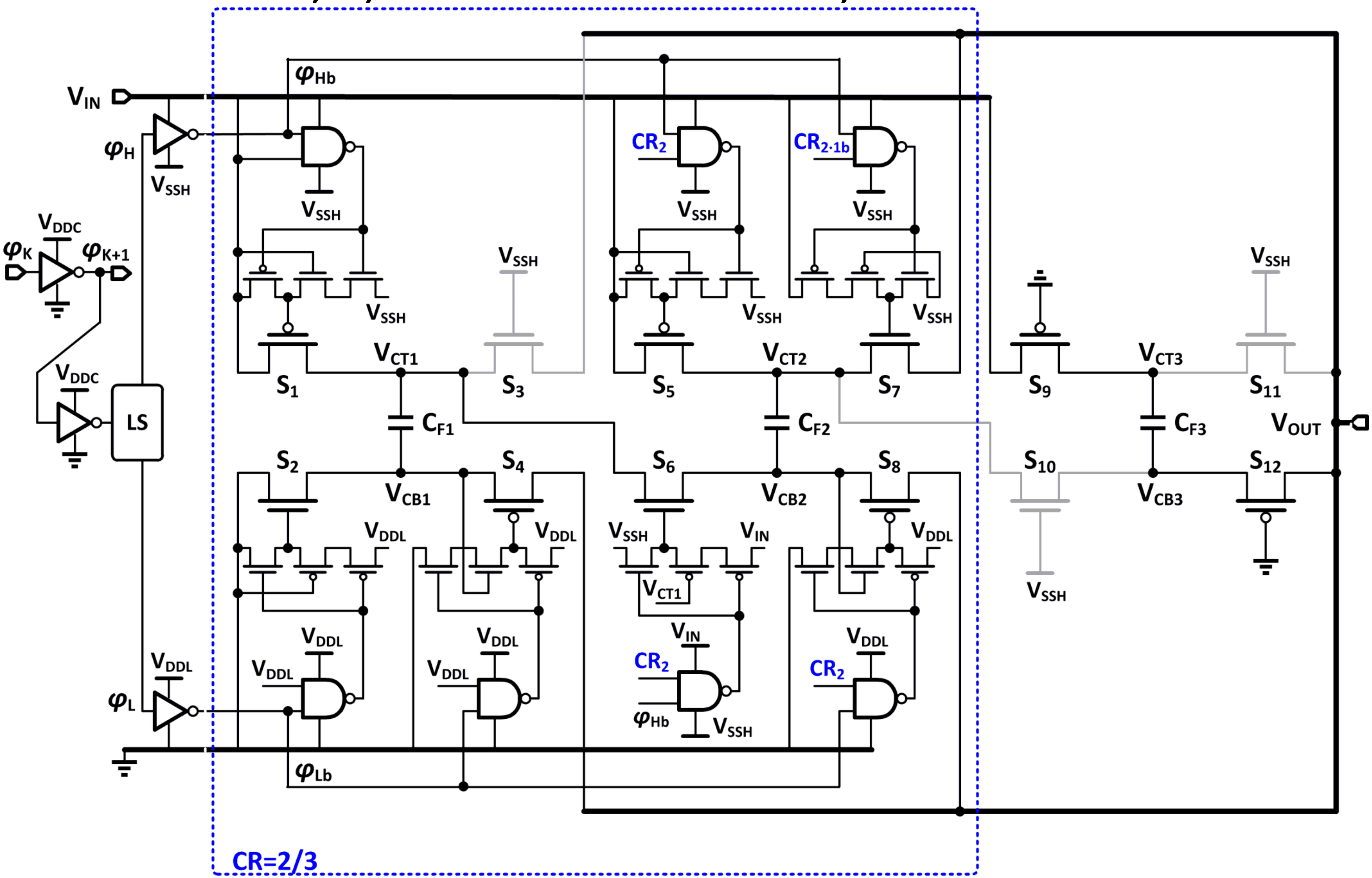
3-Transistor Based Inverters



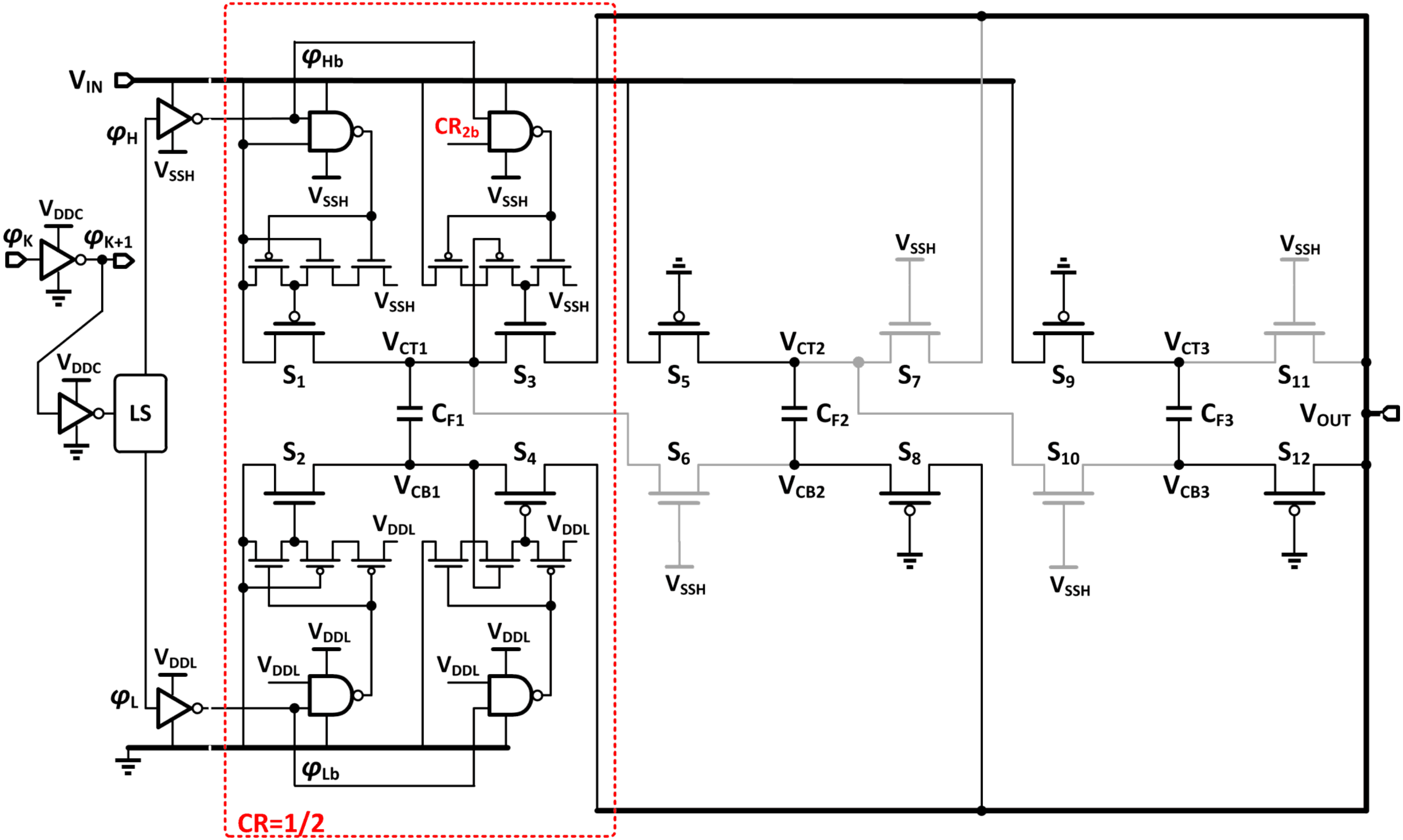
CR=3/4. S_3 and S_7 are Constant Off.



CR=2/3. $S_{3,10,11}$ Constant Off, $S_{9,12}$ Constant On.

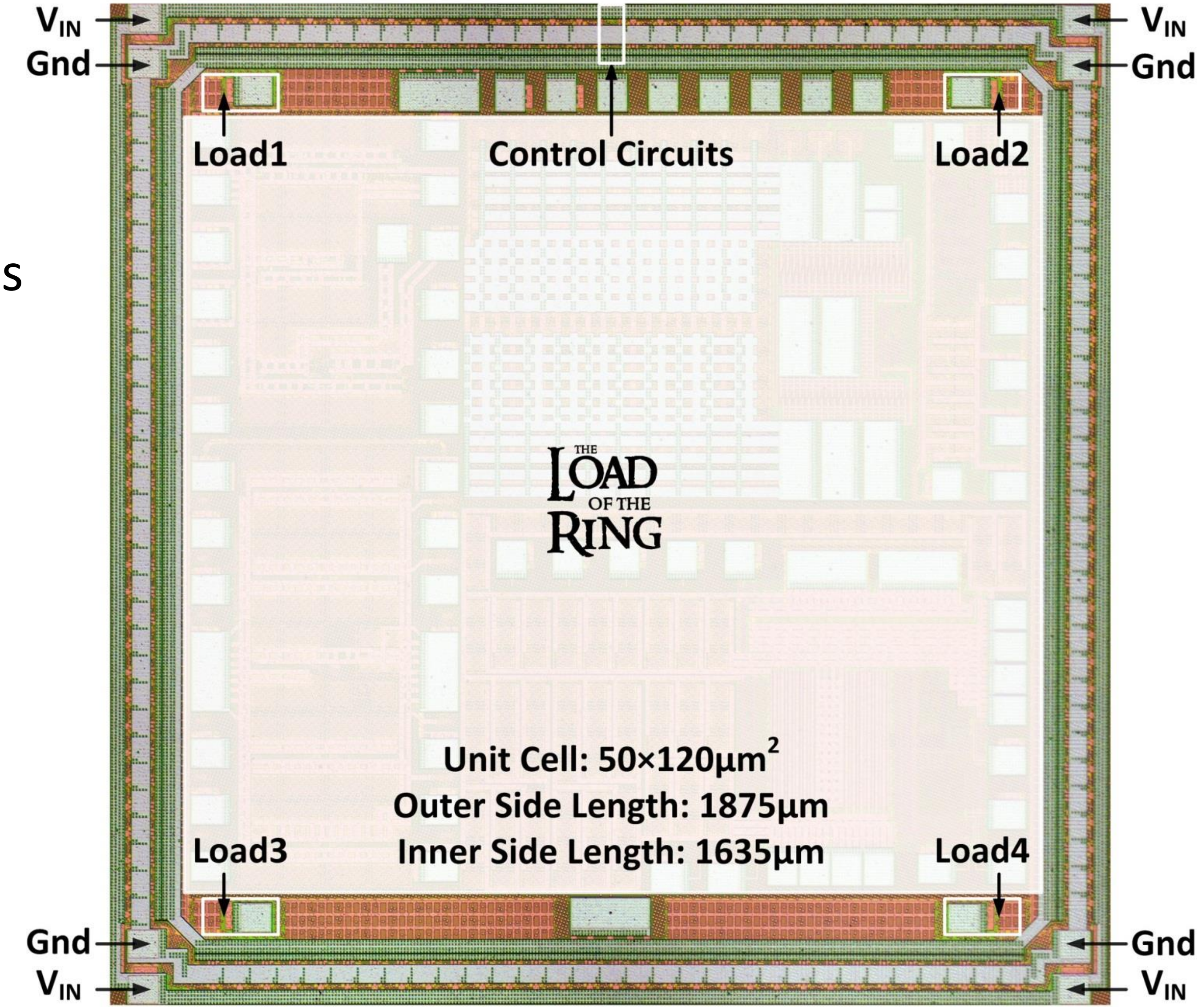


CR=1/2. $S_{6,7,10,11}$ Constant Off, $S_{5,8,9,12}$ Constant On.

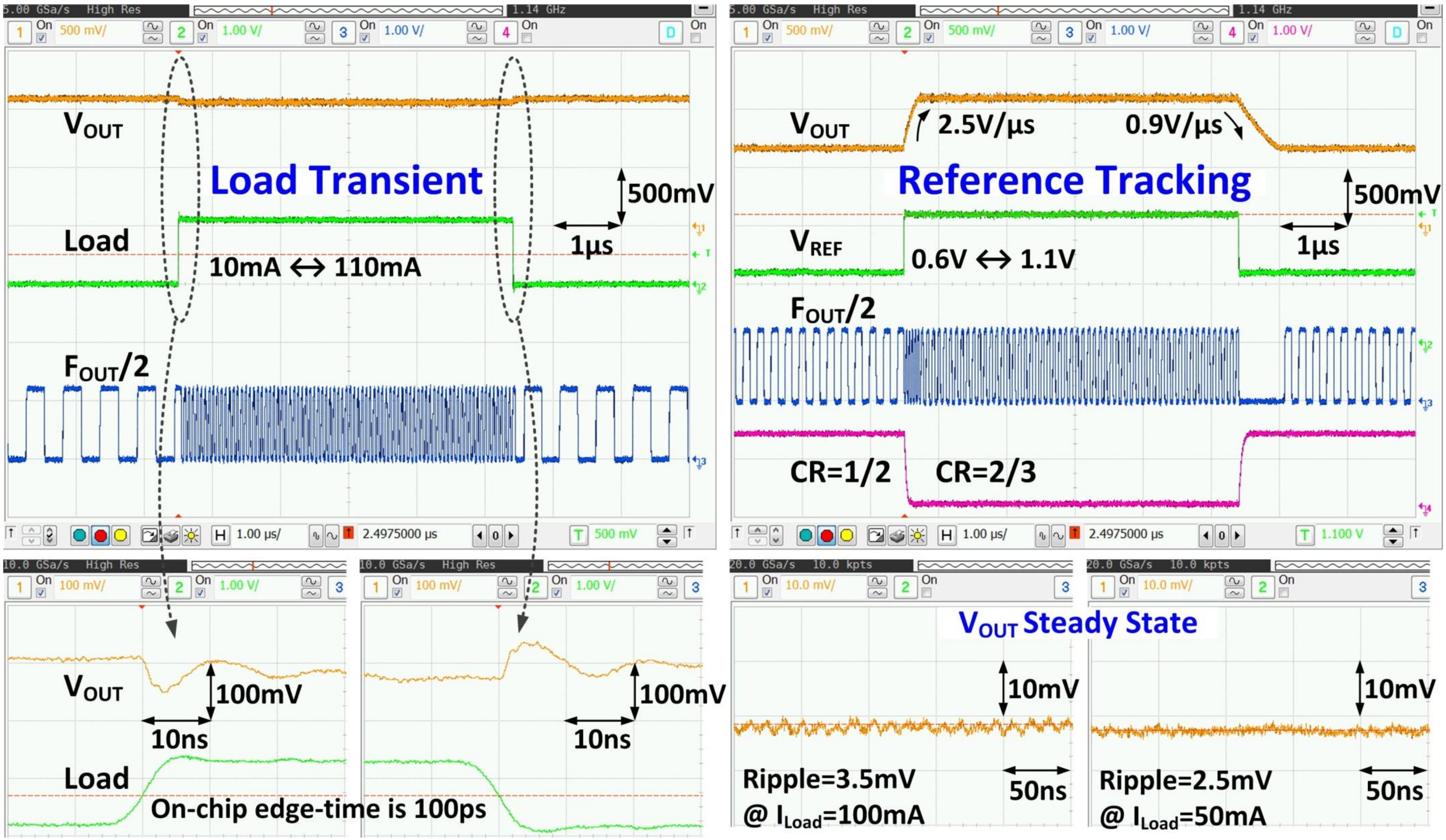


Chip Micrograph

- 65nm CMOS
- 1.2V LL Devices
- Stacked MOS, MOM, MIM capacitors
- Effective area: $0.84mm^2$



Measured Transient Results

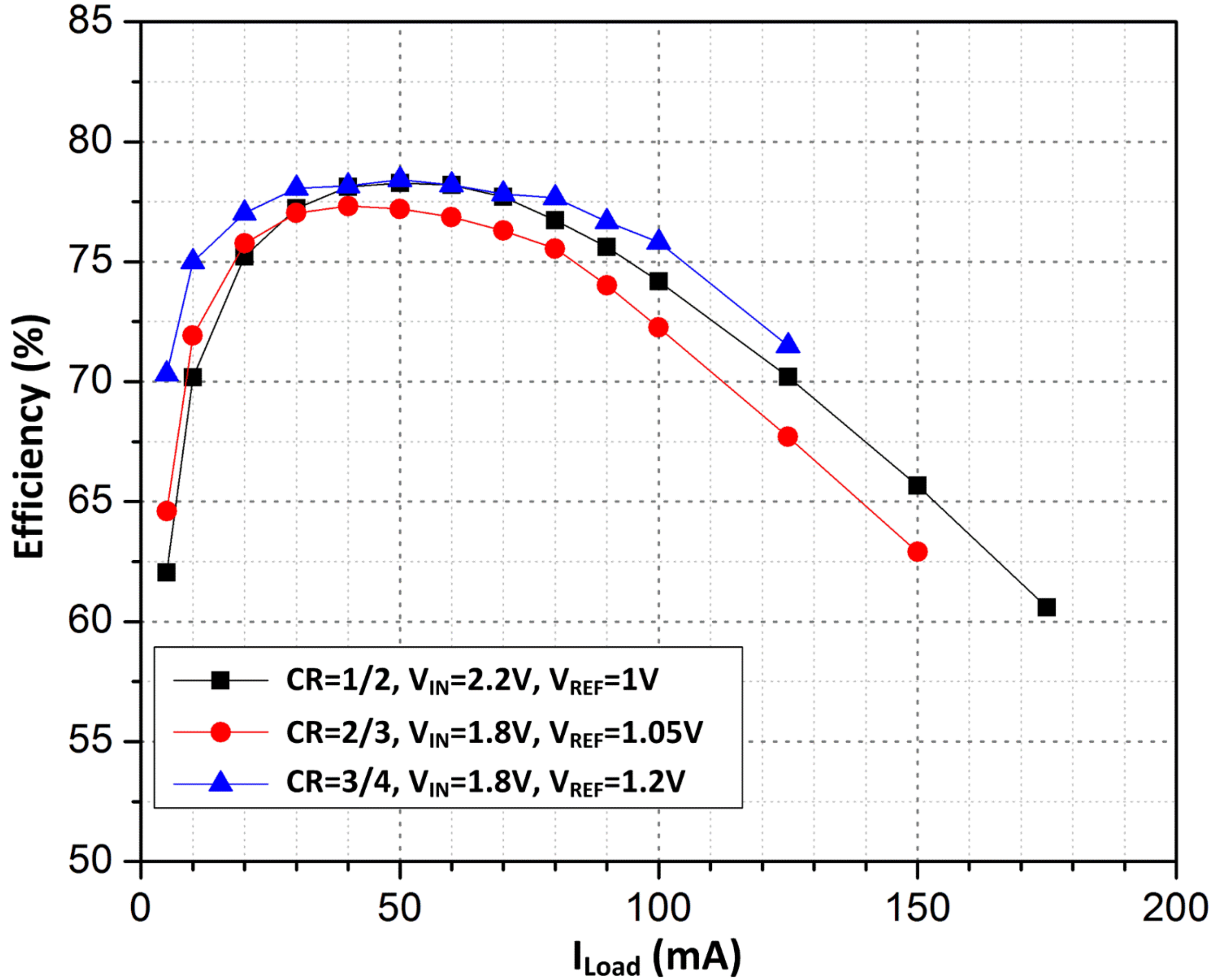


Measured Power Conversion Efficiencies

78%@I_{Load}=50mA

75%@I_{Load}=100mA

65%@I_{Load}=150mA



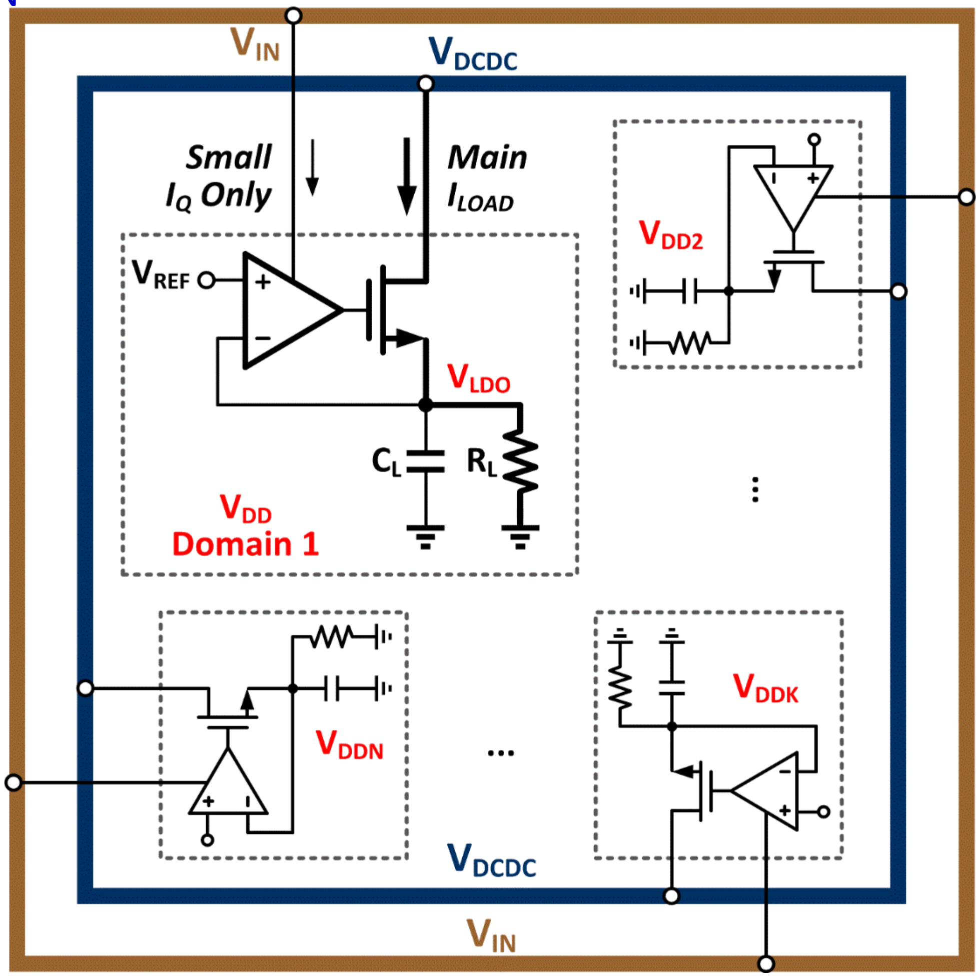
Comparison Table

Publication	Le, JSSC '11	Piqué ISSCC '12	Le, ISSCC '13	Jain, JSSC '14	This work '15
Process	32nm SOI	90nm	65nm	22nm Tri-gate	**65nm**
Conv. Ratios	2/3, 1/2, 1/3	1/2, 2/3	1/3, 2/5	1/2, 2/3, 4/5, 1	**1/2, 2/3, 3/4**
Phase No.	32	41	18	8	**123**
V_{IN}	2	1.2-2V	3-4V	1.225V	**1.6-2.2V**
V_{OUT}	0.5-1.2V	0.7V	1V	0.45-1V	**0.6-1.2V**
F_S @η_{Peak}	300MHz*	50MHz	N/A	250MHz	**33MHz**
η_{Peak}	79.8%	81%	74.3%	82.7%	**80.0%**
Power Density	860mW/mm^2	39mW/mm^2	190mW/mm^2	250mW/mm^2	**180mW/mm^2**
$P_{OUT,Max}$	600mW*	10mW	162mW	25mW	**152mW**
Ripple Range	N/A	3.8mV-N/A	N/A	43mV-125mV*	**2.2mV-30mV**
ΔV_{OUT} @T_{Edge}	N/A	N/A	76mV @50ps	N/A	**58mV @100ps**
DVS Speed	N/A	N/A	N/A	N/A	**2.5V/µs**

*Estimated from figure.

Multiple V_{DD} Domains in Converter-Ring

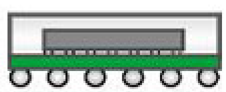
- Cascade NMOS LDO for multiple V_{DD} domains.
- Only µA of I_Q is drawn from V_{IN}.
- Main I_{LOAD} provided by V_{DCDC}.



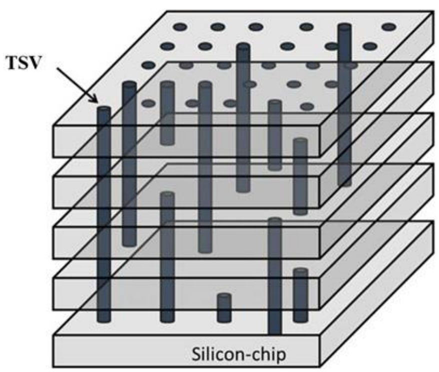
Y. Lu, et al., "An NMOS-LDO Regulated Switched-Capacitor DC–DC Converter …," *IEEE TPEL*, Feb. 2016.

Power Converter Grid?

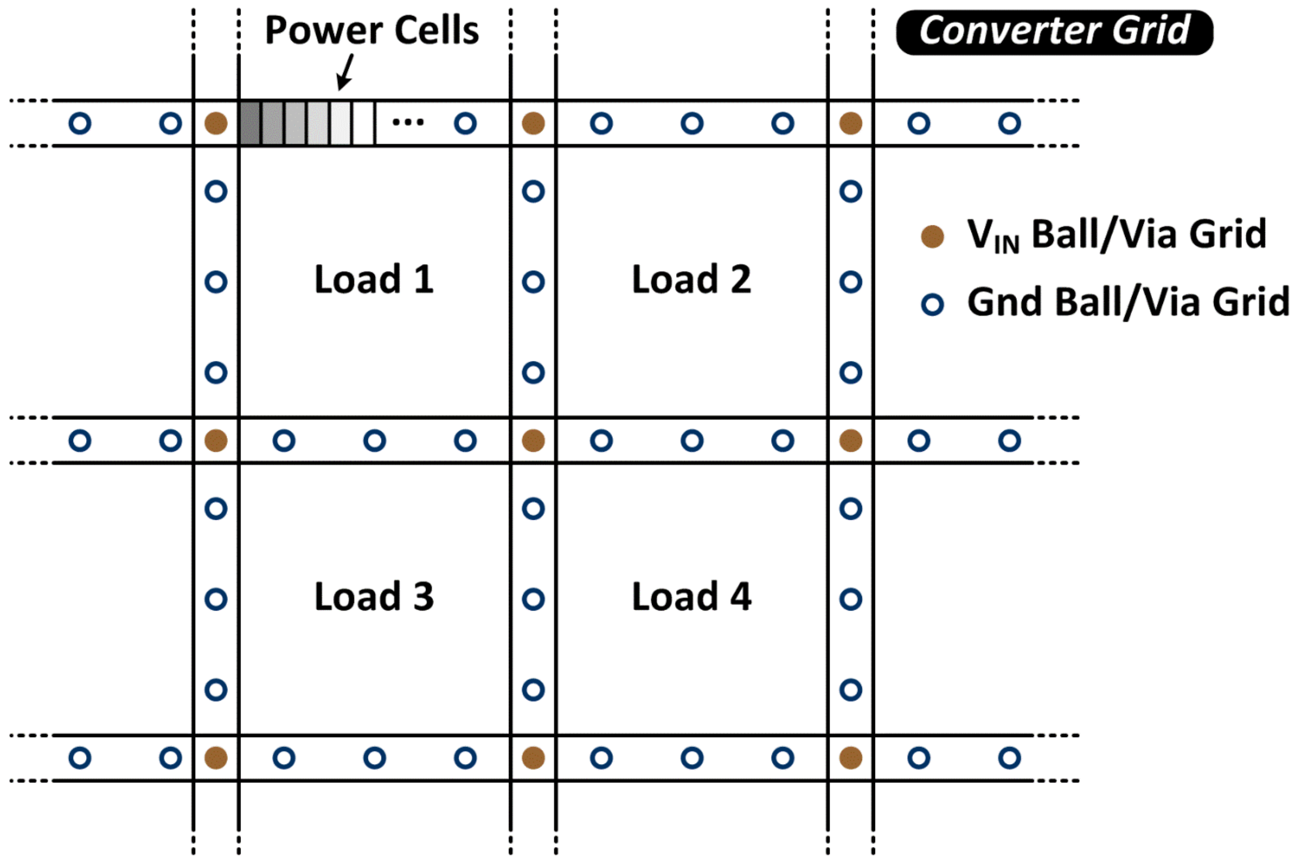
- On-chip power converter grid with flip chip or through silicon via (TSV) in 3D IC?



Flip Chip



TSV in 3D IC



Conclusions

- A Ring-Shaped Multiphase Switched-Capacitor DC-DC Converter is proposed for on-chip power delivery.
- Unity gain bandwidth is designed to be a few times higher than the switching frequency of the DC-DC Converter, enabled by
  1. Setting the dominant pole at V_{OUT};
  2. Designing a high speed EA;
  3. Tuning the $V_{DD}CO$ frequency through its supply voltage.
- Possible solutions (NMOS-LDO regulation, power converter grid) are proposed.

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