Ferric

PWR SOC 16

DC-DC Power Conversion with CMOS Integrated Thin-Film Inductors

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FERRIC
THE COMPANY

- Fabless semiconductor technology company, founded in 2011
    - Located in New York
- Integrated magnetic component and power conversion technology
- Ferric integrated power inductors are available at TSMC now
- Team expertise:
    - semiconductor device manufacturing
    - magnetic thin-films
    - RF device design, characterization and modeling
    - CMOS IC design for power conversion applications
- Chip Sales, Design, IP and Process Licensing

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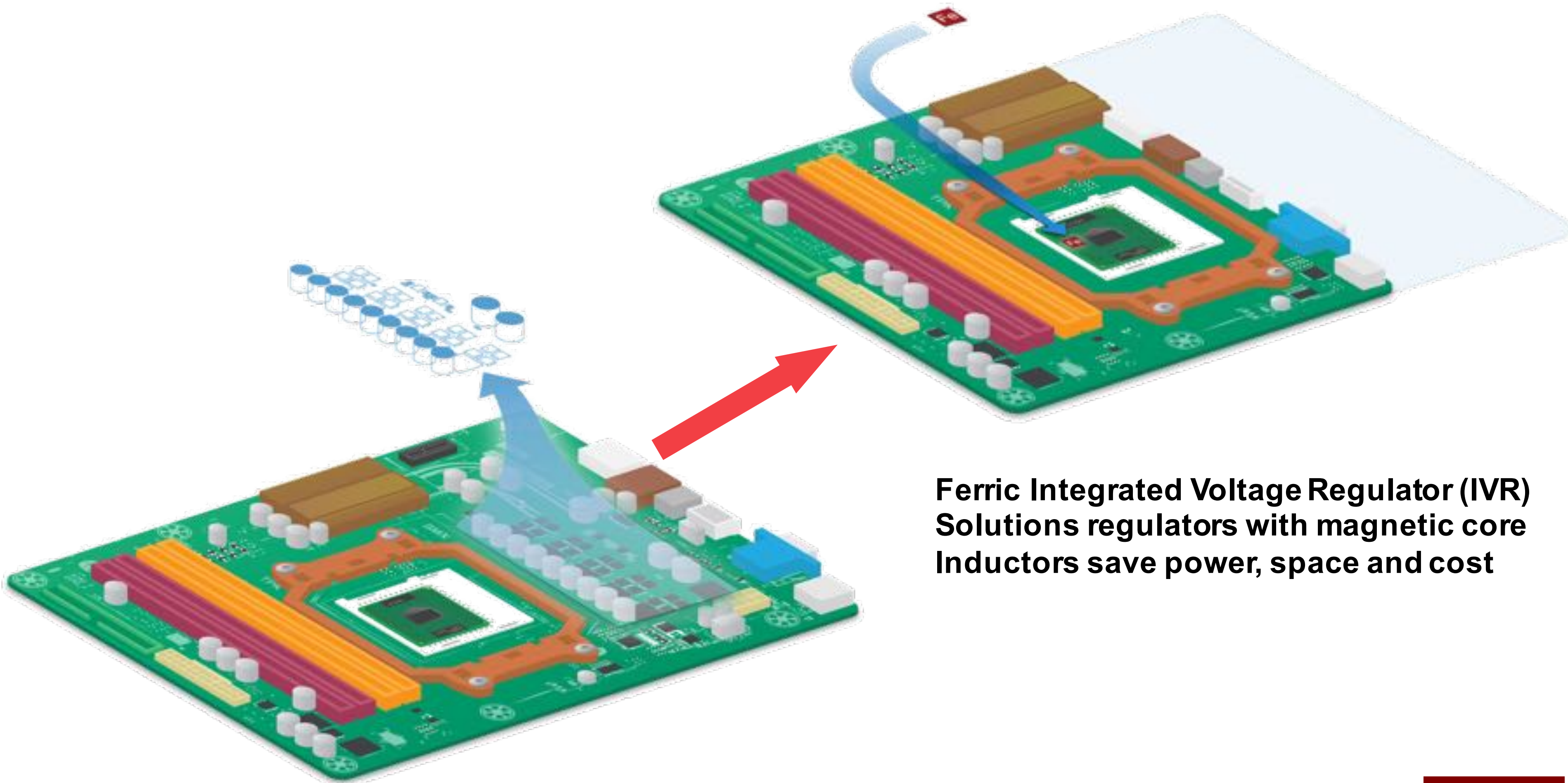
FERRIC TECHNOLOGY

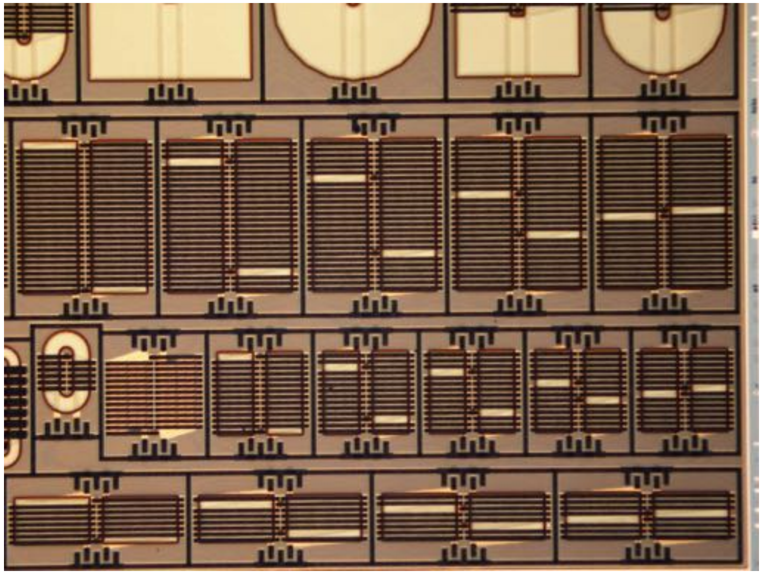
On-chip Magnetic Thin-Film Inductors Save Power, Space And Cost



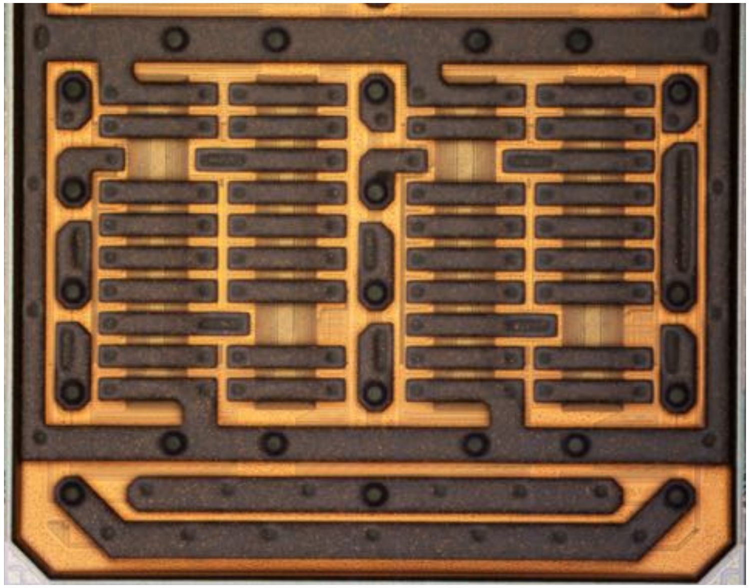
Ferric Integrated Voltage Regulator (IVR) Solutions regulators with magnetic core Inductors save power, space and cost

FERRIC TECHNOLOGY ELEMENTS

- **Integrated Inductors**
  - Inductance density
    - > 300nH/mm^2, > 8,500nH/mm^3
  - Current density > 12A/mm^2
  - DC Resistance < 100mΩ
  - Magnetic Coupling k > 0.9
  - Available monolithically at TSMC or on IPDs



- **Integrated Circuit Designs**
  - High switching frequency
  - High bandwidth controller
  - Optimization for high efficiency
  - Optimization for high density



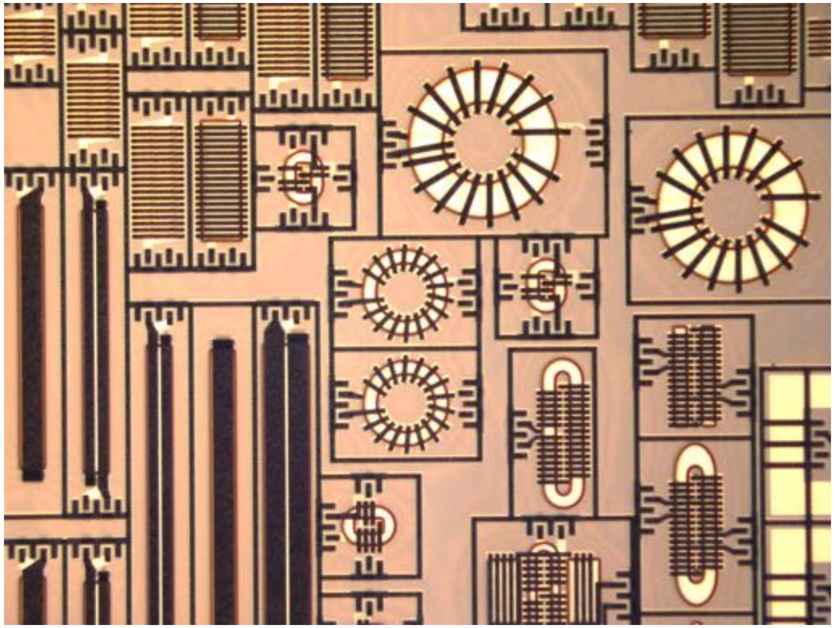
AGENDA

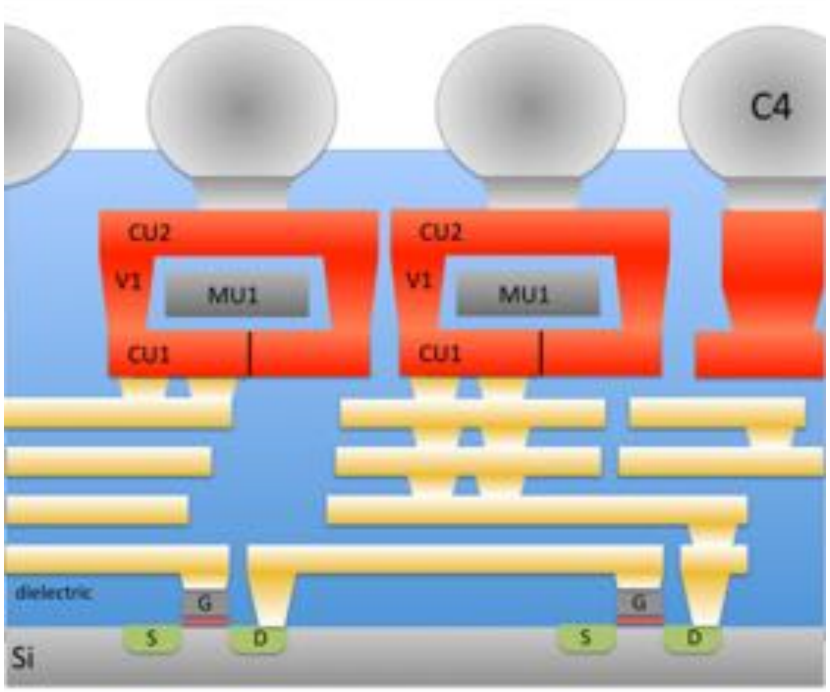
- **Ferric Thin-Film Power Inductors & Transformers**
- Ferric Device Libraries, Design Support and Models
- Ferric Power Converters

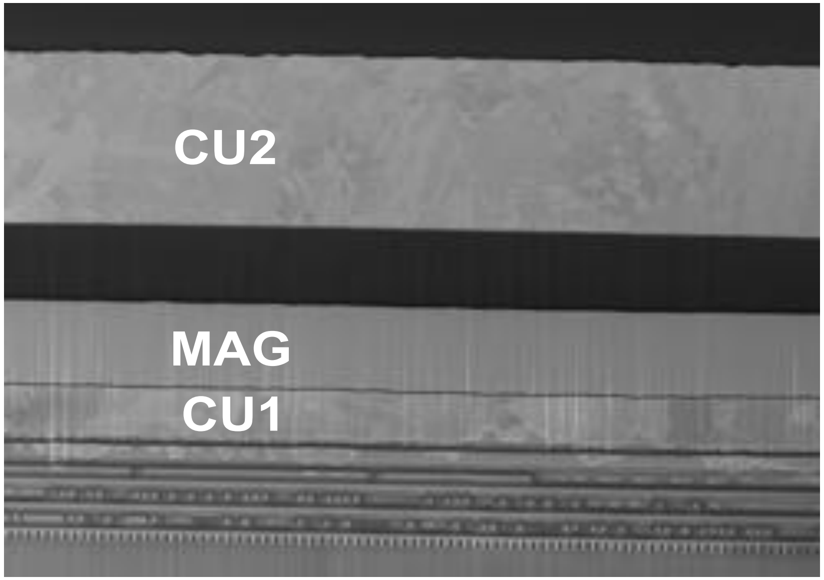
FERRIC ***INDUCTORS***

Ferric CMOS integrated magnetic thin-films enable high-quality, high density, low-profile on-chip/on-package inductive components

- **Integrated with Standard CMOS Flow**
  - Inductor layers available as BEOL process option (similar to MIM)
  - Circuit models, LVS, DRC
  - Inductor Cell Library







FERRIC *INDUCTORS* | *Highlights*

- Peak Q Factor – 17 @ ~315MHz
- Peak Inductance Density ~300nH/mm^2
- L/R_{DC} >200nH/Ω for L > 100nH
- L/R_{DC} of 120nH/Ω for L ~ 10nH
- Current Density exceeding 12A/mm^2 for coupled inductors (balanced current)
- Saturation Current exceeding 1.5A for single inductors
- Cross wafer inductance variability $\sigma < 3\%$
- Other Devices in development:
  - Transformers, Baluns, transmission lines, antennas, improved inductor designs

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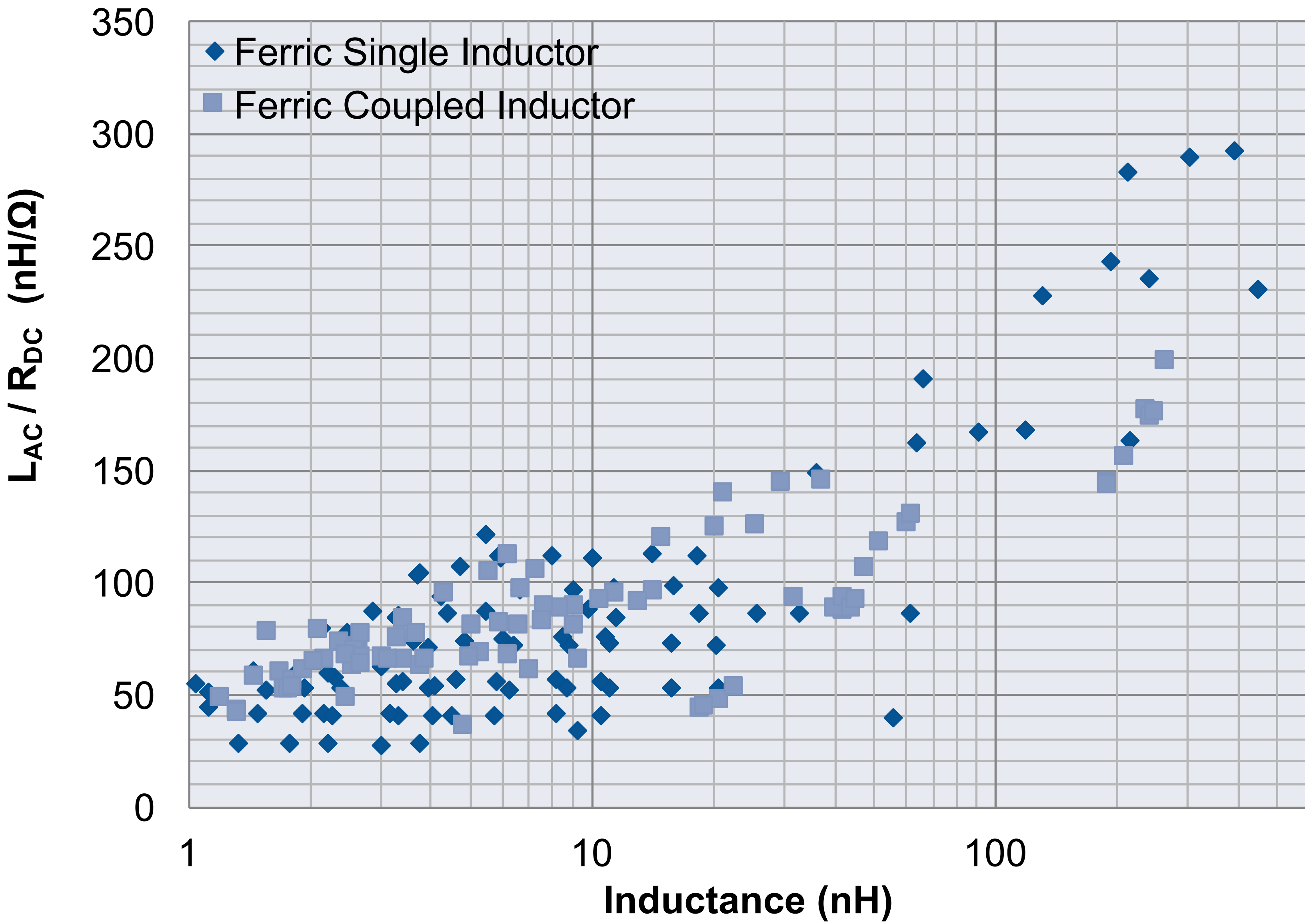
FERRIC INDUCTORS | ELECTRICAL PERFORMANCE



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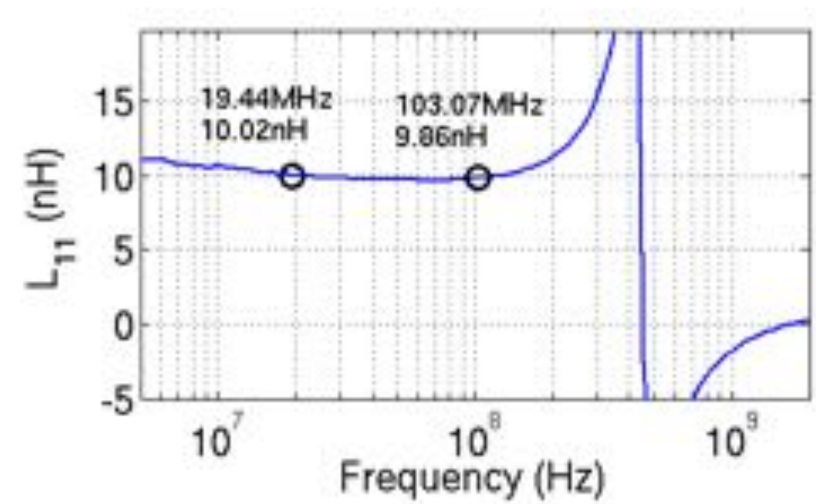
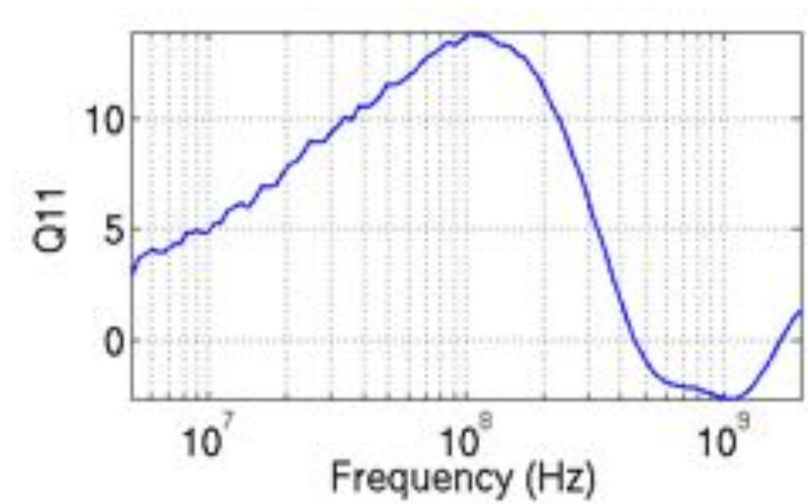
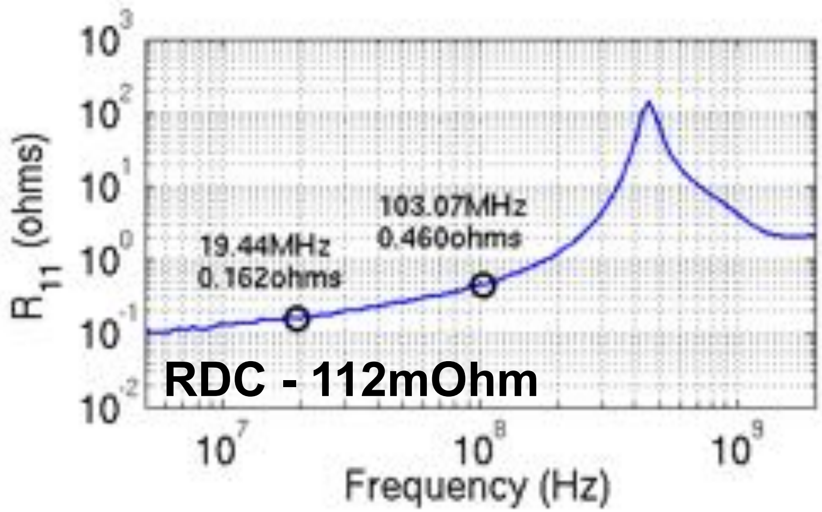
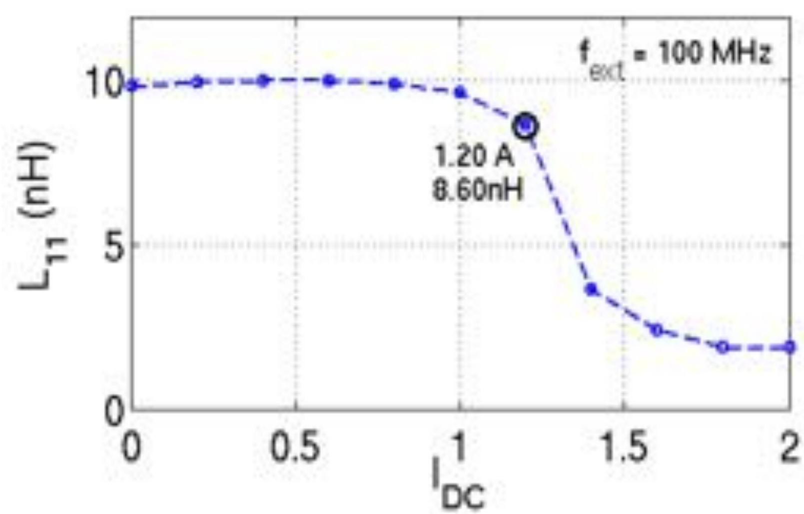
FERRIC INDUCTORS | SOLENOID EXAMPLE

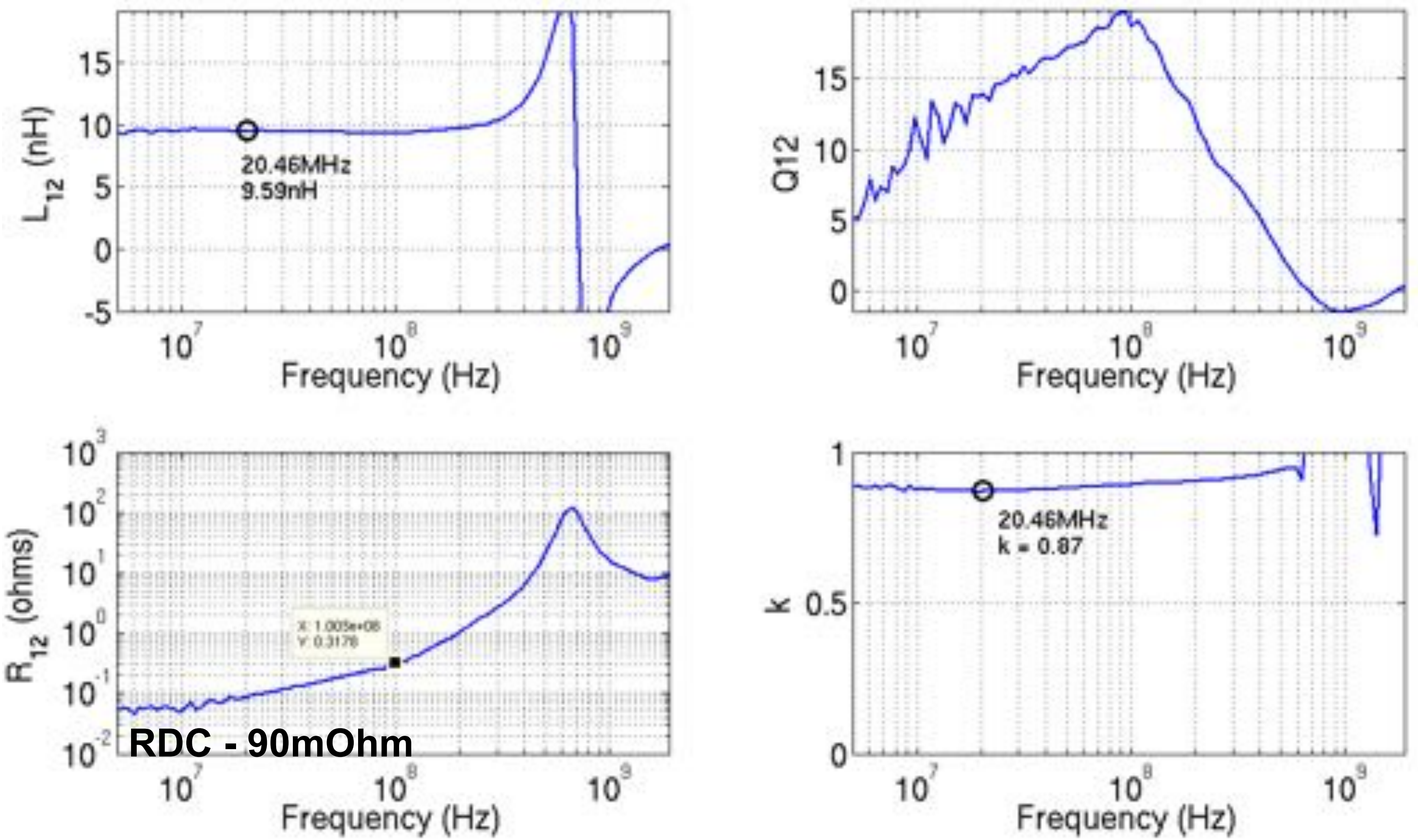






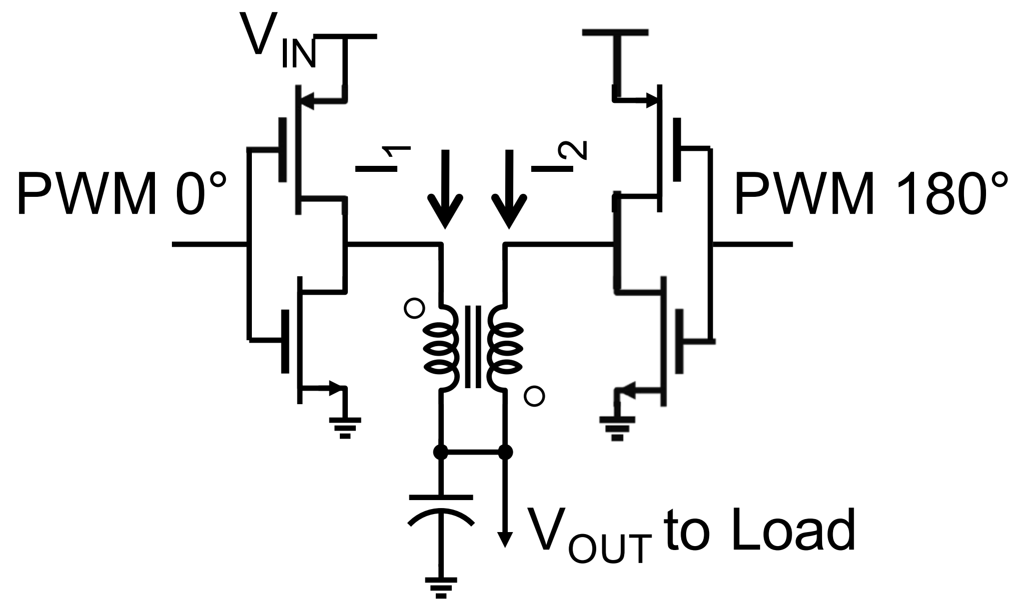


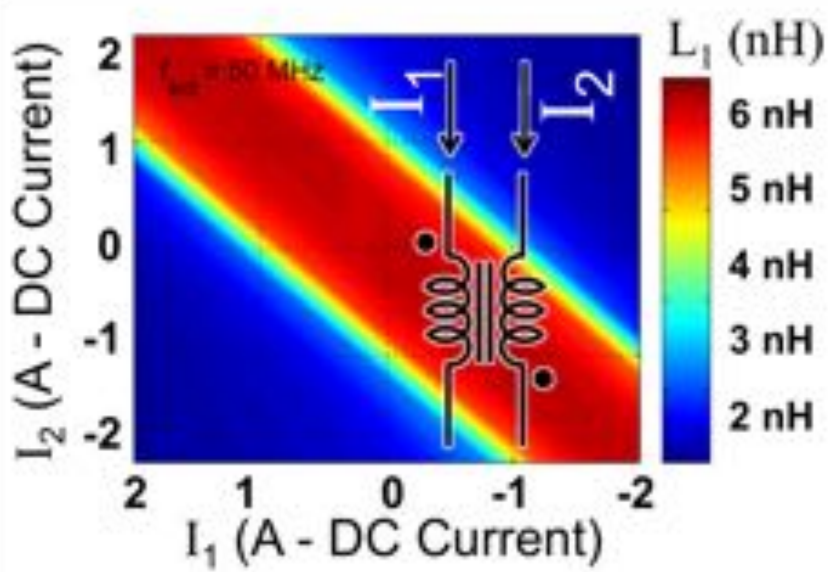
FERRIC INDUCTORS | COUPLED SOLENOID EXAMPLE

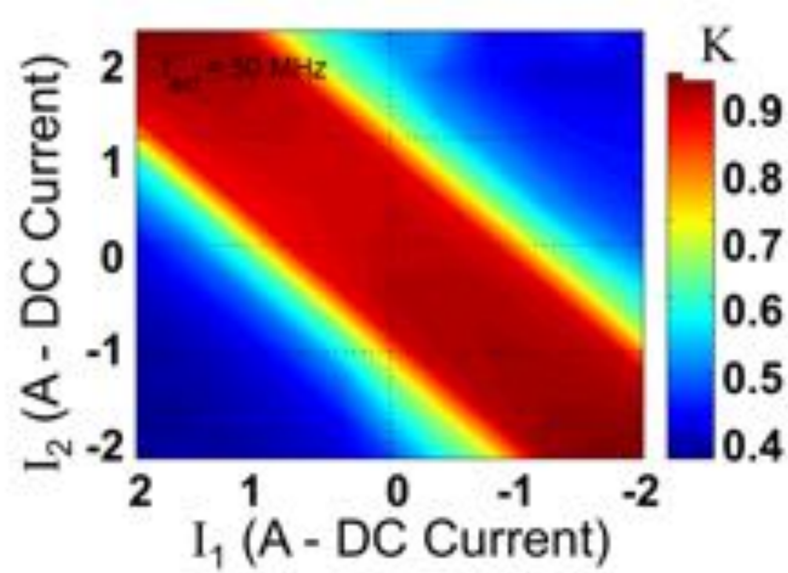


FERRIC *INDUCTORS | COUPLED INDUCTOR SATURATION*

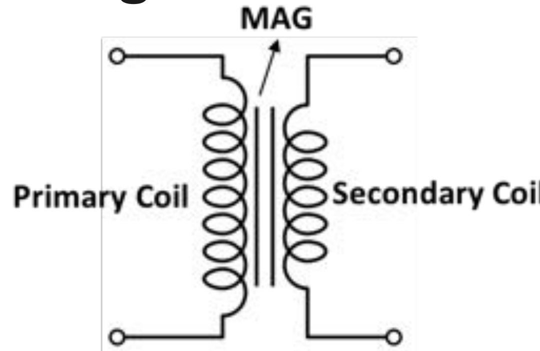
Inductor coupling is used in two-phase buck converters to avoid magnetic saturation



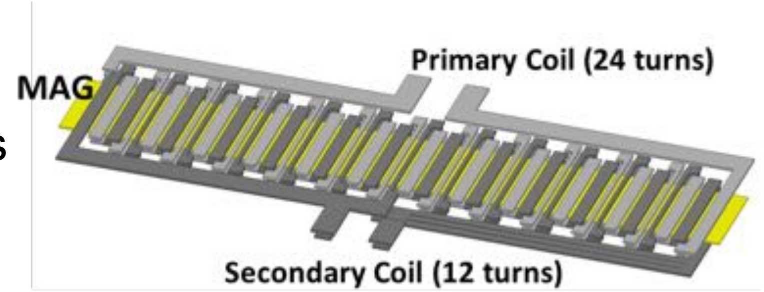




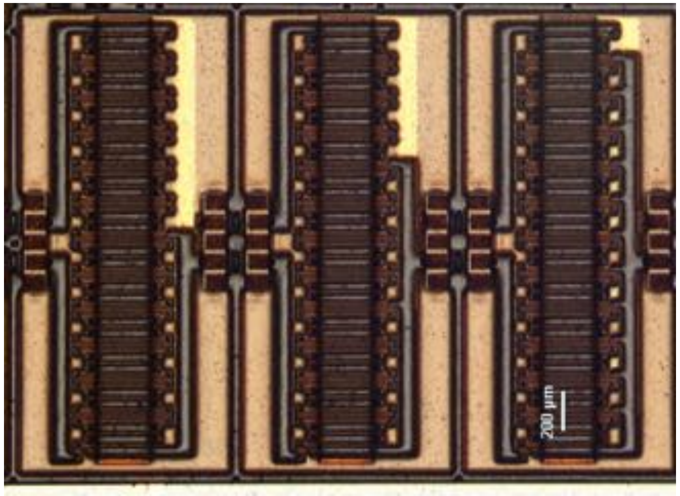
FERRIC **DEVICES** | *Transformers Design*



- Solenoid structure
  - Minimize capacitive/inductive coupling
- Elongated magnetic cores
  - Maximize permeability
- 24-turn primary coil
  - Number of secondary coil turns varies

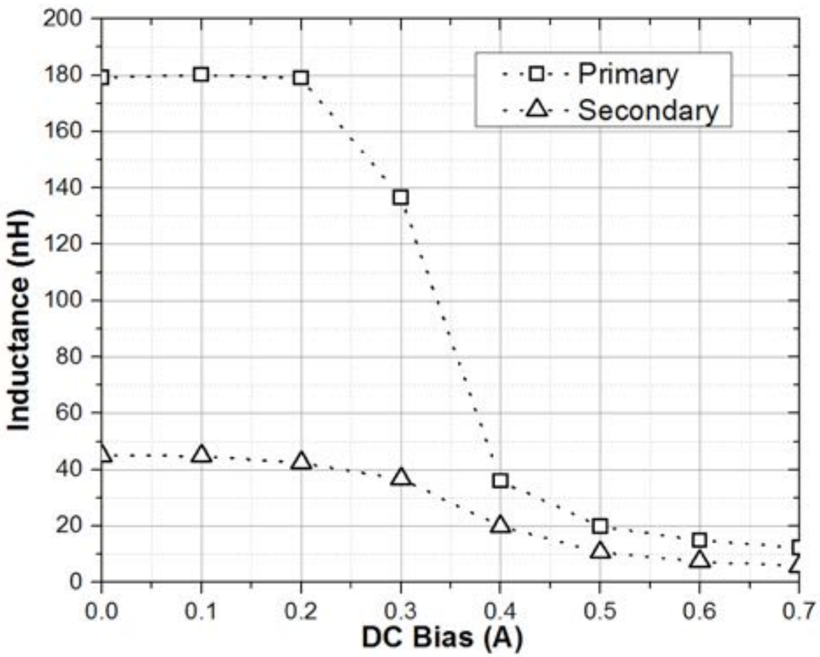


	Design (i)	Design (ii)	Design (iii)
Turns ratio	2:1	3:1	12:1
Primary Turns	24	24	24
Secondary Turns	12	8	2
Coil Width, µm	40	40	40
Core Width, µm	300	300	300
Core Length, µm	2200	2200	2200
Device Width, µm	712	721	712
Device Length, µm	2286	2286	2286

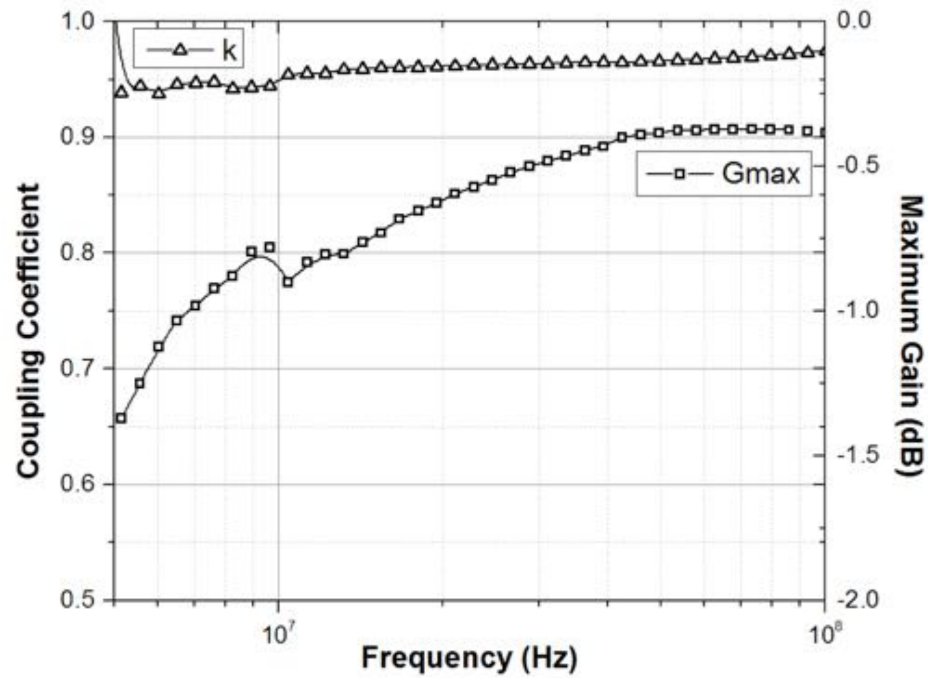


FERRIC DEVICES | *Transformer Electrical Performance*

	Design (i)	Design (ii)	Design (iii)
Turns ratio	2:1	3:1	12:1
DC resistance, Ω (primary, secondary)	1.35, 0.34	1.36, 0.17	1.39, 0.02
Inductance, nH (primary, secondary)	175, 44	166, 19	151, 2
Peak Q	16	14	11
Frequency, MHz	up to 80	up to 80	up to 100
Coupling coefficient	0.96	0.95	0.74
Saturation current, mA	300	300	300



Inductance versus applied DC bias of transformer design (i). The saturation current is defined as current when L drops by 20%, which is around 300 mA in this plot.



Coupling coefficient and maximum available gain of transformer design (i).

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- Ferric Thin-Film Power Inductors
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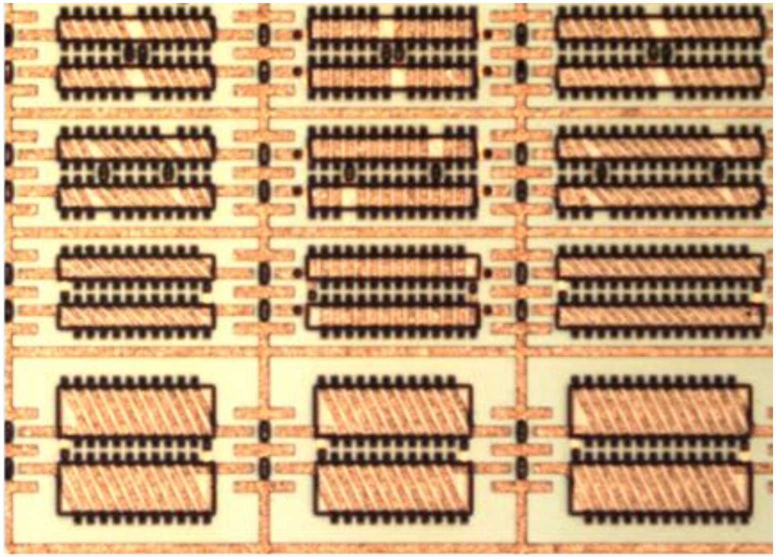
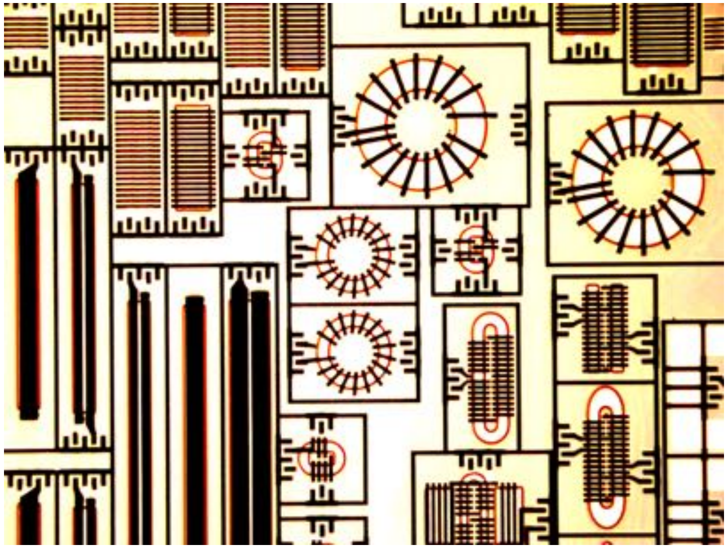
FERRIC INDUCTOR LIBRARY

- Many electrical parameters controlled by design with single fabrication process
  - Inductance, Resistance and saturation current
  - Coupling coefficient and turns ratio for transformers





Microscope image for a subset of Ferric Inductor Cell library devices

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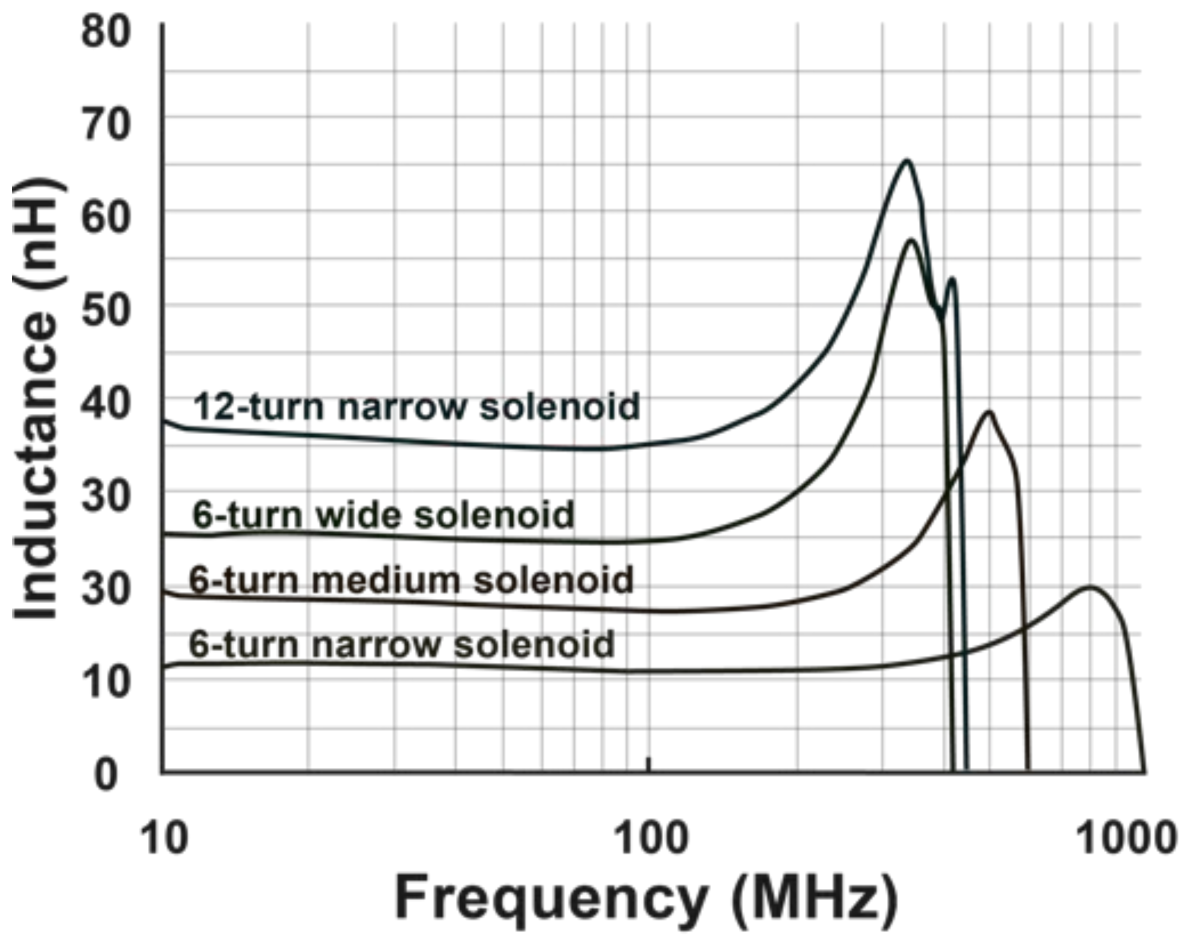
FERRIC INDUCTOR LIBRARY

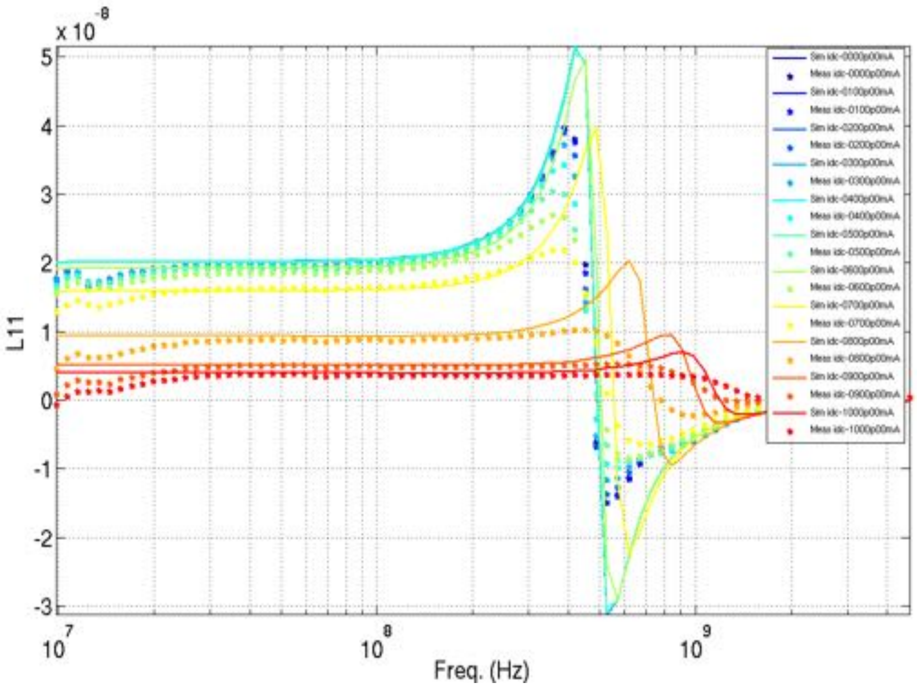
Wide inductor design space is covered with a single manufacturing process



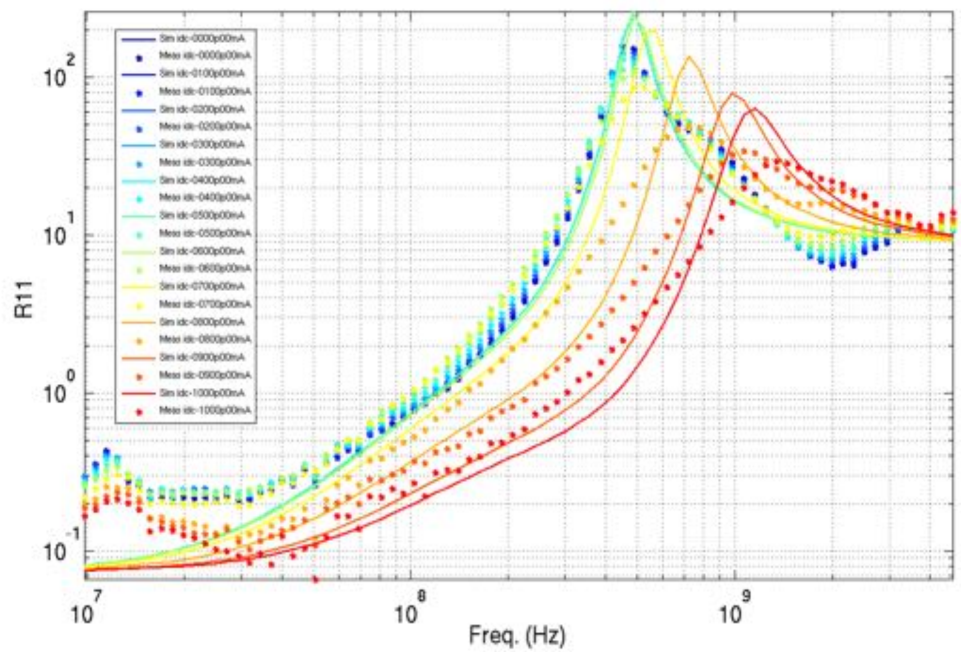
FERRIC INDUCTOR MODELS

L & R VS. FREQUENCY WITH I_{AVG} SWEEP: MEASUREMENT & SIMULATION

Broadband compact circuit models are available for Ferric Library devices including magnetic saturation



Measured inductor inductance data (dots) compared with SPECTRE model (lines)



Measured inductor resistance data (dots) compared with SPECTRE model (lines)

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FERRIC POWER CONVERTERS

Ferric's Package Integrated Voltage Regulator (PVR) is a single chip power management solution that integrates all components (Inductors and Capacitors) on a thin (250um) CMOS substrate for package integration

Key Features

Single Input Supply:	1.8V – 3.3V
Programmable Output Voltage:	0.4 – 1.6V
Large output current range:	1mA – 3A
Best-in-class power density:	2.2mm × 1.4mm × 0.25mm → 50kW/in^3
Efficient Operation:	> 85% conversion efficiency
High switching frequency:	20-120MHz

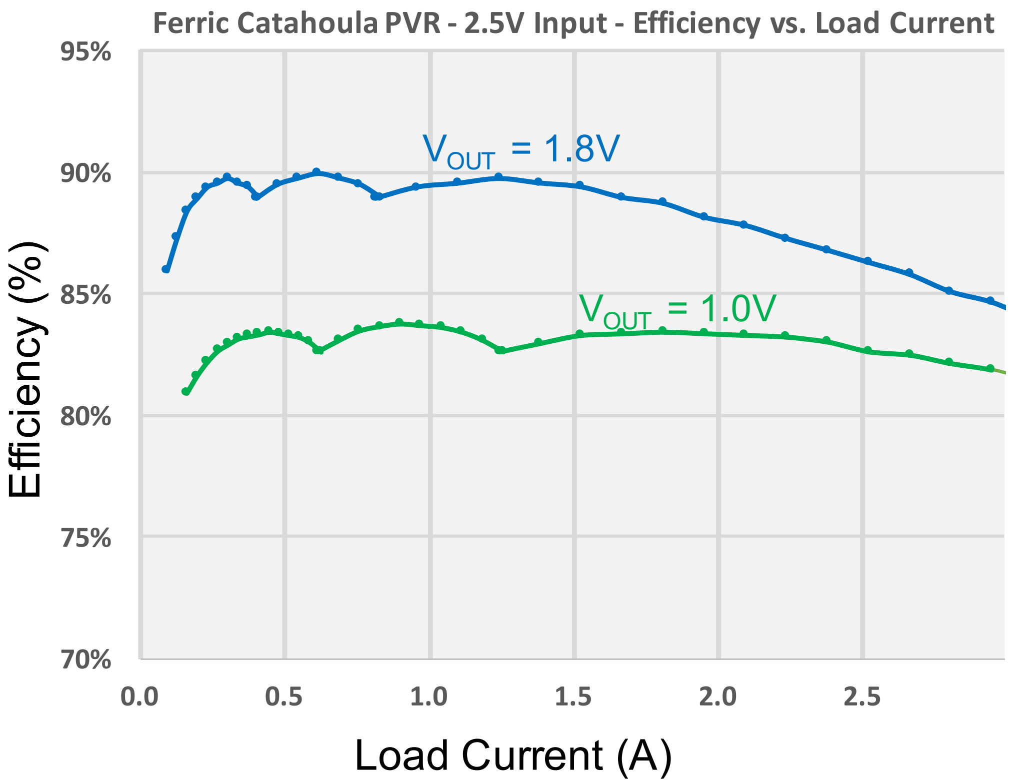
Integrated Inductor + Capacitor
Multi-Phase Operation with shedding

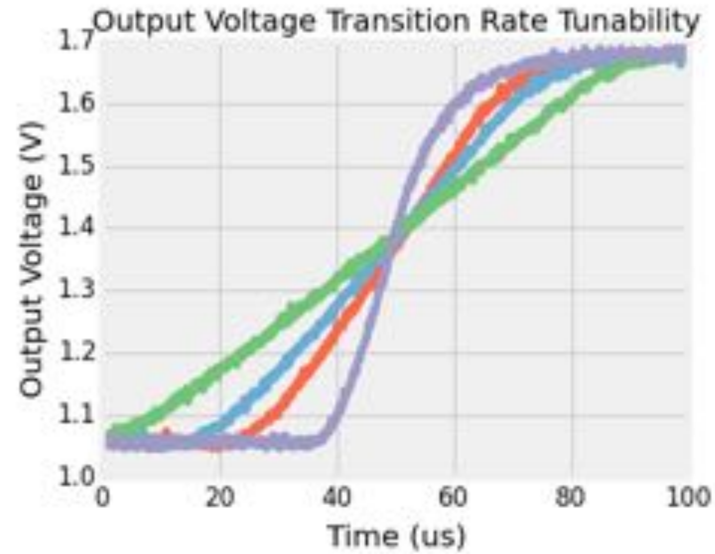
PMBus interface, Phase Shedding, Output LDO, Gang operation, Programmable soft start & Ramp Rates, Temperature sensor, Over voltage, Under voltage, Over/under current, non-volatile memory

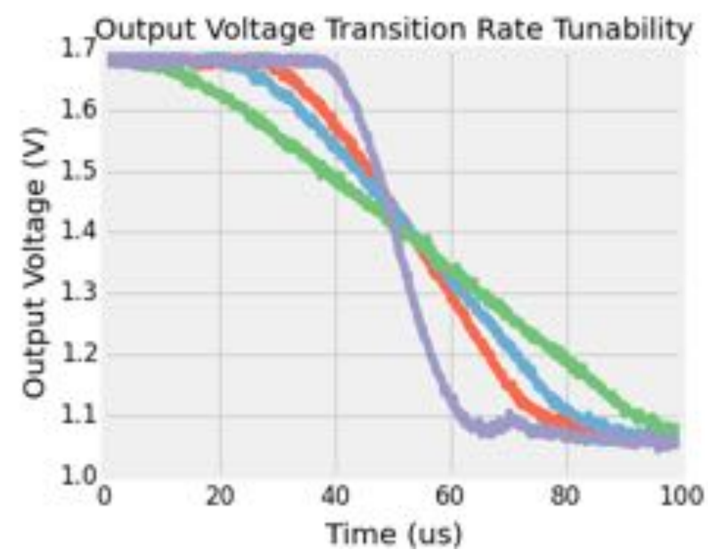
Applications

- Microprocessor Package VR
- Embedded PMIC (ePMIC)
- Smartphones & Mobile phones

FERRIC | *PVR* | *Measured Performance*

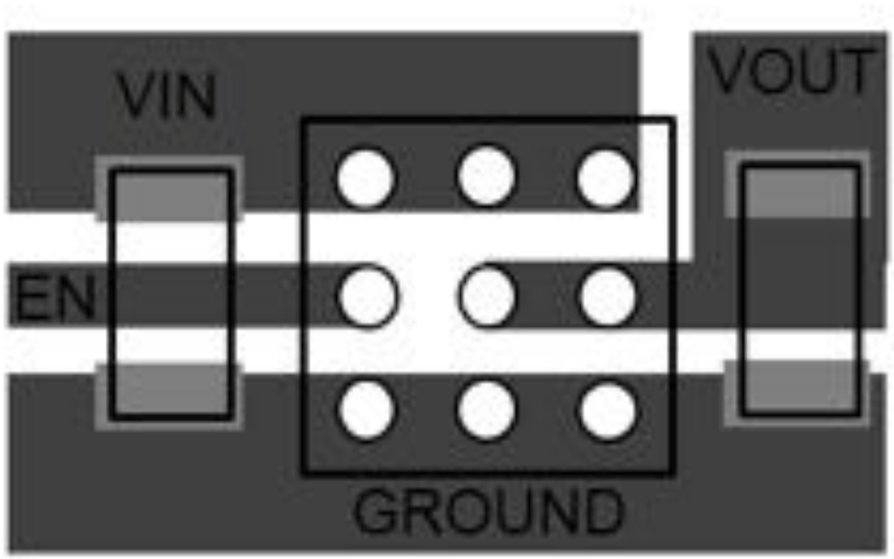






Various operating conditions (voltage, current) and current density design points have been realized

FERRIC | µVR | BOOST CONVERTER



- Total Solution Size: ~3.0mm^2
  - 1x WLCSP Boost Converter Chip (1x 1.44mm^2)
  - 2x 0402 Discrete Capacitors(2x 0.5mm^2)

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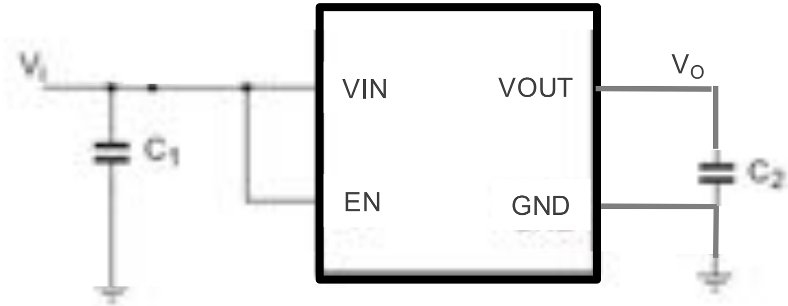
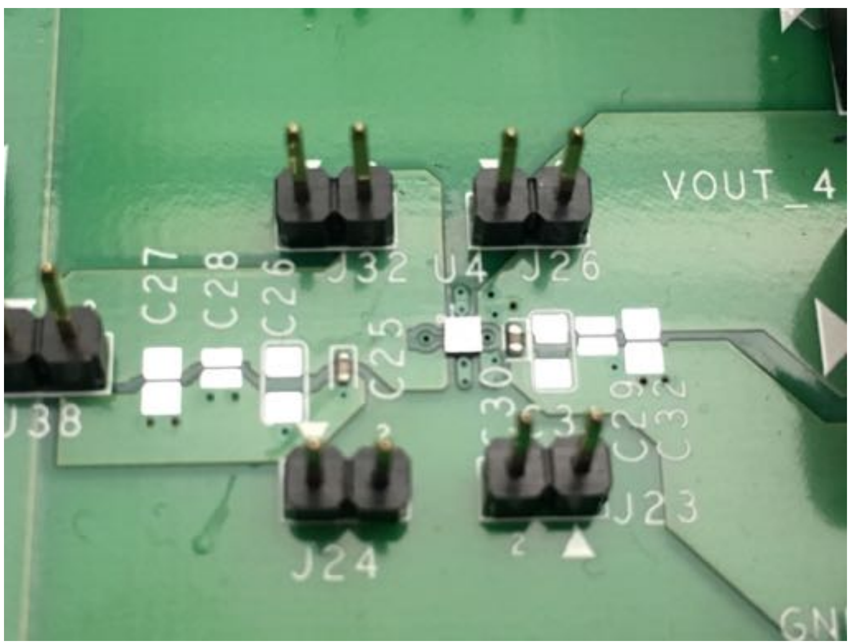
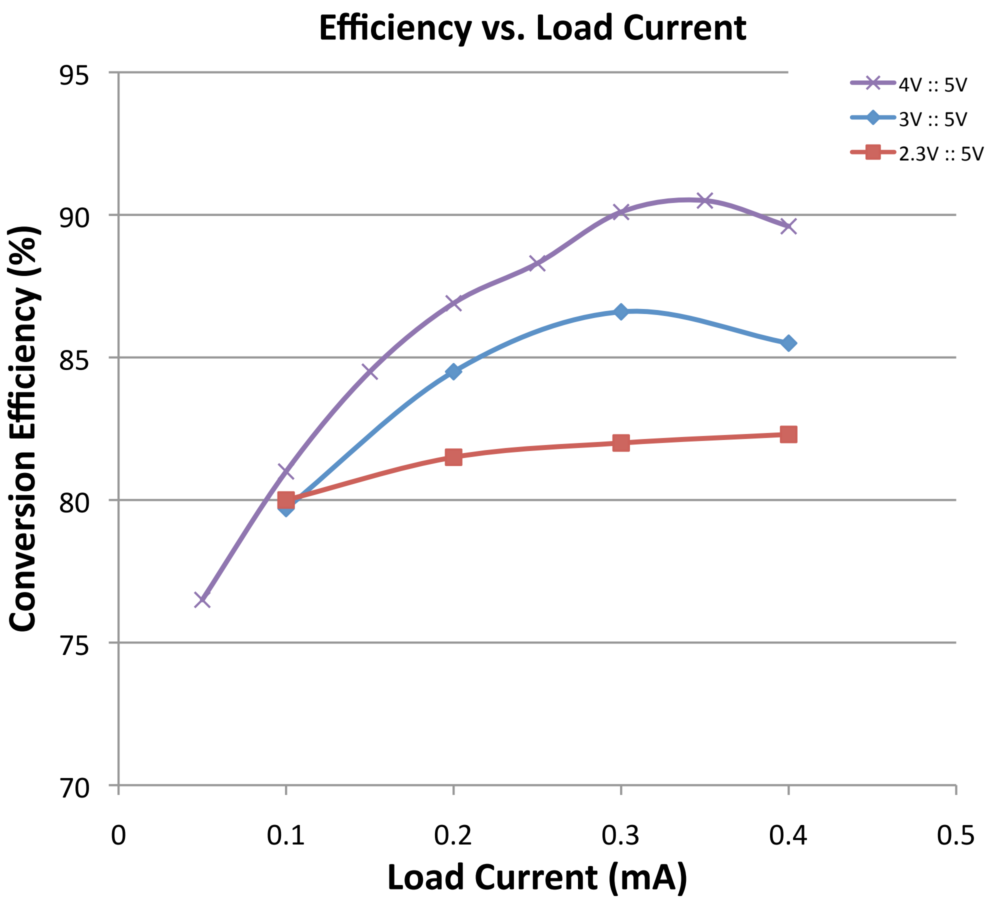
FERRIC | µVR | BOOST CONVERTER

Ferric Integrated Inductors at TSMC removes requirement for external inductors





FERRIC | μVR | BOOST CONVERTER



	Voltage
VOUT	5V
VIN	4.6V - 2.3V
CMOS node	TSMC 130nm (CM013G)
IO tech	WLCSP - 400um Pitch
Chip dimensions	1.2mm X 1.2mm
Inductance	Integrated
Capacitance[1]	2x 20uF External
operating temperature	0C - 85C (ambient)

1- Efficiency projections determined by spectre simulation with TSMC 0.13um PDK models and Ferric inductor models

QUESTIONS?