Electrical and Thermal Packaging Challenges for GaN Devices

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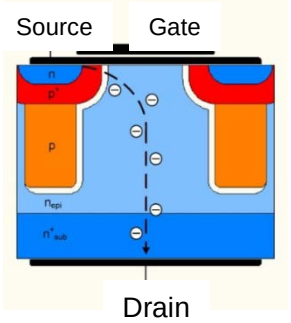
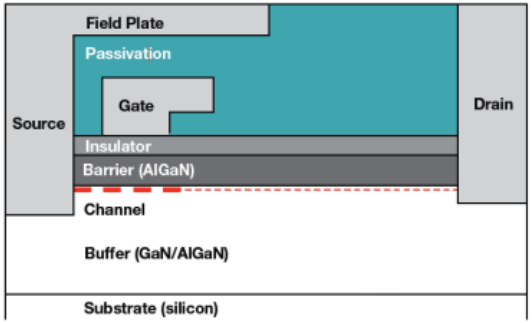
Outline

- Why GaN?
- Hard-Switching Losses
- Parasitic Inductance Effects on Switching
- Thermal Challenges of Surface Mount Packages

Why GaN?

- Zero reverse-recovery enables efficient hard-switched CCM converters
- Low output capacitance reduces switch charging losses enabling faster switching speeds
- Low input capacitance reduces gate drive losses enabling higher switching frequency
- Higher switching speeds reduce transformers, inductors, and capacitors size
- Lateral structure enables integration

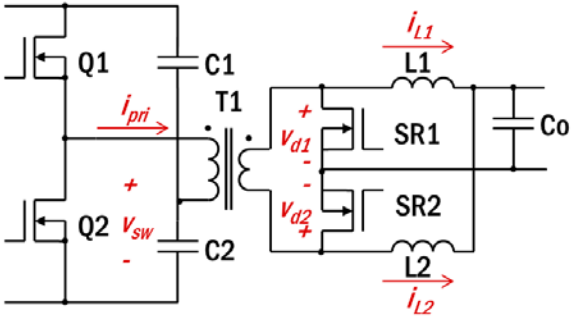




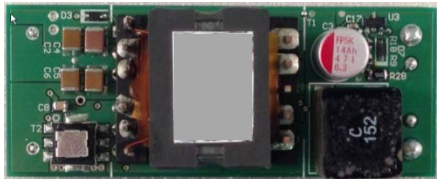
	Silicon MOSFET	TI – GaN (HEMT)
Device Structure	Vertical – no integration	Lateral- allows integration
Rds,on – Area metric	>10 mΩ-cm^2	5-8 mΩ-cm^2
Gate Charge	~ 4 nC-Ω	~ 1-1.5 nC-Ω
Output Charge	~25 nC-Ω	~ 5 nC-Ω
Reverse Recovery	Significant	None

Why GaN? - 48V to POL

- GaN enables single stage efficient hard-switched POL converter
- Single conversion
  - reduces component count in half
  - ~3x power density improvement
- Hard-switched topology improves transient response



48V – 12V Bus Converter
92-97% Efficient

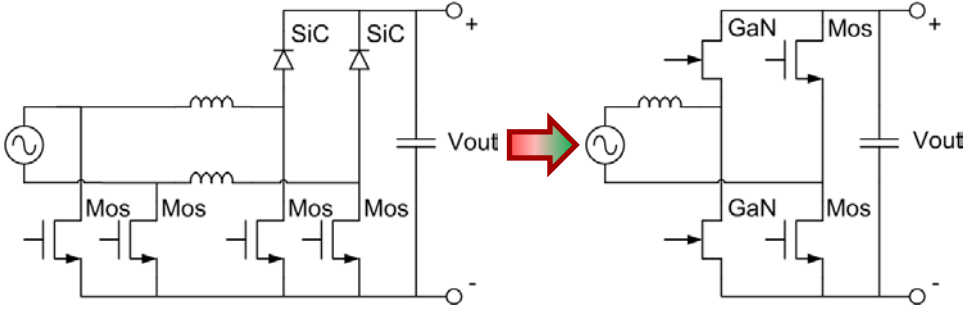


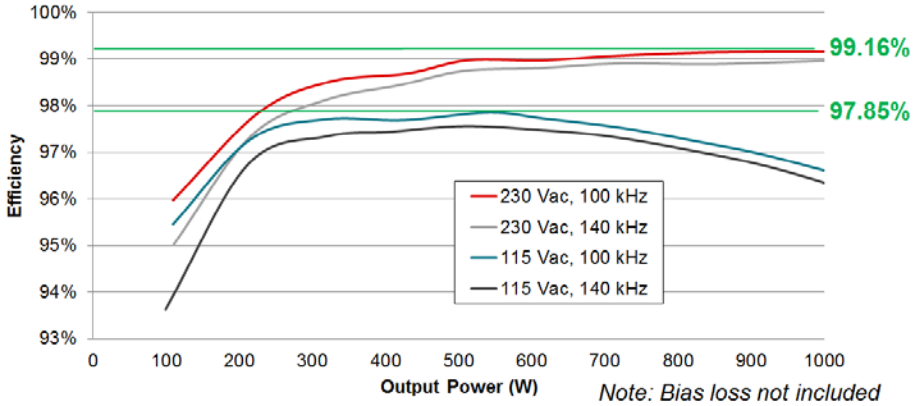
12V POL Multi-phase Buck
85-93% Efficient

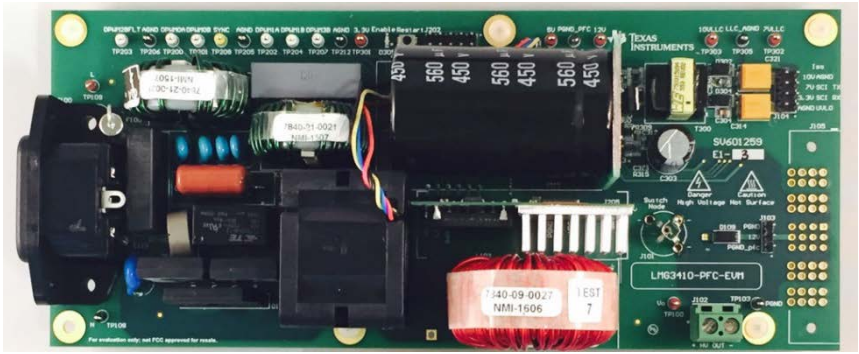
LMG5200POL EVM: 48V to 1V

Why GaN? – CCM Totem Pole PFC

- GaN enables CCM Totem Pole PFC
  - No Qrr
  - Low switching losses
- GaN enables higher switching frequency
  - Reduces inductor size
- CCM Totem
  - Lower components
  - 30% higher power density







1kW Totem Pole PFC

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- Why GaN?
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- Parasitic Inductance Effects on Switching
- Thermal Challenges of Surface Mount Packages

Hard Switching Loss

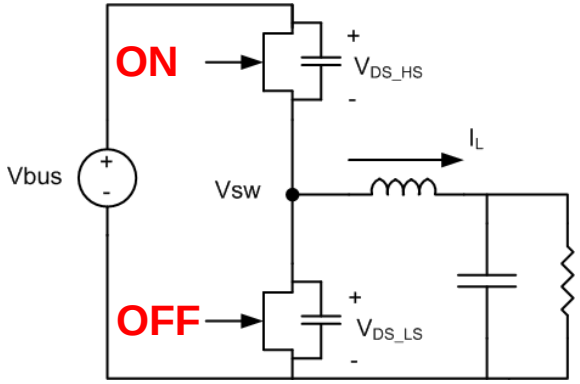
In CCM with positive inductor current, the high-side device dominates the switching losses. Turning on the high-side device faster will reduce the losses due to the inductor conducted through the high-side device during $t_1 – t_2$ and $t_2 – t_3$. E_{oss} and E_{ch} are determined by C_{oss} and Vbus.

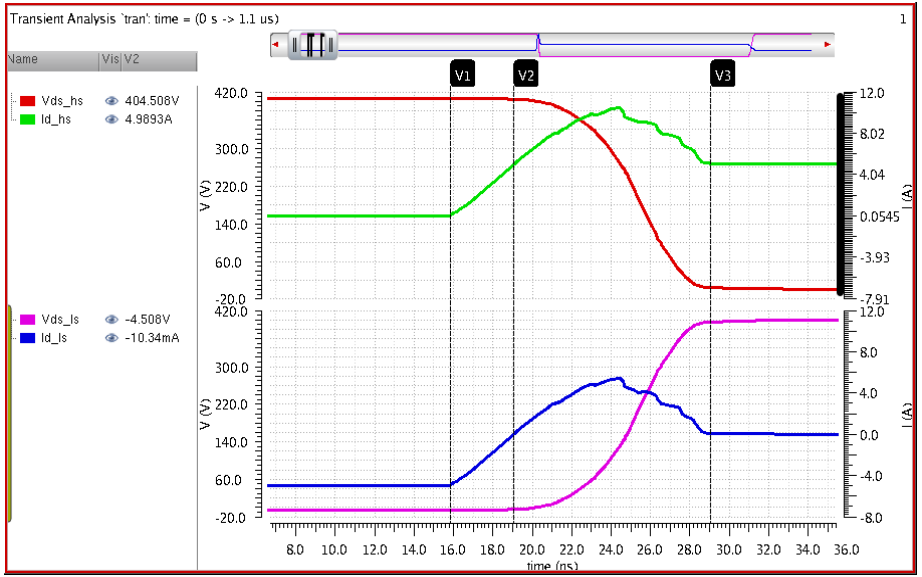
High Side Loss:

$$P_{hs} = V_{bus} * \frac{I_{ind}}{2} * \frac{t_{1\_2}}{\tau} + \frac{V_{bus}}{2} * I_{ind} * \frac{t_{2\_3}}{\tau} + f_{sw} * (E_{oss} + E_{ch})$$

Low-Side Loss:

$$P_{ls} = V_{ds\_3q} * \frac{I_{ind}}{2} * \frac{t_{1\_2}}{\tau}$$





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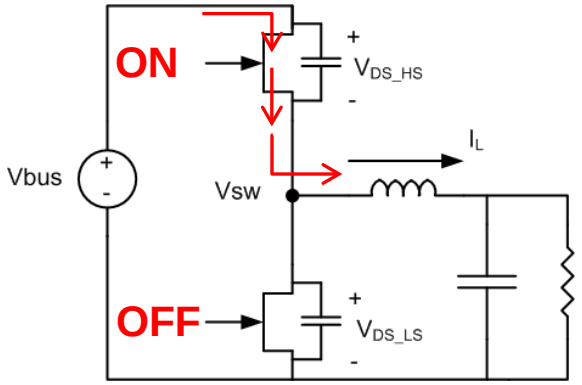

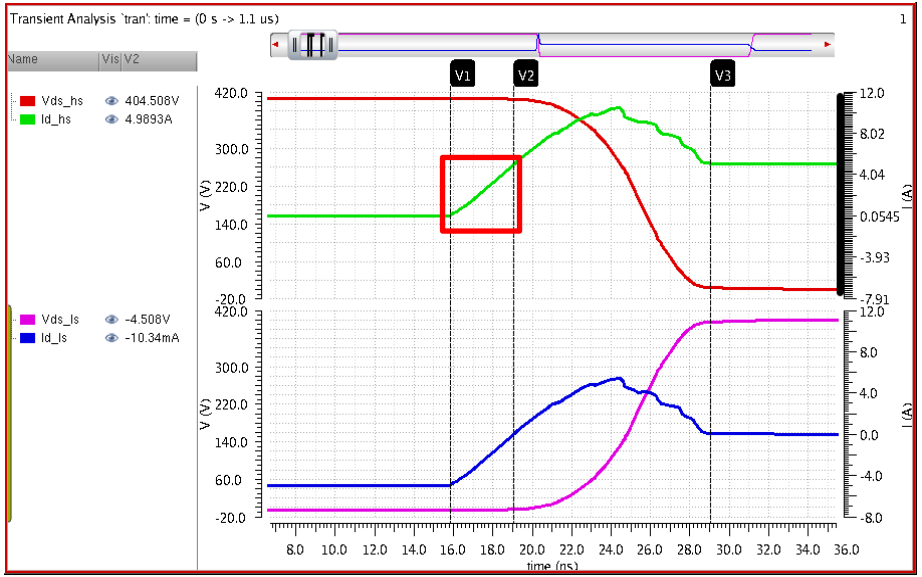

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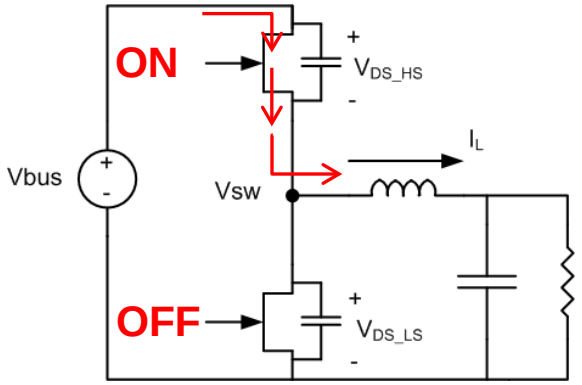

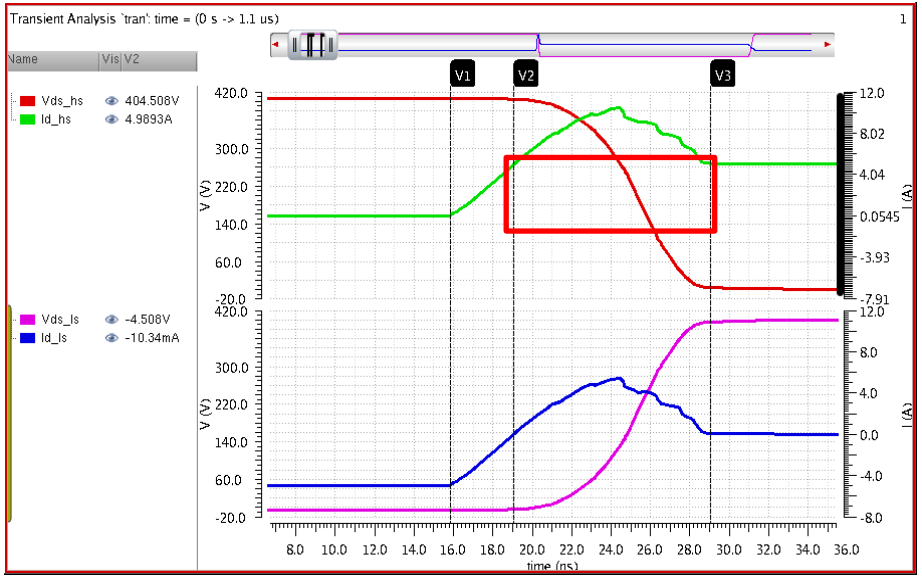

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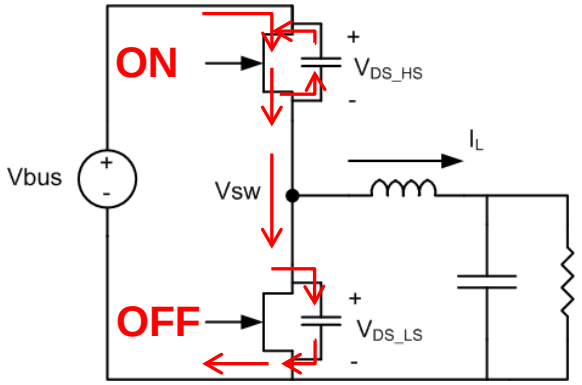
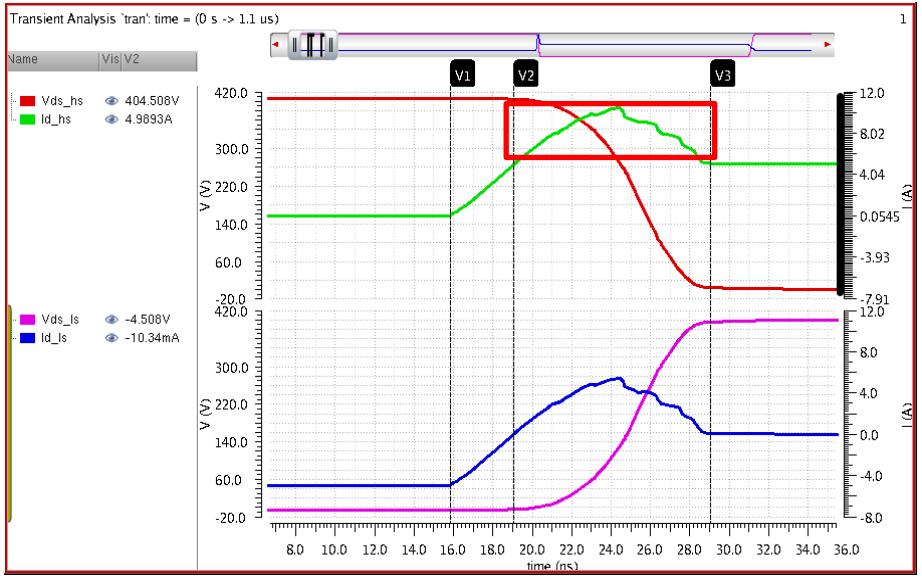




Eoss vs Ech

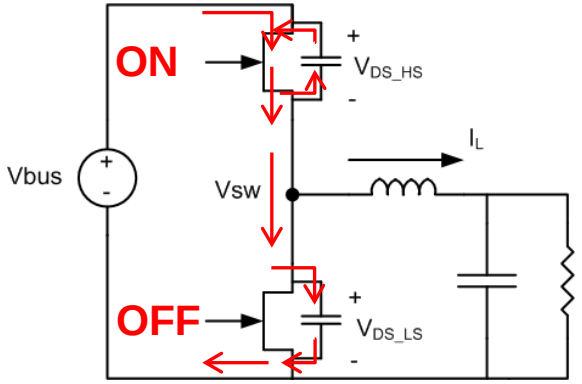
- C_{oss} is very non-linear for GaN and most high voltage power devices
- E_{oss} is the energy stored in the C_{oss} at a defined V_{ds}

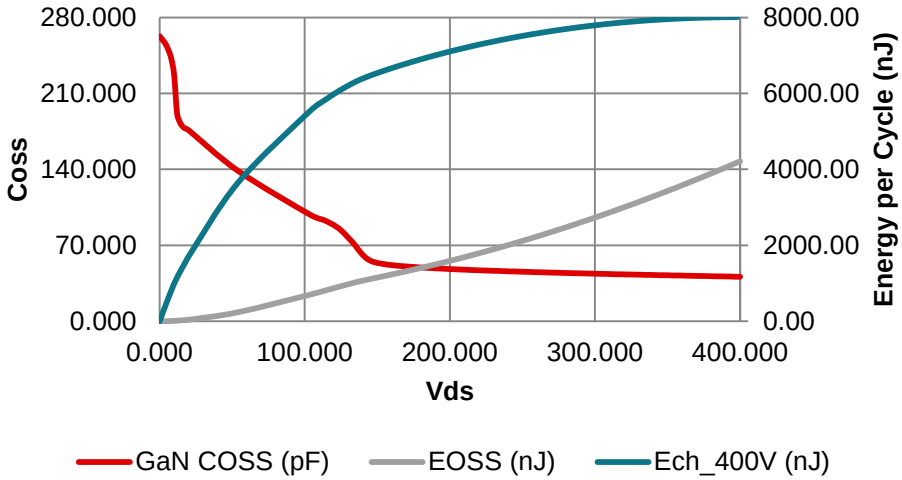
$$E_{oss} = \int_0^{V_{bus}} C_{oss}(V_{ds}) * V_{ds}\, dV$$

- E_{ch} is the energy dissipated in the high-side when charging the low-side C_{oss}

$$E_{ch} = \int_0^{V_{bus}} C_{oss}(V_{ds\_ls}) * (V_{bus} - V_{ds\_ls}) dV$$

- $E_{ch} > E_{oss}$ when C_{oss} is larger at low V_{ds}
- Any parasitic SW node capacitance will sum with C_{oss} of the low-side fet
  - No snubbers





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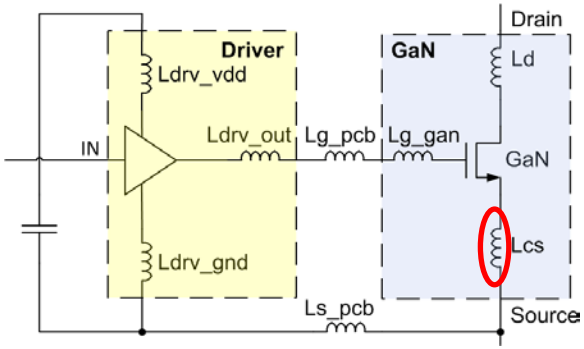
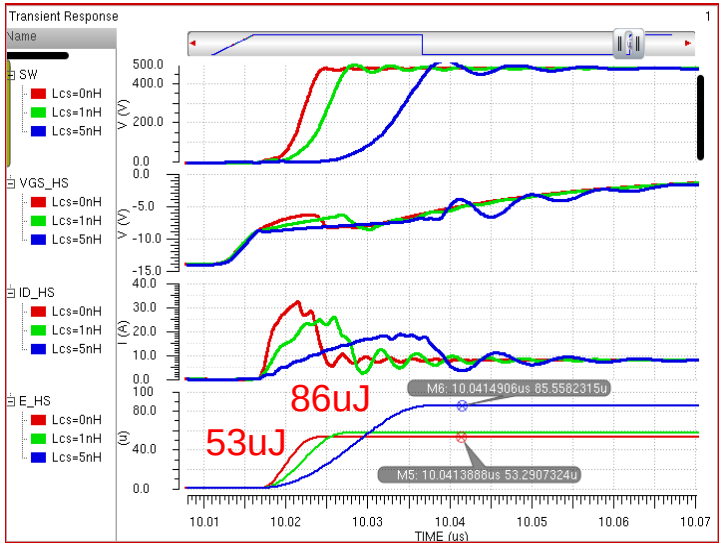
- Parasitic Inductance Effects on Switching
- Thermal Challenges of Surface Mount Packages

Common Source Inductance

- Common Source inductance reduces the di/dt during turn-on and turn-off.
  - Increases power dissipated during the di/dt ramp
- 5nH common source inductance increases turn-on loss by 60%

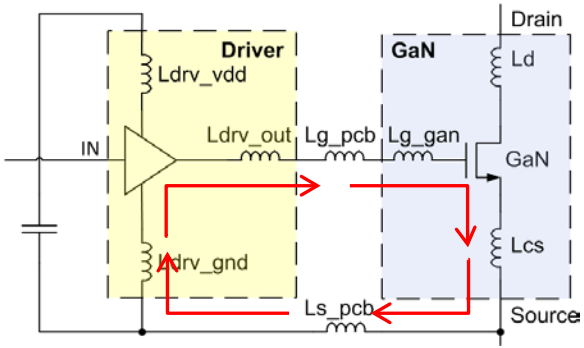


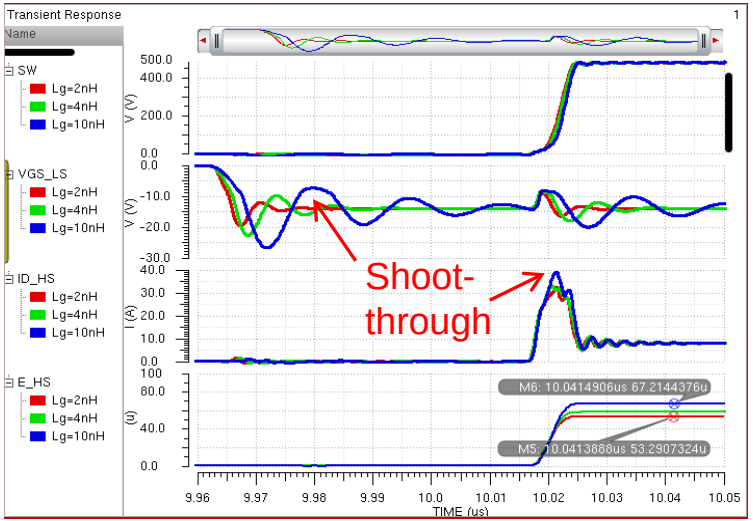


High-side turn on versus common-source inductance: red = 0 nH, green = 1 nH, blue = 5 nH

Gate Loop Inductance

- Gate loop inductance increases the impedance between the gate and the driver.
  - Limits the ability to hold off the GaN device during the Vds ramp
  - Shoot through increases the power dissipated in the high-side device and can cause it to fail due to SOA.
- Gate loop inductance increases ringing
  - Higher stress on gate
  - Ringing can cause the device to turn-on/off
  - Loop resistance is required to dampen ringing

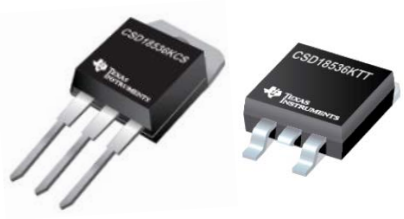




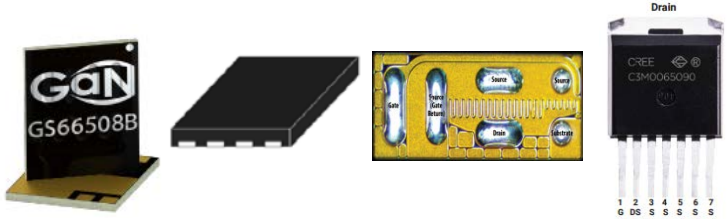
Low-side hold-off versus gate-loop inductance
red = 2 nH, green = 4 nH, blue = 10 nH

Reduction of Common Source & Gate Loop Inductance

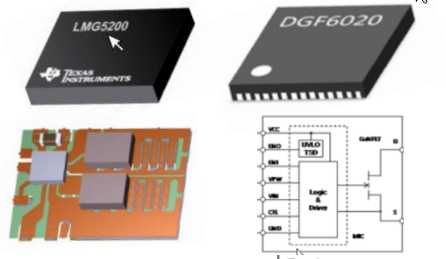
Standard Packages

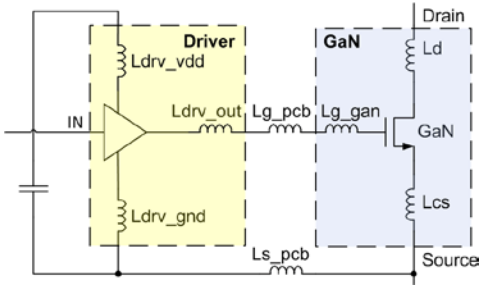


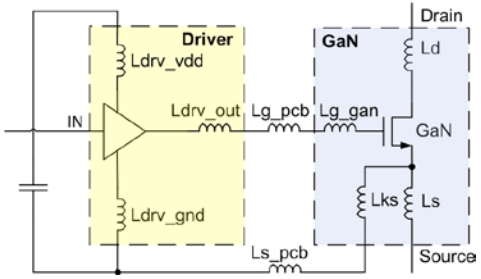
Kelvin Source Packages

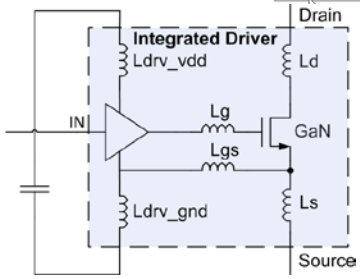


Integrated Driver Packages





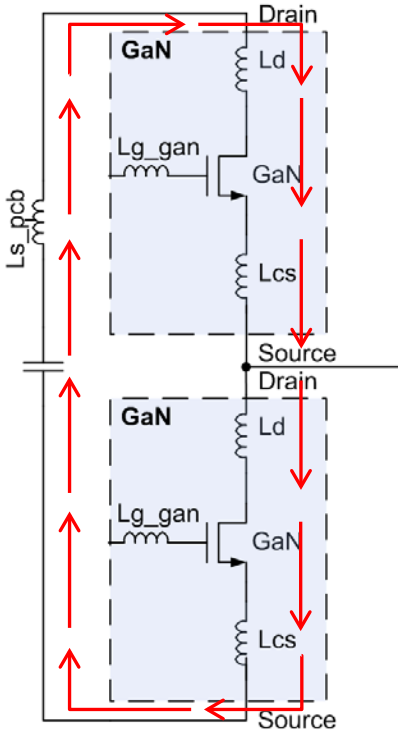


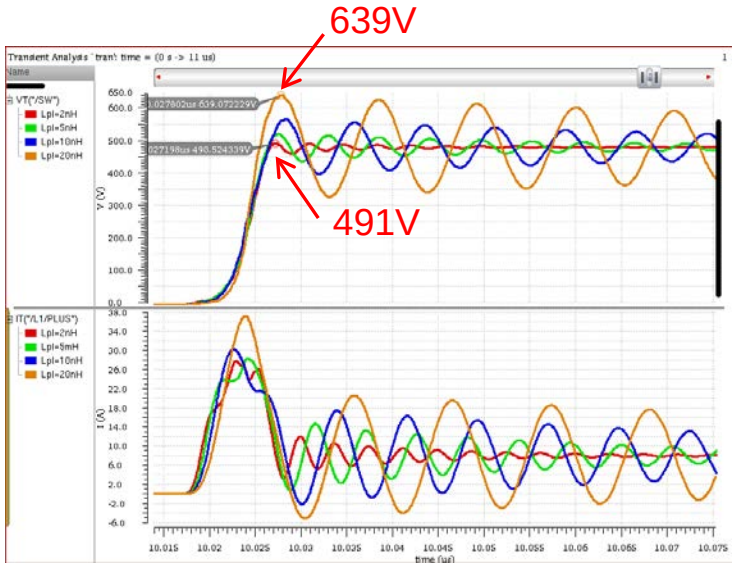


	Standard Power Package	Kelvin Source Power Package	Integrated Driver Power Package
Common Source	2nH -10nH	<1nH	<1nH
Gate Loop	5nH – 20nH	5nH – 20nH	1nH – 4nH

Power Loop Inductance

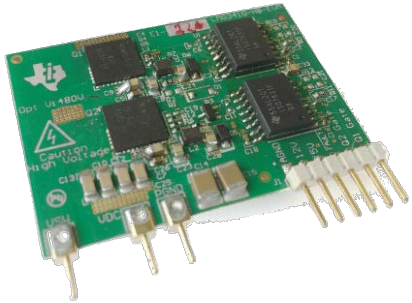
- Power loop inductance
  - Increases Ringing and EMI
  - Increases V_{ds} voltage stress
  - Increase switching losses
- Package must be designed to enables low power loop inductance PCB layout
- GaN must be switched without snubber to have high efficiency



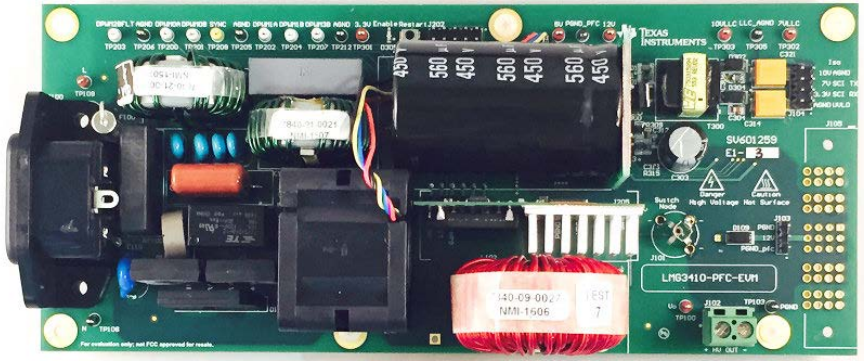


V_{sw} ringing versus power loop inductance
red = 2nH, green = 5nH, blue = 10nH, orange = 20nH

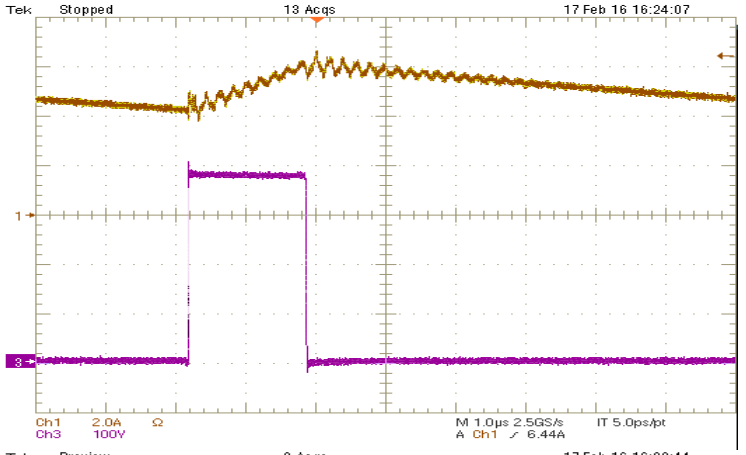
CCM Switching Waveforms

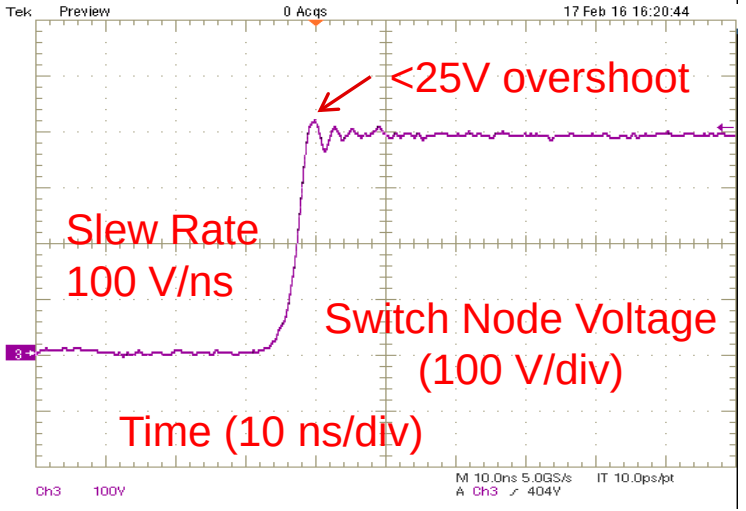


LMG3410 HB EVM



1kW Totem Pole PFC





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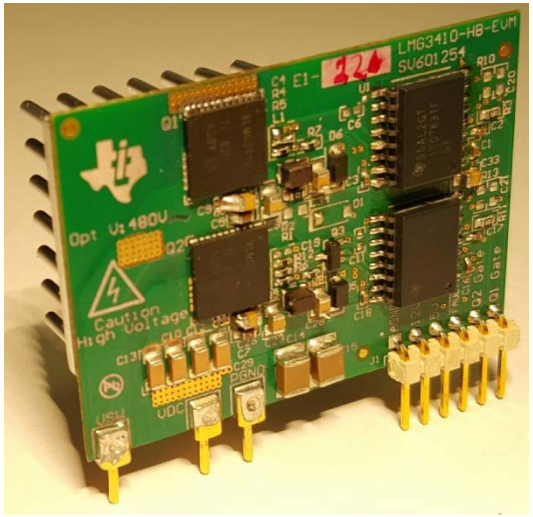
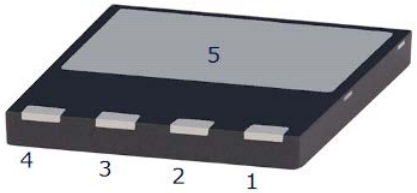
Thermal

- Power packages need to have good thermal dissipation capability
- GaN has high R_{ds_on} temperature coefficient.
  - Lower junction temperature reduces conduction loss
- Surface mount packages do not dissipate power as well as traditional leaded packages
  - Heat dissipates through PCB
  - Typically have smaller heat spreaders

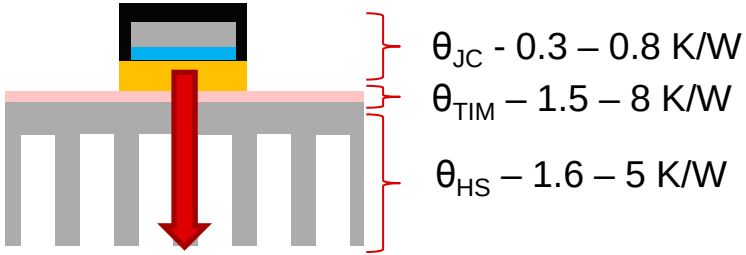


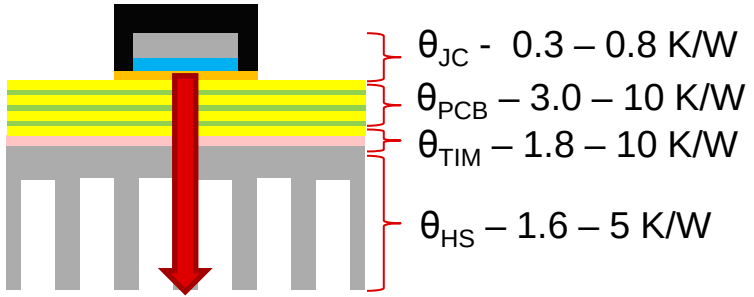
Thermal Dissipation

Power dissipation: ~12 W
(50C ambient and 110C max junction temperature)



Power dissipation: ~7 W
(50C ambient and 110C max junction temperature)

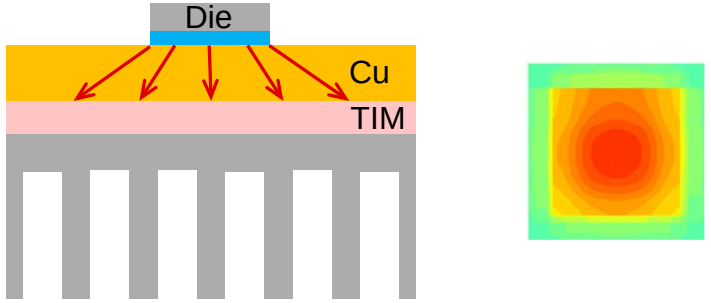




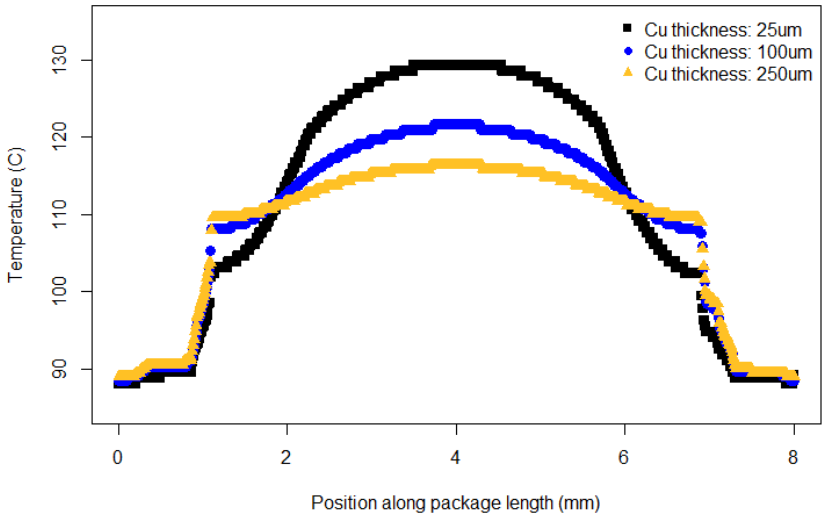
Package Thermal Pad

- Area of thermal pad must large enough to reduce thermal resistance of TIM
- Thermal pad must have sufficient thickness to spread heat over TIM

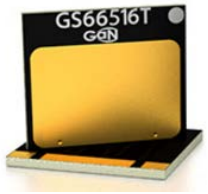
$$\Delta T_{TIM} = \frac{P_{diss} \times A_{TIM}}{d_{TIM} \times \lambda_{TIM}}$$

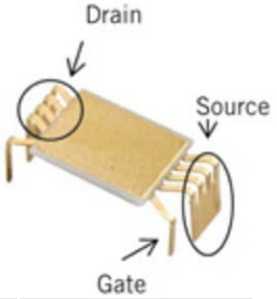


7x7mm Thermal Pad vs Thickness



Package Comparison





Package	TO220	QFN	Bumped Die	Embedded	TOLL	Sintered Dual Cool
Common Source Ind	--*	++	++	++	++	++
Gate Loop Ind	--	++	++	++	++	+
Power Loop Ind	--	++	++	++	++	+
Thermal	++	+	-	+	+	++**
Cost	++	++	++	-	+	--

* Additional kelvin source pin eliminates common source inductance

** Includes isolation

Conclusions

- GaN's lower switching losses enables high efficiency and high density designs
  - No reverse recovery
  - Low Qoss and Qiss
- Low inductance package is required to realize GaN switching performance
  - Low common source inductance to reduce losses during di/dt phases
  - Low gate loop inductance to hold device off and reduce gate ringing
    - Integrating the driver in the package will minimize gate loop and common source inductance
  - Package must enable low power loop inductance PCB layout
    - Power loop must be designed without snubbers
- GaN package must have good thermal performance
  - Large thick power pad to spread heat and lower TIM drop
  - Direct thermal connection to heat sink eliminates PCB thermal resistance

Thank You