Heterogeneously Integrated Power Stages enable Granular Power Delivery

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Agenda

- **Introduction**
- **GaAs Enables Smallest, Fastest Voltage Regulators**
- **Integration is Required for Maximum Performance**
- **Heterogeneously Integrated Power Stage (HIPS)**
  - HIPS Prototypes Demonstrate Low Switching Loss
  - HIPS Advantages Versus MOSFETs and GaN FETs
  - HIPS Enables Granular Power
- **Summary**

Requirement: Double Compute Density Every 2 Years

- **10x increase in performance and data consumption**
  - IoT (Internet of Things)
  - Artificial intelligence (AI)
  - Cyber security
  - Virtual reality

	2014	2020
Digital universe (zettabytes)	4.4	44
Mobile data (exabytes per month)	3.3	30.5
Wireless networks *Data rates*	3G *2 Mbps*	5G *>1 Gbps*
Internet users (billions)	2.8	3.9
Connected devices (billions)	14	50
Connected sensors (billions)		200

- **10x increase in compute density**
  - 2.4 → 24 GFLOPS/Watt (2015 → 2023)
  - Requires radical improvement in energy efficiency

$$\text{Compute Density} = \frac{\text{Performance (GFLOPS)}}{\text{Power (Watts)}}$$

Increase performance in given thermal envelope

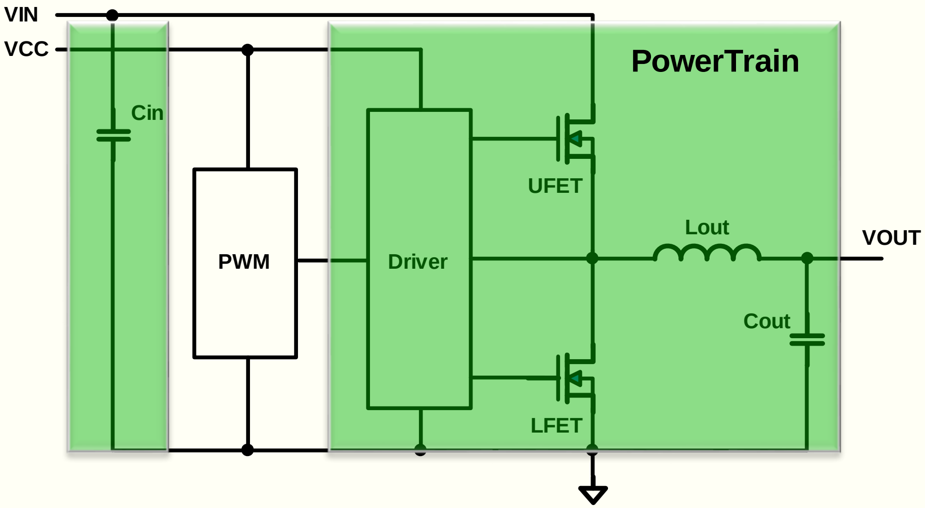
2015 International Technology Roadmap for Semiconductors (ITRS)
Running out of Power for Data Centers

- **Small, fast voltage regulators provide a new "tool-in-the-toolbox" to increase compute density**

ARDA

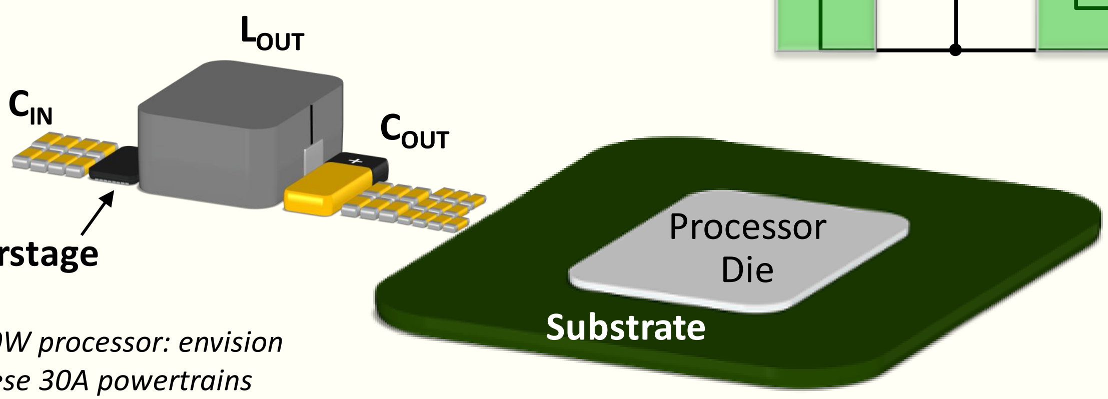
State-of-the-art VRs for SoCs

Simplified Buck Voltage Regulator (VR)



Typical 12Vin, 1Vout, 30-40A Power Train:

Fsw ~ 500-800kHz



For 150W processor: envision 5 of these 30A powertrains

Today's board-mounted VRs

- ***Good "static" efficiency*** – typically >90% achievable
- ***Bulky***
- ***Slow***

Another Approach: Fully Integrated Voltage Regulator (FIVR)

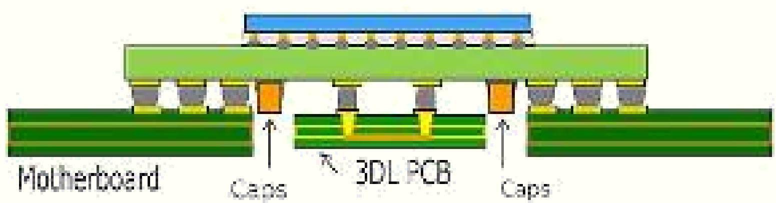
Advantages

- Many VRs integrated in processor die individually convert V_{in} to voltage levels needed for different processor cores
- 1.8V V_{in} relaxes external VR's duty cycle requirements

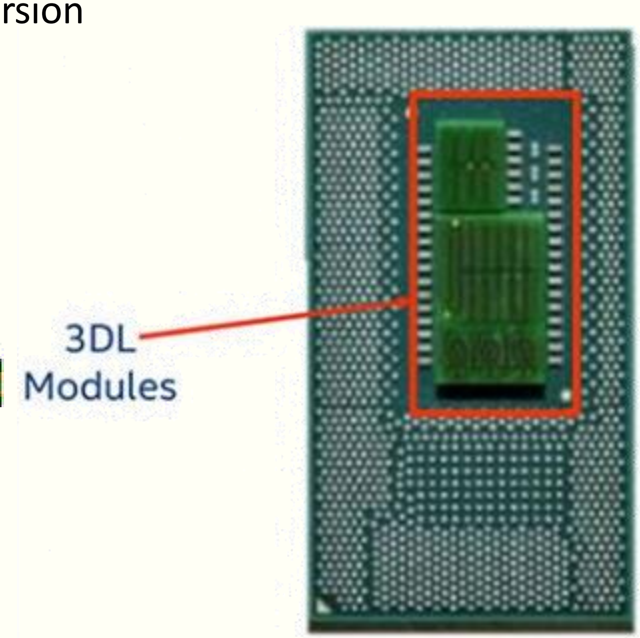
Disadvantages

- VR heat dissipation consumes part of processor's thermal budget
- High cost due to:
  - Inductors
  - MOSFETs consume expensive processor die area
- Susceptible to voltage droops (due to small on-chip LC filter)
- Requires VR on system motherboard to supply 1.8V
- Low efficiency due to 2-stage conversion

Supplier: Intel



The Broadwell SoC and Module

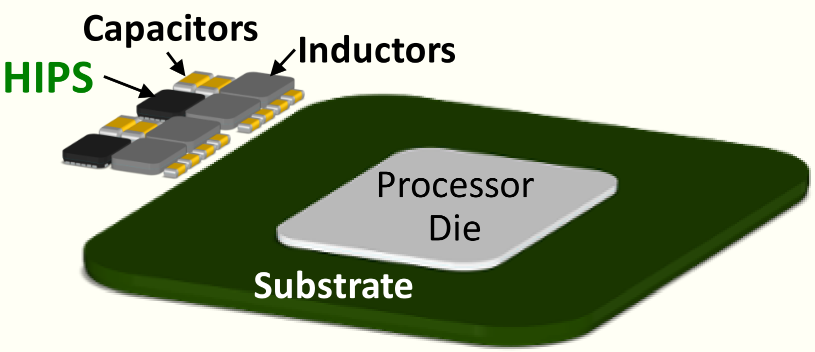


Sarda's Approach

Market Entry

High Density Board-mounted VRs

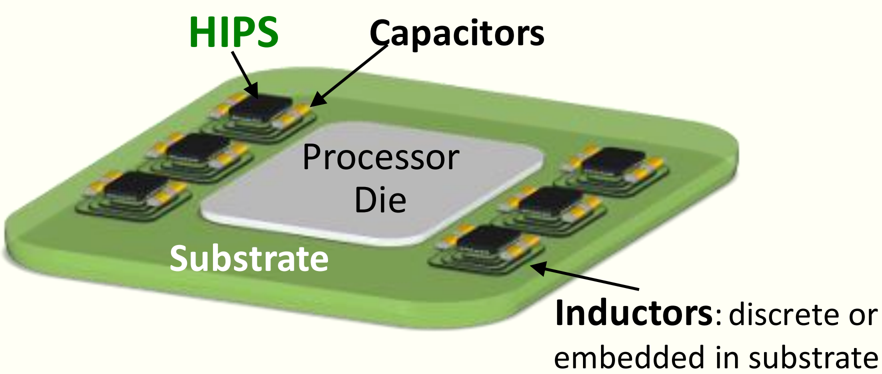
Fsw = 2-5MHz



Ultimately

Package-integrated VRs (PIVRs)

Fsw = 5-10MHz+



Advantages vs. slow, bulky VRs

- ***Frees up board space*** – for more processing power, memory, etc
- ***Lower profile*** – fit under heat sinks, on back side of board
- ***Improved "dynamic" efficiency***
- ***More granularity***

HIPS: Heterogeneously Integrated Power Stage

Advantages vs. Fully Integrated VRs

- ***Higher performance*** – higher efficiency due to single-stage dc-dc
- ***Higher input voltage*** (4-12V) – reduces number of power/ground pins
- ***Flexible*** – more easily optimized for different processor speed bins
- ***Better thermally*** – VR heat dissipated into substrate/heat sink

Advantages of GaAs FETs

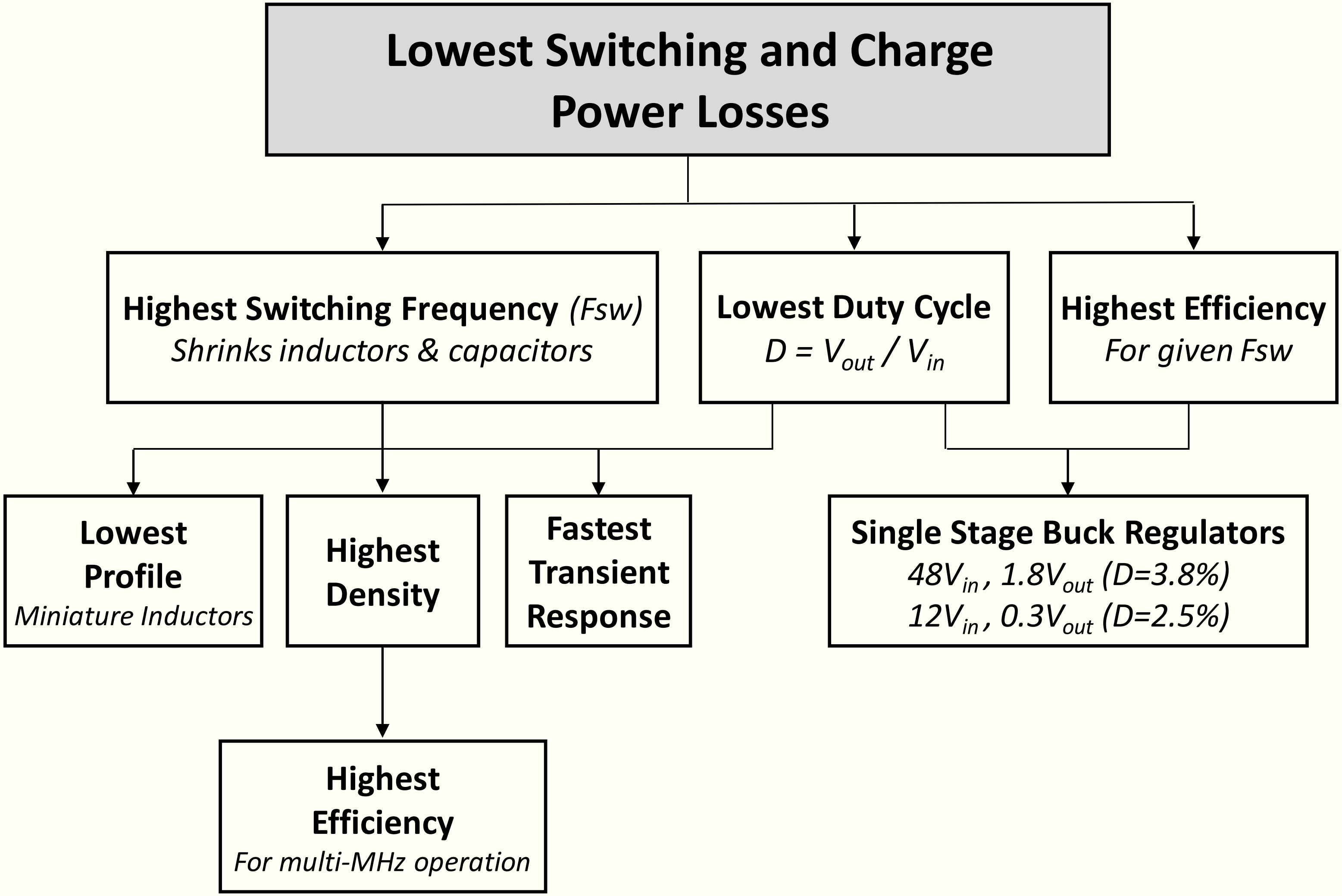
Versus GaN FETs and Silicon MOSFETs for >10A, 12V_{in}

Merit
Demerit

	GaAs FETs	GaN-on-Silicon FETs	Vertical MOSFETs	GaAs Benefits
Electron mobility (cm^2/Vs)	8,500	1,800	1,400	Faster switching
$R_{DS(on)}$*Q_G (mΩ-nC)	<10	20-30	20-60	Lower switching loss
FET switching times (ns)	<1	1-2	2-5	
Body diode	No	No	Yes	
Loop Inductance (nH)	~0.2	~0.4	1-2	
FET structure	Lateral	Lateral	Vertical	Multiple FET monolithic integration • Reduces parasitics • Enables multiple outputs / phases
Bandgap (eV)	1.4	3.4	1.1	Higher junction temperature
Activation energy (eV)	2.5	1.1-2.5	0.3-1.2	Higher reliability
Gate oxide?	no	yes	yes	
2018 market size	$8B	$0.4B	>$10B	Leverages proven manufacturing

GaAs FET Benefits

For 12-48V_{in} Power Stages



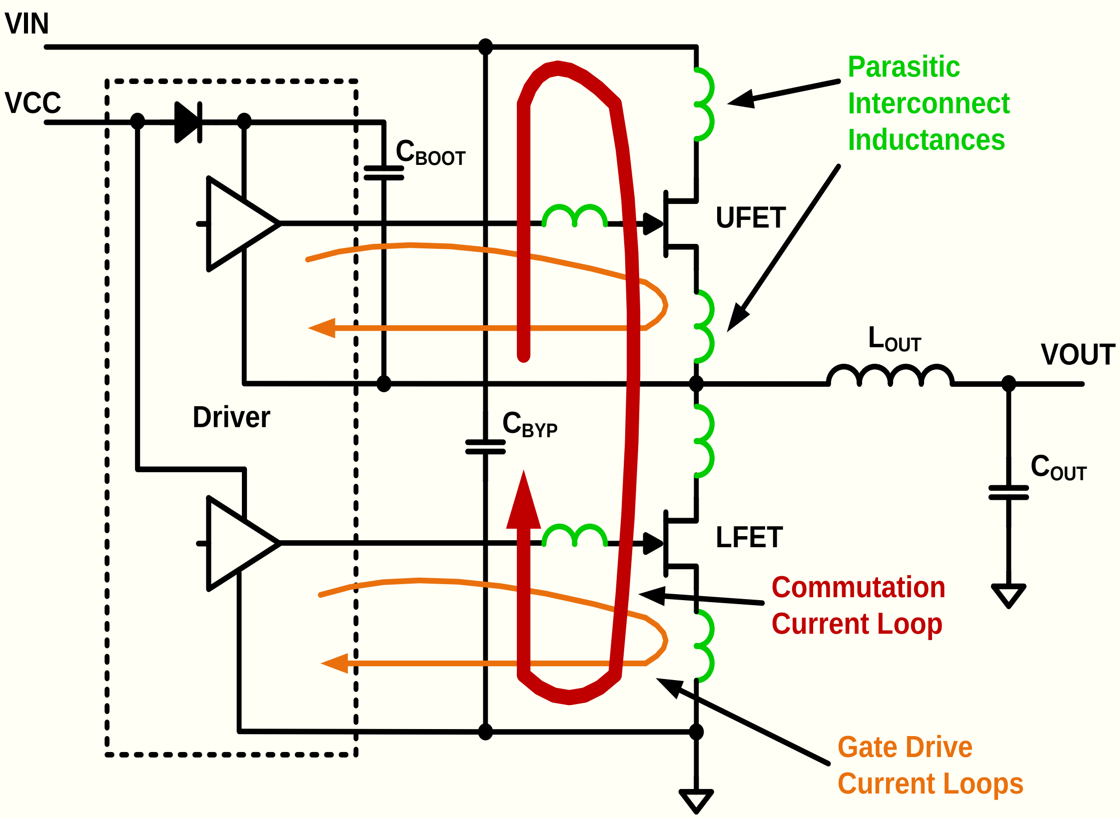
Integration is Required for Maximum Performance

Minimize

- Common source inductance
- Gate drive loop
- High frequency input commutation current loop

Approach

- Monolithic integration of GaAs FETs
- Co-pack GaAs FETs and drivers
- Co-pack GaAs FETs and bypass capacitors



Heterogeneously Integrated Power Stage (HIPS)

Integrates in 3D SiP *(3-dimensional system-in-package)* for **efficient, multi-MHz operation**

- **GaAs FET die**
- **CMOS driver die**
- **Passive components**
  Minimize parasitics

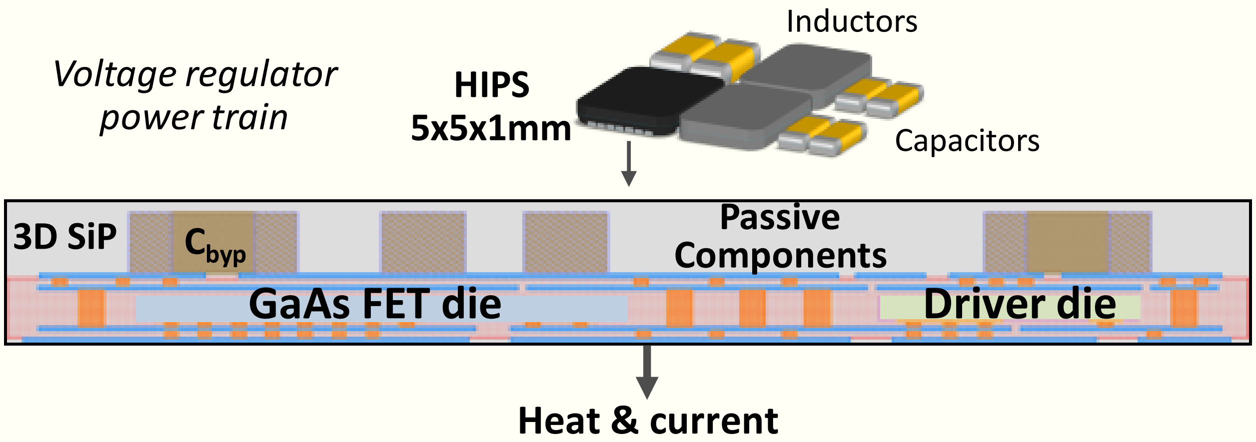
Many phases

Support ever widening dynamic range

I_{out} = 5-20A per phase

I_{max} = ~30A per phase

Voltage regulator power train



No heat sink

<2.5W at I_{out}

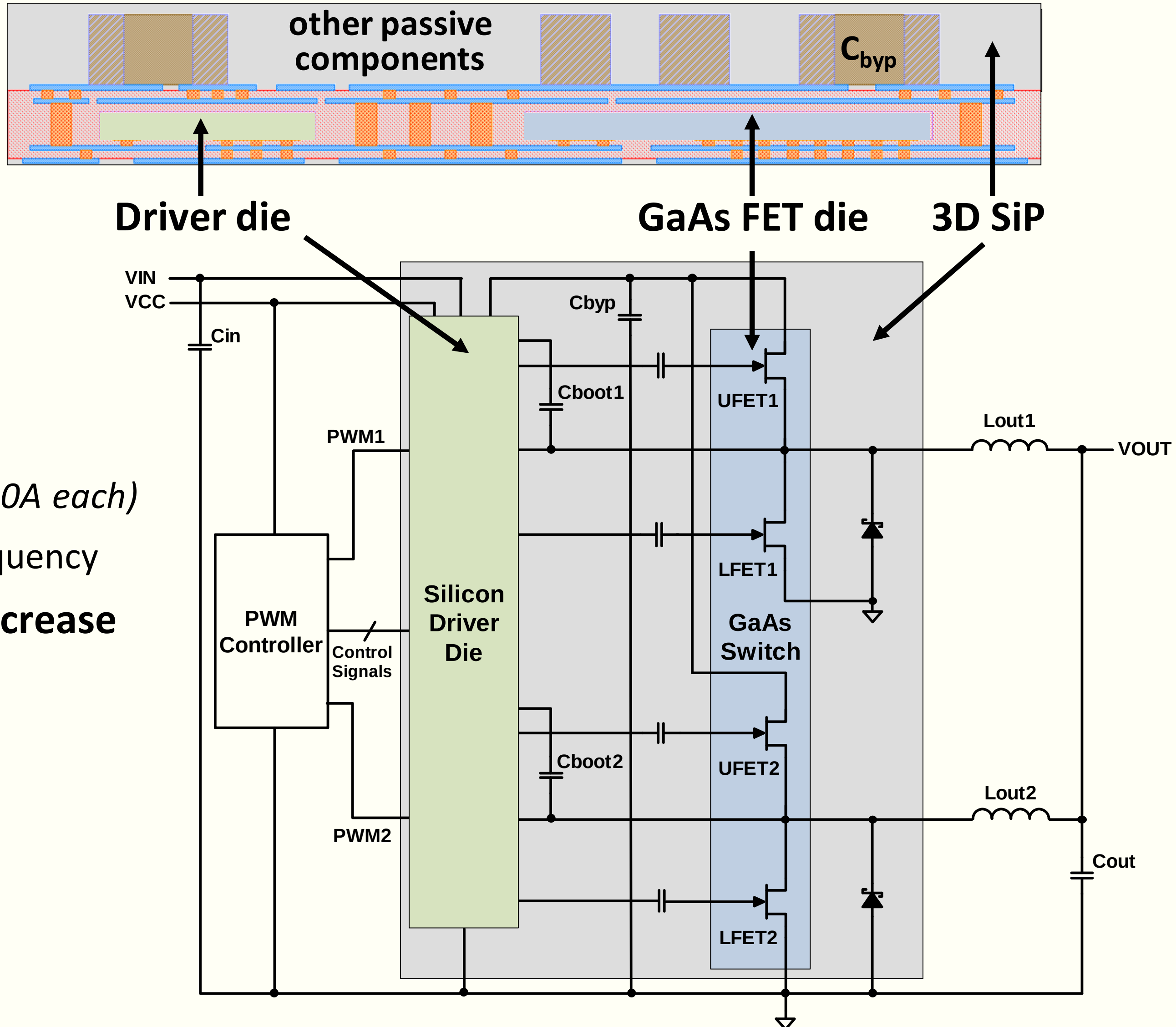
Leverages $8B GaAs industry

HIPS similar to integrated multi-band RF power amplifiers

Integrates GaAs, CMOS and passives in compact, low-cost module

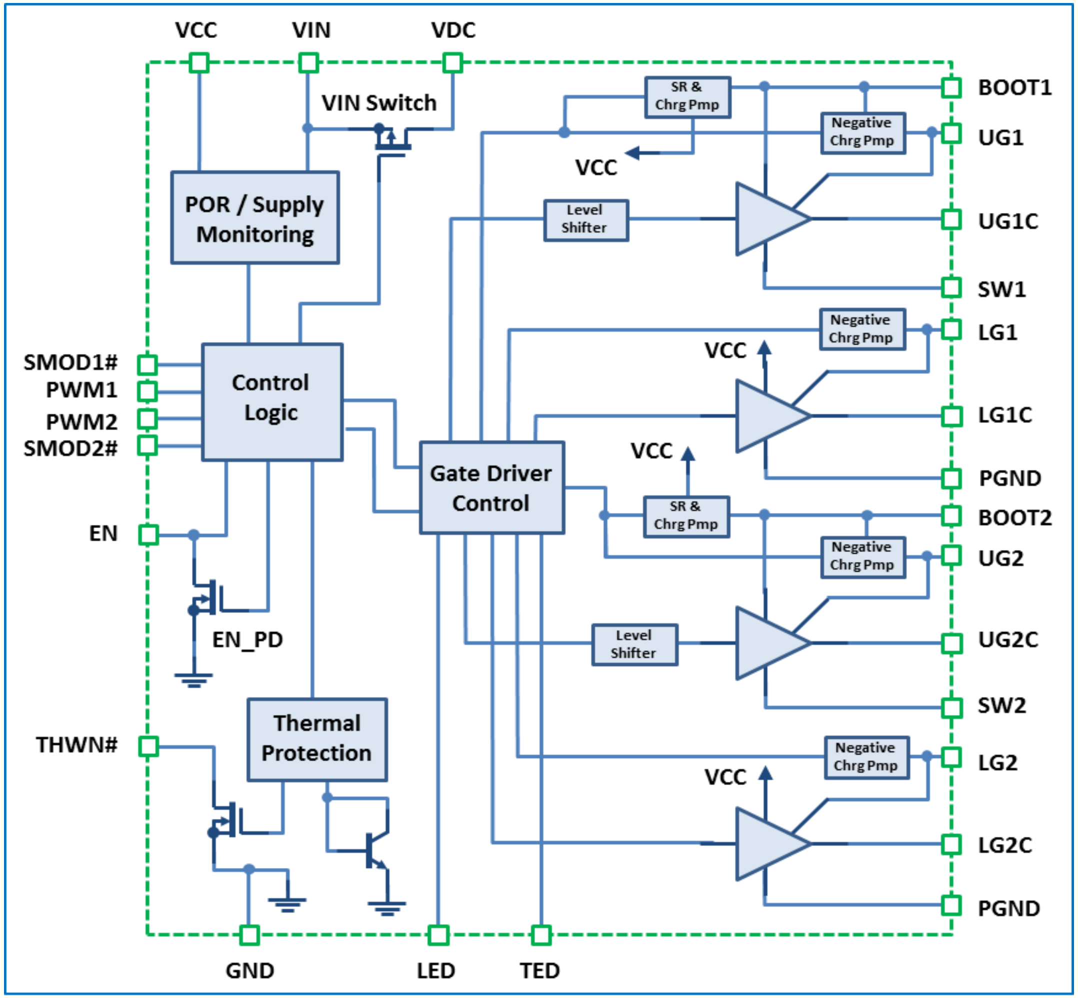
Technology Approach for Family of HIPS

- **Use 3rd party**
  - PWM controllers
  - Inductors
  - Capacitors
- **Lead product**
  - 12V input
  - 0.5-1.8V output
  - 20A output
    2 phases or outputs (10A each)
  - 2-5MHz switching frequency
- **Follow-on products increase**
  - Input voltage
  - Switching frequency
  - Efficiency
  - Output current



Sarda's CMOS Driver IC

- Integrates logic functions (so GaAs integrates only FETs)
- Transparently implements GaAs-specific gate drive
- Provides standard interface to controller



Major Functions

- **2-phase Driver Output Stage** for depletion-mode GaAs FETs
- **Negative Charge Pumps** to turn off GaAs FETs at startup, shutdown, fault, etc
- **Positive Charge Pumps** to ensure adequate upper drive during periods of inactivity
- **Synchronous Rectifiers** to eliminate BOOT Schottky diodes
- **Level Shifters** for high-side signals referenced to SX
- **Vin Switch** to prevent normally-on GaAs FETs shorting input
- **Gate Drive Control** (deadtime adjust) to trim deadtime minimally
- **Control Logic / POR** to handle all system-level start-up, shutdown, fault, and mode scenarios
- **Thermal Protection**

SARDA

Sarda Solves Issues Previously Limiting GaAs Use for VRs

- **Previous efforts to use GaAs for VRs**
  Bell Labs, Texas Instruments, Alcatel, Coldwatt,
  Rensselaer Polytechnic Institute

- **Previous efforts failed because**
  - GaAs die size and cost was too high
  - Driver to handle unique gate drive requirements of GaAs not available
  - 3D SiP (3-dimensional system-in-package) not available

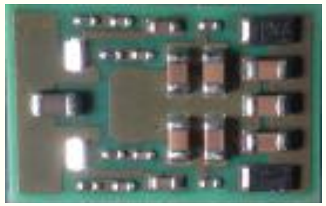
- **Sarda resolves impediments for commercializing GaAs for VRs**
  - Unique technology (14 issued US patents) reduces die size and cost by 80%
  - Developed custom driver IC for GaAs → total solution
  - Employs 3D SIP now available in high-volume production

HIPS Prototypes Demonstrate Value Proposition

Low switching loss at 2-5MHz, 12V input, 14A output

HIPS
Photos

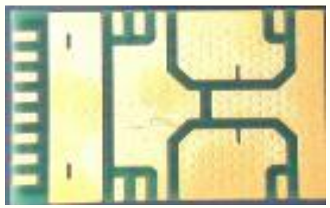
Front Side



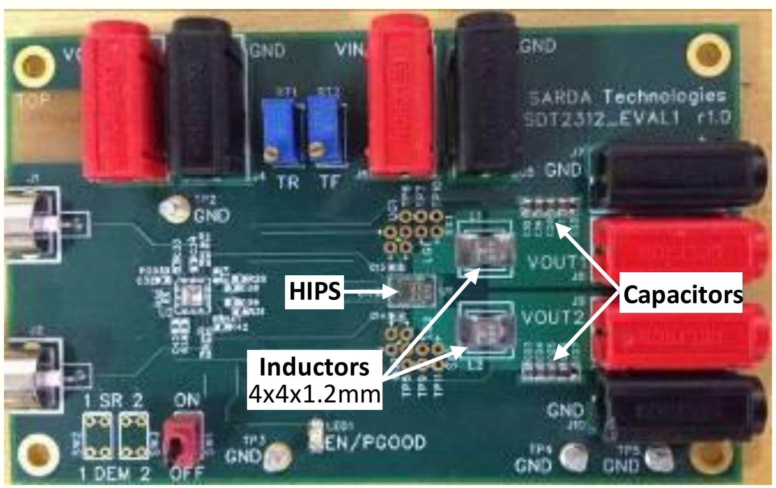
4.5mm

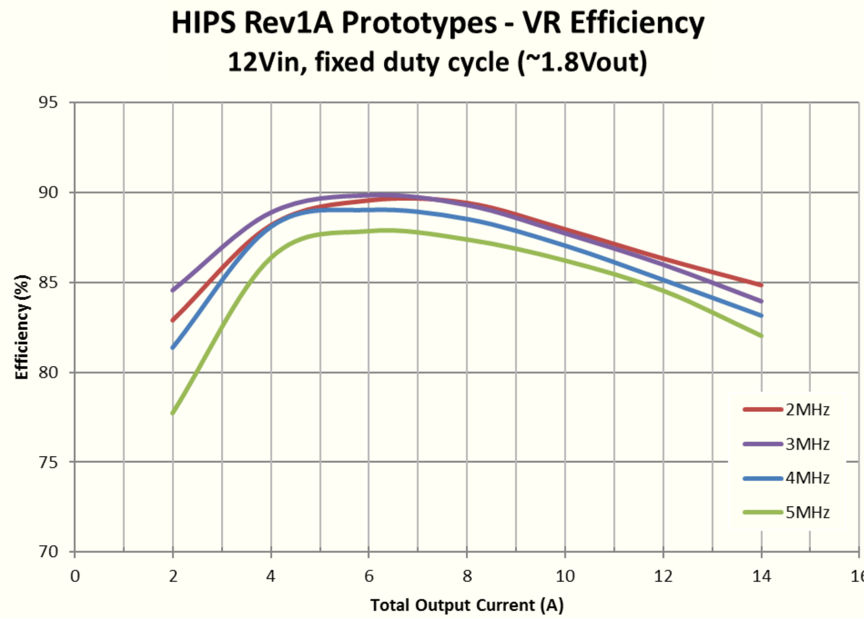
7.2mm

Back Side



HIPS
Evaluation Board





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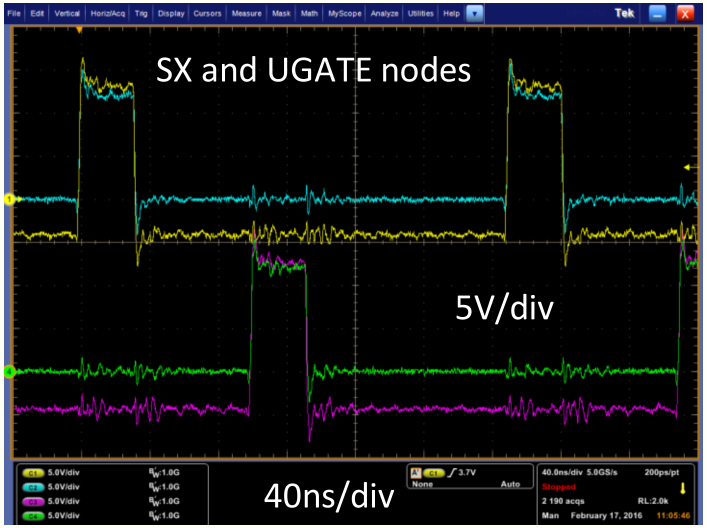
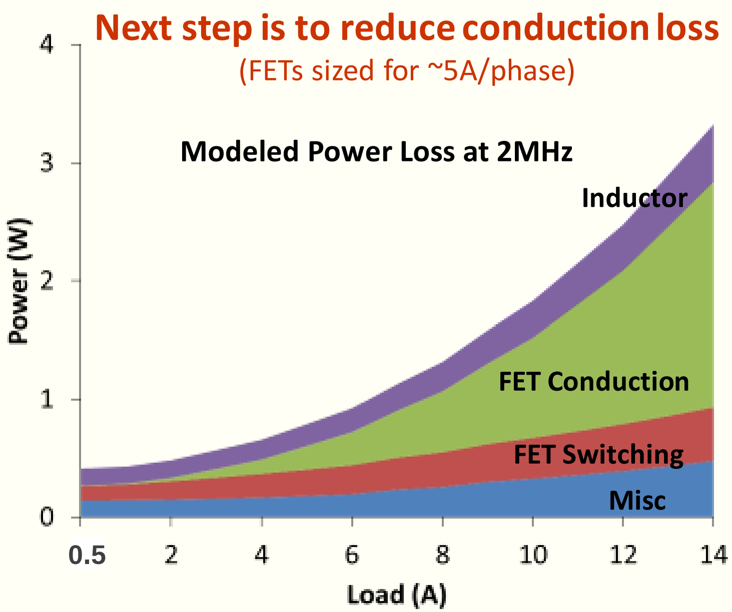
Very Low Switching Power Loss

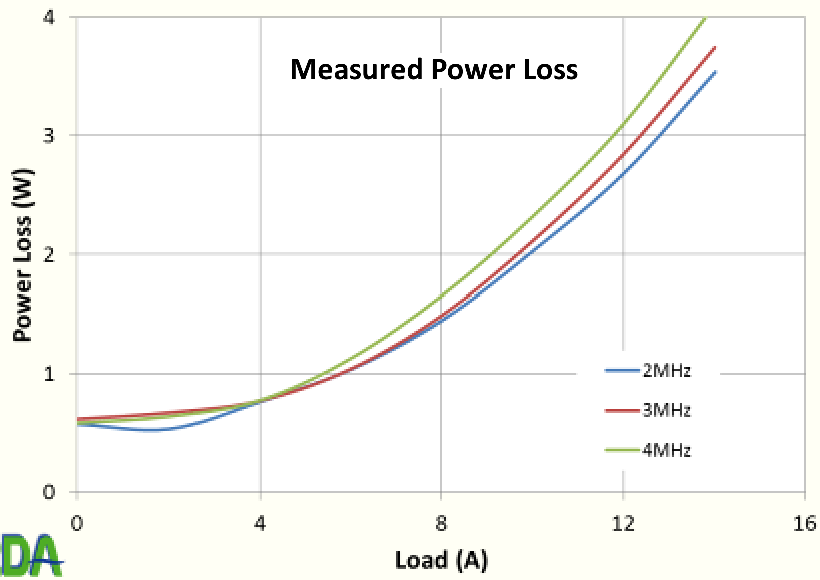
Excellent Correlation to Model

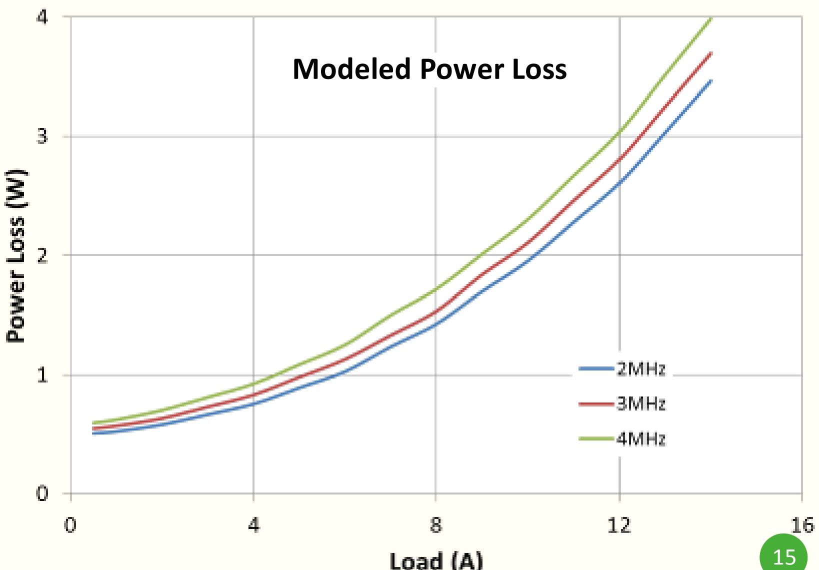
~30ns pulse widths
sub-ns edges
4MHz





Excellent correlation measured to model





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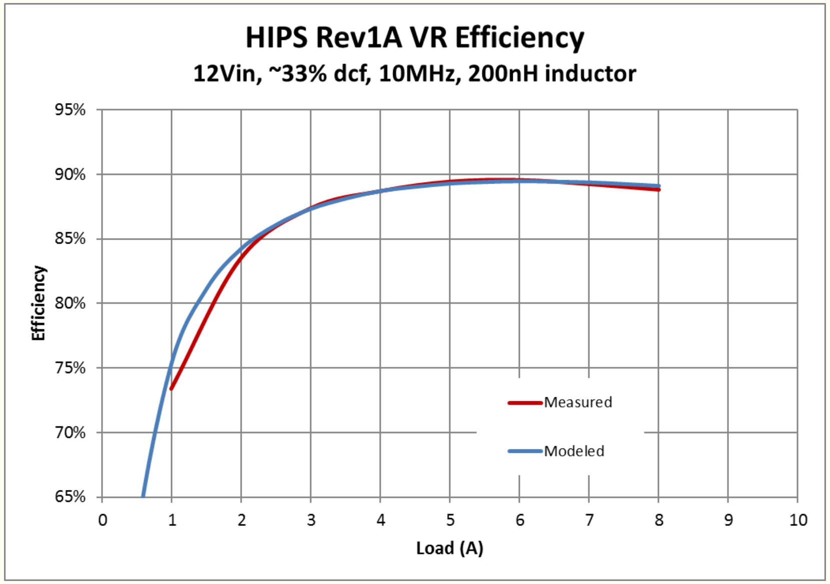
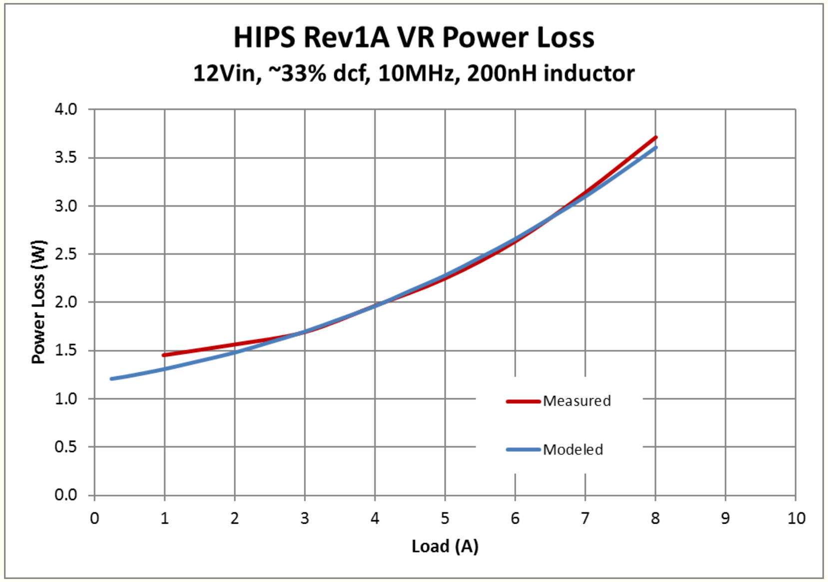
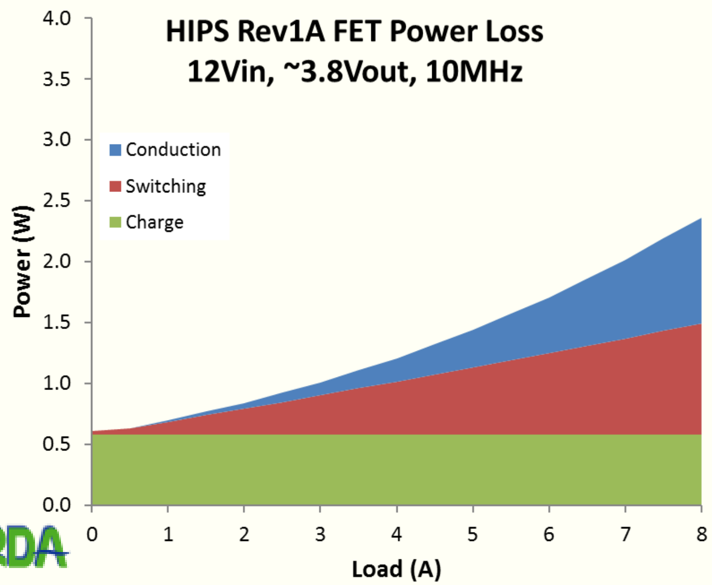
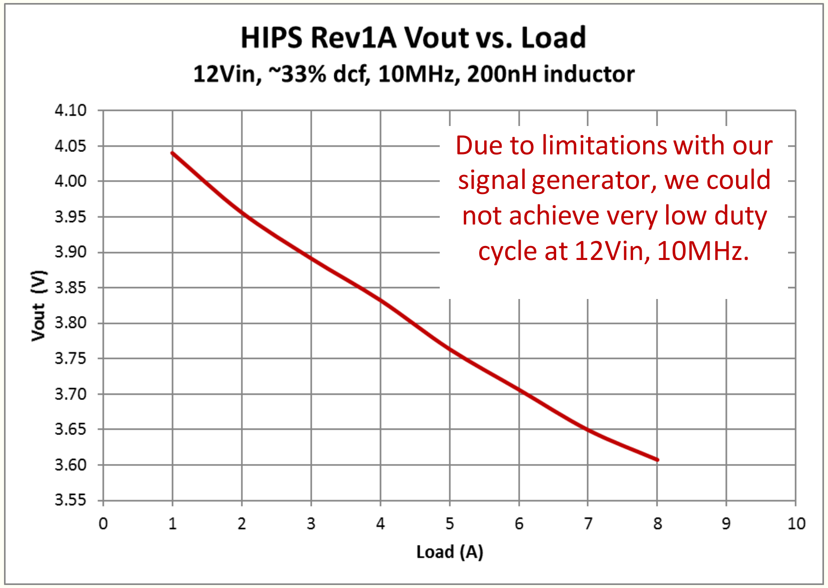
Rev1A Power Loss Analysis at 12Vin, 10MHz

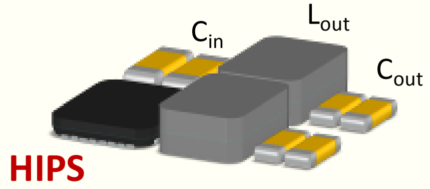








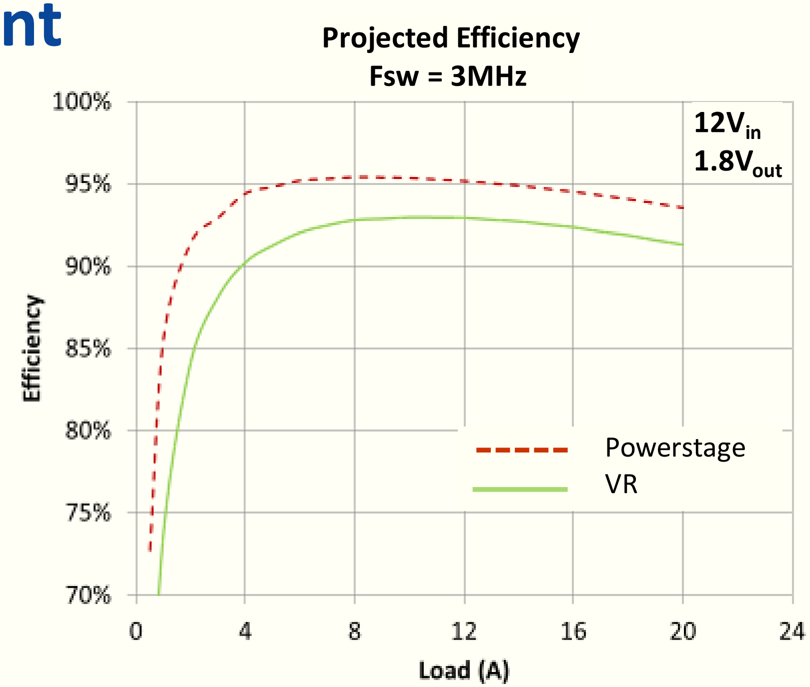
Kitty Hawk HIPS – In Development

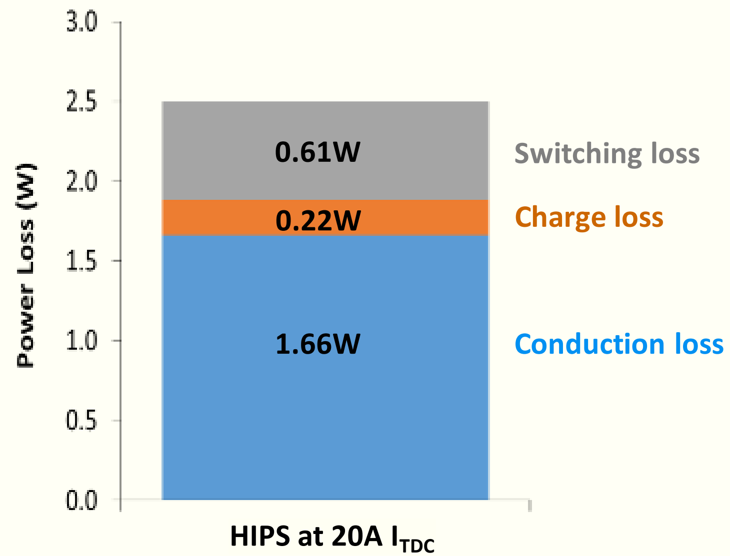


L_{out}	150nH, 1mΩ, 4.3x4.3x3mm
Fsw	3MHz
I_{TDC}	20A (2x10A)
Efficiency at I_{TDC}	91%
C_{out}	40µF
V_{out} slew rate	240mV/µs
Density	63mA/mm^3 (190mA/mm^2)

FET parameters, per phase

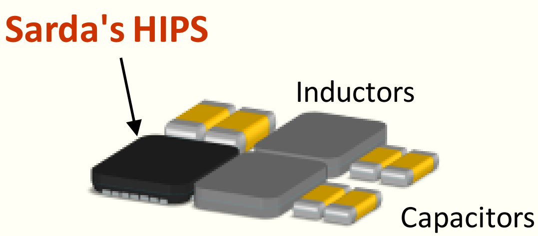
	UFET	LFET
Rdson	16mΩ	4.5mΩ
Q_g	0.56nC	2nC
Rdson • Q_g	9mΩ•nC	9mΩ•nC
Q_{oss}	0.9nC	3.2nC
Q_{rr}	-	0
t_{on}	0.5ns	0.9ns
t_{off}	0.5ns	0.9ns
t_{dead}	1ns	1ns

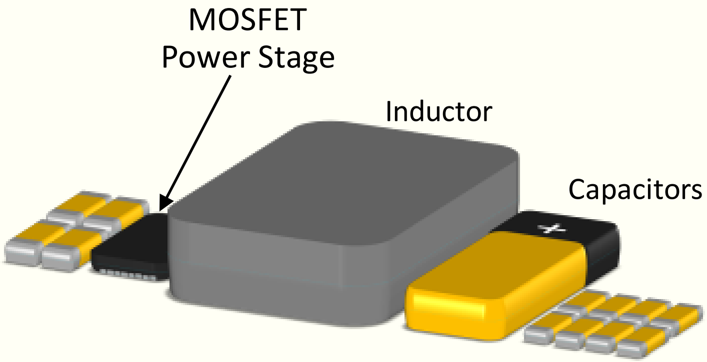




HIPS vs. MOSFET Power Stage

VR power train





HIPS' VR Benefits

- **Lowest switching power loss**
- **Highest switching frequency**
- **Fastest transient response**
- **Smallest size**
  Shrinks inductors and capacitors

HIPS' System Benefits

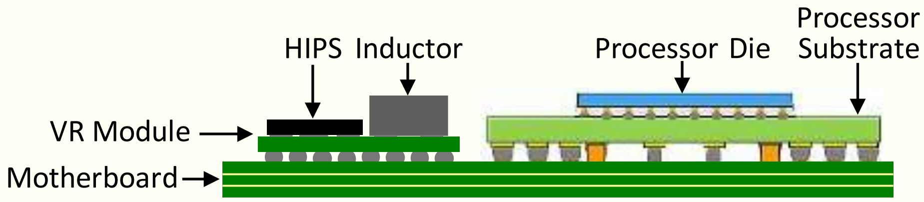
- **Reduce power consumption**
  Granular power management
  (Dedicated fast, small VR for each load)
- **Lowers cost**
  - *Component count*
  - *Board space ($0.03-$0.05/mm^3)*
  - *Thermal management*
- **Increase compute density**

HIPS Enables VR Modules Close to Load

1) Next to processor

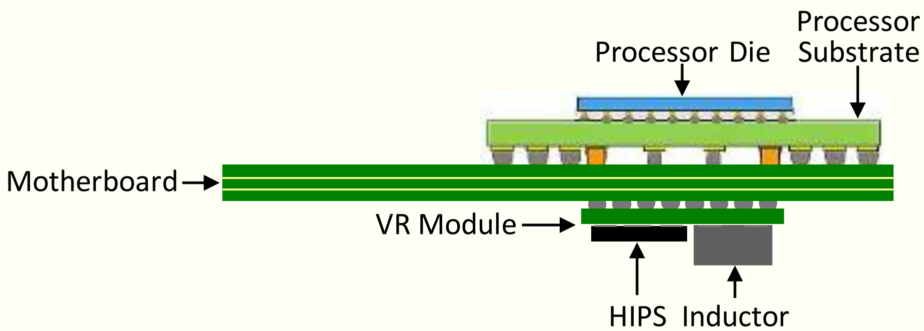
Low profile

- Enables fitting HIPS-based VR modules where silicon-based modules cannot fit
- Avoids blocking air flow



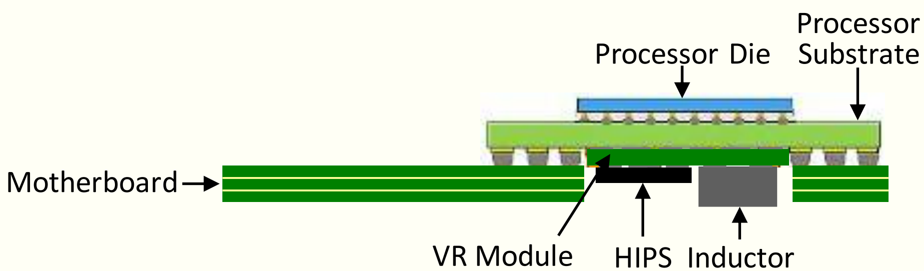
2) Under processor

- Reduces I^2R loss
- Frees up topside for more components



3) Integrated in processor package

- Facilitates processor final test
- Ultimate point-of-load regulator



HIPS Uniquely Enables High Efficiency at High Fsw

	Sarda's HIPS	Best MOSFET
t_{on}, t_{off}	<1 ns	~2 - 5 ns
L_{loop}	~0.2nH	~1nH
t_{dead}	~1ns	~3-5 ns
Q_{rr}	0	10-30nC
Ron*Q_g	<10 mΩ-nC	30-40 mΩ-nC
Ron*Q_{oss}	30 mΩ-nC	50-70 mΩ-nC

Ron On-resistance
Q_g Gate charge
Q_{oss} Output charge
Q_{rr} Reverse recovery charge
t_{on} Turn on time
t_{off} Turn off time
t_{dead} Dead time

V_{in} Input voltage
V_{out} Output voltage
D Duty cycle (V_{out} / V_{in})
I_{out} Continuous output current
Fsw Switching frequency
V_{fwd} Forward diode voltage
V_g Gate voltage

Switching Losses

$P(sw\_UFET) \sim \frac{1}{2} \cdot V_{IN} \cdot I_{out} \cdot (\mathbf{t_{on\_UFET}} + \mathbf{t_{off\_UFET}}) \cdot F_{sw}$ Dominant switching loss term

$P(sw\_LFET) \sim \frac{1}{2} \cdot V_{fwd} \cdot I_{out} \cdot (\mathbf{t_{on\_LFET}} + \mathbf{t_{off\_LFET}}) \cdot F_{sw}$

$P(t_{dead}) = 2 \cdot \mathbf{t_{dead}} \cdot I_{out} \cdot V_{fwd} \cdot F_{sw}$ $V_{fwd} \sim 0.8V$

Charge Losses

$P(Q_g) = (V_g \cdot \mathbf{Q_g}) \cdot F_{sw}$

$P(Q_{oss}) = \frac{1}{2} \cdot (V_{IN} \cdot \mathbf{Q_{oss}}) \cdot F_{sw}$ Dominant charge loss term

$P(Q_{rr}) = (V_{IN} \cdot \mathbf{Q_{rr\_LFET}}) \cdot F_{sw}$ Zero Q_{rr} for GaAs

Conduction Losses

$P(cond) = [(D \cdot Ron_{UFET} + (1 - D) \cdot Ron_{LFET}) \cdot I_{out}^2] \cdot T_{coeff}$ T_{coeff}: increase of Ron with temperature

12Vin HIPS' Advantages

Shown in Red

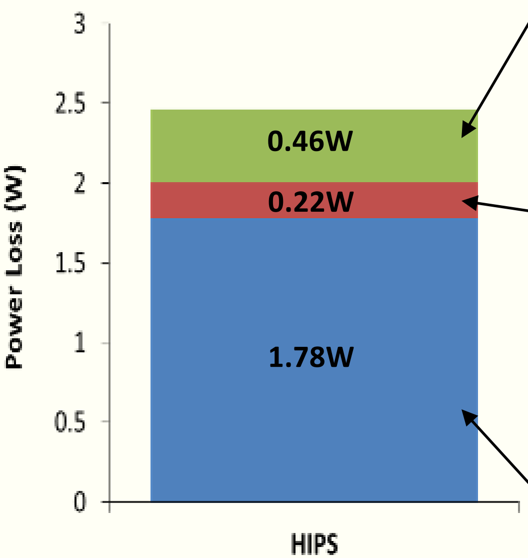
Provide highest switching frequency
3MHz for 20A for 12Vin, 1.8Vout

Ron • Qg = 9

		UFET	LFET
Rdson	**On-resistance**	16mΩ	4.5mΩ
Q_g	**Gate charge**	0.56nC	2nC
Q_{oss}	**Output charge**	0.94nC	3.33nC
Q_{rr}	**Reverse recovery charge**	-	0
t_{on}	**Turn on time (est)**	0.45ns	0.9ns
t_{off}	**Turn off time (est)**	0.45ns	0.9ns
t_{dead}	**Dead time**	1ns	1ns

2-phase, parameters per channel

~2.5W max for solution without heatsink



2-phase, 20A Load

Switching Losses

$P(sw\_UFET) \sim \frac{1}{2} \cdot V_{IN} \cdot I_{out} \cdot (t_{on\_UFET} + t_{off\_UFET}) \cdot F_{sw}$

$P(sw\_LFET) \sim \frac{1}{2} \cdot V_{fwd} \cdot I_{out} \cdot (t_{on\_LFET} + t_{off\_LFET}) \cdot F_{sw}$

$P(t_{dead}) = 2 \cdot t_{dead} \cdot I_{out} \cdot V_{fwd} \cdot F_{sw}$

Charge Losses

$P(Q_g) = (V_g \cdot Q_g) \cdot F_{sw}$

$P(Q_{oss}) = \frac{1}{2} \cdot (V_{IN} \cdot Q_{oss}) \cdot F_{sw}$

$P(Q_{rr}) = (V_{IN} \cdot Q_{rr\_LFET}) \cdot F_{sw}$

Conduction Losses

$P(cond) = [(D \cdot Ron_{UFET} + (1 - D) \cdot Ron_{LFET}) \cdot I_{out}^2] \cdot T_{coeff}$

12Vin MOSFET's Disadvantages
Shown in Red

Ron • Qg = 25

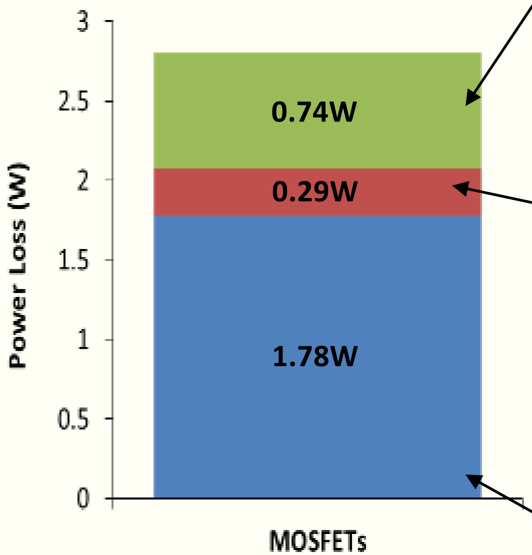
		UFET	LFET
Rdson	On-resistance	8mΩ	2.25mΩ
Q_g	Gate charge	3.1nC	11.1nC
Q_{oss}	Output charge	5.2nC	18.5nC
Q_{rr}	Reverse recovery charge	-	13nC
t_{on}	Turn on time (est)	3ns	5ns
t_{off}	Turn off time (est)	3ns	5ns
t_{dead}	Dead time	4ns	4ns

Lower switching frequency

800kHz for 20A for 12Vin, 1.8Vout

Much larger solution

~2.5W max for solution without heatsink



1-phase, 20A Load
(limited more to ~19A)

Switching Losses

$P(sw\_UFET) \sim \frac{1}{2} \cdot V_{IN} \cdot I_{out} \cdot (t_{on\_UFET} + t_{off\_UFET}) \cdot F_{sw}$

$P(sw\_LFET) \sim \frac{1}{2} \cdot V_{fwd} \cdot I_{out} \cdot (t_{on\_LFET} + t_{off\_LFET}) \cdot F_{sw}$

$P(t_{dead}) = 2 \cdot t_{dead} \cdot I_{out} \cdot V_{fwd} \cdot F_{sw}$

Charge Losses

$P(Q_g) = (V_g \cdot Q_g) \cdot F_{sw}$

Both Q_g and Q_{oss} dominant charge loss terms

$P(Q_{oss}) = \frac{1}{2} \cdot (V_{IN} \cdot Q_{oss}) \cdot F_{sw}$

$P(Q_{rr}) = (V_{IN} \cdot Q_{rr\_LFET}) \cdot F_{sw}$

Significant Q_{rr}

Conduction Losses

$P(cond) = [(D \cdot Ron_{UFET} + (1 - D) \cdot Ron_{LFET}) \cdot I_{out}{}^2] \cdot T_{coeff}$

12Vin MOSFET's Disadvantages

Shown in Red

Rds • Qg = 25

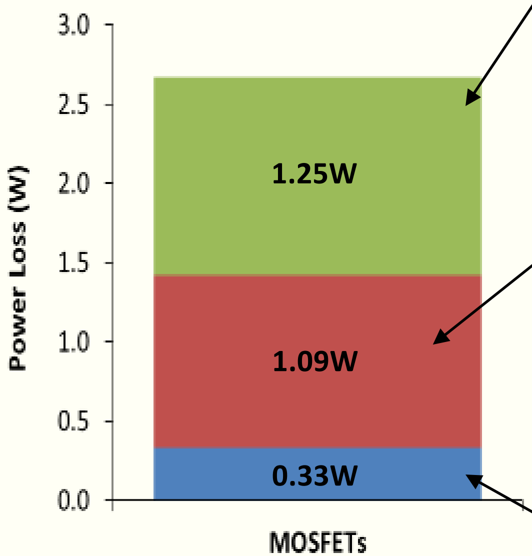
		UFET	LFET
Rdson	On-resistance	8mΩ	2.25mΩ
Q_g	Gate charge	3.1nC	11.1nC
Q_{oss}	Output charge	5.2nC	18.5nC
Q_{rr}	Reverse recovery charge	-	13nC
t_{on}	Turn on time (est)	3ns	5ns
t_{off}	Turn off time (est)	3ns	5ns
t_{dead}	Dead time	4ns	4ns

At same switching frequency:

3MHz for 9A for 12Vin, 1.8Vout

Much less current capability

~2.5W max for solution without heatsink



1-phase, 9A Load

Switching Losses

$P(sw\_UFET) \sim \frac{1}{2} \cdot V_{IN} \cdot I_{out} \cdot (t_{on\_UFET} + t_{off\_UFET}) \cdot F_{sw}$

$P(sw\_LFET) \sim \frac{1}{2} \cdot V_{fwd} \cdot I_{out} \cdot (t_{on\_LFET} + t_{off\_LFET}) \cdot F_{sw}$

$P(t_{dead}) = 2 \cdot t_{dead} \cdot I_{out} \cdot V_{fwd} \cdot F_{sw}$

Charge Losses

$P(Q_g) = (V_g \cdot Q_g) \cdot F_{sw}$

Both Q_g and Q_{oss} dominant charge loss terms

$P(Q_{oss}) = \frac{1}{2} \cdot (V_{IN} \cdot Q_{oss}) \cdot F_{sw}$

$P(Q_{rr}) = (V_{IN} \cdot Q_{rr\_LFET}) \cdot F_{sw}$

~44% of charge loss due to Q_{rr}

Conduction Losses

$P(cond) = [(D \cdot Ron_{UFET} + (1 - D) \cdot Ron_{LFET}) \cdot I_{out}^2] \cdot T_{coeff}$

12Vin GaN FET's Disadvantages

Shown in Red

Ron • Qg = 20

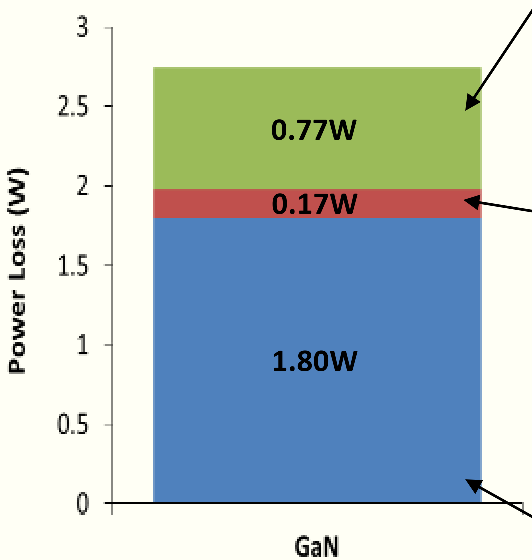
		UFET	LFET
Rdson	On-resistance	8mΩ	2.25mΩ
Q_g	Gate charge	2.5nC	8.9nC
Q_{oss}	Output charge	4.2nC	14.8nC
Q_{rr}	Reverse recovery charge	-	0
t_{on}	Turn on time (est)	2.4ns	4ns
t_{off}	Turn off time (est)	2.4ns	4ns
t_{dead}	Dead time	4ns	4ns

Lower switching frequency

1MHz for 20A for 12Vin, 1.8Vout

Much larger solution

~2.5W max for solution without heatsink



1-phase, 20A Load
(limited more to ~19A)

Switching Losses

$$P(sw\_UFET) \sim \tfrac{1}{2} \cdot V_{IN} \cdot I_{out} \cdot (t_{on\_UFET} + t_{off\_UFET}) \cdot F_{sw}$$

$$P(sw\_LFET) \sim \tfrac{1}{2} \cdot V_{fwd} \cdot I_{out} \cdot (t_{on\_LFET} + t_{off\_LFET}) \cdot F_{sw}$$

$$P(t_{dead}) = 2 \cdot t_{dead} \cdot I_{out} \cdot V_{fwd} \cdot F_{sw}$$

Charge Losses

$$P(Q_g) = (V_g \cdot Q_{g\_total}) \cdot F_{sw}$$

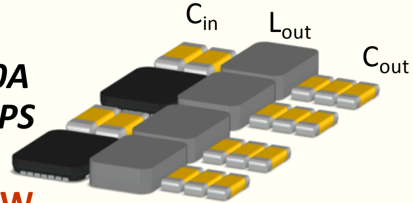
$$P(Q_{oss}) = \tfrac{1}{2} \cdot (V_{IN} \cdot Q_{oss\_total}) \cdot F_{sw}$$

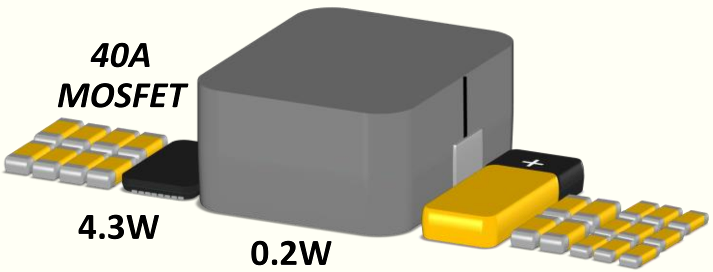
$$P(Q_{rr}) = (V_{IN} \cdot Q_{rr\_LFET}) \cdot F_{sw}$$

Conduction Losses

$$P(cond) = [(D \cdot Ron_{UFET} + (1 - D) \cdot Ron_{LFET}) \cdot I_{out}^{2}] \cdot T_{coeff}$$

40A HIPS vs. MOSFET Comparison



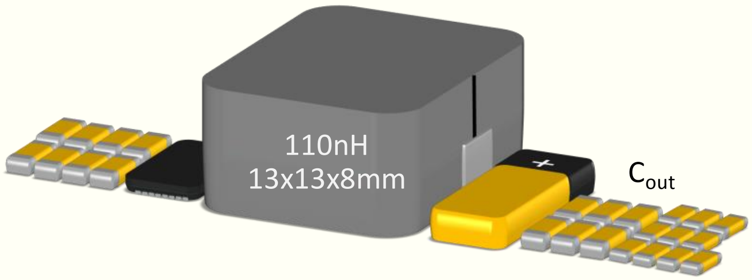


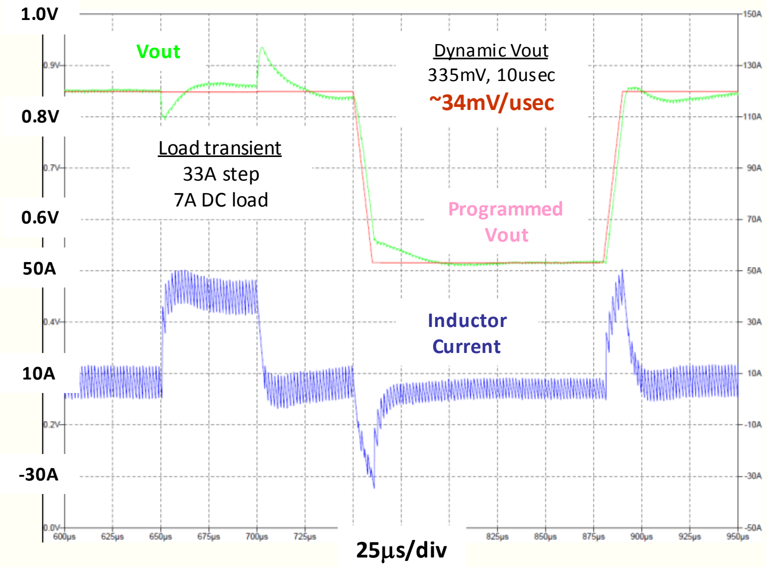
	Sarda HIPS 2MHz	**MOSFET Power Stage** 600kHz	**HIPS Advantages**
Power Loss	**1.7W each** (HIPS), **0.2W each**	**4.3W** (MOSFET), **0.2W**	
Efficiency 12Vin, 0.85Vout, 40A	89%	88%	***Similar***
Footprint (mm^2)	**200**	400	***50% pcb area***
Height (mm)	**3**	8	***40% height***
V_{out} **slew rate** (mV/µs)	**165**	30	***5-6x faster***
Load Transient Response	**~2-5µs**	15-30µs	***5-15x faster***

SARDA

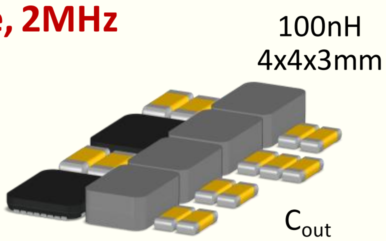
HIPS Enables Granular Power

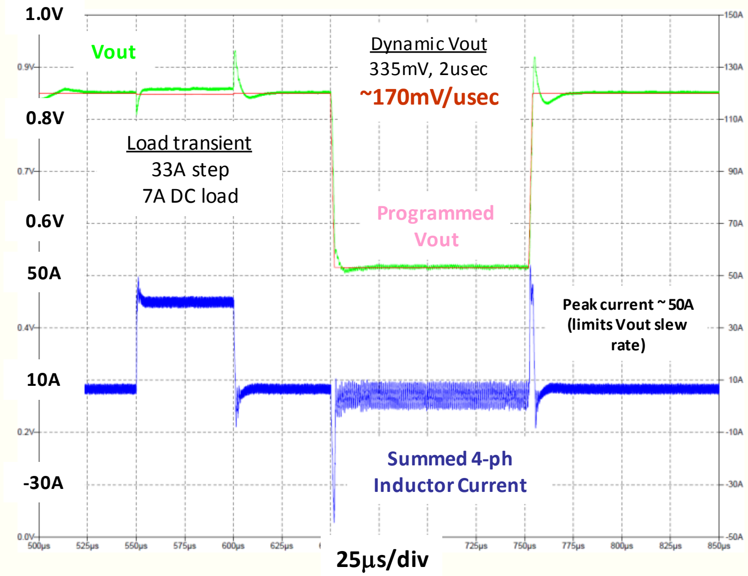
MOSFET Powerstage
1-phase, 600kHz





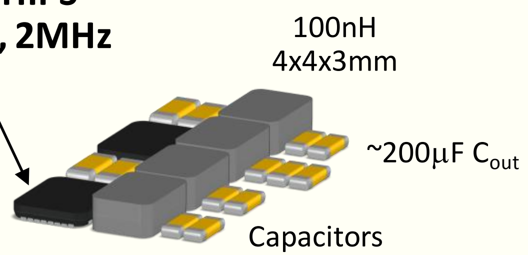
Sarda HIPS
4-phase, 2MHz



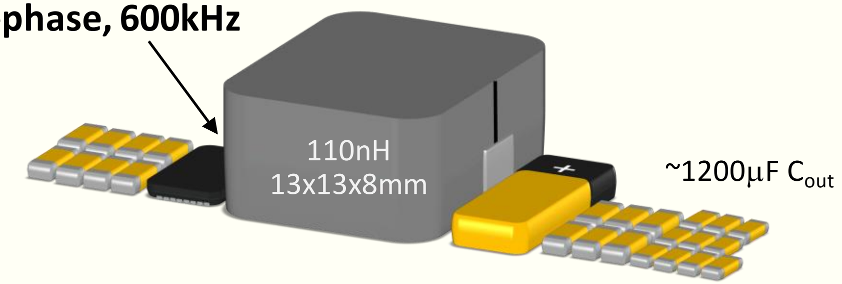


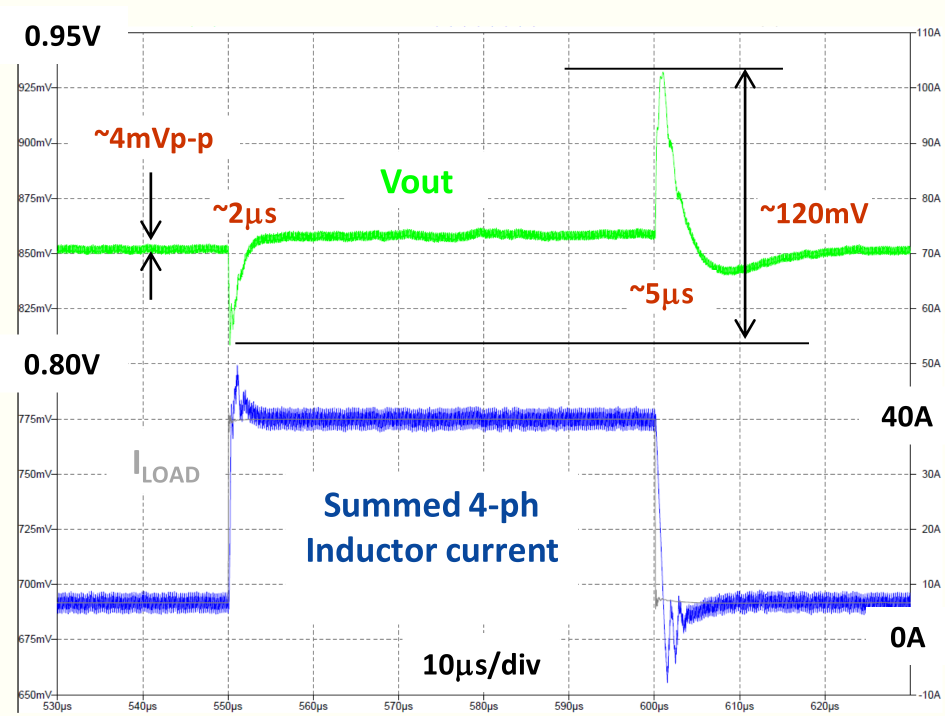
Closer Look at HIPS Load Transient Performance Advantage

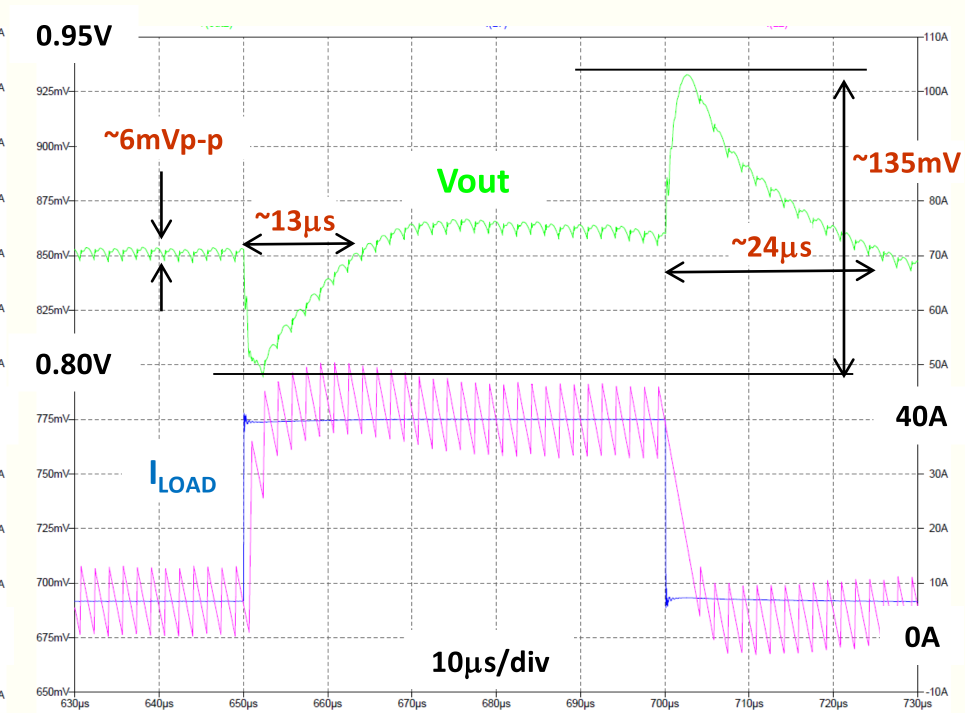
Sarda HIPS
2-phase, 2MHz



MOSFET Powerstage
1-phase, 600kHz



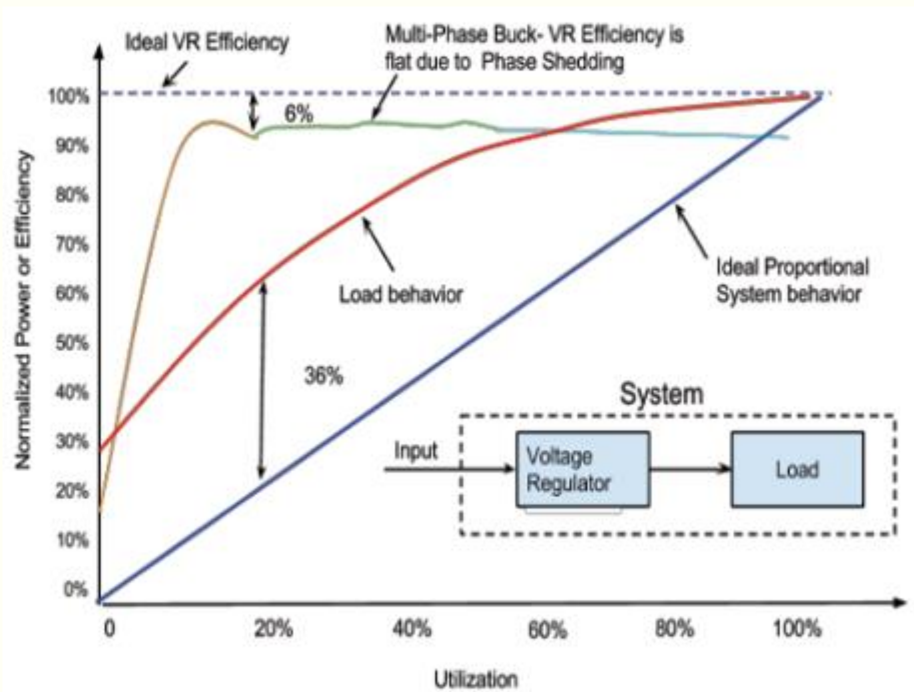


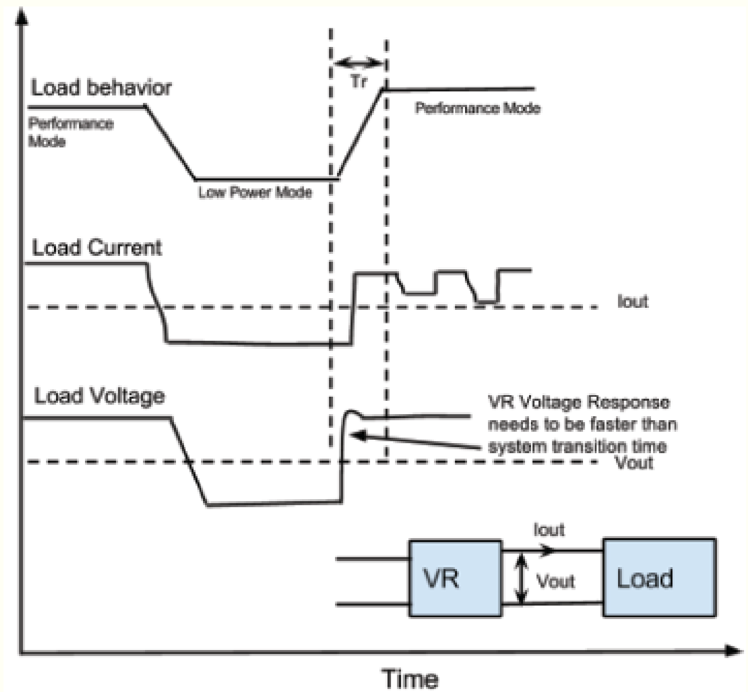


Load transient: 33A step, 7A DC load

Granular Power Reduces Energy Consumption by 30%

- **High voltage regulator (VR) efficiency during low power operation**
  For energy proportional power management
- **Fast VR response for aggressive dynamic voltage scaling**
  Increases processor performance and reduces power consumption
- **Reduced cooling requirements**
  Less heat dissipation

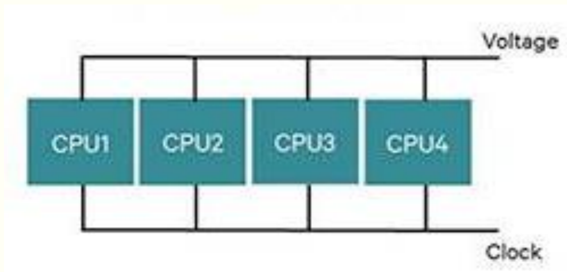


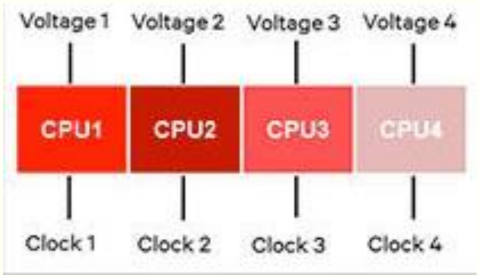


source: [Google's Energy Proportional Power Management for Data Center Applications]

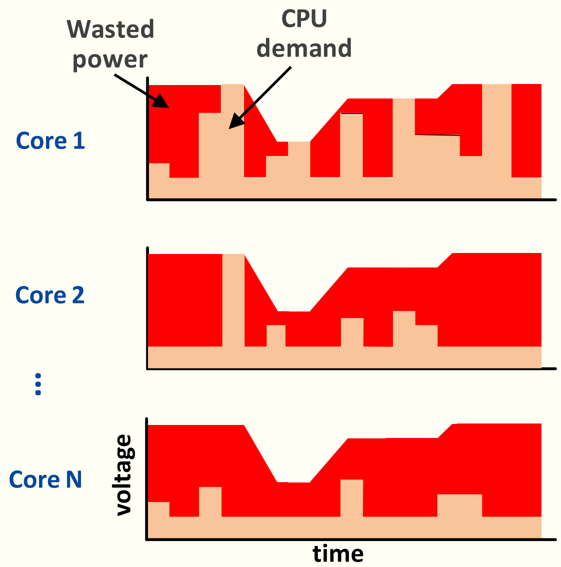
Granular Power Requires Many Fast, Small VRs

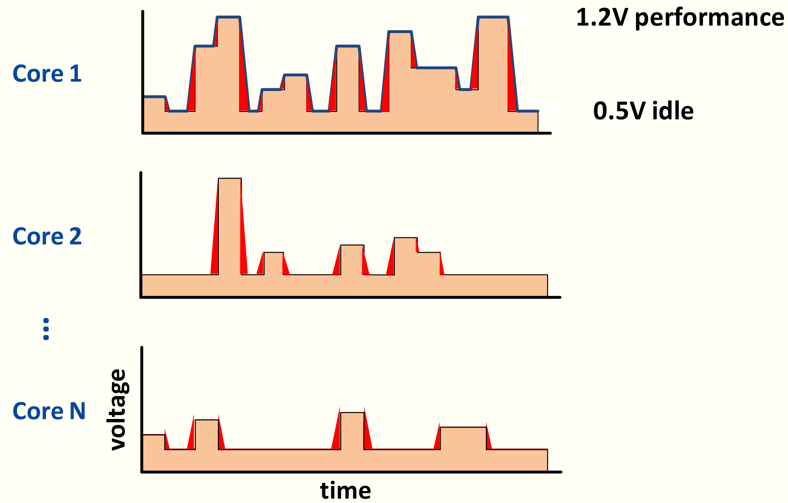
	Conventional Power	Granular Power
Voltage levels	**Single**	**Multiple**
Voltage slew rate (mV/µs)	**Low**	**High**





Source: Qualcomm





Source: The Microprocessor Report's [Sarda Delivers Granular Power]

System Benefits From HIPS

Increase Performance-per-Watt

Limited by heat and power

Increase performance (MIPS)

- Dynamic power management of each load
  - Faster transition to peak modes
  - Higher voltage setpoint
- Frees up board space for components
  e.g., memory

Reduce energy consumption

- Granular power
  Dynamic power management of each load
  - Faster transition to idle modes
  - Lower voltage setpoint
- Energy proportionality
  High efficiency at low workload
- Reduced cooling

Why More-Than-Moore Power Management Is Required to Keep Up With Exponential Growth in ICT Data Consumption

Google's Energy Proportional Power Management for Data Center Applications

Summary

- **GaAs-based HIPS enable fastest, smallest VRs**
- **Granular power** (many fast, small VRs) **increases compute density**
  - Overcomes escalating limitations with monolithic integration (Moore's Law scaling)
  - Supports heterogeneous integration (More-than-Moore scaling)
- **GaAs-based HIPS is superior technology for up to 60V input VRs**