RF LDMOS/EDMOS: embedded devices for highly integrated solutions

T. Letavic, C. Li, M. Zierak, N. Feilchenfeld, M. Li, S. Zhang, P. Shyam, V. Purakh

GLOBALFOUNDRIES®

Outline

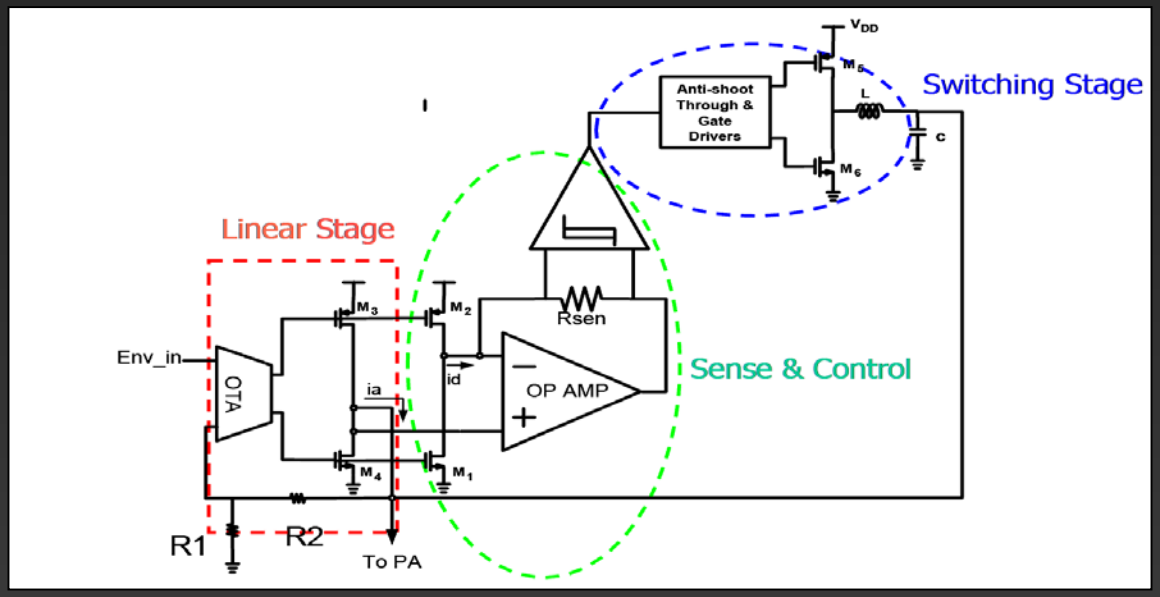
- PowerSoc systems and product drivers
  - Systems that benefit from embedded power supplies also require ..
    - Ubiquitous wireless connectivity – RF integration (802.11.54, BTLE, BT, WPAN, …)
    - MCU + memory – code, actuation, network configuration
  - IoT network edge node = miniaturized embedded power supply and RF link

- PowerSoC and RF device integration strategies
  - 180nm bulk-Si mobile power management process – LDMOS
  - 55nm bulk-Si silicon IoT platform – EDMOS
  - DC and RF benchmark to 5V CMOS

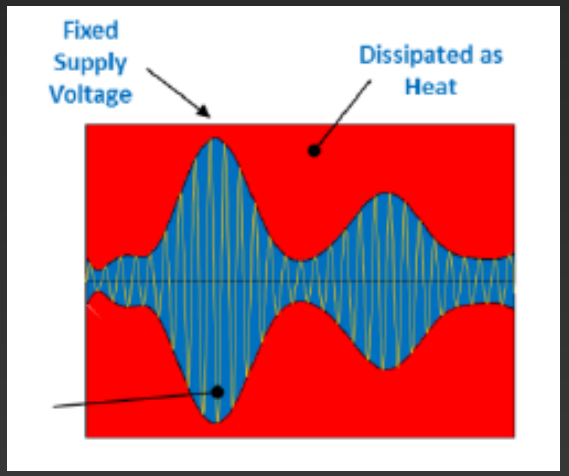
- Power and RF application characterization
  - ISM bands, WiFi, performance against cellular industry standards
  - Embedded power and RF with the same device unit cell

- Summary – PowerSoc and RF use the same device unit cell

Embedded power and RF: Envelope Tracking



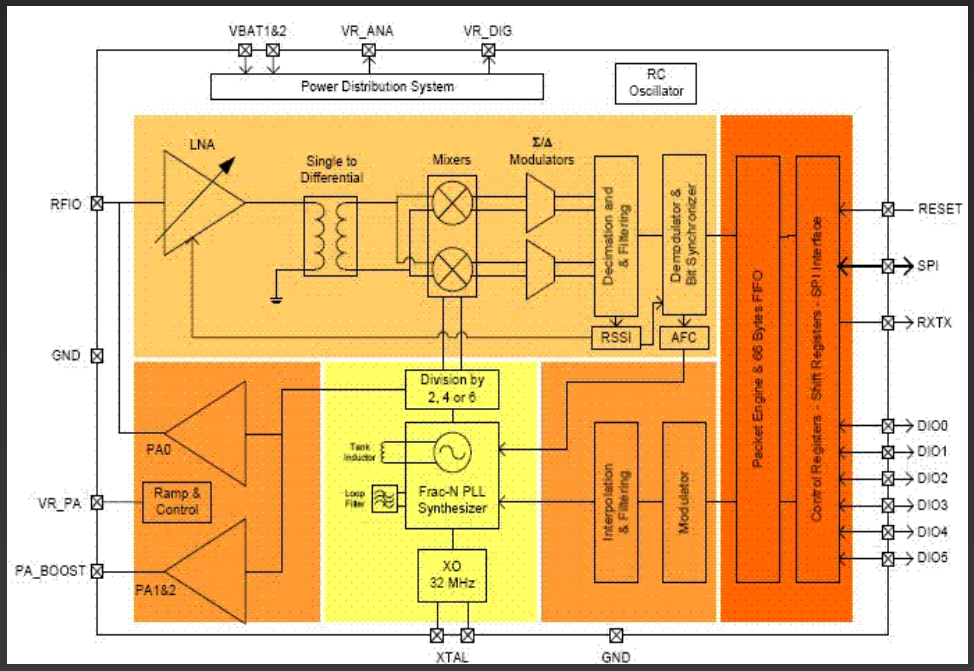
Motorola eg. US 6,407,634 B1, US 6,617,920 B2



https://www.nujira.com

- RF supply modulation to reduce power dissipation (WiFi, 4G LTE)
  - **Linear amplifier: $5V_{pk-pk}$ 80 MHz BW, >16QAM -> fT > 20 Ghz**
  - **SMPS: > 10-20 MHz f_{sw}, 5-7 V FSOA, ultra-low R_{sp}*Q_{gg} FOM**
- Optimal solution fT/fmax of cSiGe/GaN/GaAs with Si BCD voltage handling
  - *RF LDMOS and RF EDMOS are challenging the incumbents ….*

Embedded Power and RF: IoT Edge Node



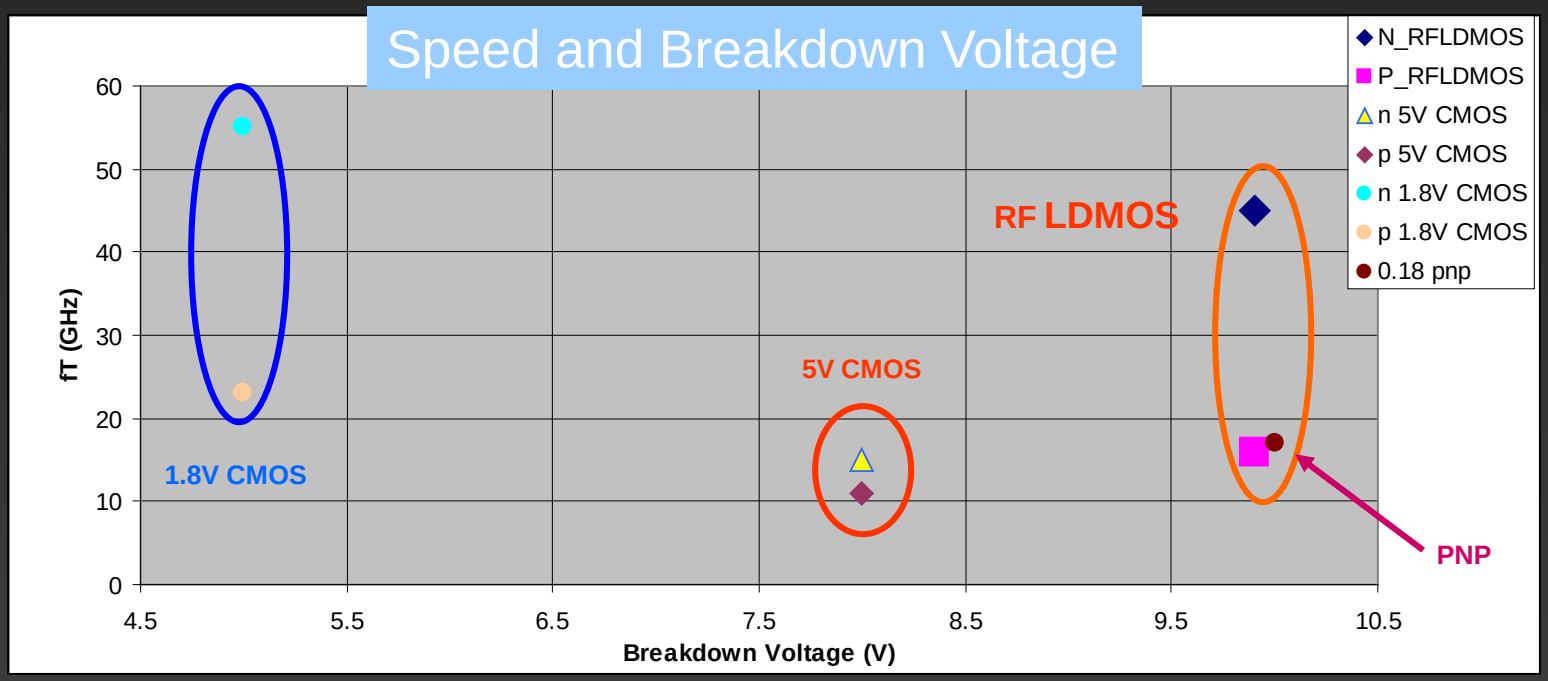
Semtech integrated RF transceiver SX123SX

- Wireless IEEE 802.15.4, IEEE 802.11.ah, 2G/3G/4G LTE MTC, ….
  - 50 B connected endpoints 2020 (Cisco Mobility Report Dec 2016)
  - **Integrated low power RF modem + PA, SMPS, MPU + digital control**
  - ISM to 2.4 GHz, P_{out}= 20-22 dBm, 0.3-1 Mbps, V_{supply} = 3.3V - 5V
- Integration options: RF + AMS or RF + DBB - lowest power key

IoT RF Landscape

	W-PAN	W-LAN	W-WAN	W-MAN
	Short and Near		Wide and Long	
Standards/ Protocol [Proprietary] [Standard] [In development]	Ant+ RFID, NFC (802.15.1)/BTClassic (802.15.1)/BTSmart 802.15.4/RFCE M-Wireless	Z-Wave, EnOcean 802.15.4/ZigBee/SEP2/HA RT/6Tisch/Thread 802.11b/g/n/ac/WiFi Bluetooth/Classic/ Smart BLE MESH	GSM/GPRS DECT-ULE 802.15.4/WiSUN 802.11ah EC-GSM LTE-NB IoT LTE-Cat M	LPWAN (LoRA (Prop) SigFox (prop) AMI/Metering (Prop)) GPS/GNSS 2G/3G LTE 5G
Spectrum	ISM (Sub-GHz, 2.4GHz)	Licensed ISM (Sub-GHz, 2.4Ghz, 5.8Mhz)	Licensed ISM (Sub-GHz, 2.4Ghz)	Licensed ISM (Sub-GHz, 2.4Ghz)
Range	<30M	30M+ P2P, Meshing	KMs	10's KM's
Coverage (size, topology)	**Point –to-point, Star Small <10 nodes**	**Star, Mesh <1000 nodes**	**Cellular, meshing, star Large, 10K+ nodes**	**Cellular, meshing, star Large, 10K+ nodes**
Power (battery life)	**Consumer: Daily Industrial meter: 10yr**	**Consumer: 2 years Industrial: 10 year**	**GSM/GPRS: Daily 10 year goal**	**LTE: Daily Industrial: 10 year**
Data rate	Low <50kbps BTC <1Mbps Audio	Low <50kbps WiFi 11Mbps (video)	Low (70kbs) to Medium 1Mbps	Low (<50kbps) to High (1Gbps)
Latency	High Latency Audio medium QoS	High Latency Video needs high QoS	Medium Latency	5G Mission Critical Cellular data/ Video high QoS
Complexity	Simple	802.15.4 moderate WiFi Complex	Complex	Complex (Cellular) Simple (star)

PowerSoC and RF: fT vs BV paradigm



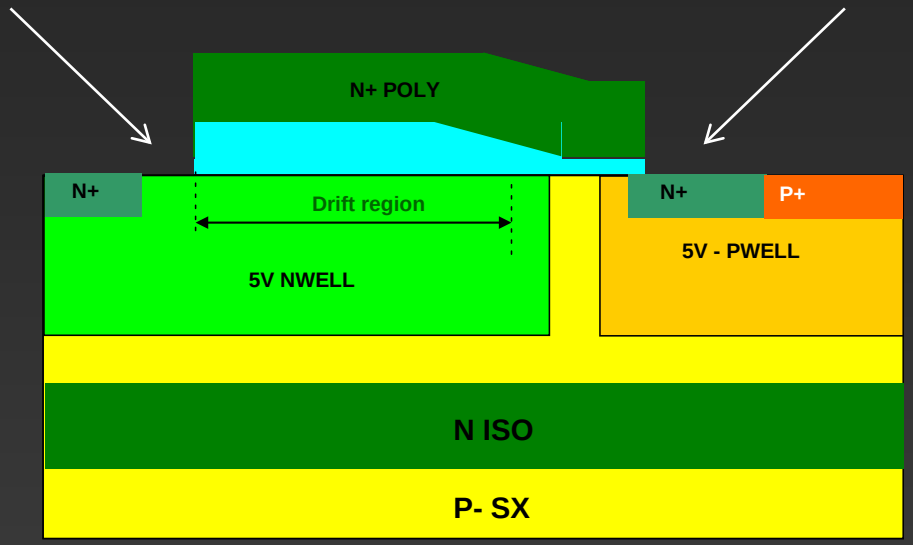
- Low dissipation RF for mobile and IoT – expanding power industry
  - 1.5-1.8V RFCMOS has the speed but not V_{rated} – stacking reduces fT !
  - 5V RFCMOS has V_{rated} but not the speed – limited by I_{eff} (R_{sp}*Q_{gg})

- *RF LDMOS and RF EDMOS* – fT of 1.8V CMOS with BV_{ds} >> 5V CMOS

180nm RF LDMOS

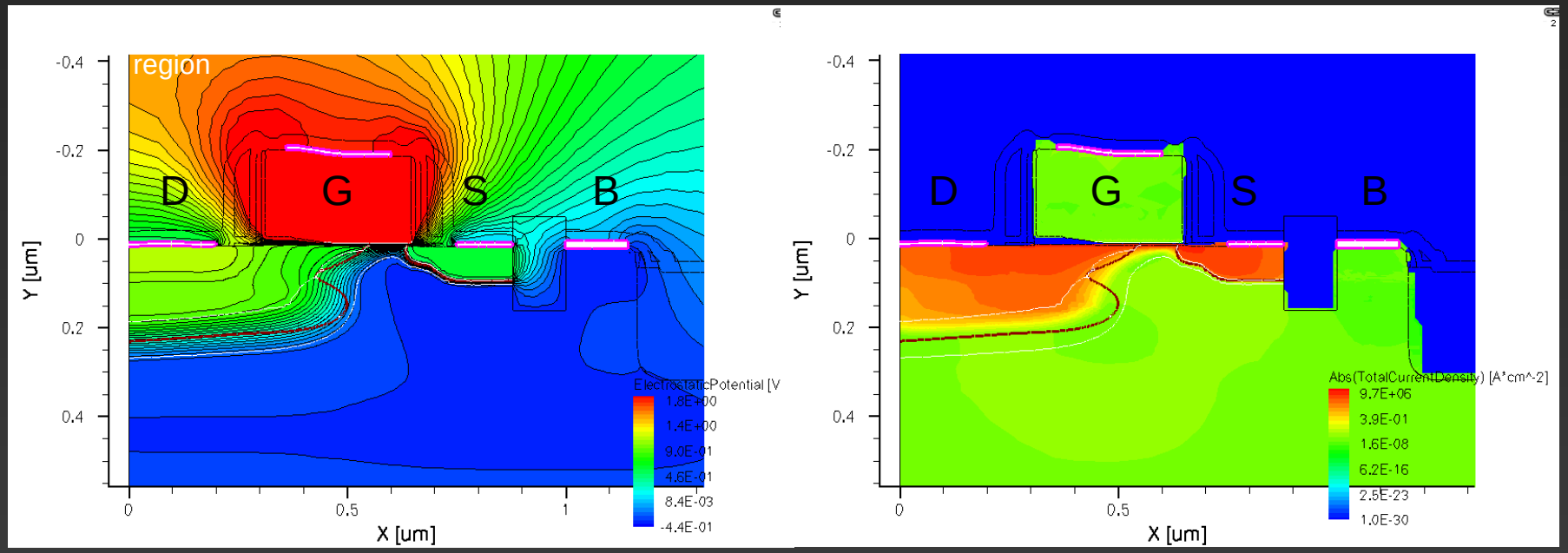
Concept, fabrication, characterization

180nm Si RFLDMOS: device concept



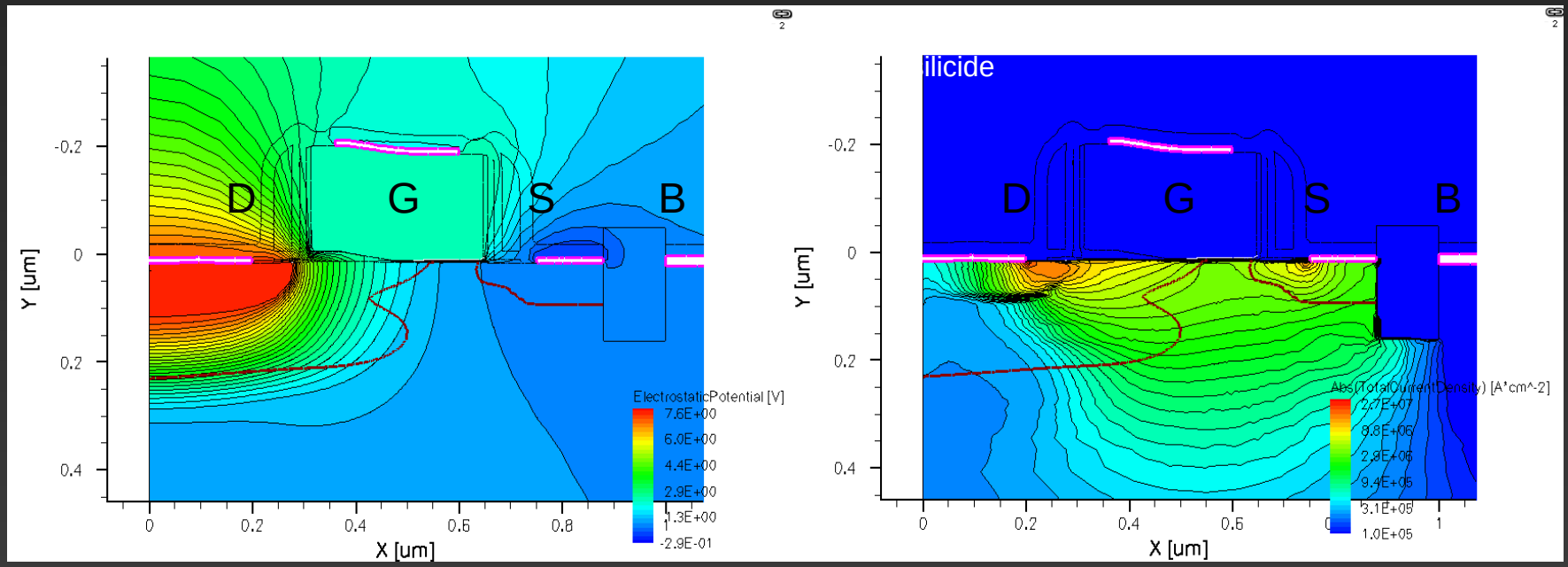
- RFLDMOS – LATiD drain and self-aligned channel for fT*BV_{ds}
  - Dual dielectrics for g_m and GIDL (BTBT) control, diffused drain reliability (not EDMOS)
  - LATiD drain *prior* to PC gate, LATid body *post* PC gate (+2ML over 5V CMOS)
  - Tapered field plate structure for linearized E_x (x) in the drift region
    - 30A – 130A, 50A – 480A

180nm RF LDMOS: On-state simulation



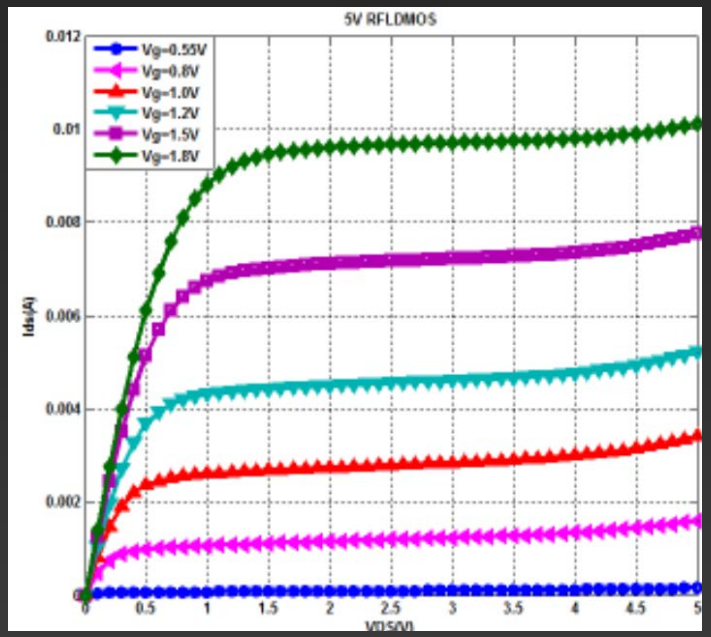
- Self-aligned channel LATiD drain LDMOS – device pitch < 1μm
  - Co-implants: 10-30` 10^{12} – 10^{13}, dual 1.8V/5V oxide, < 1μm pitch
- Device on-simulation V_{gs}=1.8V, V_{ds}=500mV, V_b=V_{iso}=0V
  - Left: potential contour channel dominant, l_{eff} < 0.18μm
  - Right: current contour – deep drain conduction away from surface

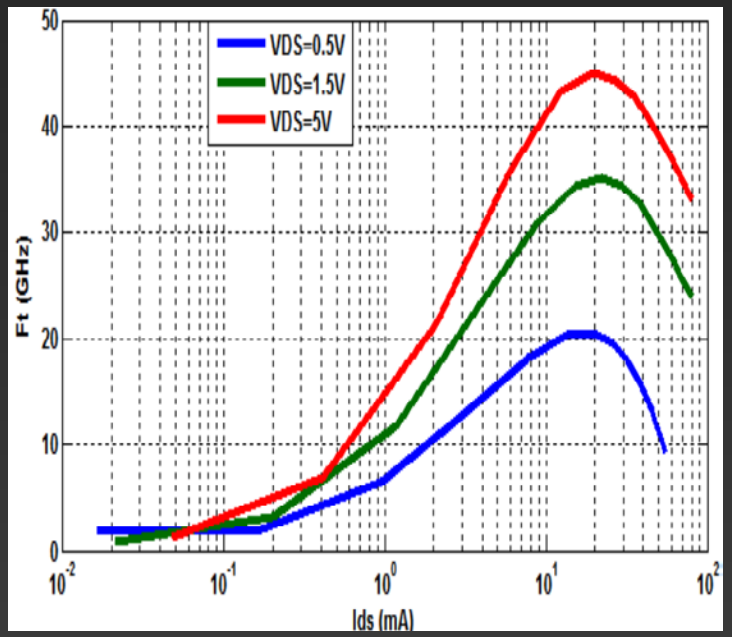
180nm RF LDMOS: Off-state simulation



- Device of-simulation (V_{ds}~7V, $V_{gs}=V_b=V_{iso}=0V$)
  - Left: equipotential contour (no channel PT)
  - Right: current density, peak near silicided drain, current BTBT limited
- Net: l_{eff} 0.18μm with BV_{ds} > 11 V – a good RF PA and embedded power device

180nm RF LDMOS: measured results





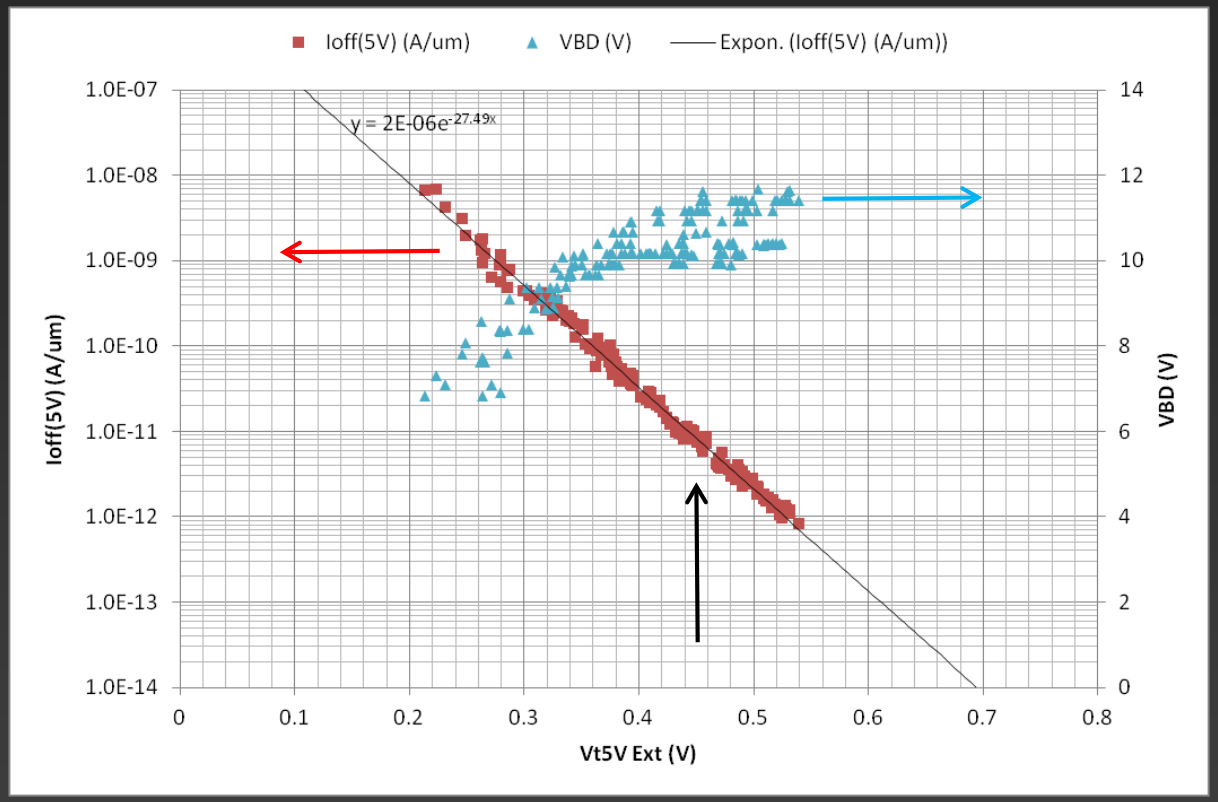
- DC and RF characteristics
  - Left: Fwd IV, I_{body} ~1% Id_{max} @ 5V, l_{eff} ~0.17um
    - **R_{sp} = 0.95 mOhm mm^2, BV_{ds} = 11.4V**
  - Right: fT vs I_{ds}, **fT_{peak}~ 48 GHz** (V_{ds}=0.5V), fT_{min}=20 GHz (V_{ds}=0.5V)
  - BV*fT = 563 V GHz

180nm Si RF LDMOS: tabulated results

		RFLDMOS		CMOS	
		5V NFET	5V PFET	5V NFET	5V PFET
Parameter	Units				
Vt(0.1V) (peak gm)	mV	525	460	610	565
Vt(1.5V)	mV	480	450		
Vt(5V)	mV	450	440	525	445
Idsat(5V)	uA/um	520	225	630	350
Ioff	pA/um	10	10	1.5	2.2
Peak f_T (Vds=500mV)	GHz	20	5		
Peak f_T (Vds=5V)	**GHz**	**45**	**16**	**15**	**11**
Ronsp	**mohm-mm^2**	**0.95**	**3.6**	**2.16**	**5.36**
BVds(I_D=10nA/um)	**V**	**9.9**	**9.3**	**8.0**	**9.5**
Gate Charge Q_{gg} (Vgs=1.8V, Vds=Vds_{NOM}) ON	fC/um	8.16			
Switching FOM Q_{gg}*Ron (Vgs=1.8V, Vds=)	**pC-ohms**	**8.3**		**18.9**	
GIDL Current (B2B) (Vgs=0V, Vds=Vds_{NOM})	pA/um	0.1	0.5		
VBD (Id=0.1um/um)	V	11.4	9.9	8	9.5
VB2B (Ib=100pA/um)	V	9.1	7.6		

- RF LDMOS vs 5V CMOS
  - 3X improvement in fT, 2.3X reduction in R_{sp}, 2.3X reduction in R_{sp}*Q_{gg}
  - The same device unit cell used for DC-DC SMPS and RF PA

180nm Si RFLDMOS: process control

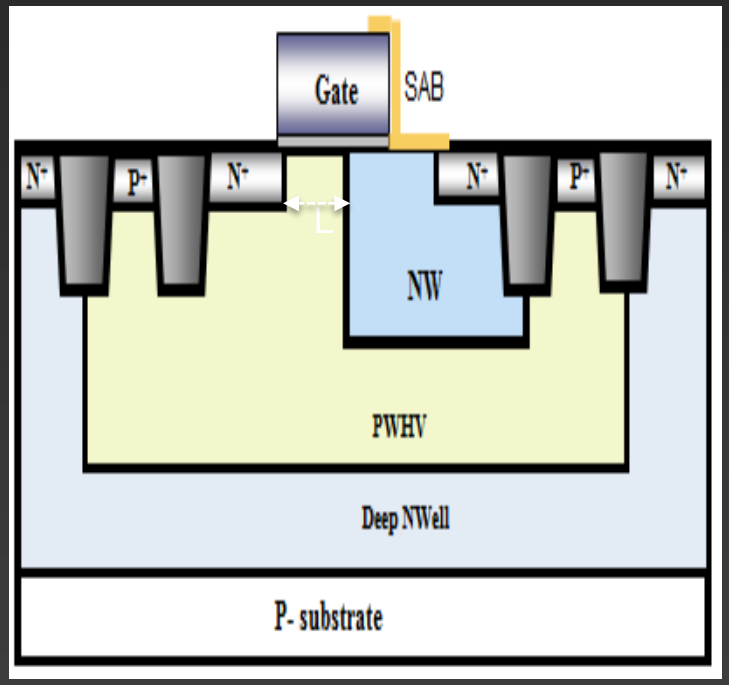


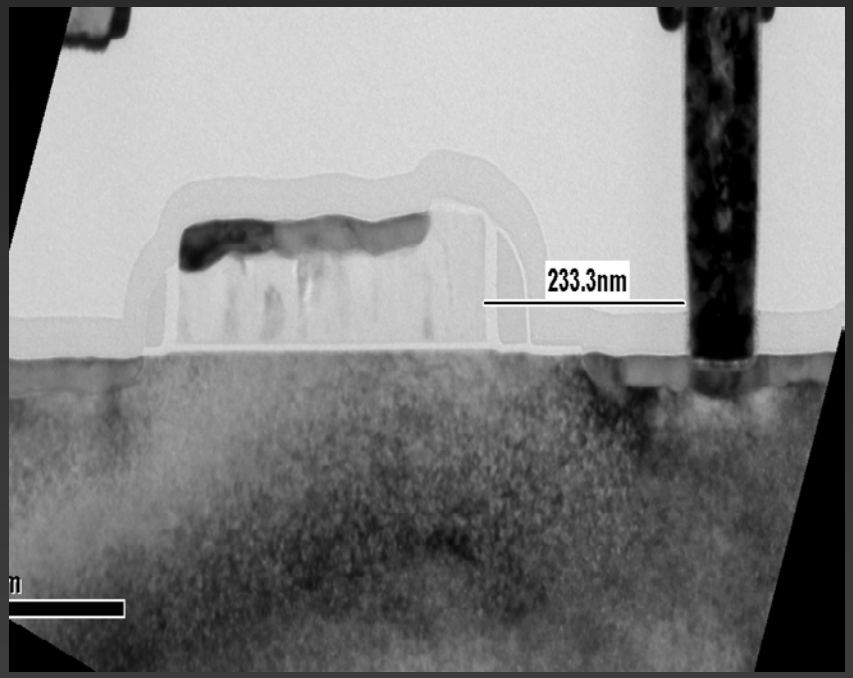
- RFLDMOS I_{off} vs Vt_{sat}, I_{off} vs BV_{ds}
  - Channel length variation through process and layout
  - V_t = 0.45 V +/- 0.1V sufficient to control I_{off}

55nm ED NMOS

Concept, fabrication, characterization

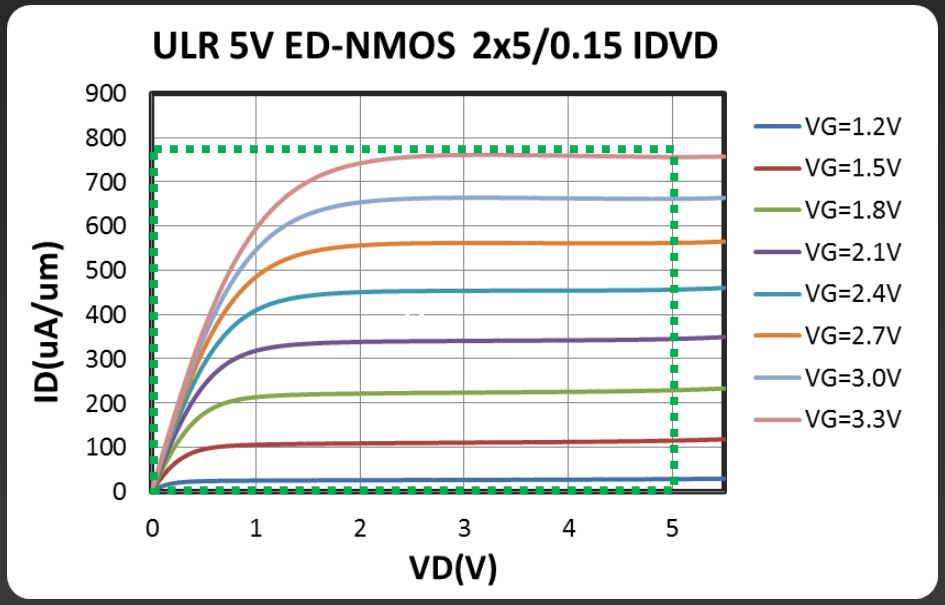
55nm RF EDMOS Design Concept

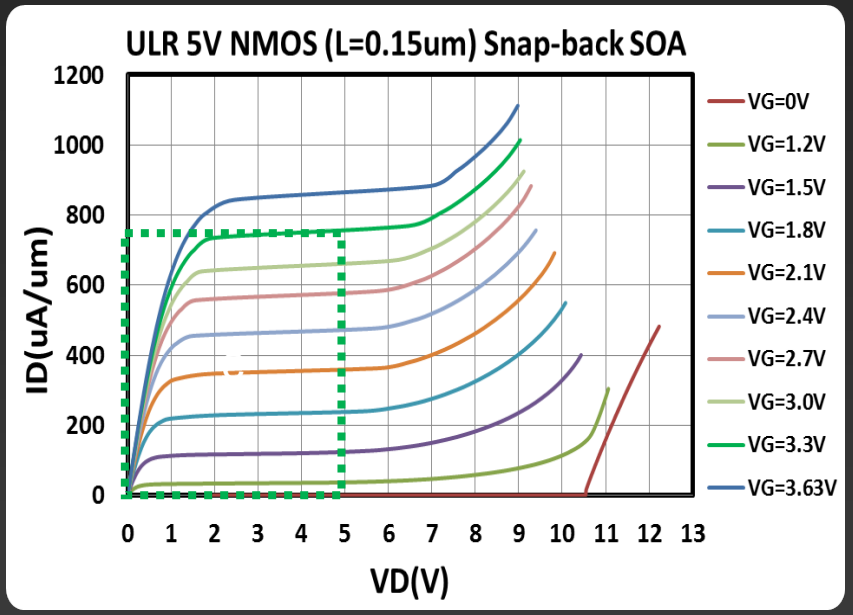




- **Key Focus on device optimization:**
  - Utilize the resolution of 55nm lithography (dimensions and overlay)
  - Minimize effective channel length by engineering pocket implant (similar solution as RF LDMOS)

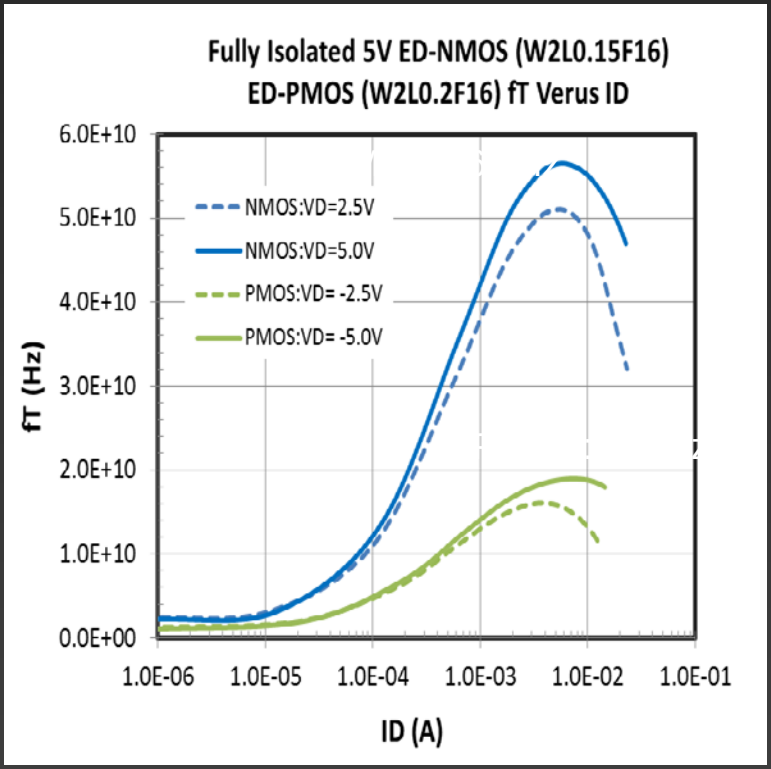
55nm 5V ED-NMOS DC Characteristics

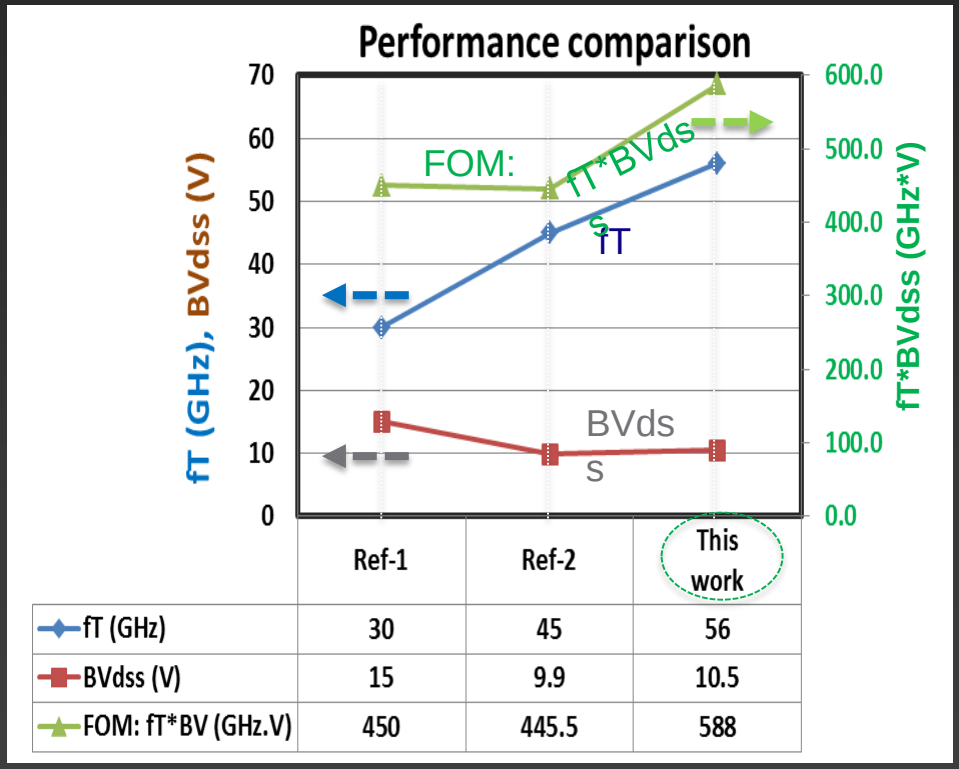




- 55nm RF EDMOS I_{ds} vs V_{ds}, FSOA
  - BV_{ds}=10.5V, R_{dson}=0.97 mohm mm^2, Id_{sat}=750 μA/μm I_{off}=0.3pA/μm
  - Rated voltages V_{gs}=3.3V, V_{ds}=5V (green box)
  - Super-linear conduction characteristic ideal for PA
- Demonstrated scalable to rated voltages in excess of 10V V_{ds}

RF Characteristics of 55nm EDMOS



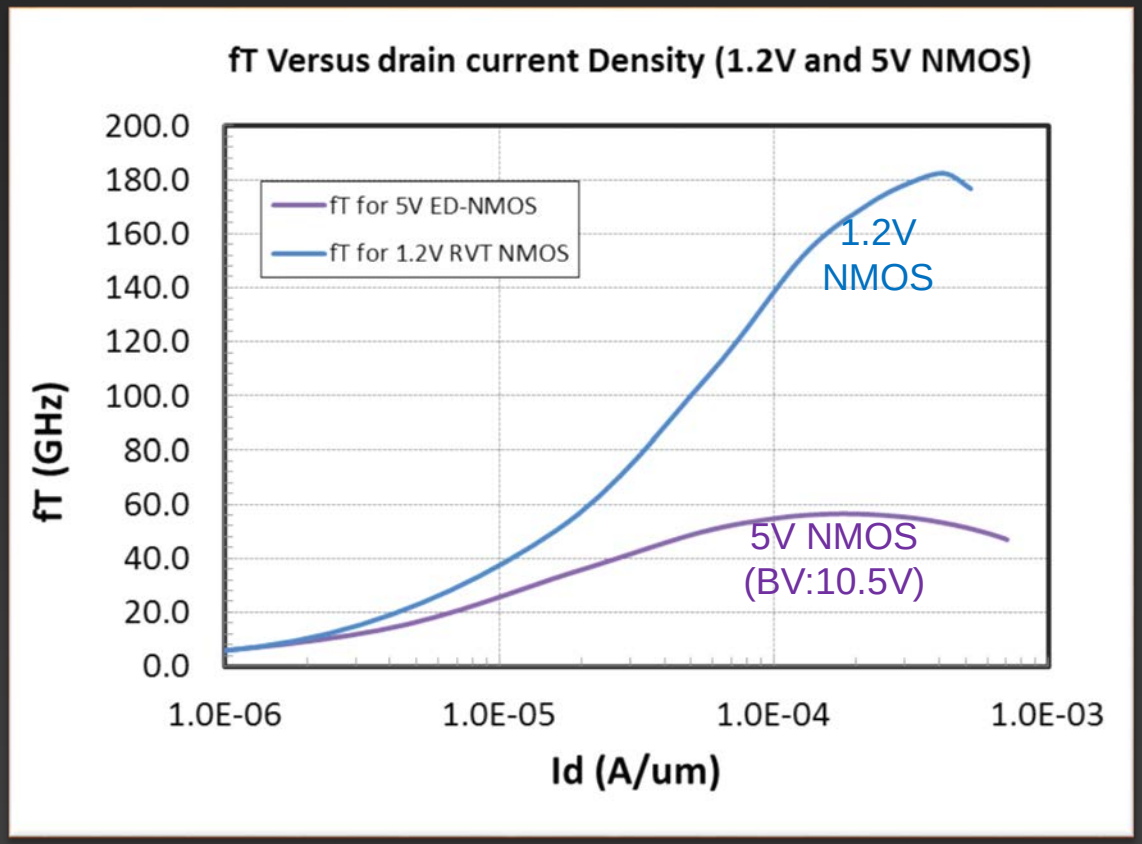


- RF EDMOS fT vs $I_{ds,}$ $fT*BV_{ds}$
  - BV_{ds}=10.5V, fT=56GHz, BV*fT = 580 VGHz

Ref 1. RFIC.2008.4561404, pp 141-

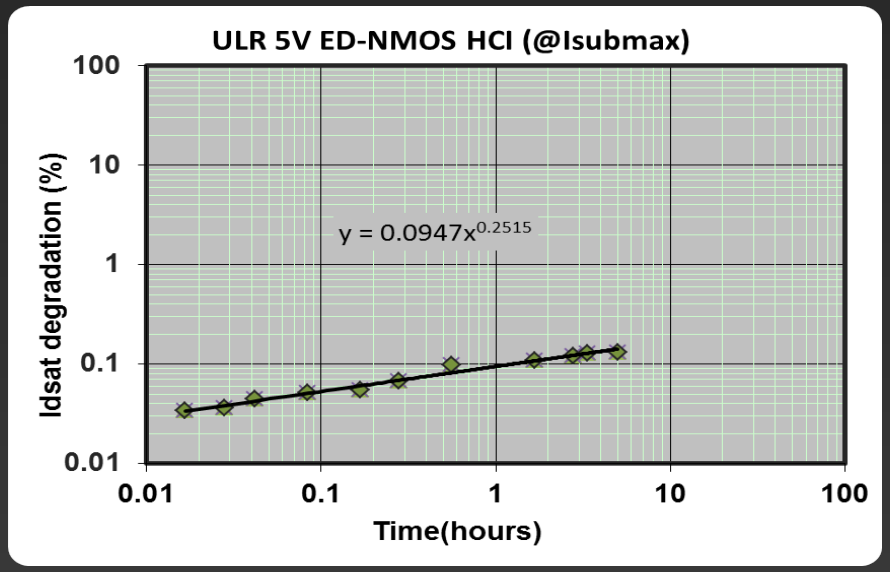
Ref 2. ISPSD May 2015, pp 337-340

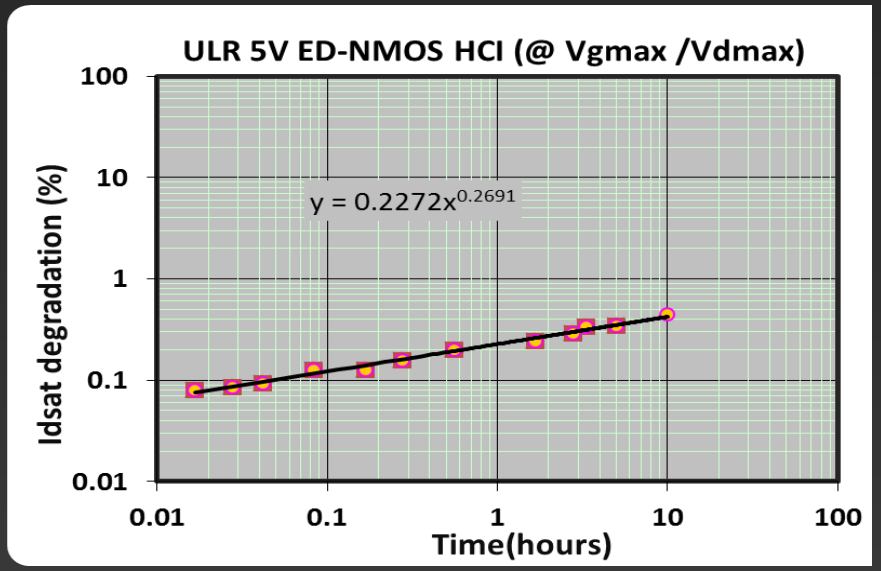
55nm Platform for IoT RF integration



- 55nm LPx RF EDMOS and CMOS
  - 1.2V CMOS core for digital, MCU, embedded memory
  - 1.2V with fT of 180GHz for LNA, VCO, PLL in a RF analog TRX
  - 5V EDMOS (BV 10.5V) fT = 56GHz for ET and RF PA in an IoT platform

55nm 5V ED-NMOS HCI Characteristics





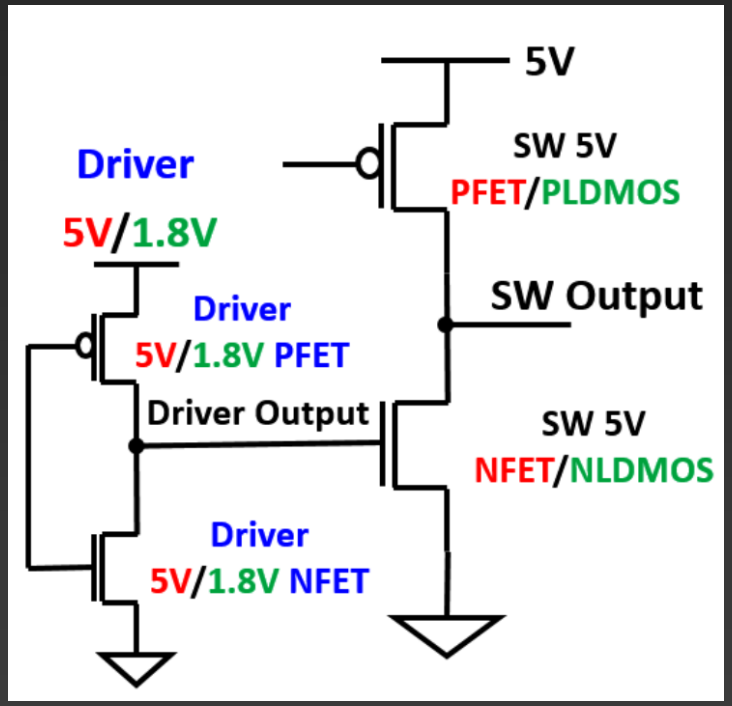
Device	DC $T_{0.5}$ (Yrs) @ Vg/Vd_{max}	DC $T_{0.5}$ (Yrs) @ $Isub_{max}$
ED-NMOS	146	12700

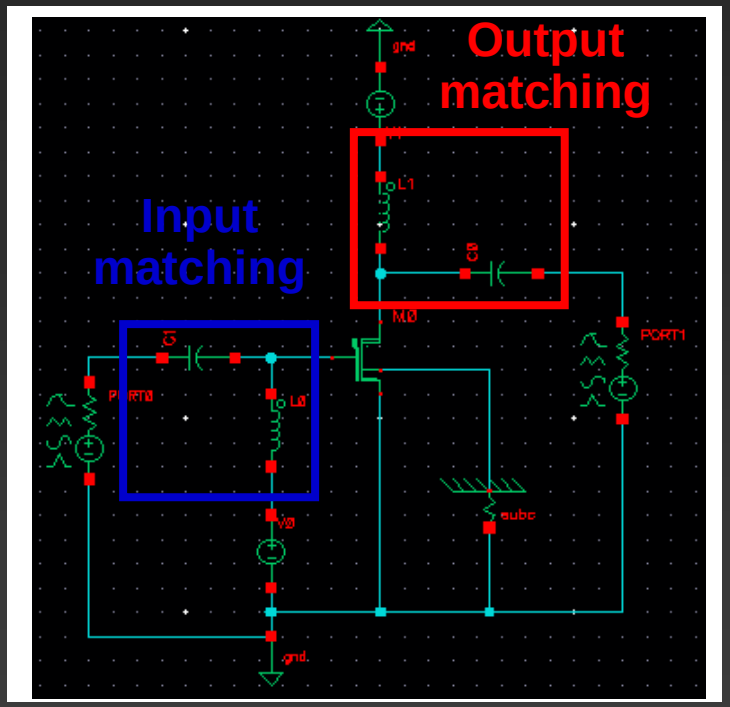
- RF EDMOS HCI
  - Power law dependence $t^{0.25}$ – typical for DMOS structure single trap mechanism
  - Time to half-population fail >> 100yrs for both maximum substrate current and maximum rated voltage stress

RF Benchmarking and Standards

Design, characterization, standards

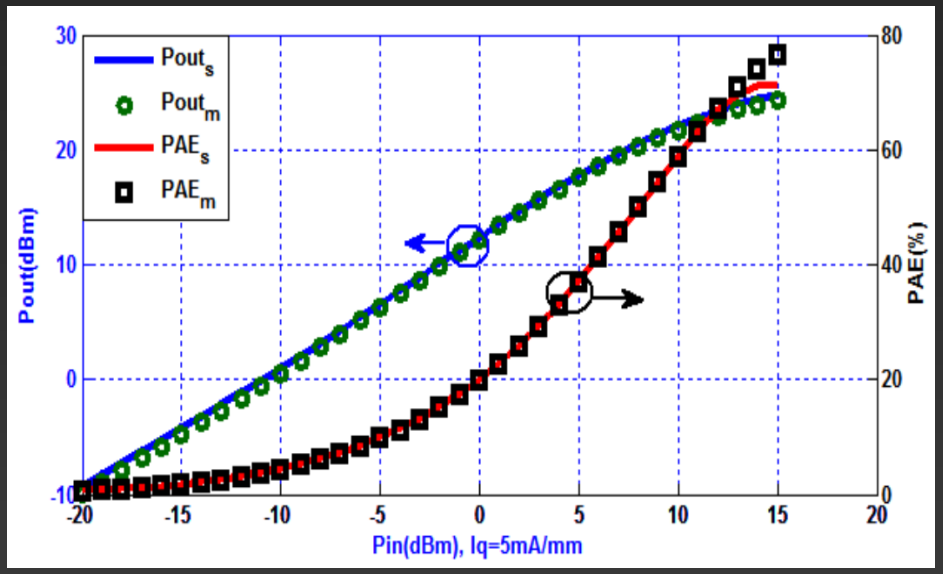
Si RF LDMOS: Application test benches

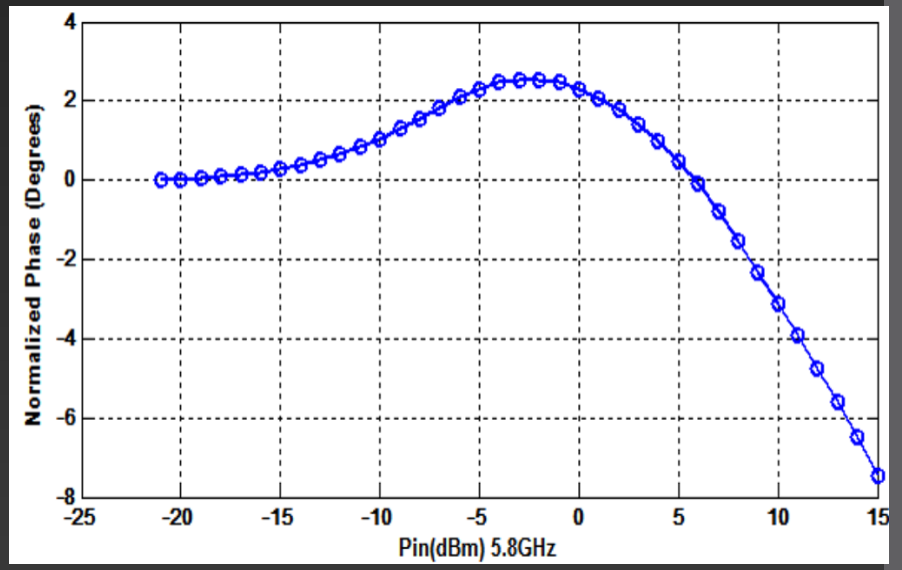




- SMPS
  - ET - quantify driver efficiency (75% reduction in driver dissipation)
- RF PA
  - Matched 2.5 GHz/ 5.8 GHz RF PA for load-pull analysis

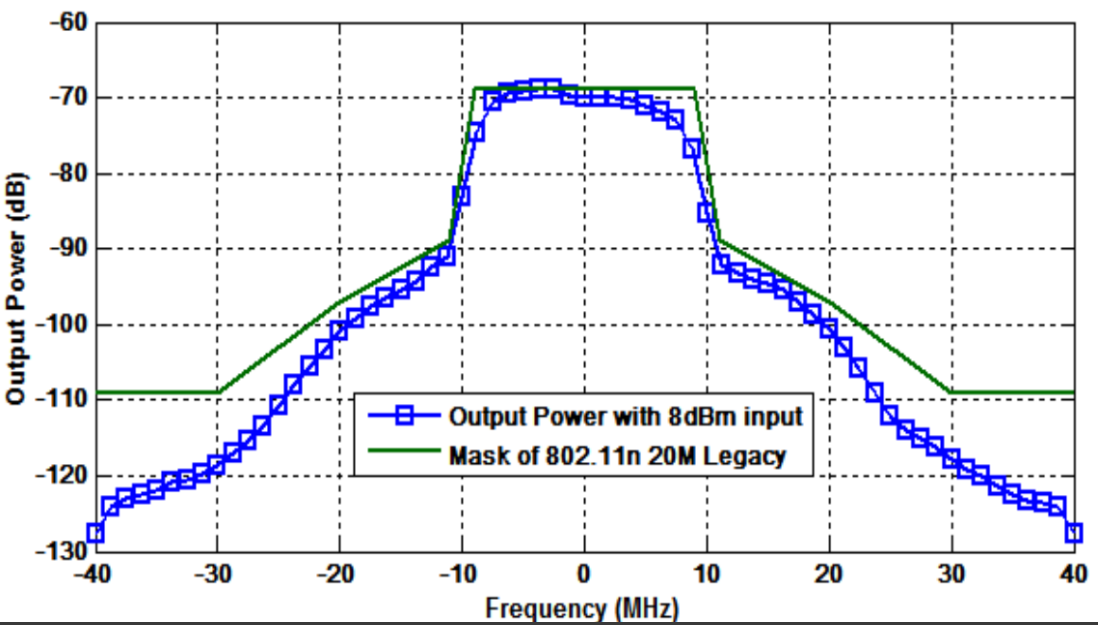
Si RF LDMOS: 5.8 GHz RF PA





- RF power cell layout and load pull to 5.8 GHz – a linearity study
  - 20MHz 64QAM modulation (HB WiFi), matched PA
  - Left – RF P_{out} vs P_{in} : 19dBm PA with > 70% PAE (saturated)
  - Right – RF AM/PM phase distortion < 3%
- RFLDMOS device performance similar to SiGe, GaAs

Si RFLDMOS: 5.8 GHz RF PA



- RFLDMOS PA linearity
  - A measure of adjacent channel power coupling – nonlinear C(V)
  - P_{in} = 8 dBm (10 dBm back-off) for high peak-to-average power
- PA meets IEEE 802.11n 20 MHz mask specification
  - “raw” performance – no digital pre-distortion

Si RFLDMOS: PA Comparison

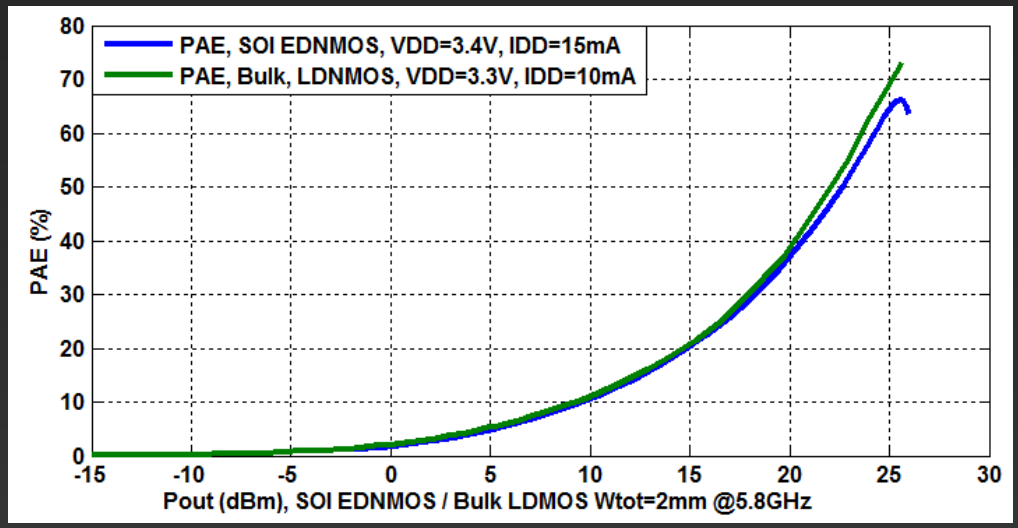
2.4 GHz RF PA Comparison					
Technology	Vcc	Pout	Gt_1	Freq	PAE
	(V)	(dBm)	(dB)	(GHz)	
RFLDMOS 2mm	**3.5**	**25.6(1dB)**	**17.6**	**2.4**	**68%(1dB)**
RFLDMOS 4mm	**3**	**27.5(sat)**	**14**	**2.4**	**72%(sat)**
130nm SOI CMOS *	6.5	32.4(sat)	14.6	1.9	47%(sat)
65nm EDMOS **	5	30	25	2	60%(sat)

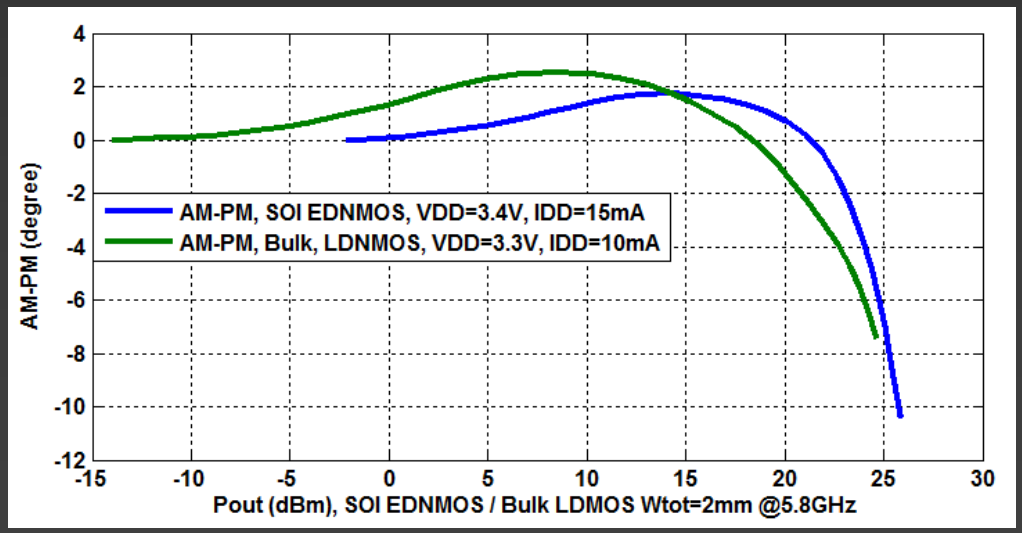
- RFLDMOS 2.4 GHz RF PA
  - Highest efficiency at lowest supply voltage
  - High single stage gain – easier layout without inter-stage matching

* Pornpromlikit et al., IEEE MTT vol 58 pp 57-64 2010
** Aposolidou et al., IEEE RFIC p 148, 2008

Si RF LDMOS and SOI EDMOS

- 5.8GHz
  - 130nm SOI EDMOS
  - V_{dd}=3.5V, Id=40mA, w=2mm
- 5.8GHz
  - 180nm bulk Si LDMOS
  - V_{dd}=3.3V, Id=10mA, w=2mm
- High-band WiFi PA
  - Load pull measurement
  - PAE for SOI EDMOS and bulk LDMOS is similar
  - Gain of SOI device is higher (16dB vs 10dB @ P_{out}=20dBm)
- Bulk and SOI are meet RF integration targets – SOI has slightly better AM/PM at P_{out}>15dBm





Summary

- PowerSoC and RF devices can be integrated using the same device unit cell
- 180nm RF LDMOS and 55nm RF EDNMOS
  - Both structures have pitch <1μm and:
  - R_{sp} < 0.95 mOhm mm^2, BV_{ds}>10.5V, fT>50 GHz (>10x HB WiFi)
  - Ideal PowerSoc implementation scenarios:
    - 180nm RF LDMOS – 5V SMPS - 2.3X lower P_{diss}, 75% lower gate driver loss
    - 55nm RF EDMOS – IoT platform with integrated RF, MCU, memory and control
  - 5V CMOS – should be replaced by asymmetric LD/EDMOS
    - Asymmetric methodology scalable to >10V rated structures <55nm nodes
- Measured RF results against wireless specifications
  - 5.8 GHz PA meets/exceeds IEEE 802.11n (802.15.4, 802.11.ah)
- LDMOS/EDMOS fabricated in high-volume foundry
  - LDMOS – manufacturable
  - EDMOS – reliable

Thank you