Fully-Integrated Digital Average Current-Mode Control Voltage Regulator Module IC

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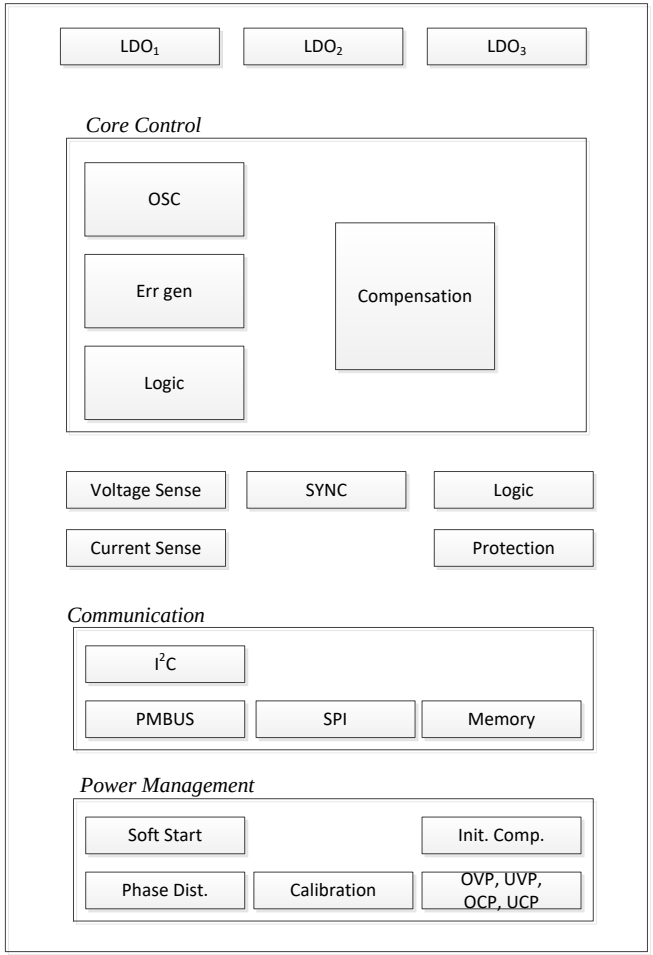
Controllers for VRMs and PoLs

Control Objectives

- Regulate the output voltage
- Obtain zero or small steady-state (DC) error
- Fast recovery from input and load changes
- Reasonable overshoot



Analog Controllers

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Still in the lead

- ✓ Accurate and efficient
- ✓ Fast response – wide bandwidth
- ✓ High (continuous) resolution
- ✓ Lower costs (<3A – All analog)

- - -

- × Labor intensive
- × Tailored compensation
- × Pin count
- × Limited flexibility/scalability
- × Communication and interface
  Big D + Big A

Digital Controllers

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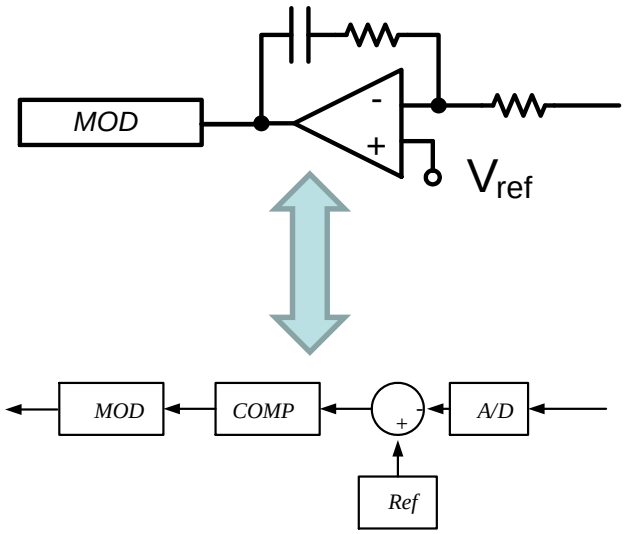
- ✓ Comparable or better dynamics
- ✓ Reduced size of overall solution
- ✓ Scalable and flexible
- ✓ Auto-tuning - No compensation
- ✓ Plug-and-play
- ✓ Lower pin count
- ✓ Efficiency optimization

- - -

- × Different design
- × Power hungry

What do we really trade for a digital controller

- Mimicking analog controller operation by a digital one
- Conventional ADCs are too expansive
- High-res PWM is power hungry
- Do we ‘settle’ for voltage-mode



Protection, power management, etc. are still in…

How “lean” can we go?

Digital Architecture
Bottom up

Create an attractive alternative to analog control

- Hardware redesign
  - Focus on the benefits of digital electronics
    - Specifically targeted to power management
  - Avoid sensitive analog units
  - Standard-cell digital design (no custom design)
- Standardize the design flow
  - Reduce labor efforts
  - Easier testing
  - Faster development

One step ahead:

Entire controller created through code

Digital Process

Synchronous

- ✓ Reliable
- ✓ Well-defined behavior
- ✓ Sequential or parallel

- × Power hungry (HS clk)
- × Synchronization hardware (e.g., clock tree)

Asynchronous

- ✓ Low power
- ✓ Ultrafast
- ✓ Area saving

- × Different design method

Objective

- Develop a compact All-digital controller architecture for VRM or PoL
- Entire hardware described through HDL
  - All standard digital design flow
  - No analog part
- Integrated switches (12V nominal input)
  - Minimize analog labor (drive)

Compensation type

Voltage-mode

$$D[n] = D[n-1] + av_{err}[n] - bv_{err}[n-1] - cv_{err}[n-2]$$

$$D[n] = D[n-1] + a * v_{err}[n] - b * v_{err}[n-1] - c * v_{err}[n-2]$$

3 multiplications + accumulator

Current-mode

$$d[n] = d[n-1] + k\left[i_{err}[n] - (1 - \frac{T_s}{t}) i_{err}[n-1] \right]$$

Single multiplication

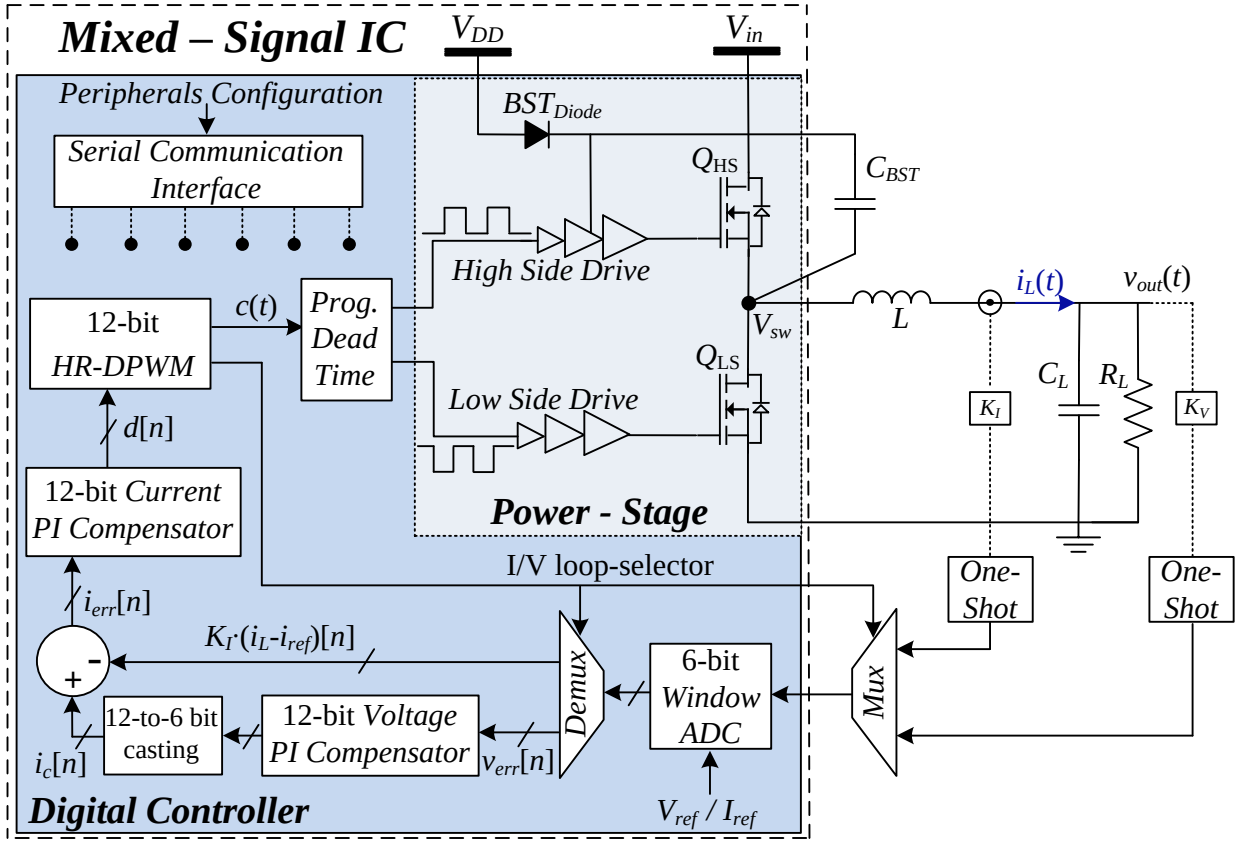
Buck IC Conceptual diagram

Core controller

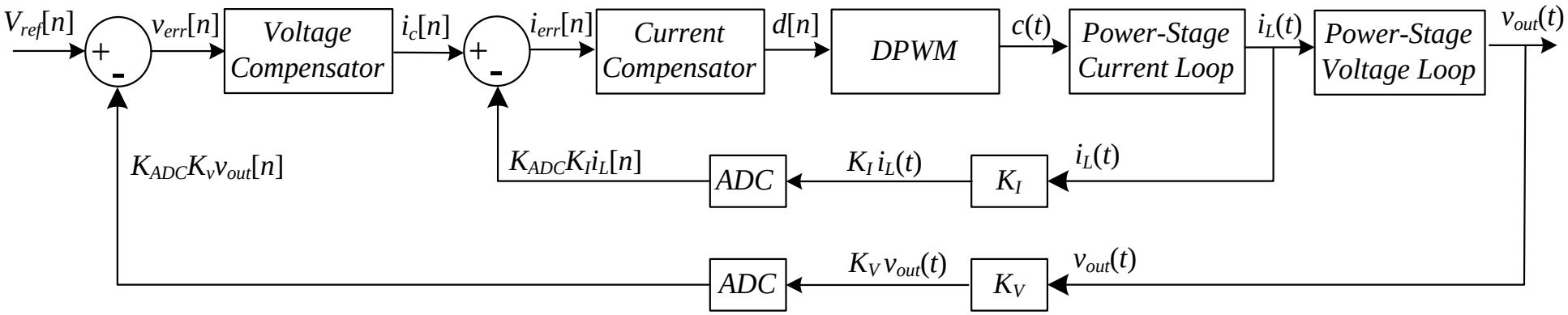
- Single-multiplier PI comp.
- Shared hardware
- 6-bit window ADC
- 12-bit HR-DPWM

Periphery

- SPI
- Programmable deadtime



Control flow

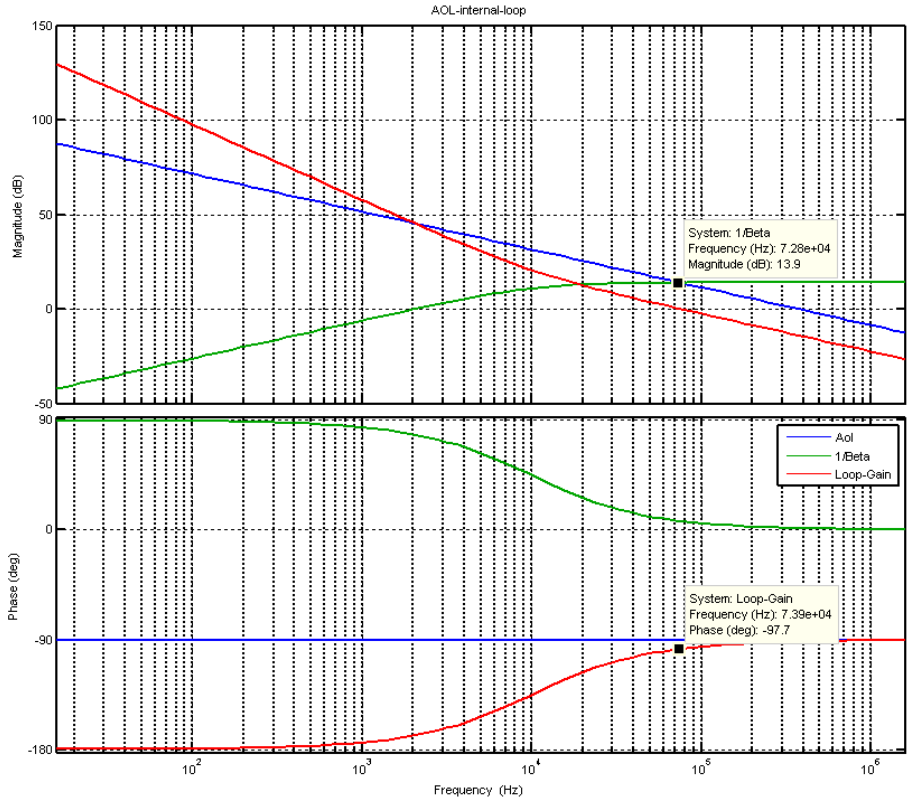


$$v_c[n] = v_c[n-1] + av_{err}[n] - bv_{err}[n-1]$$

$$a = k_p \quad , \quad b = k_p\left(1 - T_S / T_i\right)$$

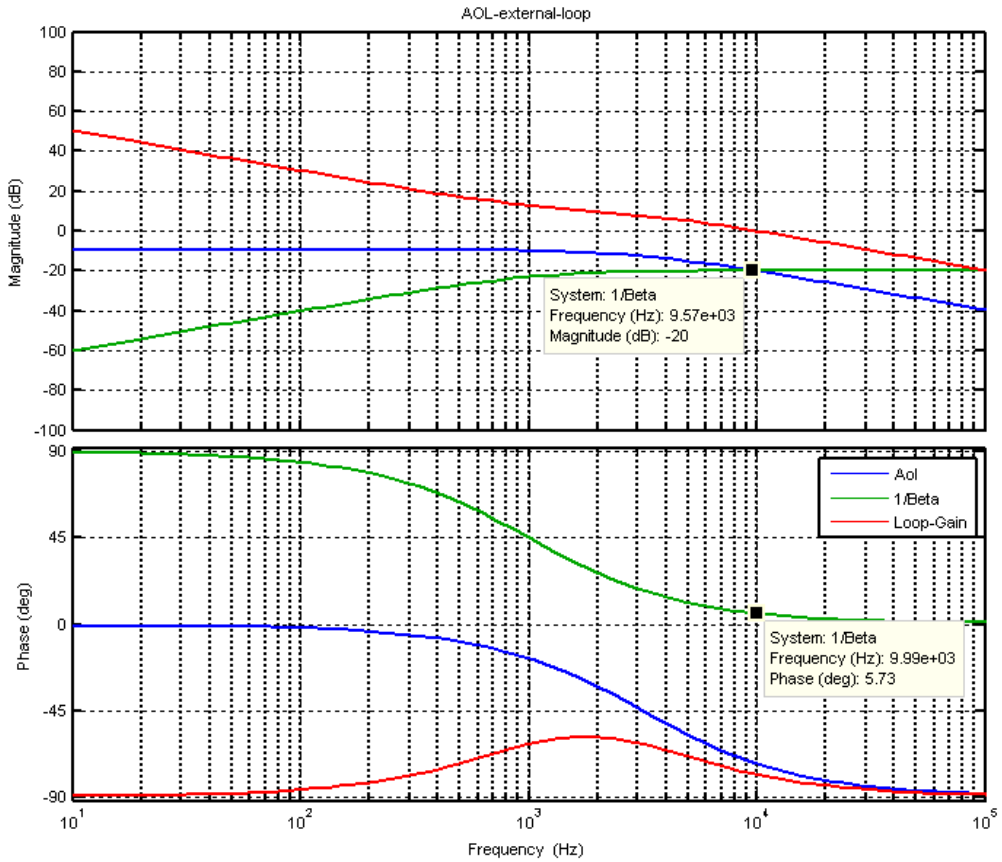
Current (inner) loop

$$d[n] = d[n-1] + k\left[i_{err}[n] - (1 - \frac{T_s}{t}) i_{err}[n-1] \right]$$



Voltage (outer) loop

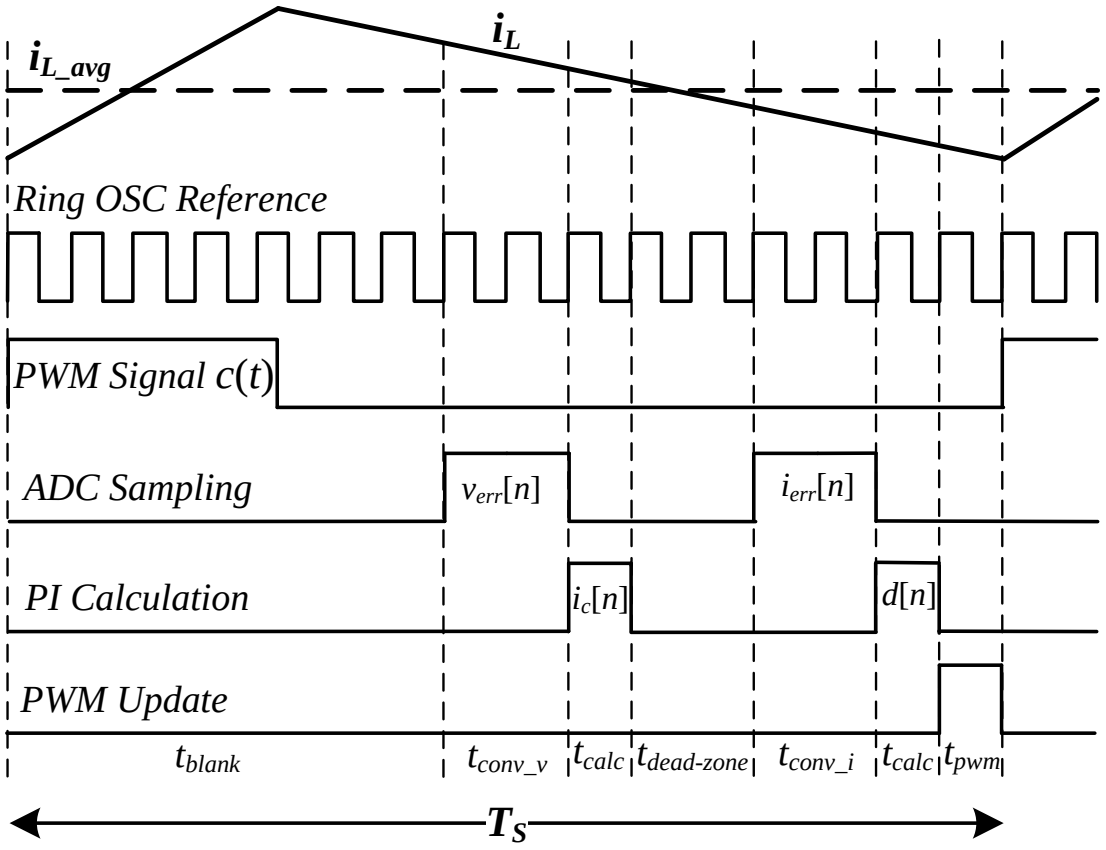
$$v_e[n] = v_e[n-1] + k\left[v_{err}[n] - (1 - \frac{T_s}{t}) v_{err}[n-1] \right]$$



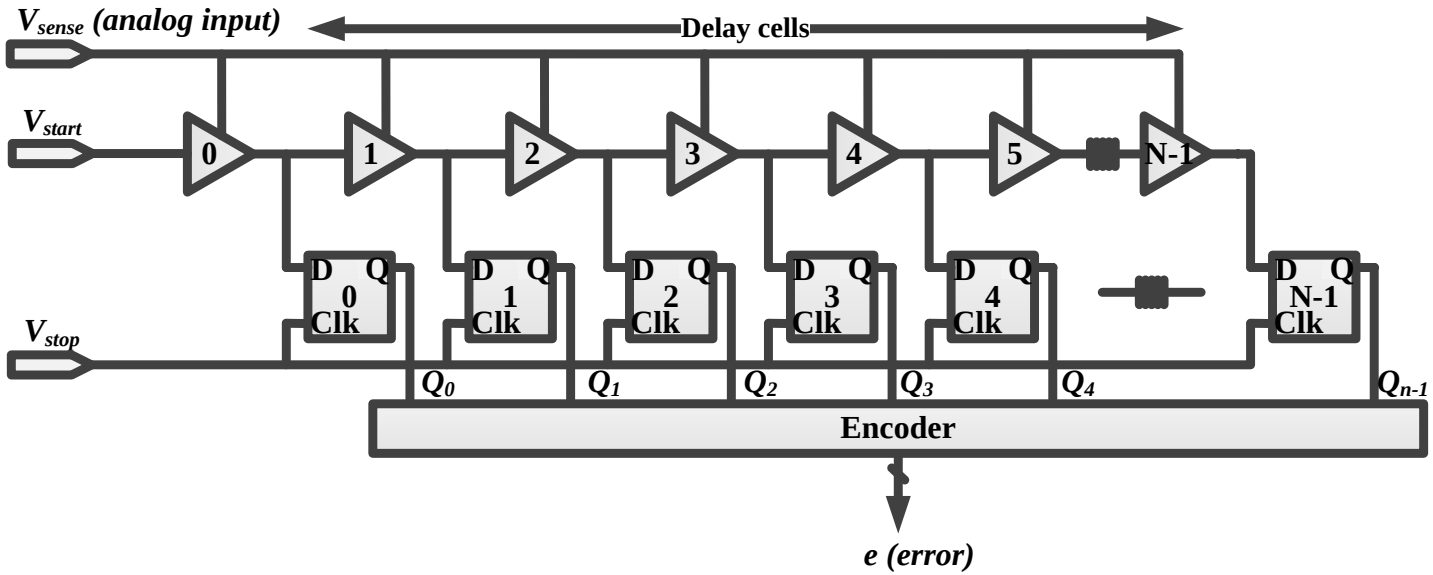
Timing sequence – key waveforms

- Ring-osc. generates mid-range frequency (10-20 MHz)
- Time-interleaved ADC
- Time scheduling PI operation

Each unit is designed as an asynchronous block



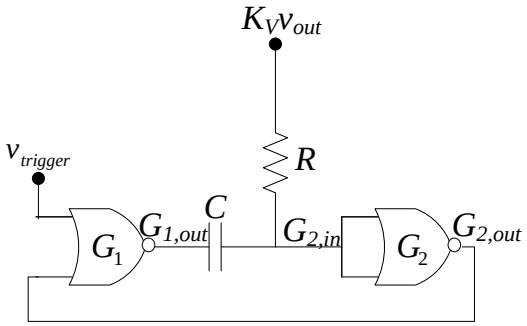
Delay-Line ADC

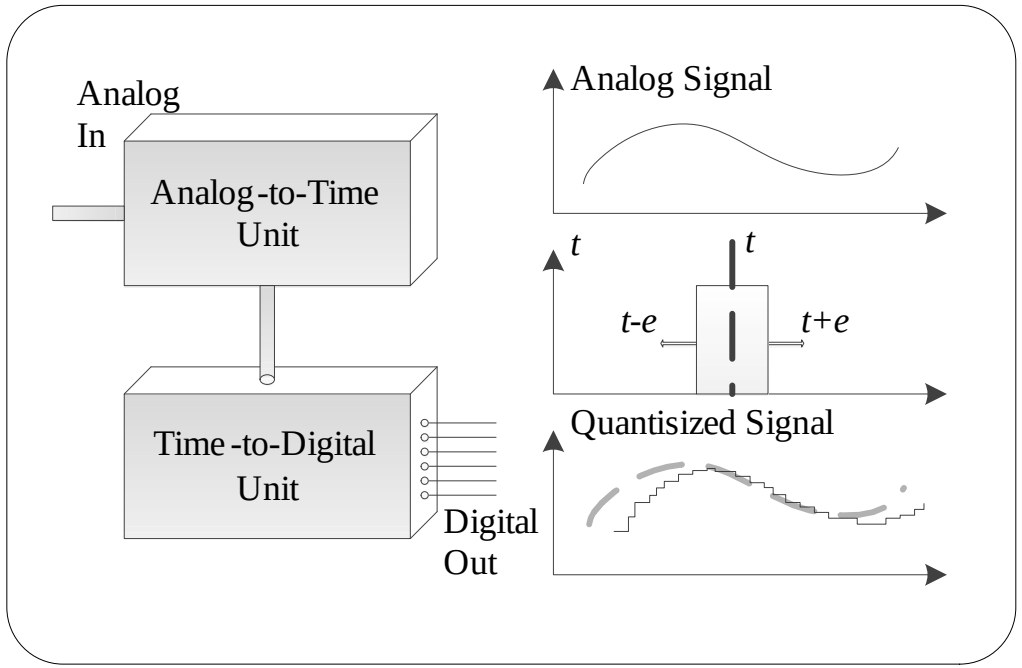


- Voltage-controlled delay
- Key factor – custom design of the delay cell
  - Not suitable for standard-cell synthesis
  - Difficult scalability
  - More complex layout

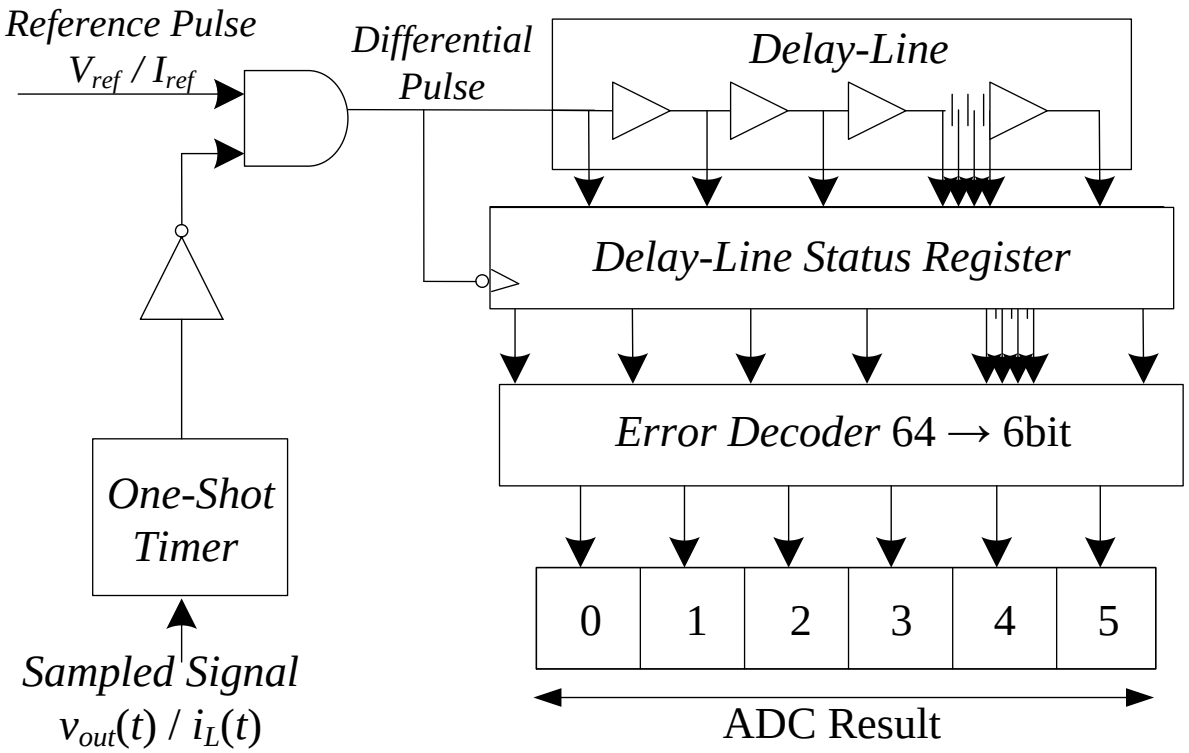
Constant-supply DL ADC

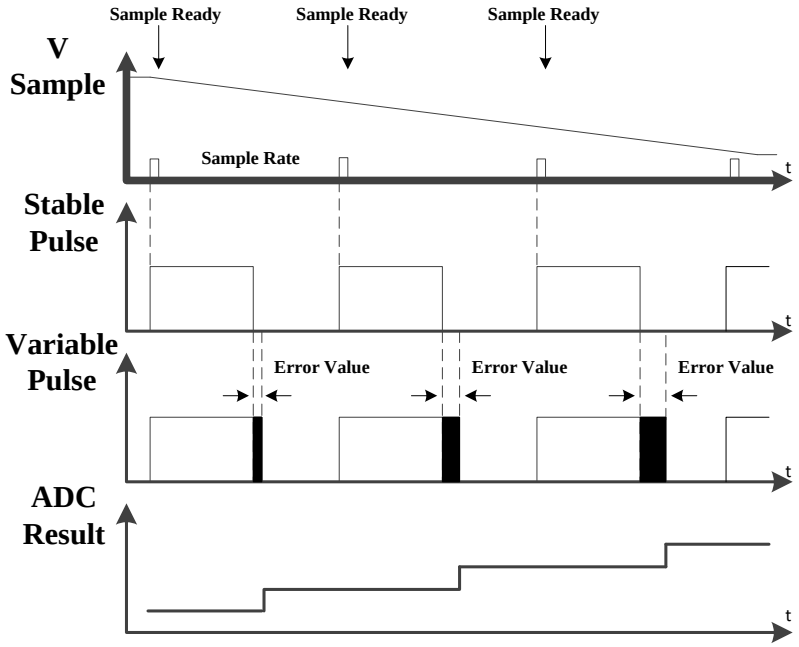
- 2-phase conversion: ATC + TDC
- ATC outside the buffer string
  - Realized by OS-timer
  - Digital gates
  - RC creates the analog link
  - No S&H





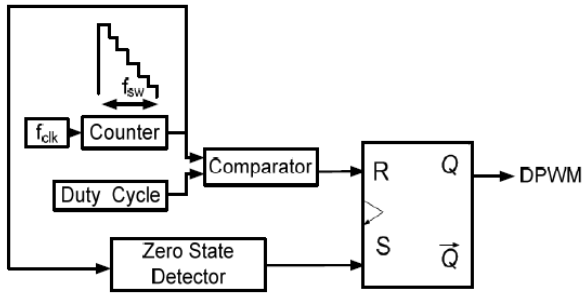
Window DL ADC



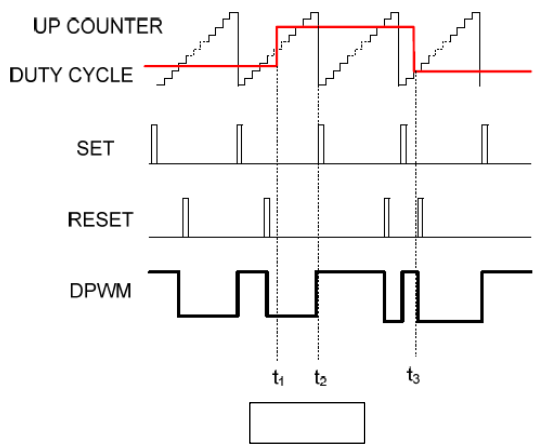


HR-DPWM
HS clock

- High power consumption
- High accuracy – very high clk freq

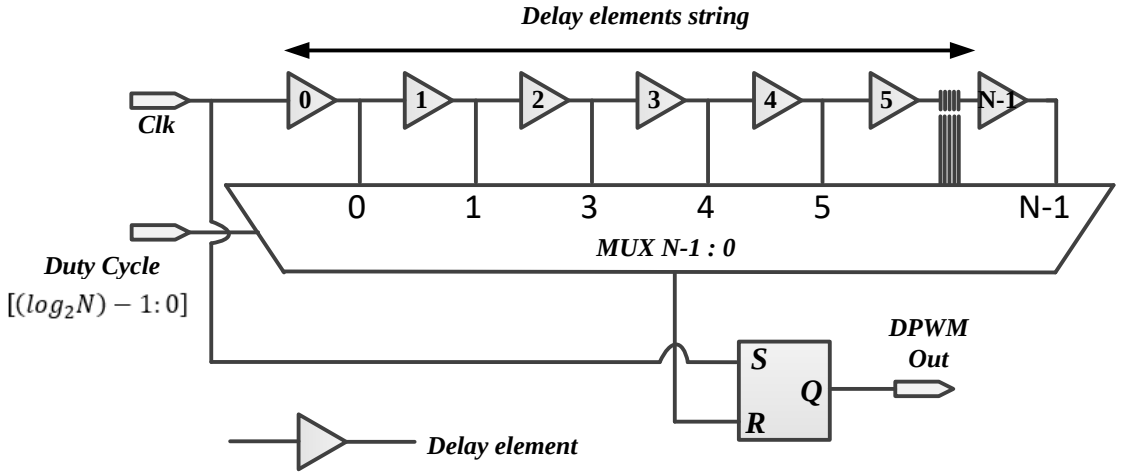


(a)

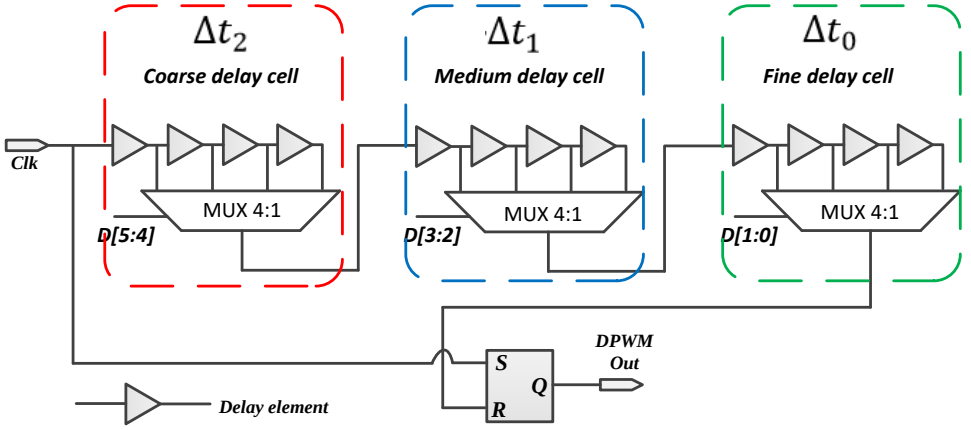


HR-DPWM Delay-Line

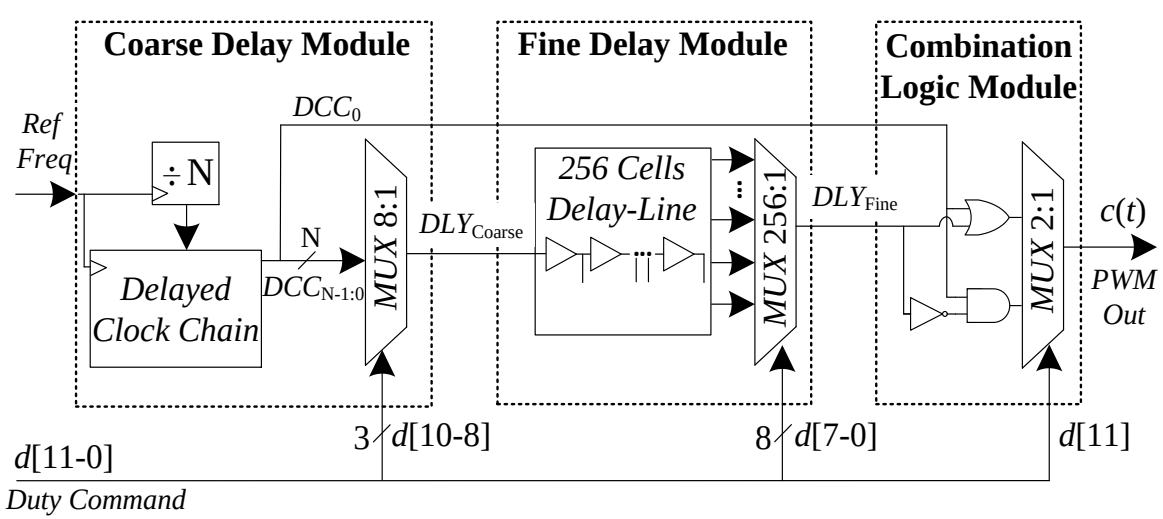
- Area demanding

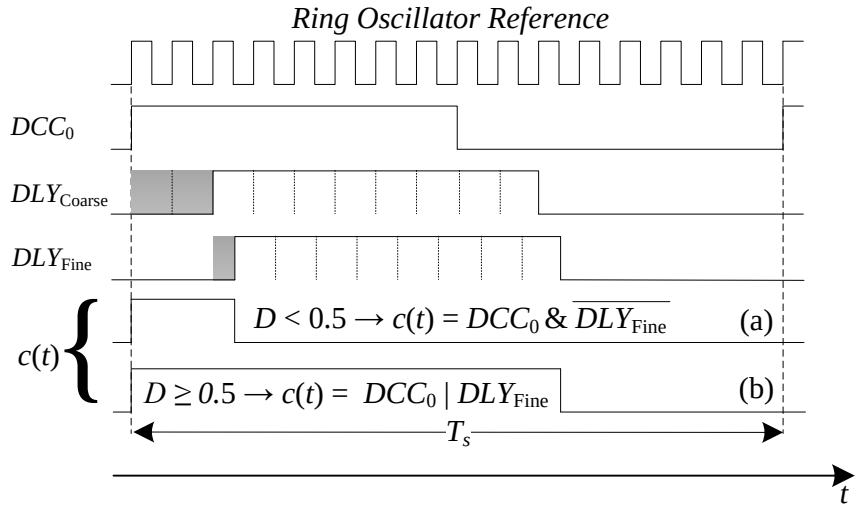


- Segmented DL



HR-DPWM
Segmented DL

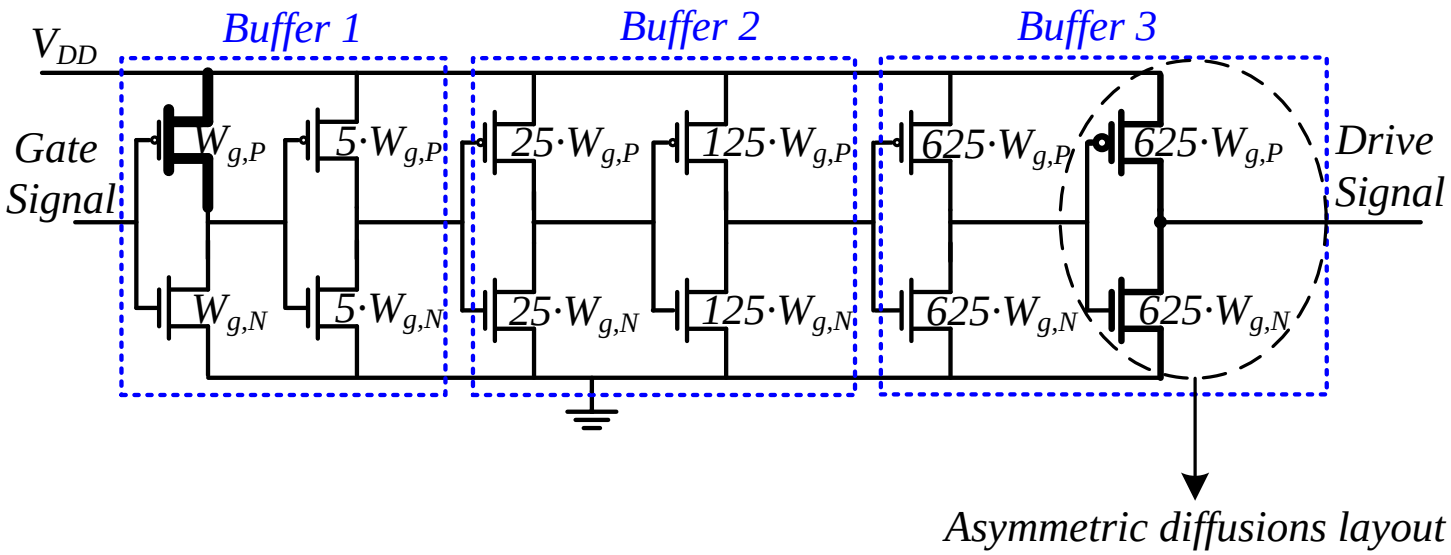




- Low power consumption
- High accuracy

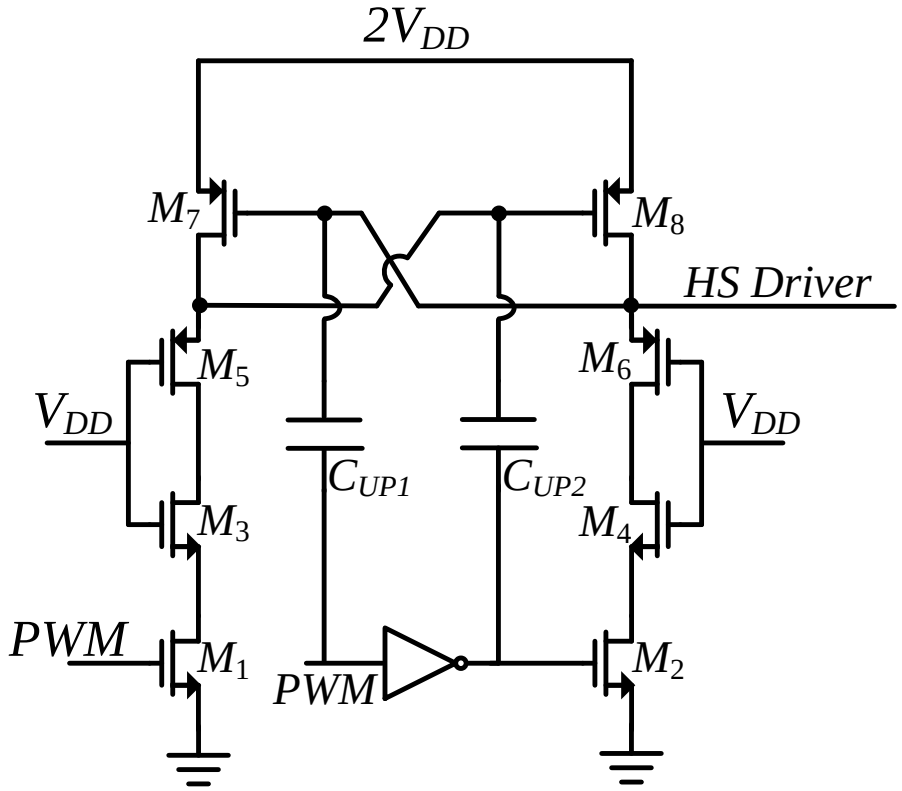
Gate driver

- Extended drain - similar to LDMOS structure
- Enabling the use of high drain-to-source voltages
- Compatible with ESD scenario

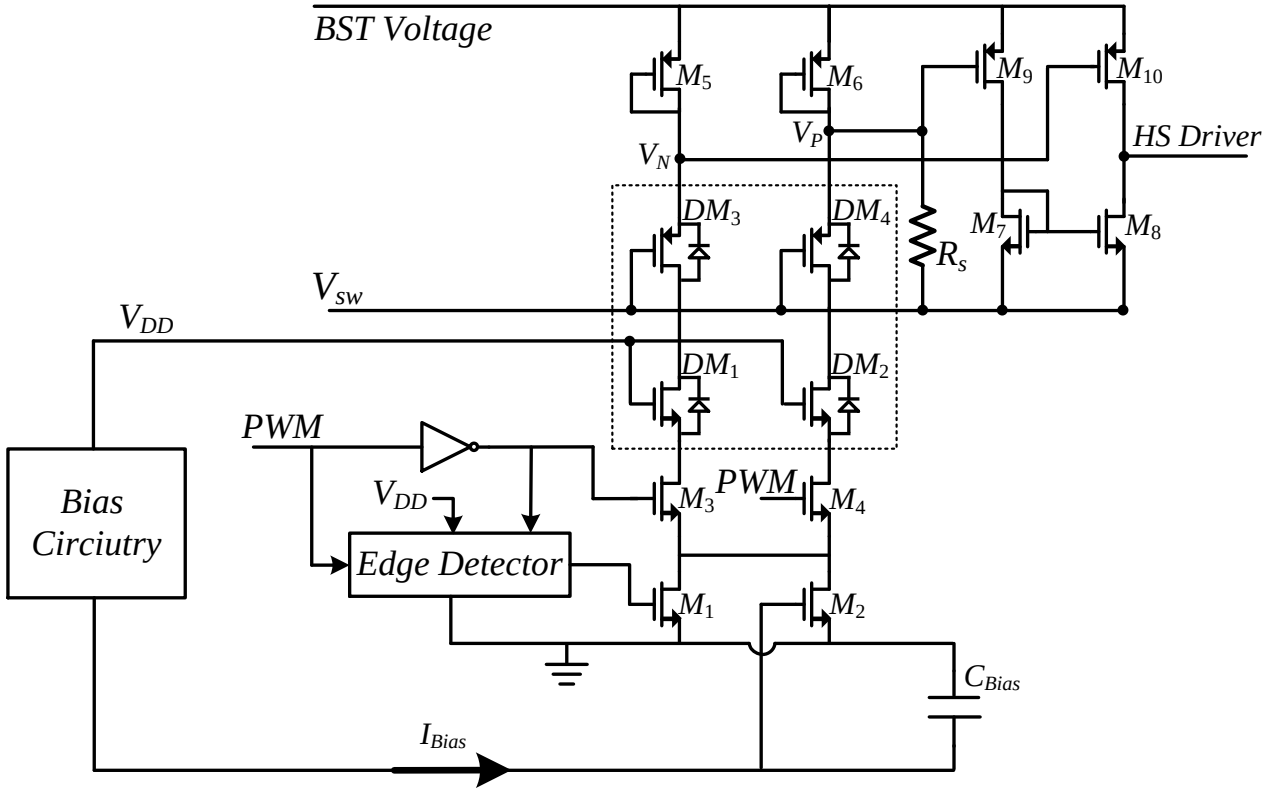


HS drive level shifter
Capacitive method

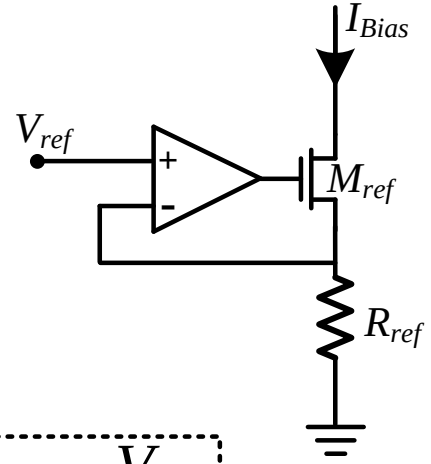
- Capacitive coupling level shifter
  - Short delay
- For higher shifting ratios (>$2V_{DD}$) – ladder configuration is essential



Level Shifter – current biased



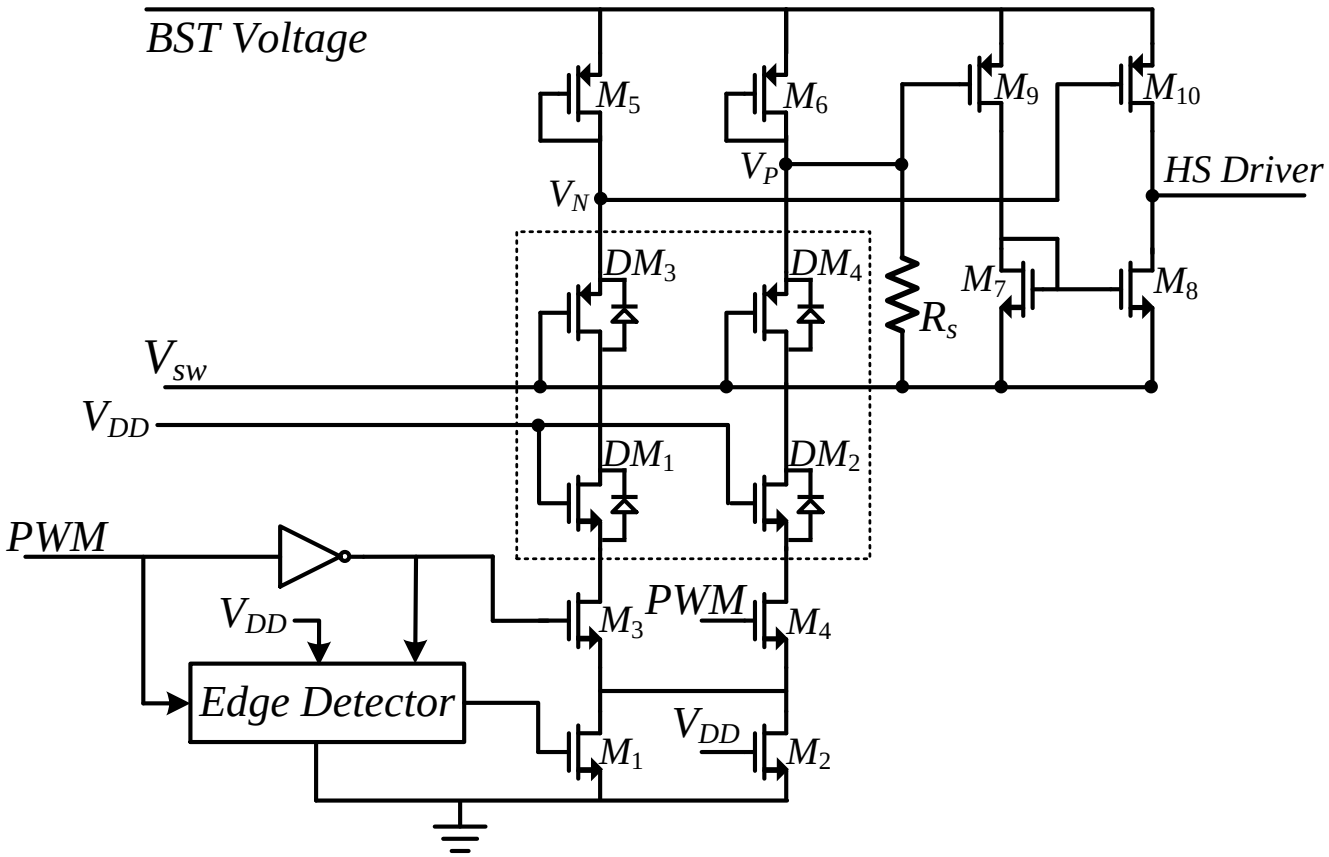
Bias circuitry



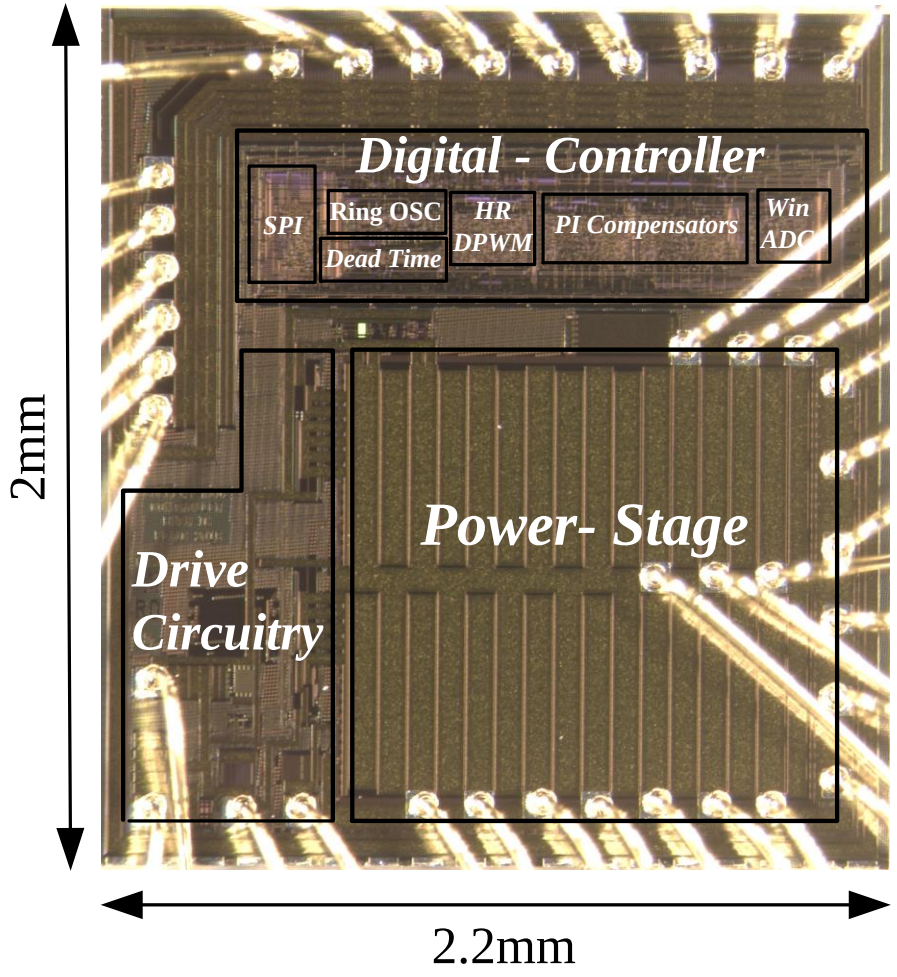
$$I_{Bias} = \frac{V_{ref}}{R_{ref}}$$

"Lean" Level shifter

Biasing circuitry (Analog) removed



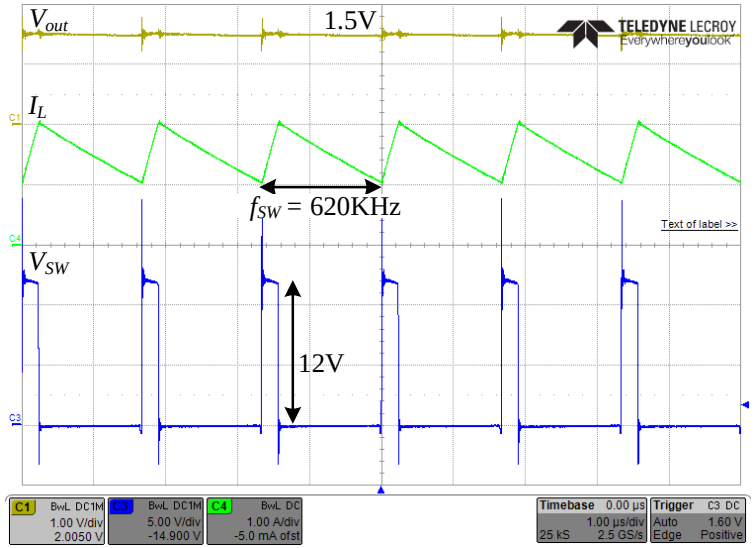
Fabricated IC

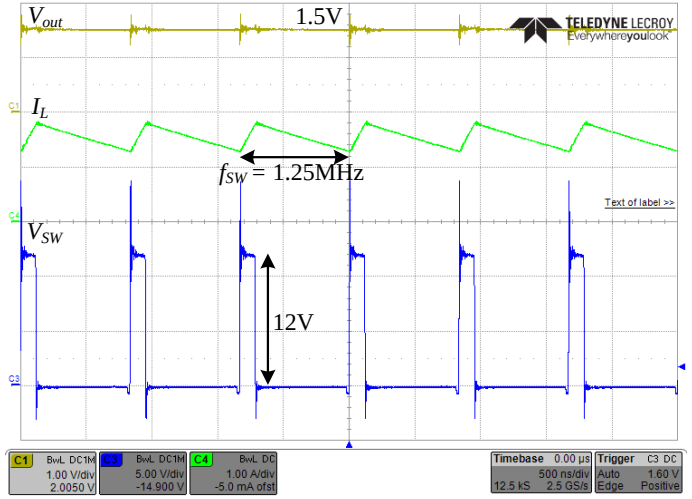


IC Block / Digital Core	0.18µm CMOS
Supply Voltage	5V
DPWM resolution	12-bits
DPWM nominal frequency	1.25MHz
DPWM Si area	0.03 mm^2
ADC resolution	6-bit
ADC conversion time	20nSec
ADC Si area	0.022 mm^2
PI calculation time	< 40nSec
PI Si area	0.034 mm^2
Effective controller Si area including Ring-Oscillator, Dead-Time and SPI	0.16 mm^2

Experimental results

Specifications	*Value*
Package	5x5 QFN - MLP
V_{in}	12V
Power-stage R_{on}	~160mΩ
Nominal V_{out}	1.5V
Nominal I_{out}	1.5A
Off-chip LC filter	2.2µH, 50µF
Switching frequency f_{sw}	1.25MHz (620KHz)
Peak efficiency	70% (76%)
***package limited	
Total chip Si area	4.4mm^2



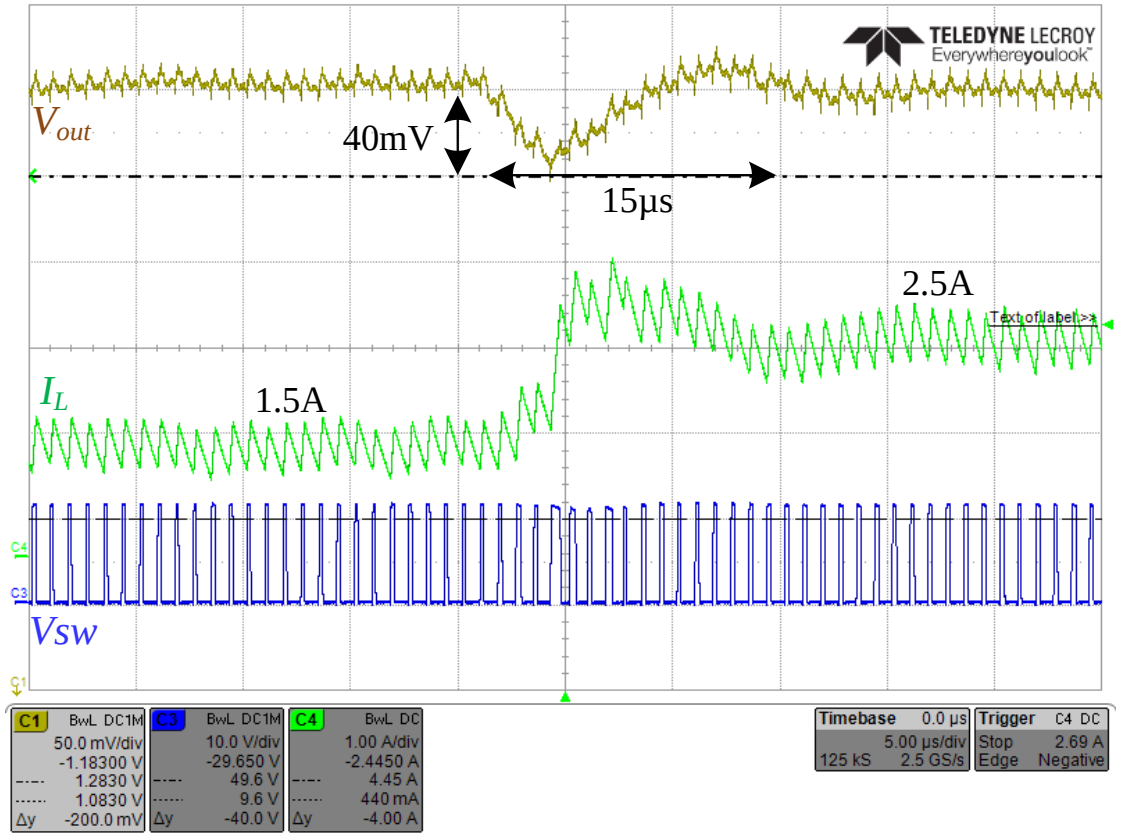


PWR SOC16

Loading Transient

Loading transient 1.5A ->2.5A

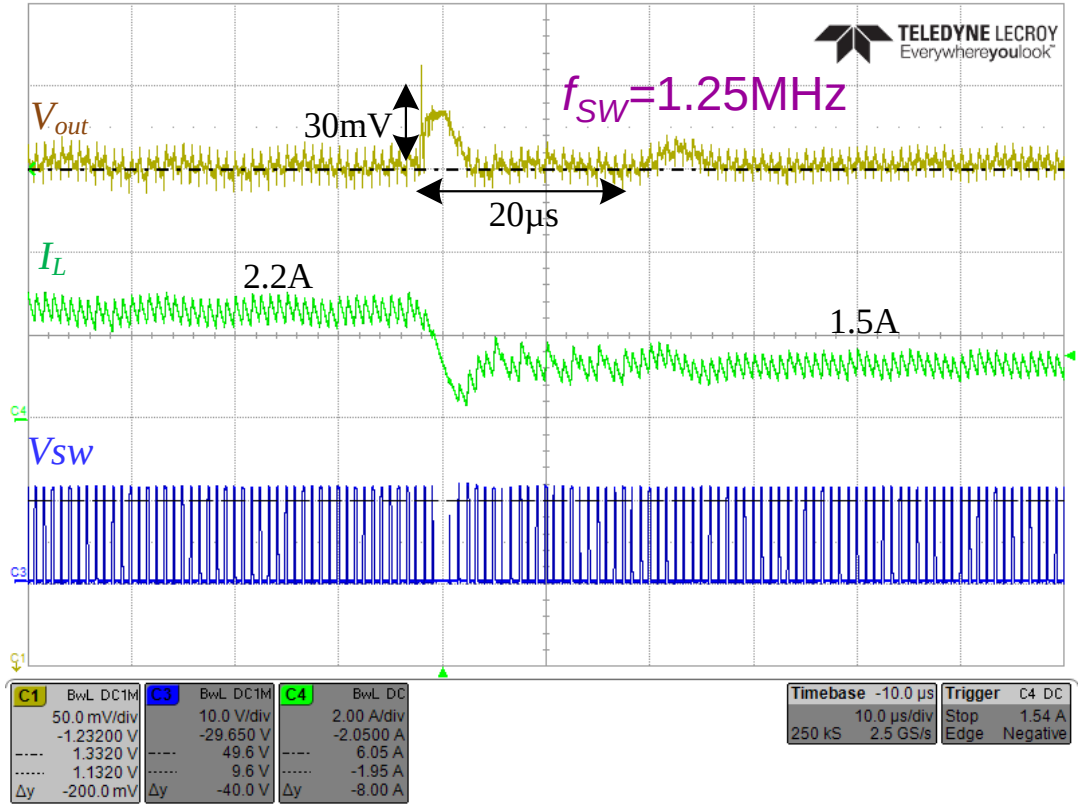
Vin=12V, Vout=1.3V

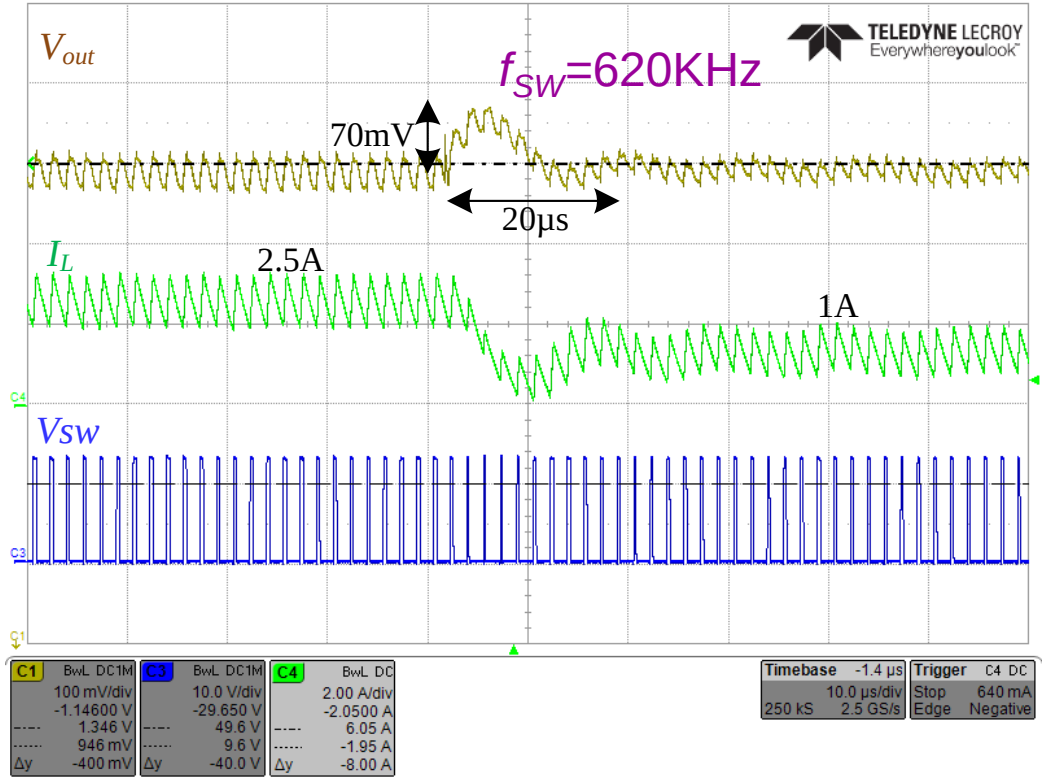


Unloading Transient

Unloading transient 2.5A ->1A

Vin=12V, Vout=1.3V,





Acknowledgements

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Thank You !