Towards Fully Integrated Power Management

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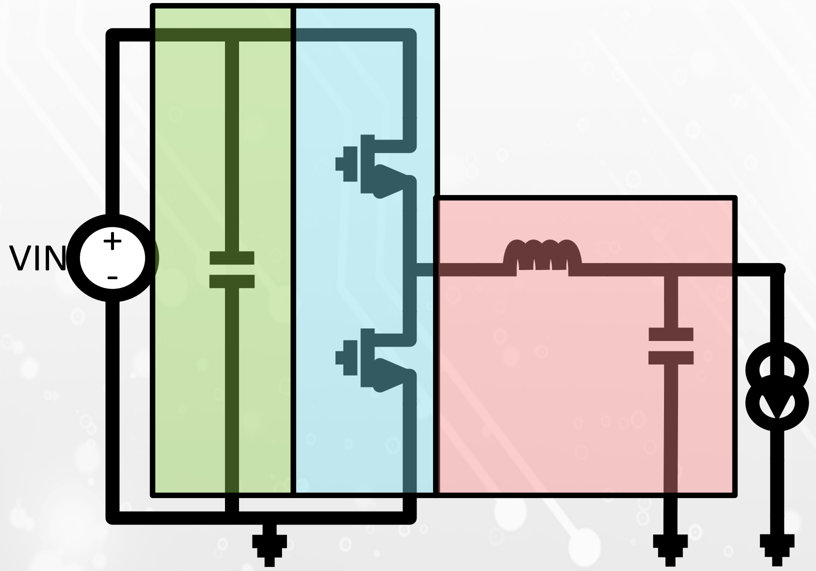
Texas Instruments

The Power Management End-Game

Invisible → 100% Efficiency, 0 Volume

Easy-to-Use → Complete power management in 1 chip, no EMI

Power Supply On a Chip

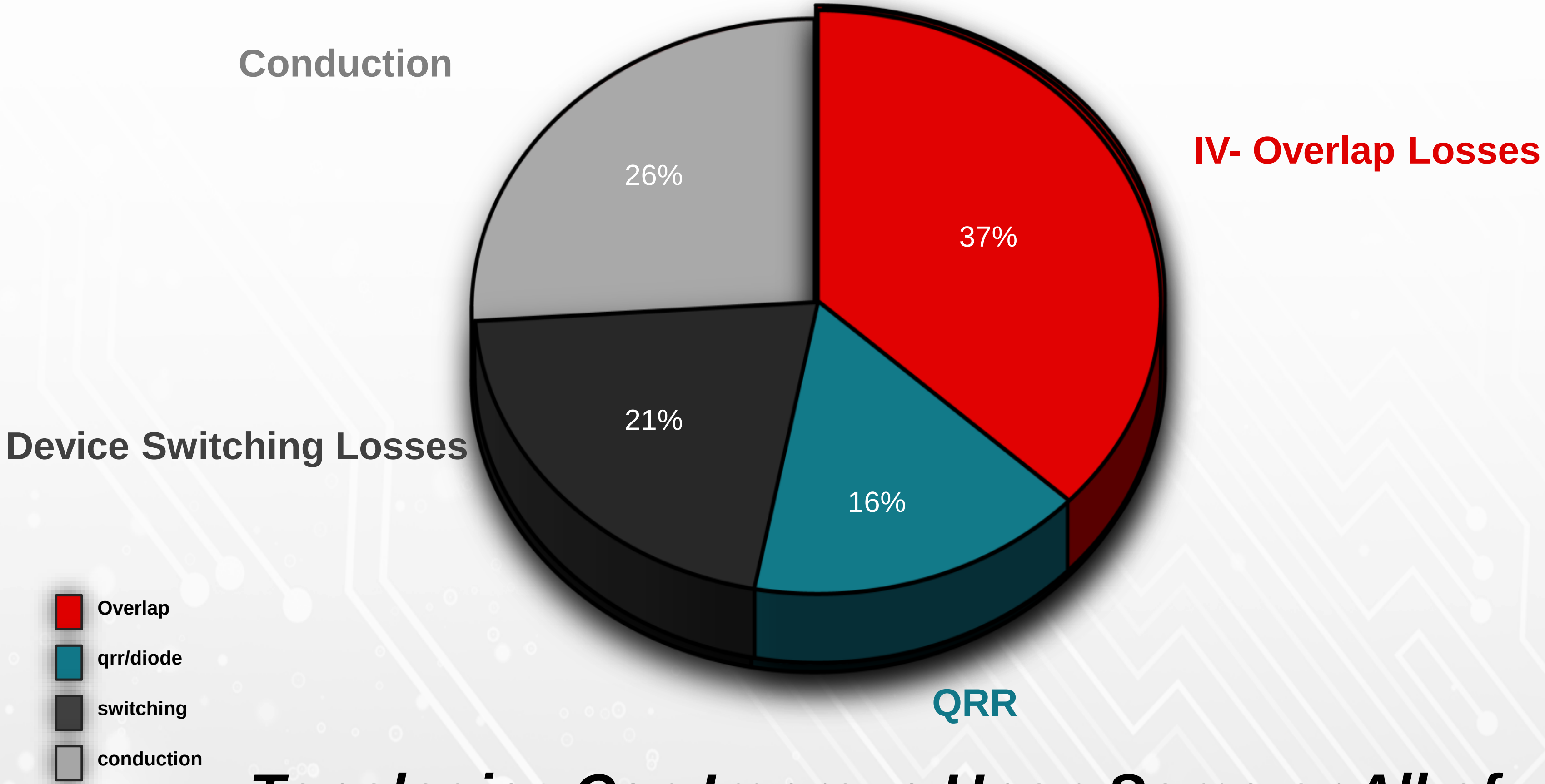


Devices
- Conduction Losses
- Charge Losses

Passives
- Magnetics
- Capacitors

Parasitics
- Device Ringing – IV Overlap
- Reverse Recovery

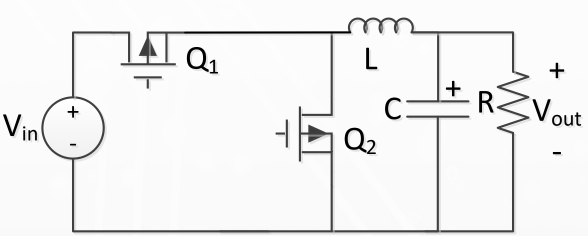
Typical Loss Breakdown – Buck Converter



Topologies Can Improve Upon Some or All of the Above

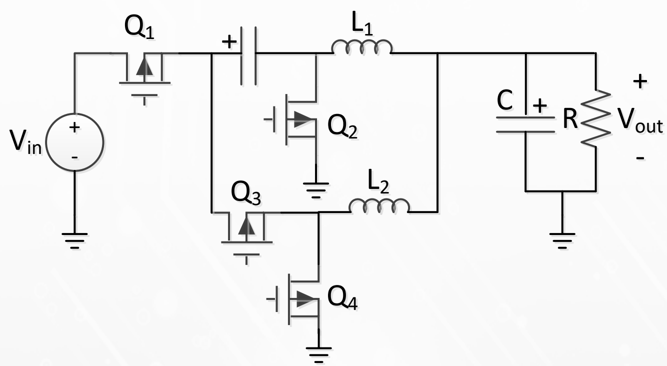
Topology Classes

Standard Converters



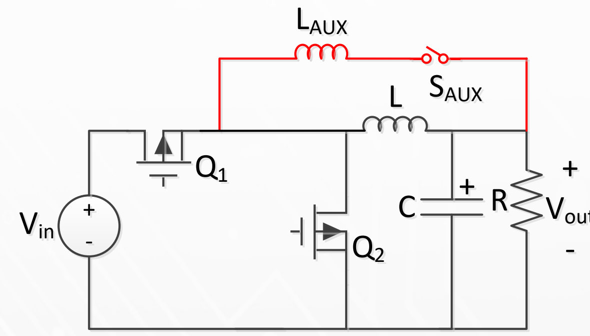
- ✓ Simple and proven
- ✓ Low Cost
- X Hard Switched
- X Full VIN rated devices

Hybrid Converters



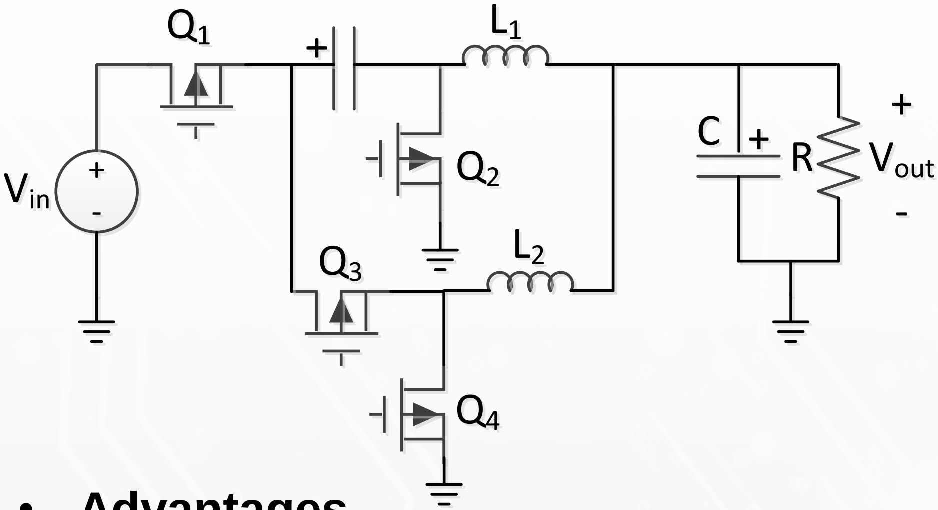
- ✓ Reduced Device Voltage Stresses
- ✓ Reduced Energy Storage In Inductors
- X Hard Switched
- X Additional Component(s)

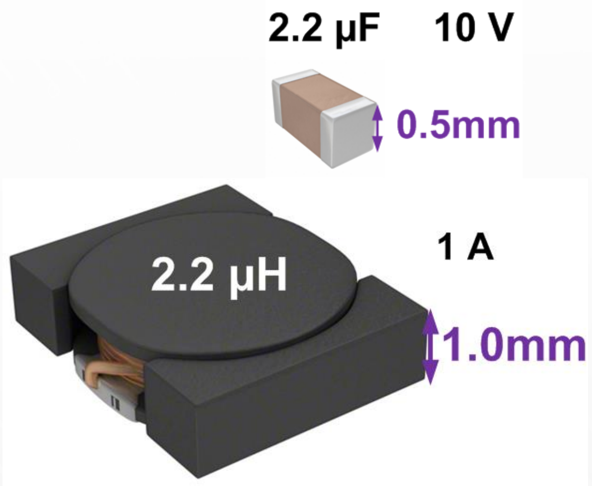
Resonant Converters



- ✓ Reduced or eliminated switching losses
- ✓ Majority of energy storage still in L
- X Additional Component(s)

Hybrid Converter Example



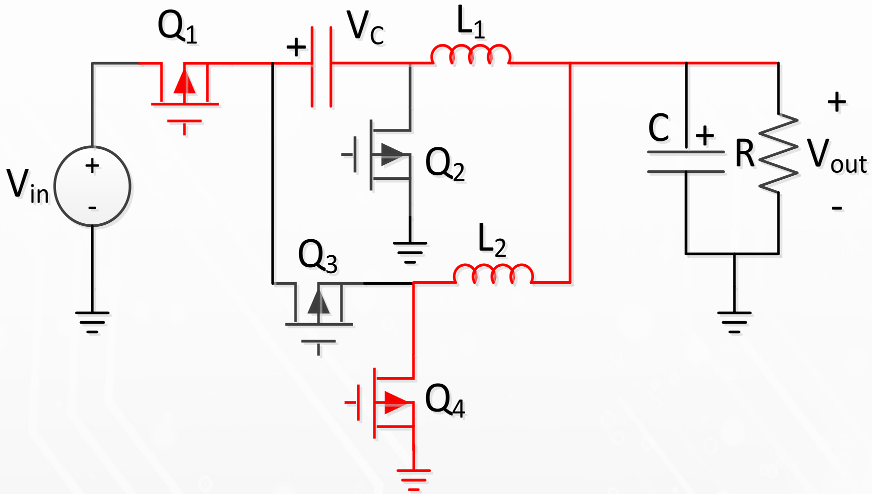


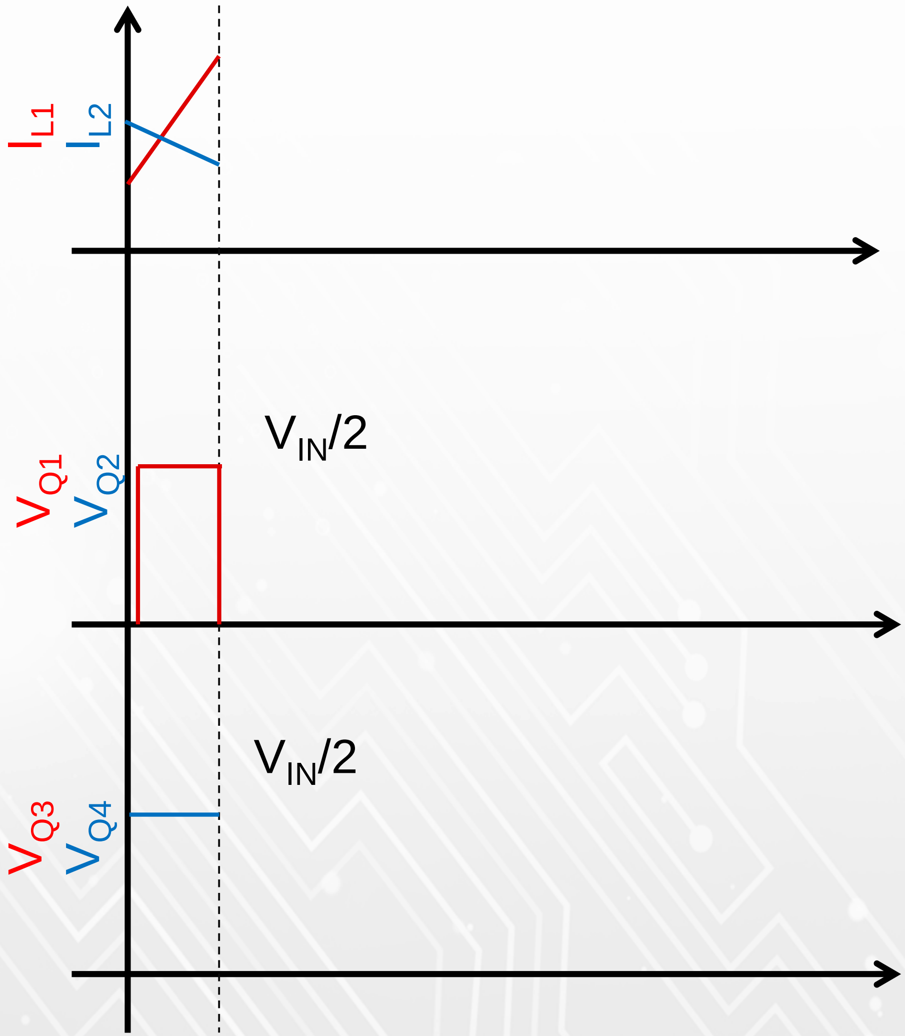
17x smaller footprint
34X smaller volume

- **Advantages**
  - More energy storage in caps, less in inductors
  - Lower switch ratings and stress
  - Smaller current ripple
- **Disadvantages**
  - Added component
  - Duty cycle limitation

[Nishijima, 2005]
[Shenoy], 2015

Hybrid Converter Example

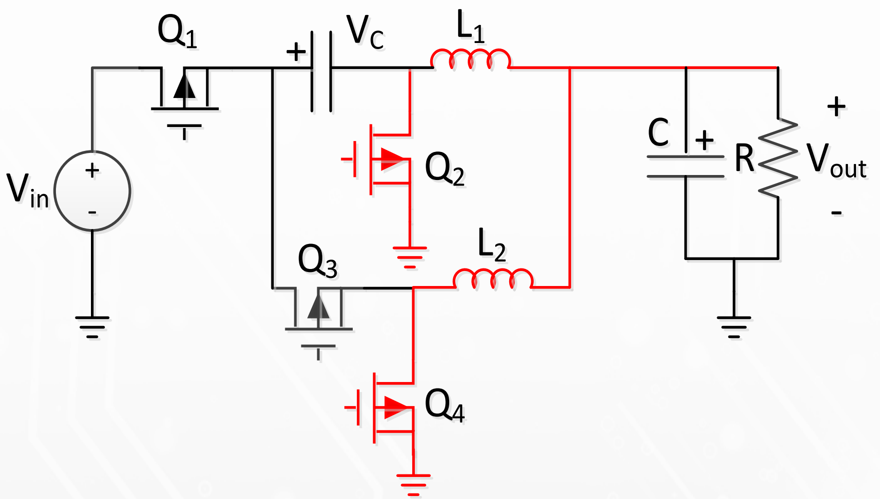


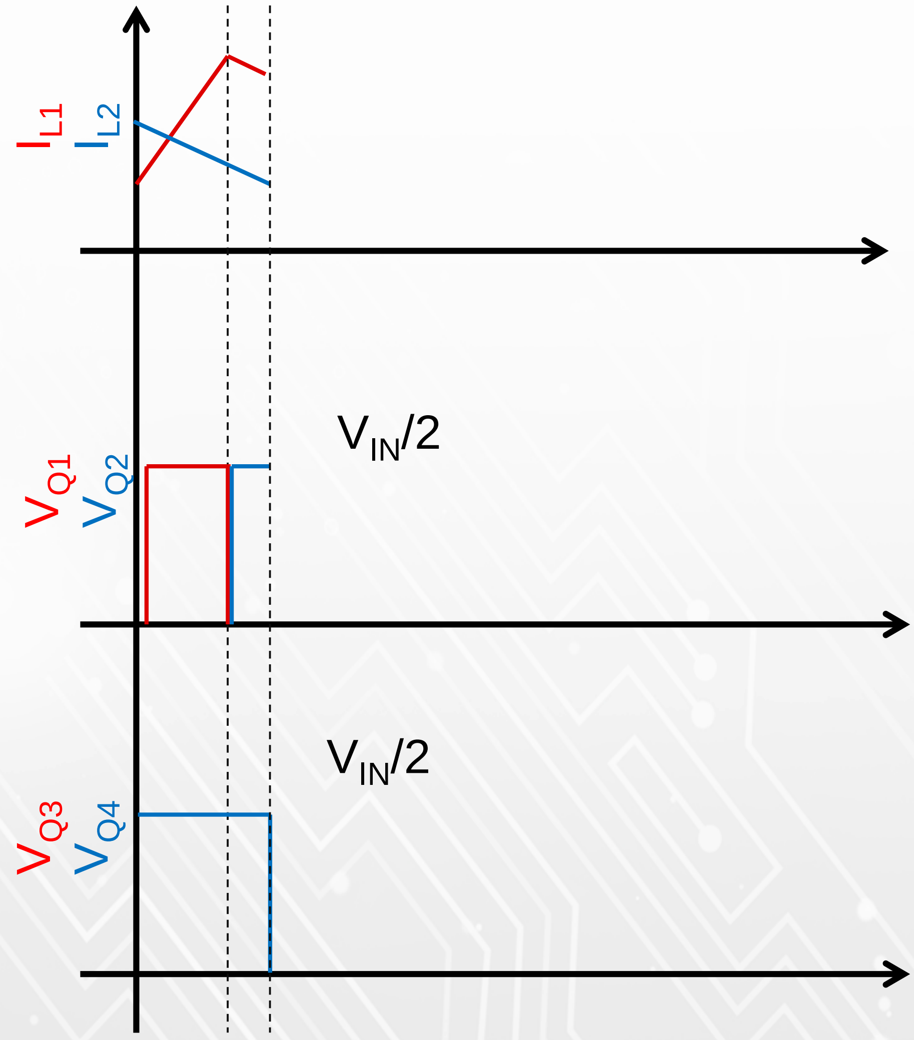


- V_{IN} – VC Applied to L_1
- V_C charged through phase 1 path
- L_2 current decreases

[Nishijima, 2005]
[Shenoy], 2015

Hybrid Converter Example

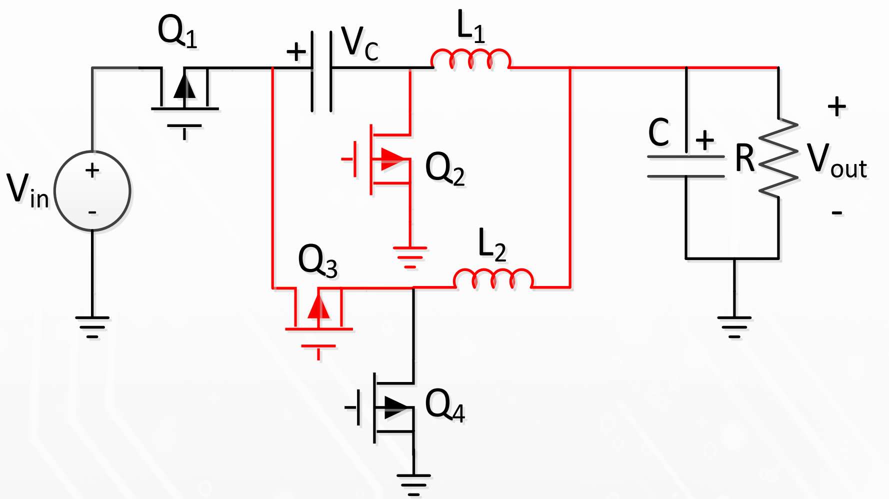


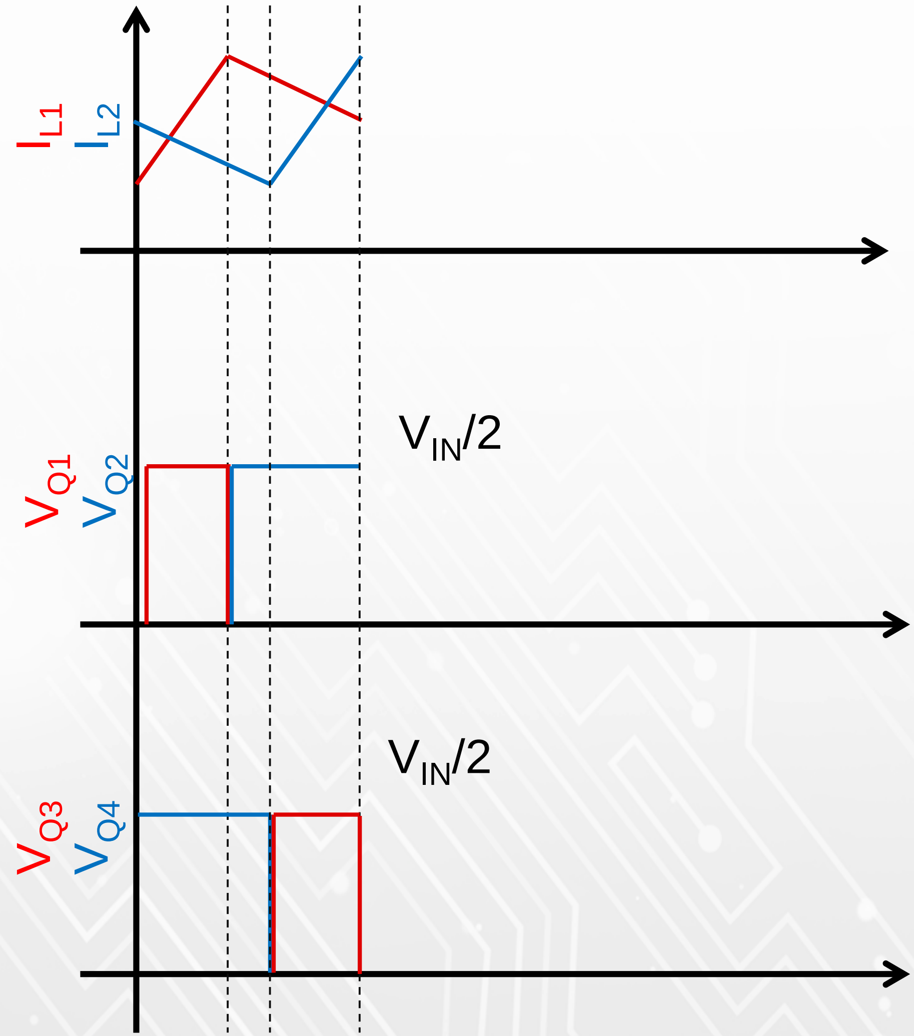


- Current in both inductors decreases
- No current flowing through V_c

[Nishijima, 2005]
[Shenoy], 2015

Hybrid Converter Example

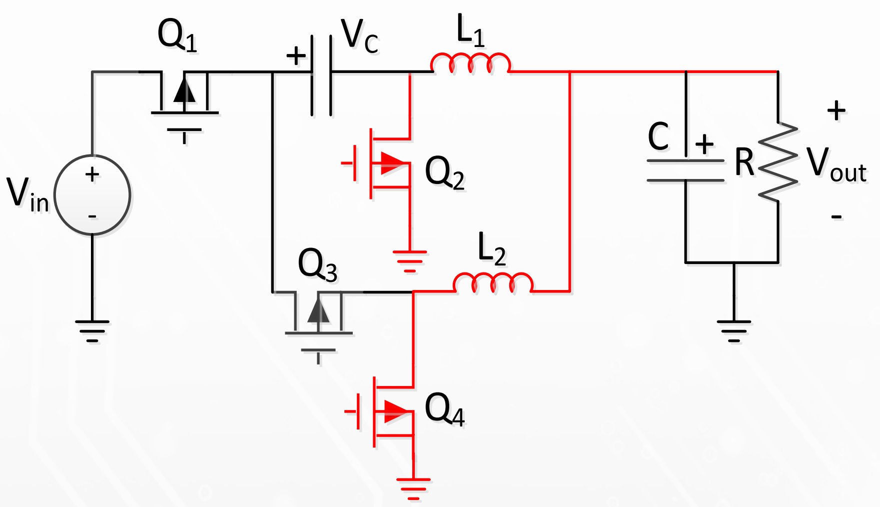


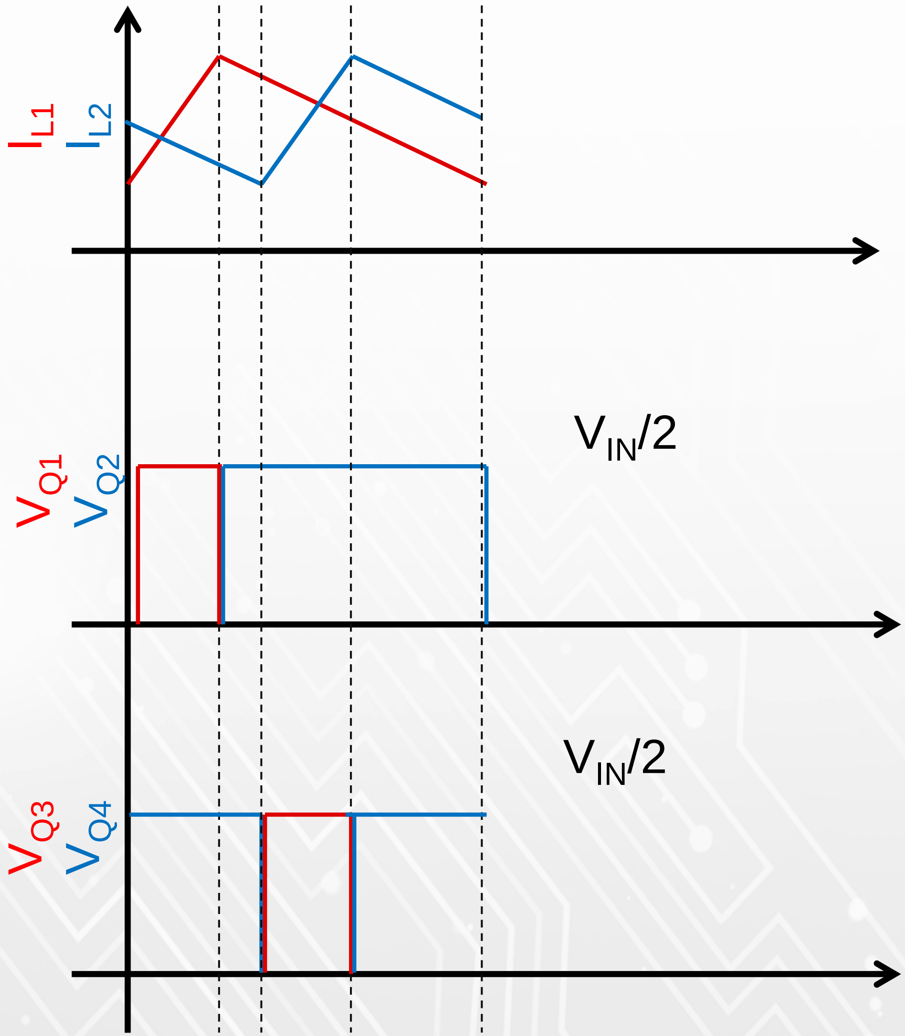


- L_1 current decreases
- V_C Applied to $L_2 \rightarrow$ Becomes Phase 2 source
- L_2 current increases

[Nishijima, 2005]
[Shenoy], 2015

Hybrid Converter Example





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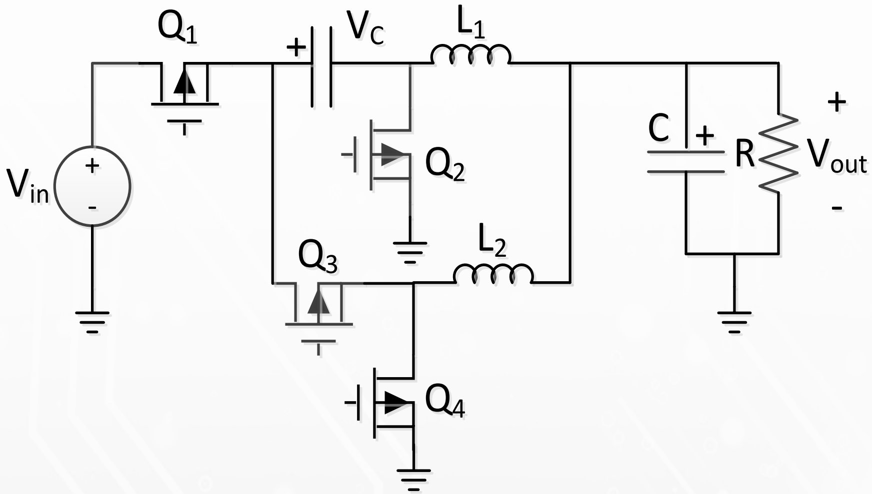
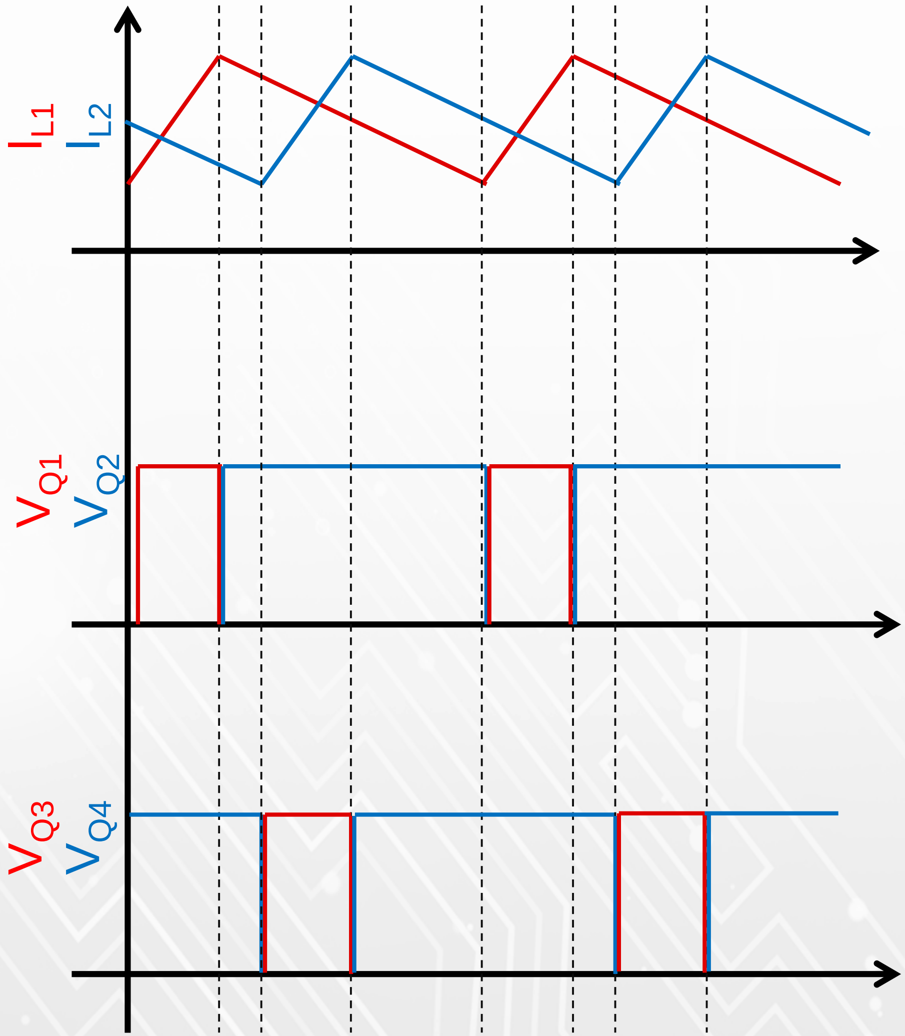
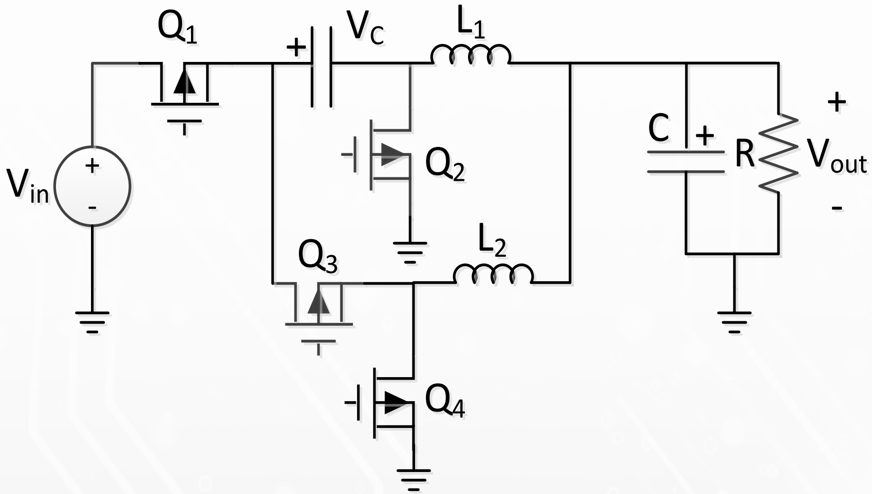
Hybrid Converter Example





- ✓ Capacitor Voltage and Inductor currents naturally balanced
- ✓ More energy storage in the capacitor, less in inductors
- ✓ Device rated for $V_{IN}/2$
- X Hard Switched
- X Additional Component(s)
- X Duty Cycle Limitation

Advantages – Capacitors vs. Inductors



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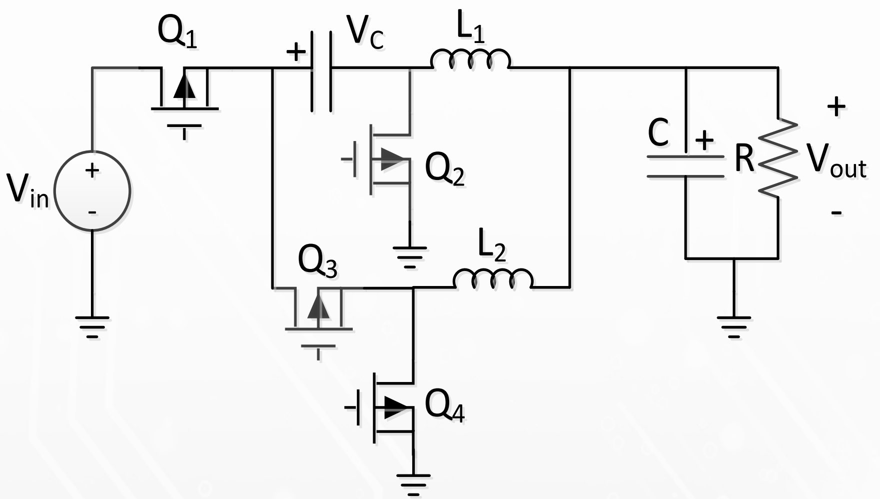
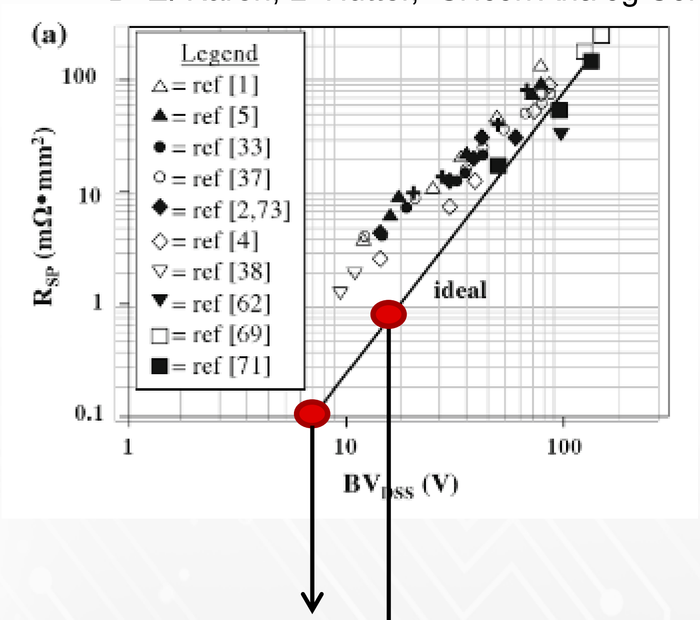
Rsp Advantages



*B. El-Kareh, L. Hutter, "Silicon Analog Components"



~8V Rated
~0.1mΩ-mm²

~16V Rated
~0.6mΩ-mm²

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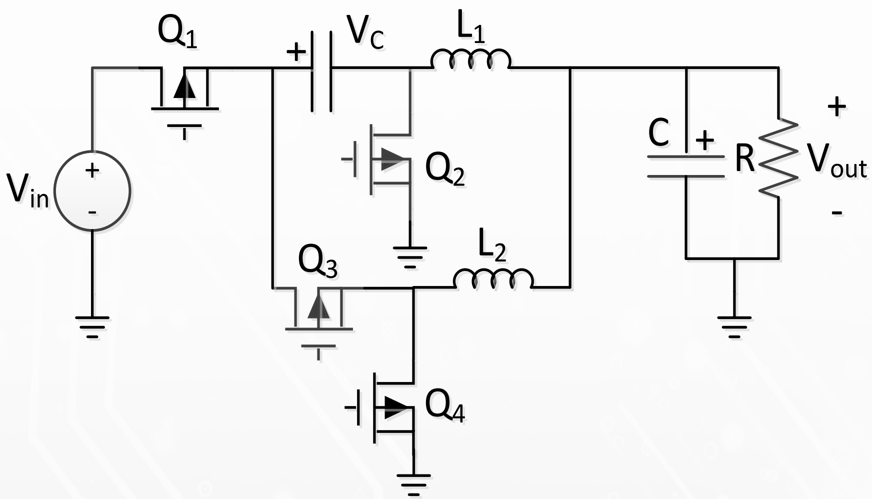
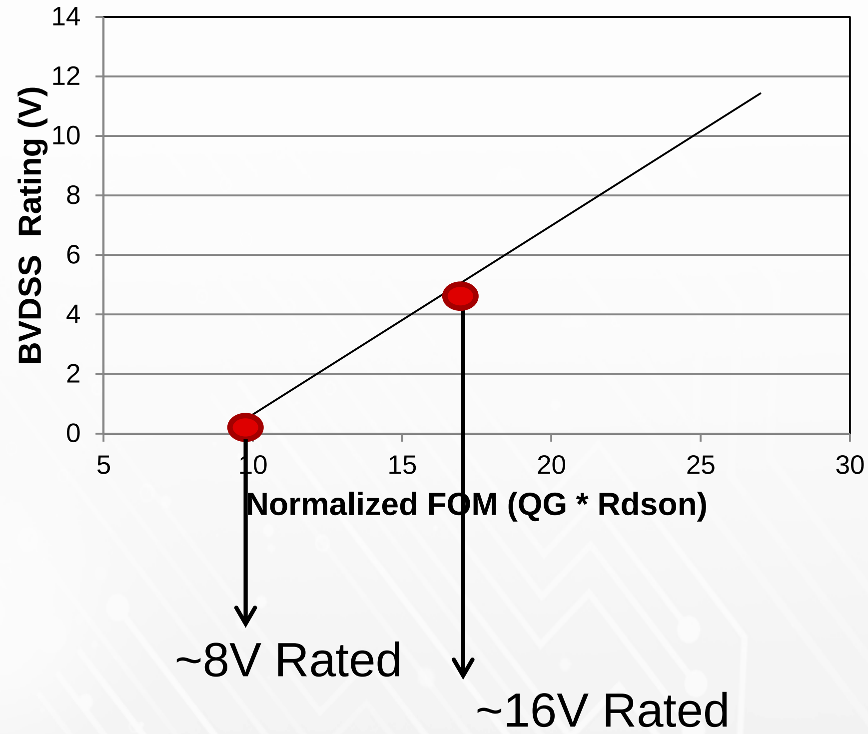
- Enables Smaller Die Area -- $$ Savings

FOM Advantages





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- ✓ **Device rated for $V_{IN}/2$**
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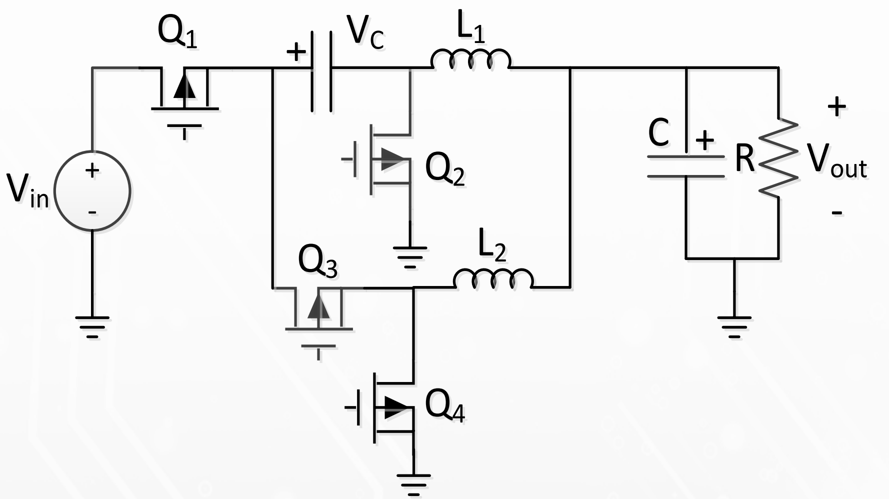
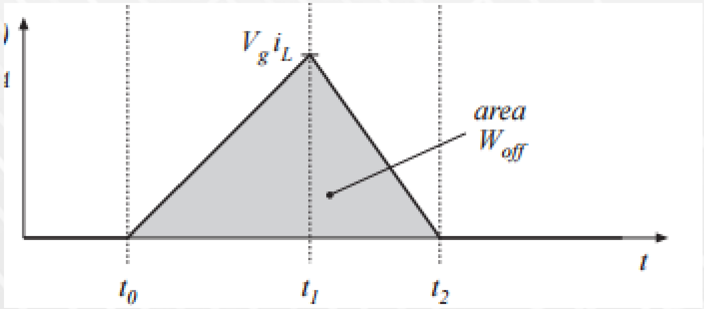
- ~3x-5x better FOM in this example

CV^2 and I-V Overlap Losses



- ***Hard Switching Losses Reduced***
  - $1/2CV^2$
    - ***V/2 and C decreases w/FOM improvements***
  - IV Overlap – $\frac{1}{2}\frac{V_{IN}}{2}I_L t_r$
    - Assume same DV/DT and DI/DT as a Buck
    - t_R halves, 2x more transitions,
    - ***1/4 the transition losses***



✓ Capacitor Voltage and Inductor currents naturally balanced

✓ More energy storage in the capacitor, less in inductors

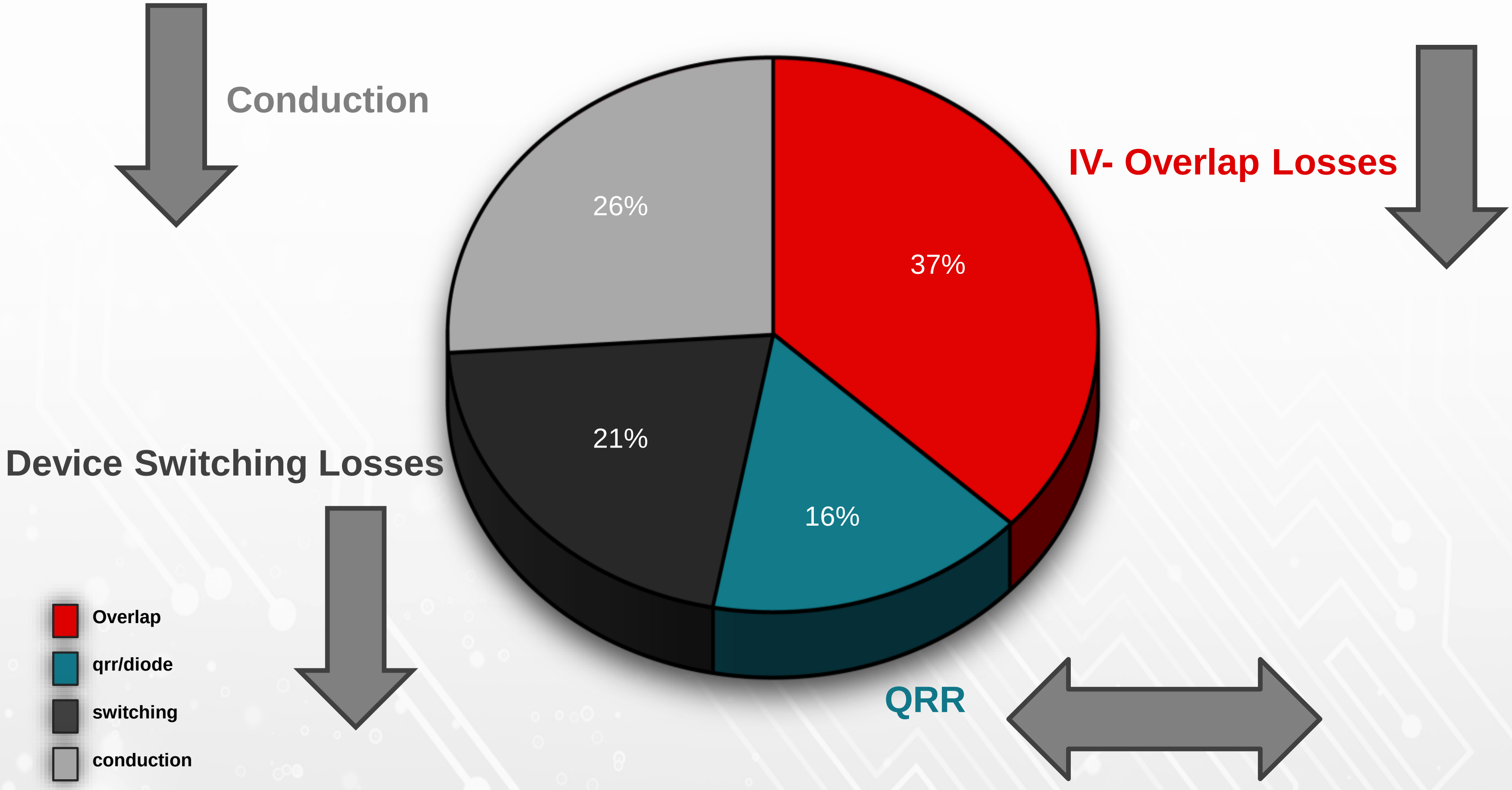
✓ **Device rated for $V_{IN}/2$**

X Hard Switched

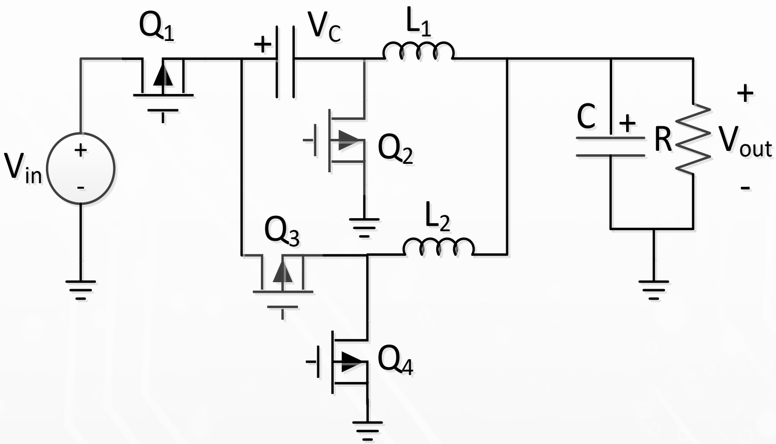
X Additional Component(s)

X Duty Cycle Limitation

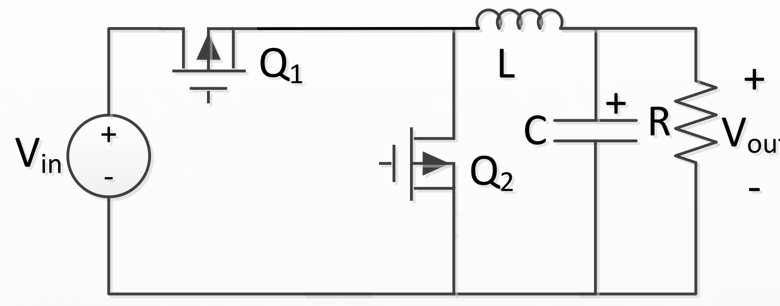
Buck Converter vs. SC Buck

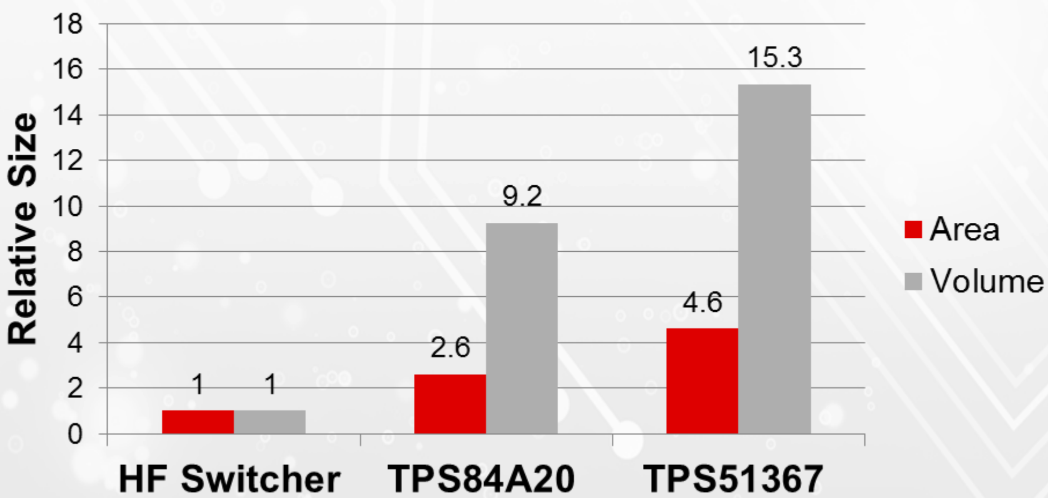


Adding It All Up



Vs.

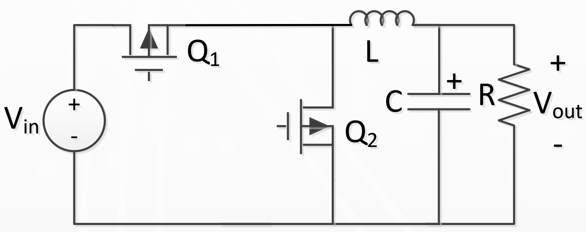




- Dramatic Size Reduction
- Efficiency the same or better than comparison points
- Major downside of duty cycle limitations

Topology Classes

Standard Converters



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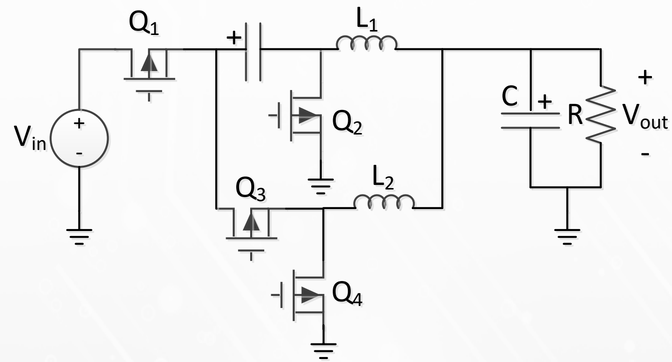
Hybrid Converters



- ✓ Reduced Device Voltage Stresses
- ✓ Reduced Energy Storage In Inductors
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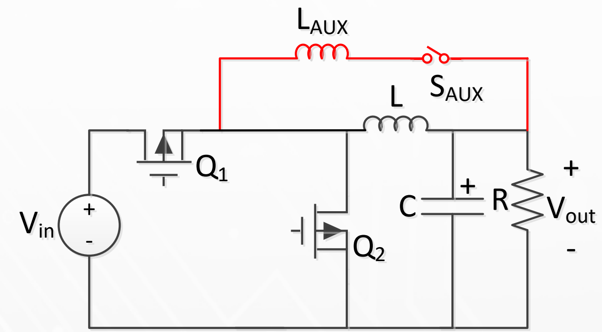
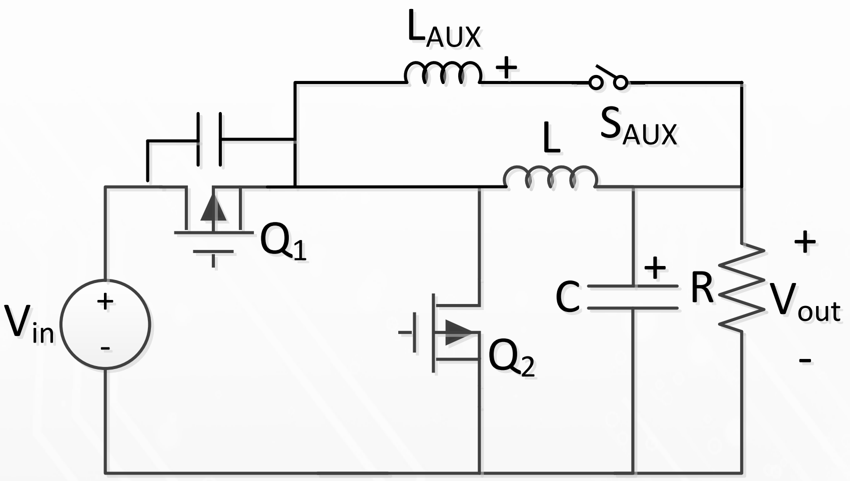
Resonant Converters



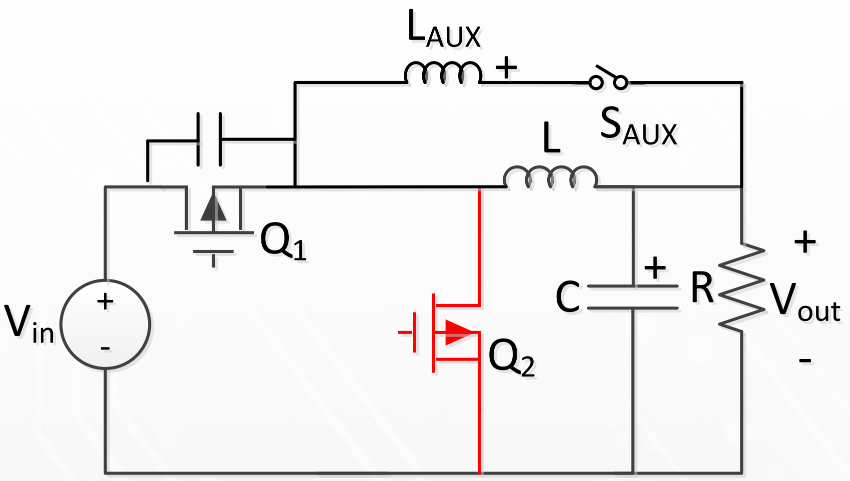
- ✓ Reduced or eliminated switching losses
- ✓ Majority of energy storage still in L
- X Additional Component(s)

Resonant Converter Example

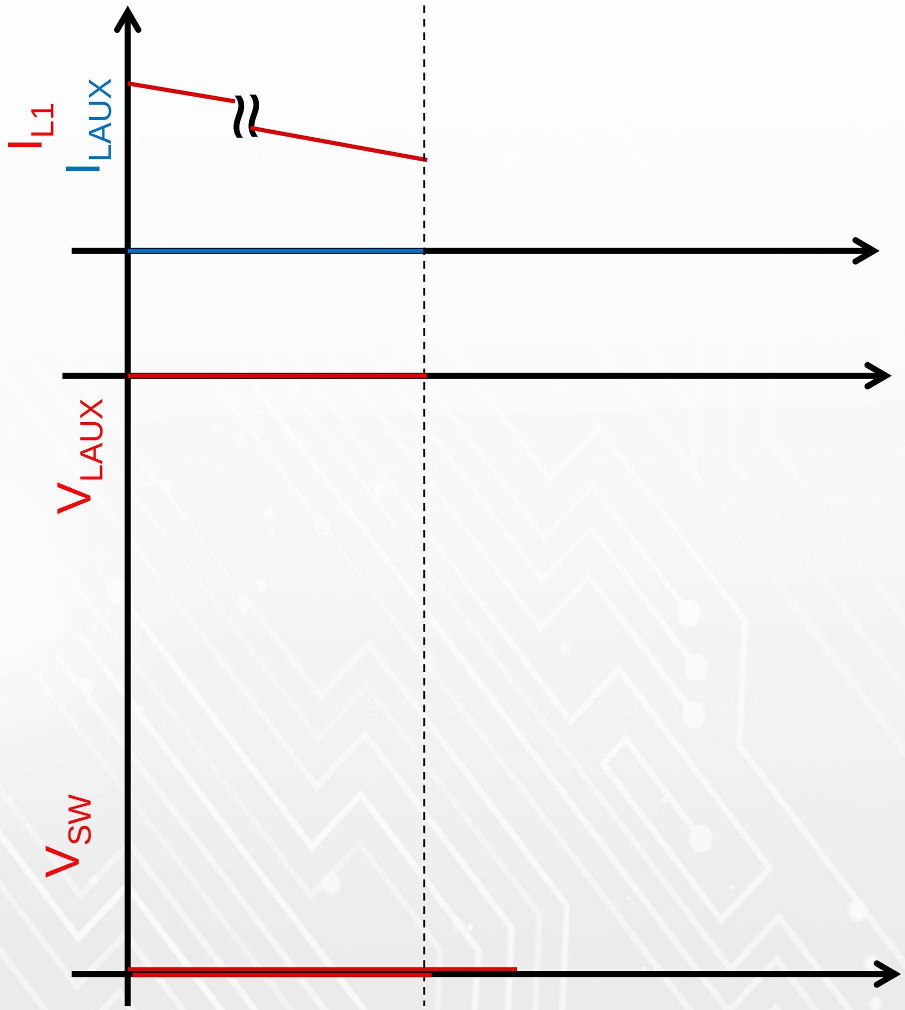


C. Nan, R. Ayyanar, “A 1 MHz Bi-directional Soft-switching DC-DC Converter with Planar Coupled Inductor for Dual Voltage Automotive Systems”

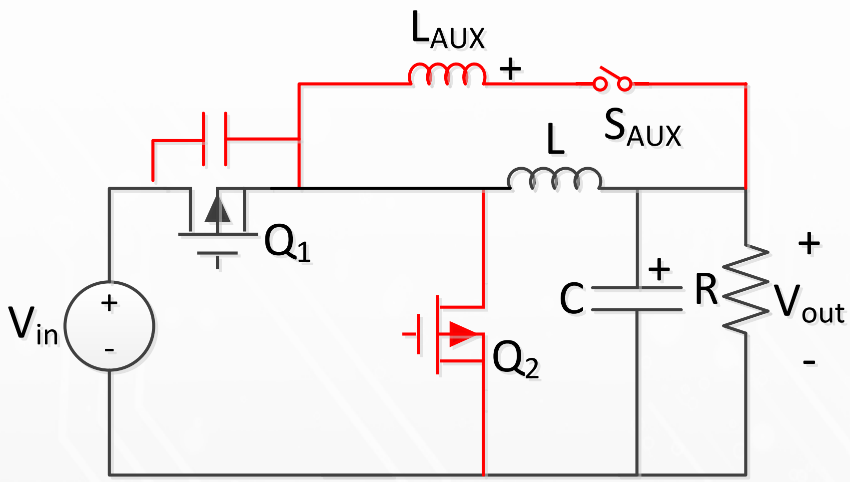
Resonant Converter Example

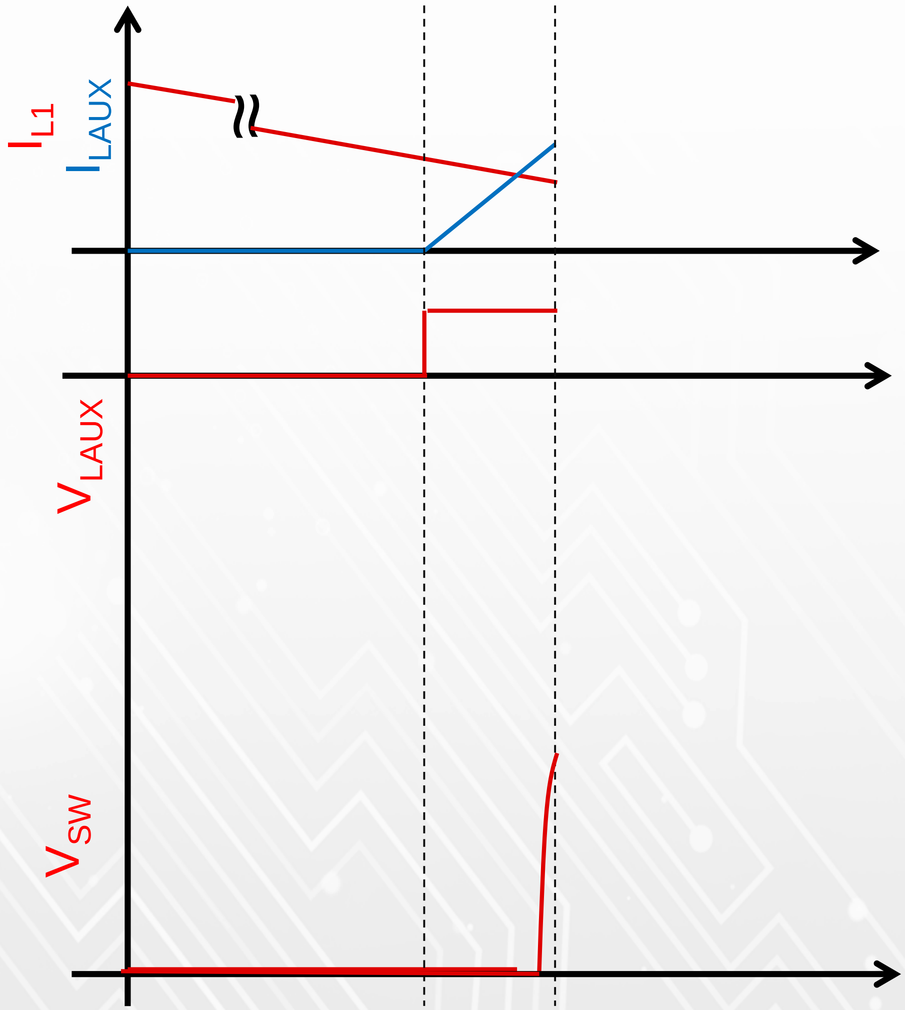


- Typical Buck Operation
- Inductor current slews down



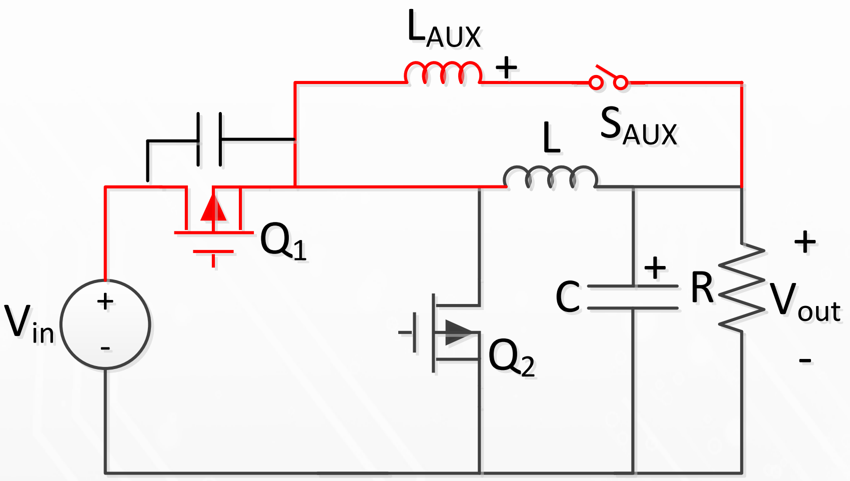
Resonant Converter Example



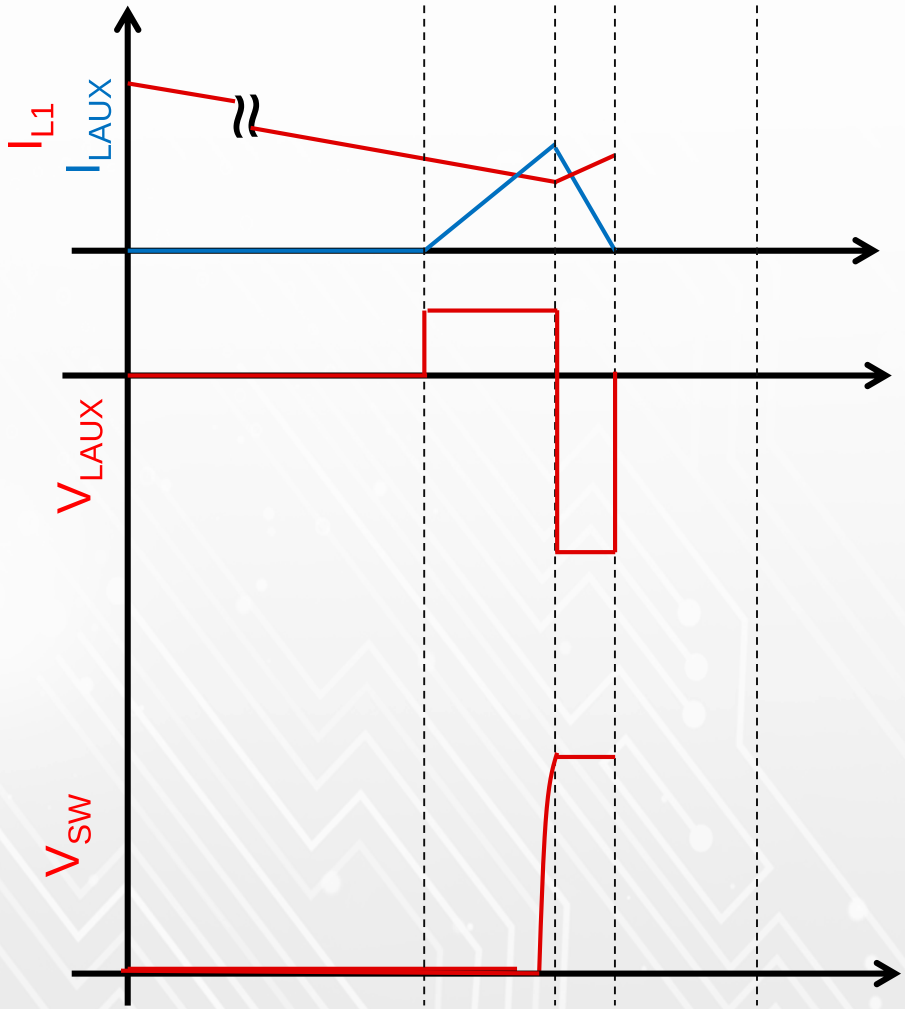


- Q2 remains ON holding switched node at ground
- SAUX turns ON ramping up current in LAUX
- Once AUX current is greater than L current, Q1 Coss conducts

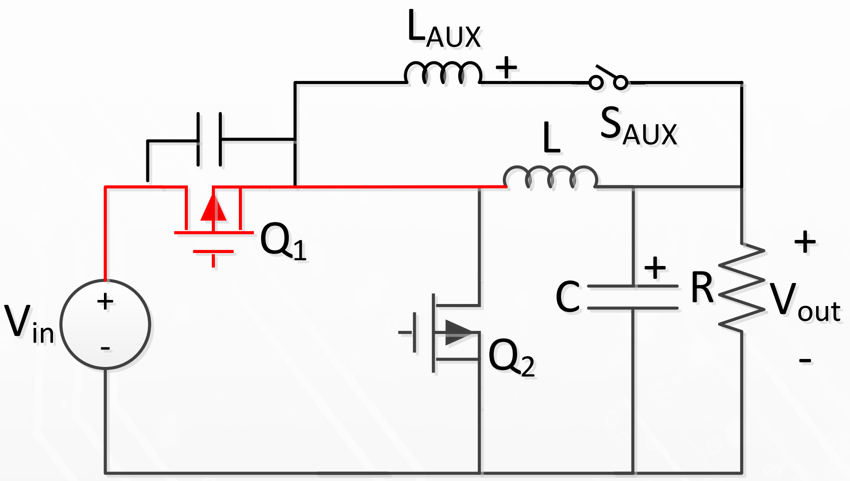
Resonant Converter Example

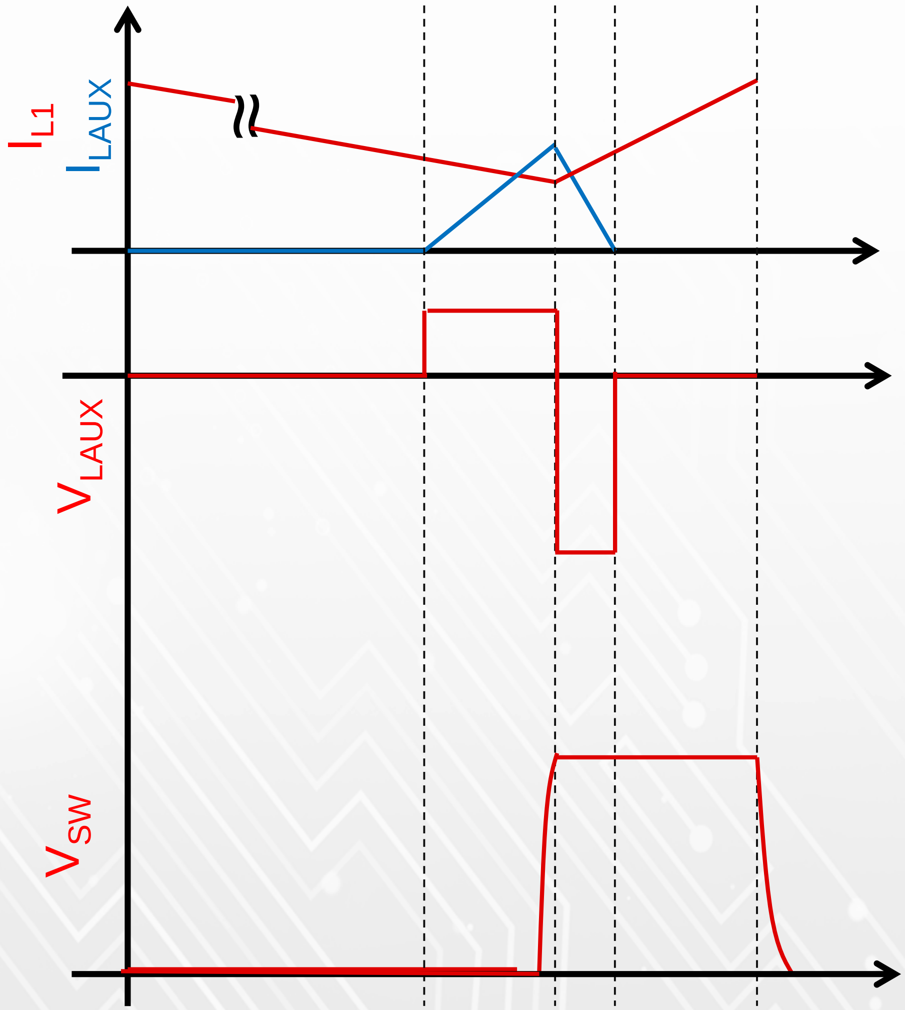


- Turn ON Q1 with ZVS
- LAUX current ramps down to zero after which SAUX is turned off



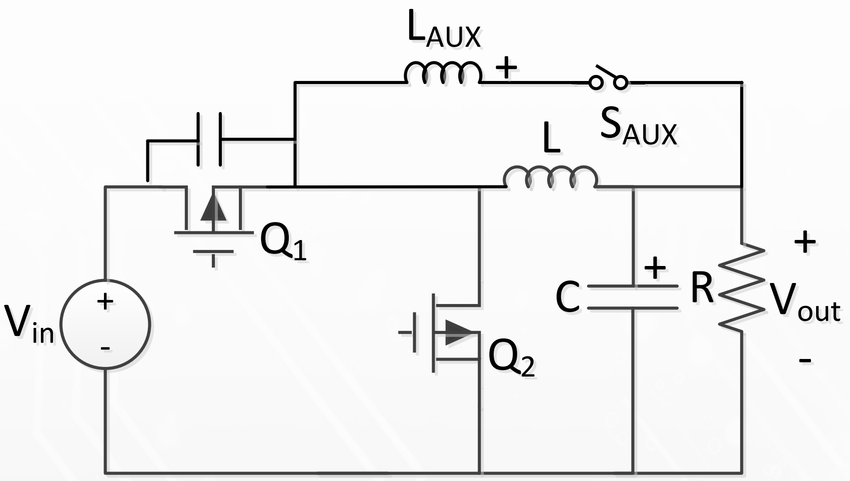
Resonant Converter Example

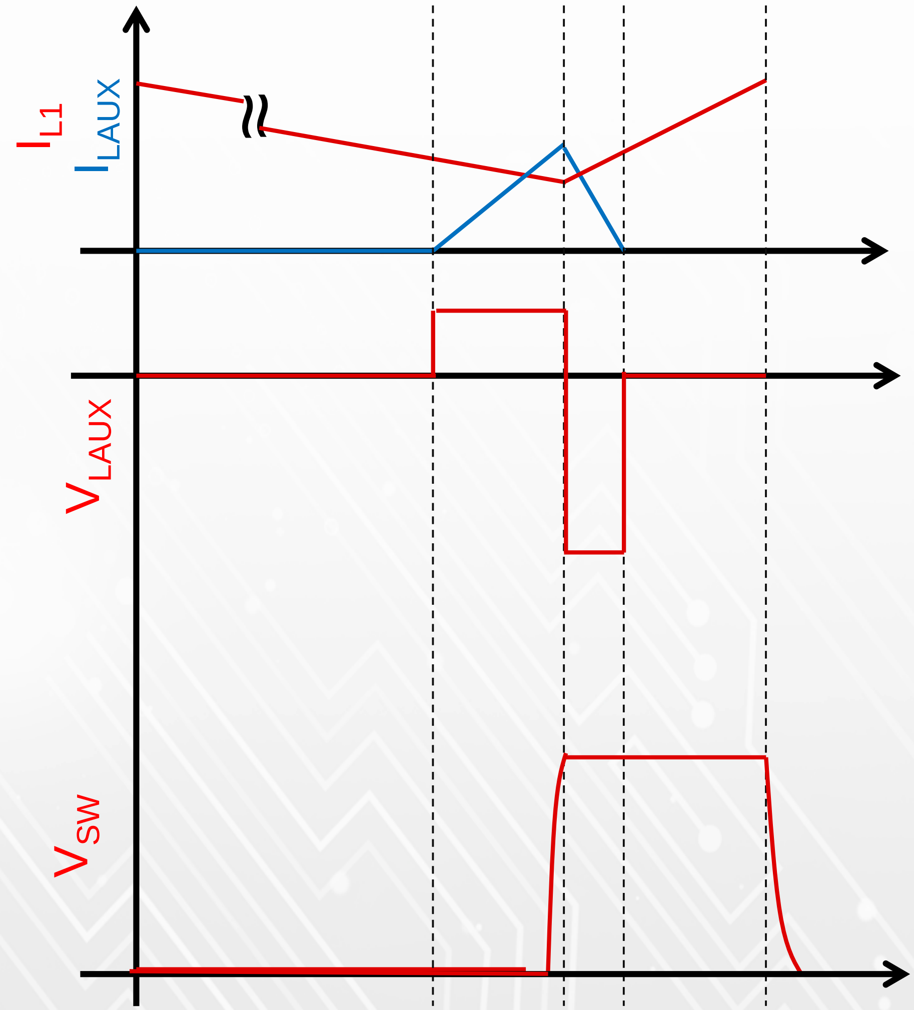




- Q1 conducts remainder of interval as in typical buck converter

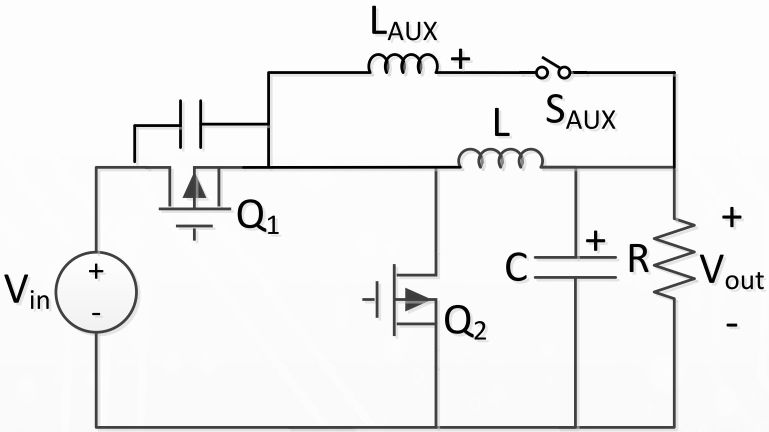
Resonant Converter Example





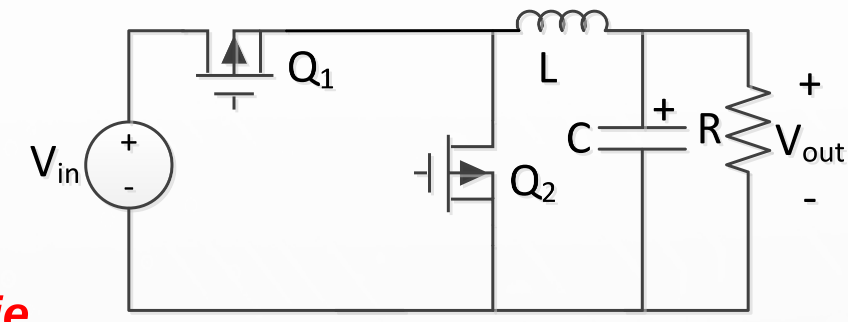
- ✓ ZVS turn on of Q_1
- ✓ ZCS turn off of S_{AUX}
- ✓ No I-V turn on losses for Q_1
- X Added conduction losses for S_{AUX}
- X Added die area for S_{AUX}
- X Extra component losses

Analysis and Comparison



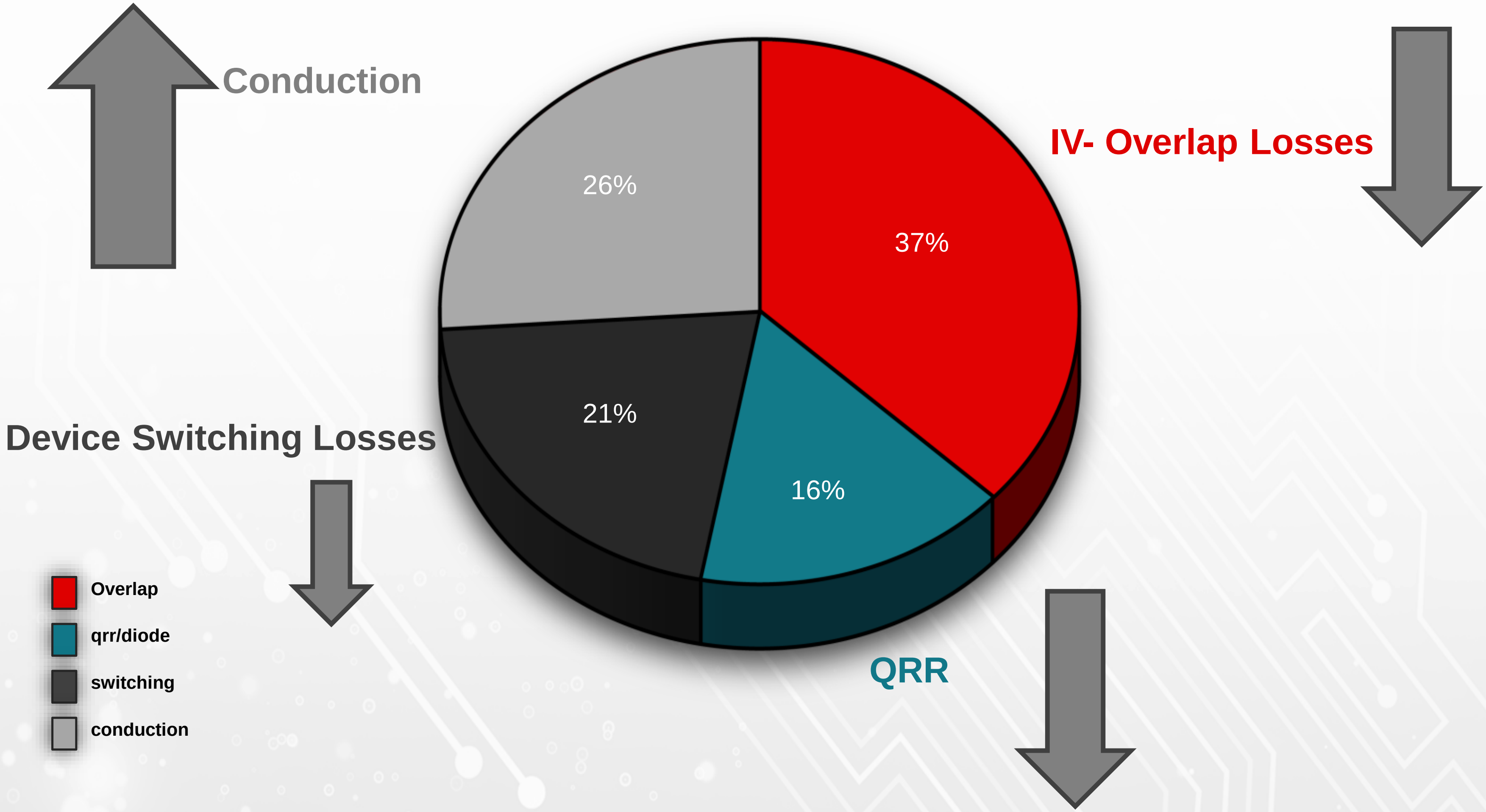
Vs.

20% Smaller Die

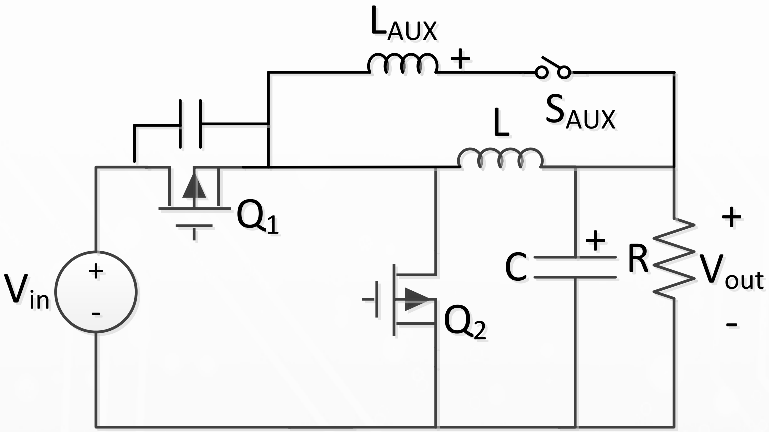


Loss Breakdown	Buck (1MHz)	ZVT (1MHz)
Cond. Loss $L + L_{AUX}$	1.0x	~2.3x
Q_{OSS}	1.0x	0.5x
Q_{rr}	1.0x	0x
IV-Overlap (ON)	1.0x	0x
IV-Overlap (OFF)	1.0x	1.0x
D_{RR} Cond.	1.0x	0.2x
P_{GATE}	1.0x	1.2x
P_{TOT}	1.0x	0.96x

Buck Converter Vs. ZVT



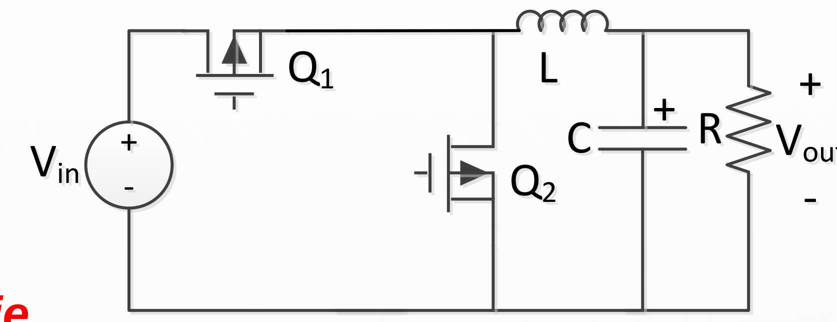
Opportunities



Vs.

20%

Smaller Die



- If cost is a non-factor (usually isn't), large efficiency gains possible
- Other main challenge → The Magnetic element
  - Conduction Losses
  - Core losses
  - Cost
  - Size

Summary

New Topologies offer opportunity to move towards full power supply on a chip

Options and alternatives with various pros and cons

Still need improvements on:

- Inductor integration
- Capacitor integration
- Better FETs
- Better packages

Questions