PwrSoC enabling architectures in different applications

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http://www.dtu.dk/centre/ele/English.aspx

Applications for PwrSoC
Enablers: semiconductors
Disablers: passive components
What’s new on the architecture side?

AGENDA

Applications for PwrSoC

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What's new on the architecture side?

AGENDA

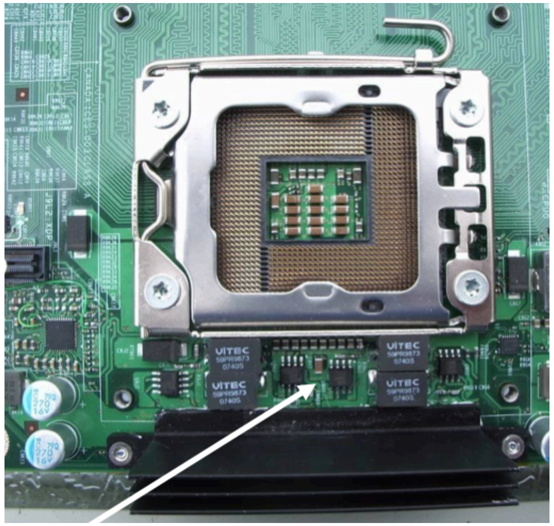
Popular applications

- Chargers

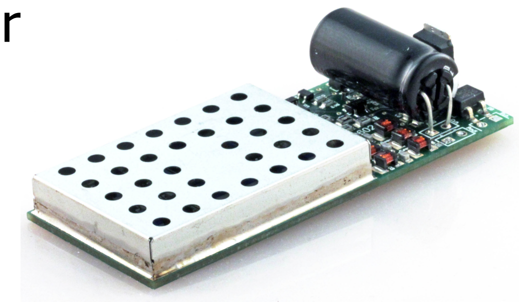
(http://www.folomojo.com/ces-2015-beyond-smartphones-mind-blowing-new-devices-revealed/)

- Point of load

(Integrated Power Delivery for High Performance Server Based Microprocessors, J. Ted DiBene II, PowerSoC08)



- LED driver



LED drivers

3 colors à 8 bit (=256) => 24 bit total

Quantity

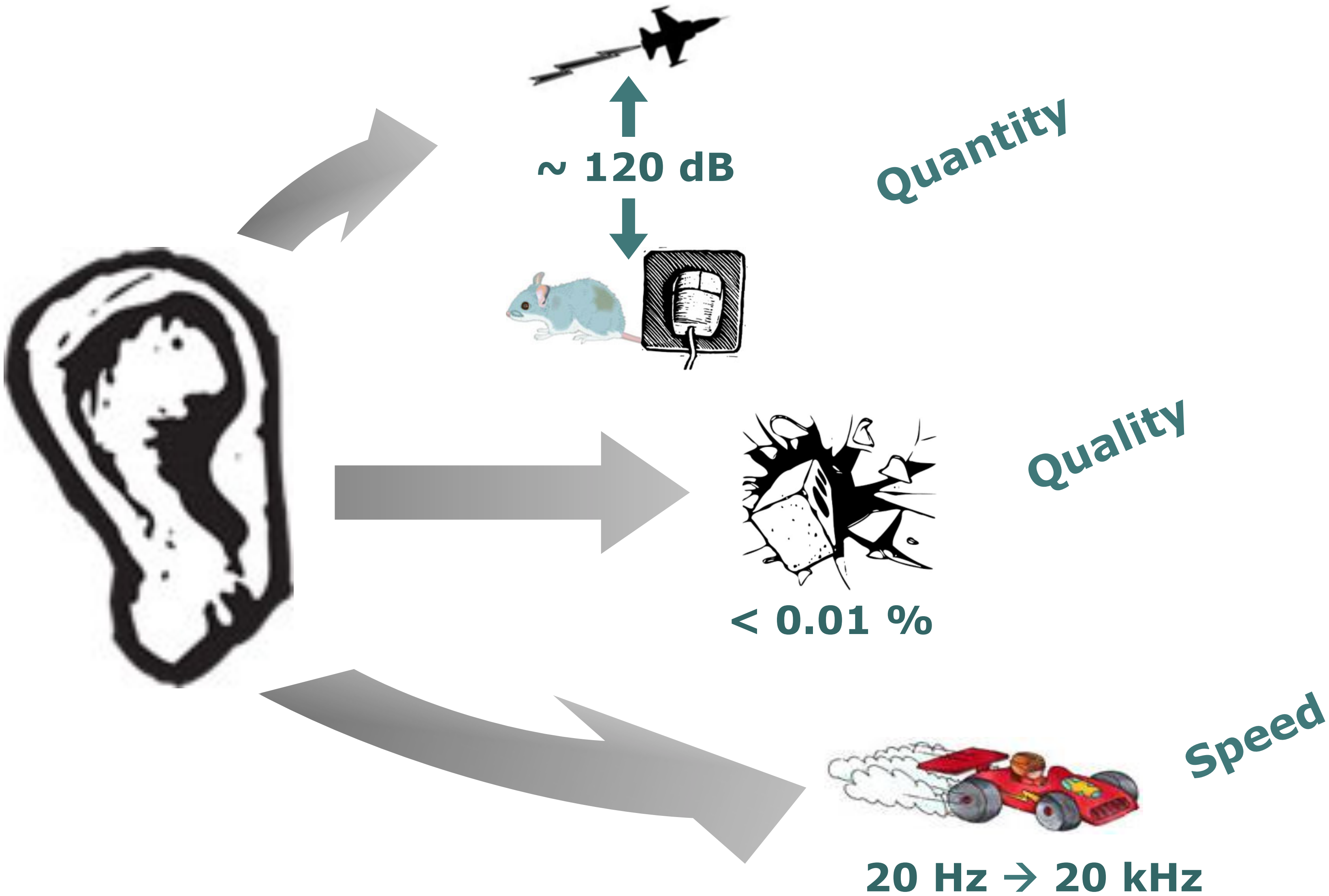
compression of jpg’s & mpg’s

Quality

100 Hz TV: eye can’t follow!

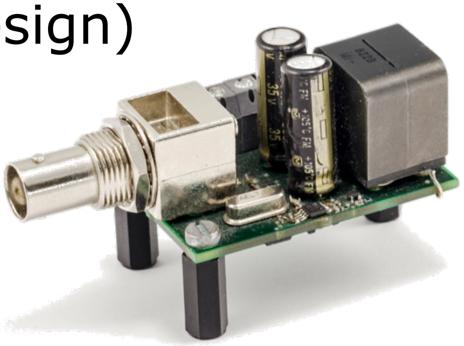
Speed

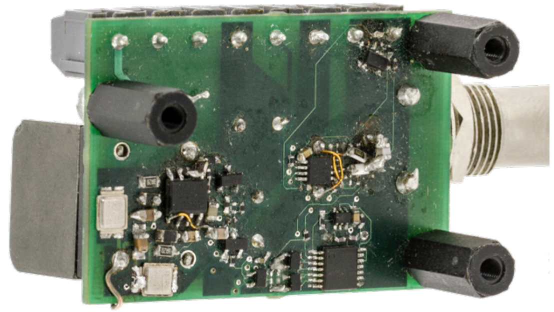
So, what's different in audio applications?



Todays audio power amplifiers

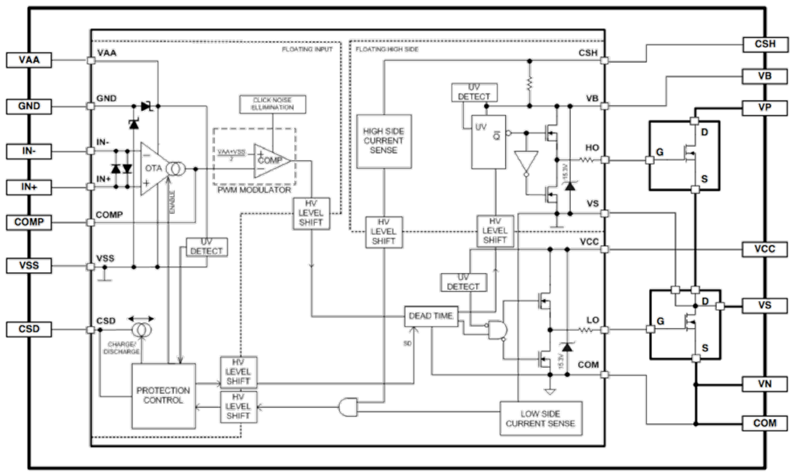
- 100 W (discrete design)

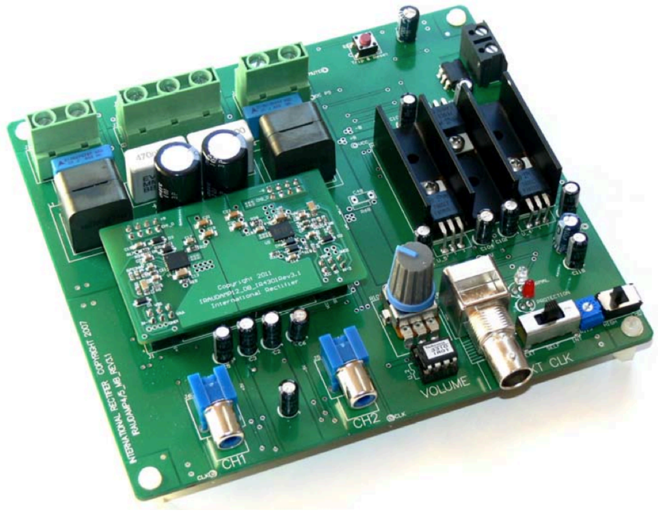




- 90 W / 135 W (IR4321M in IRAUDAMP21)

5 x 6 mm^2
PQFN22

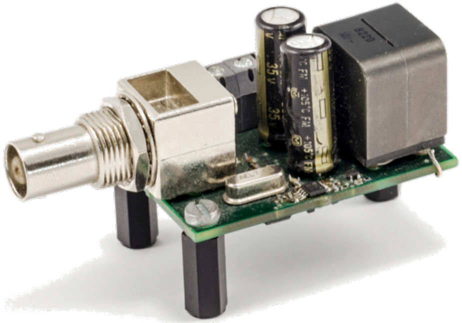




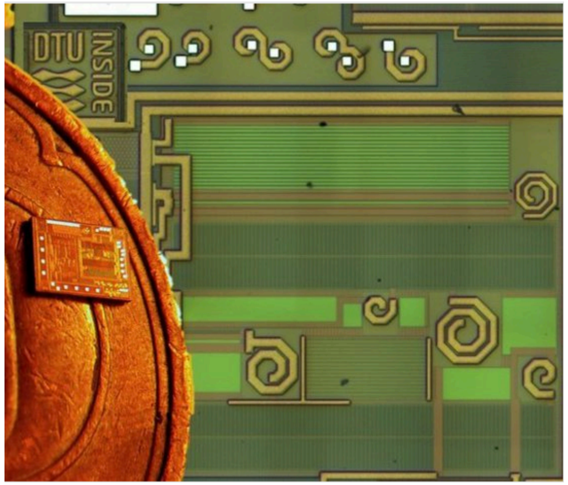
- Similar examples from TI, NXP, ST and others

My research goal

- Fully integrated audio power amplifier with high efficiency…



… and any other power application in DC/AC, AC/DC, DC/DC



Applications for PwrSoC

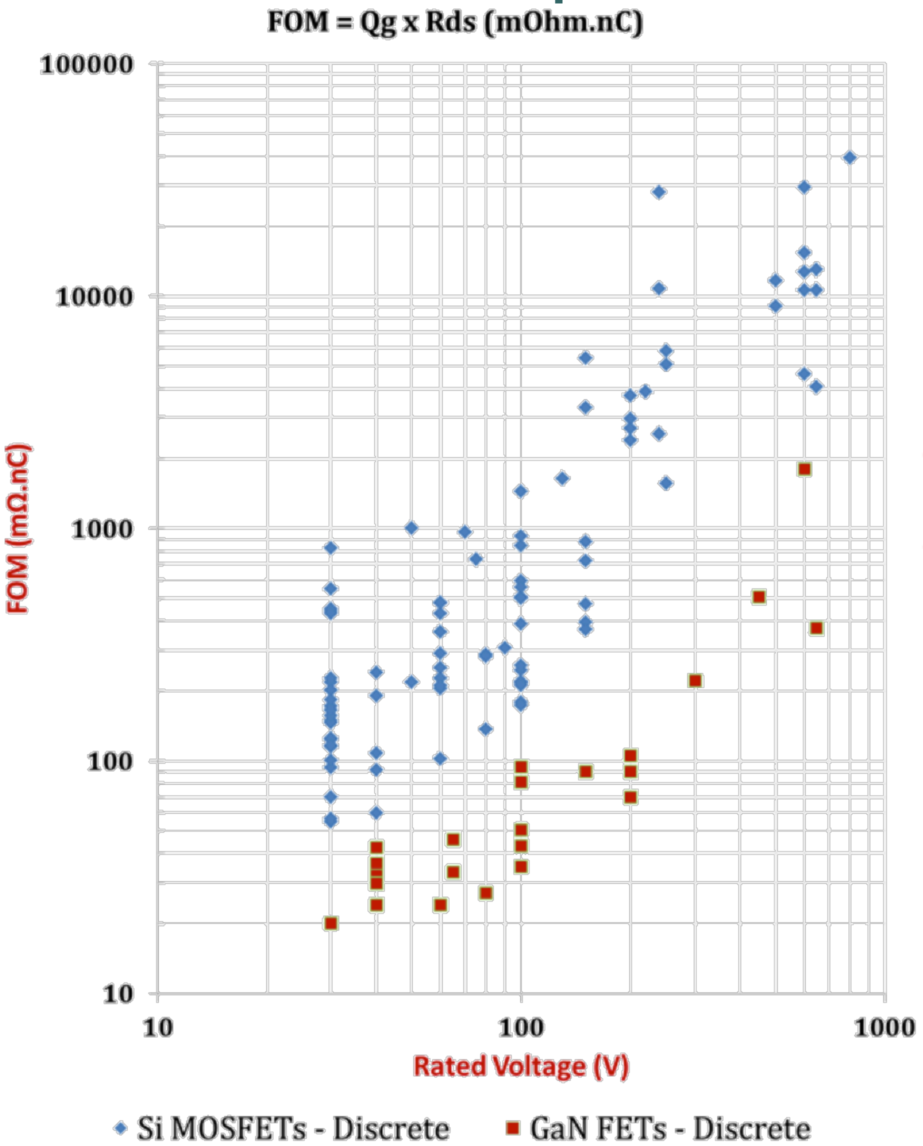
Enablers: semiconductors

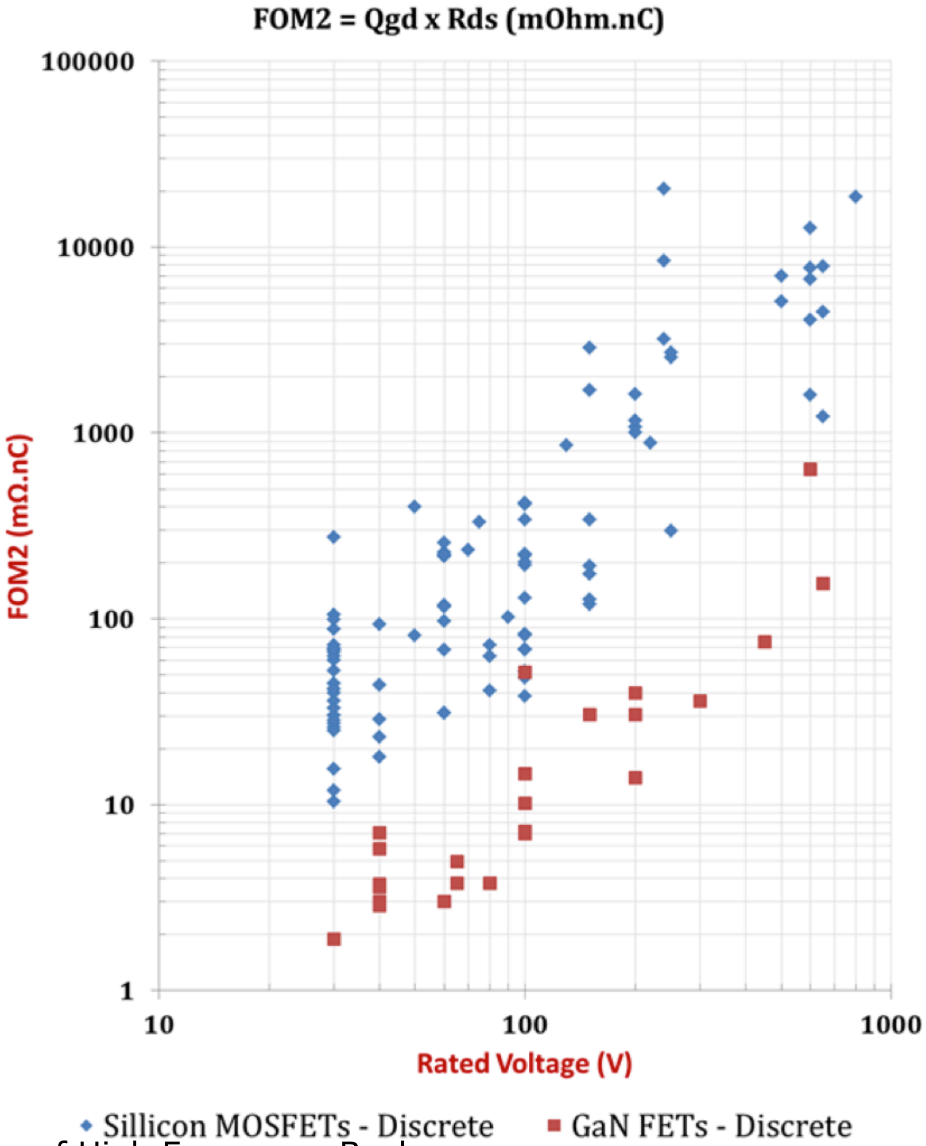
Disablers: passive components

What's new on the architecture side

AGENDA

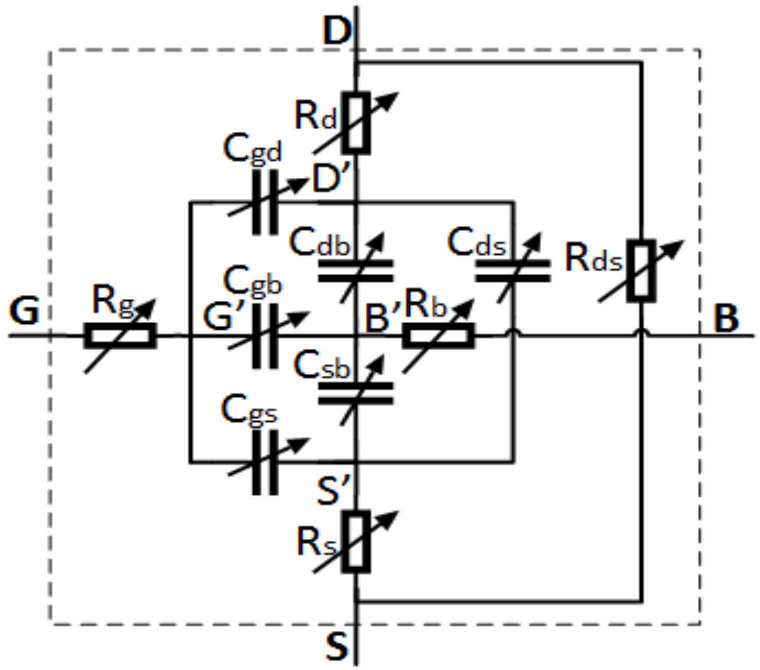
FOMs on input of GaN & Si

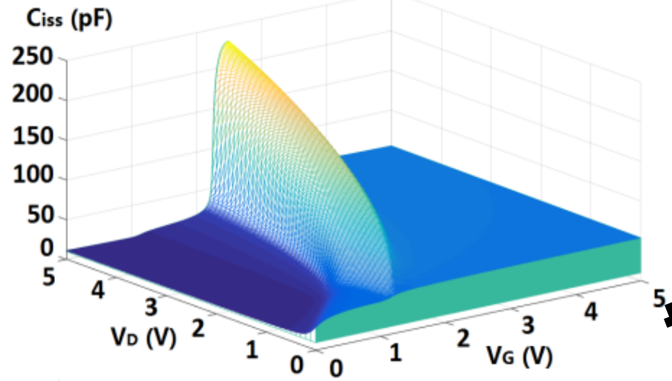


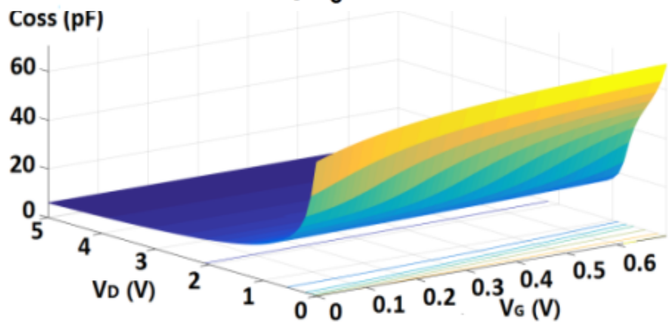


Design and Implementation of High Frequency Buck Converter Using Multi-Layer PCB Inductor, Y. Nour et. al, IECON 2016

Nonlinear capacitance modeling

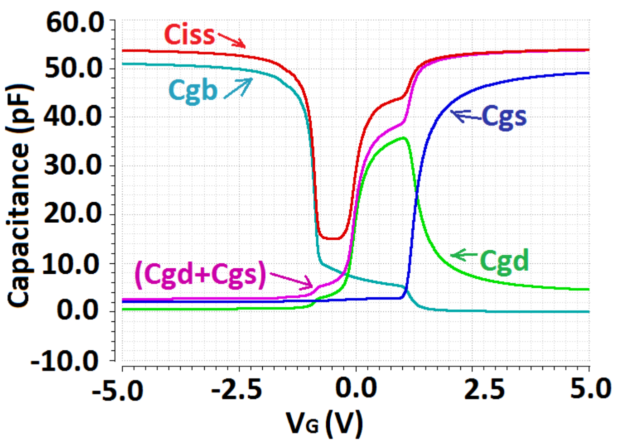


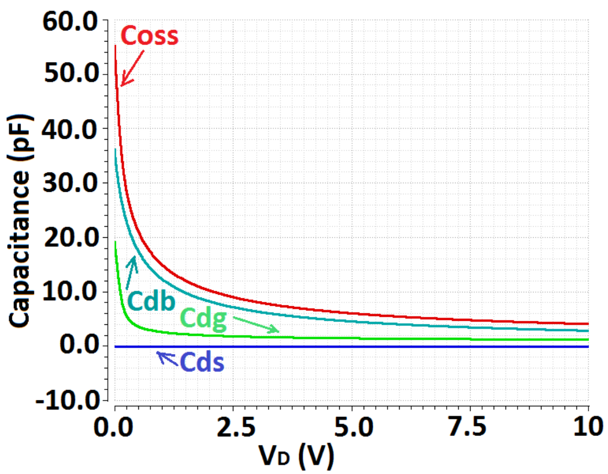


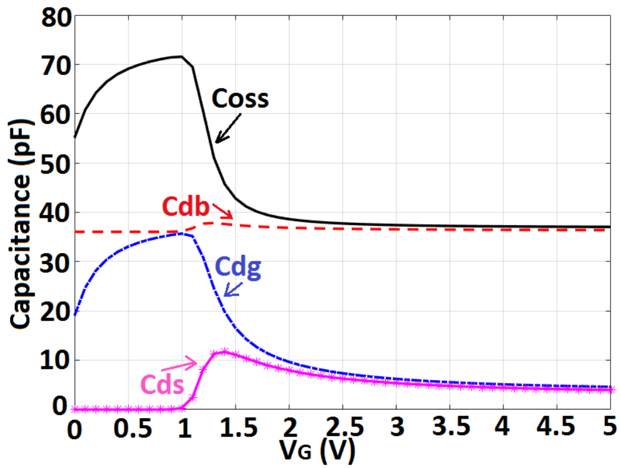


E-poster tomorrow!

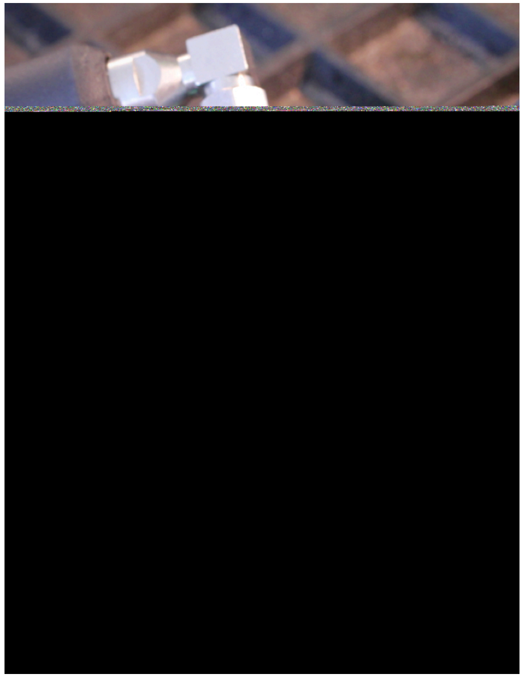
Fan L., et. Al, "Nonlinear Parasitic Capacitance Modelling of High Voltage Power MOSFETs in Partial SOI Process." *Elektronika ir Elektrotechnika* 22.3 (2016): 37-43.

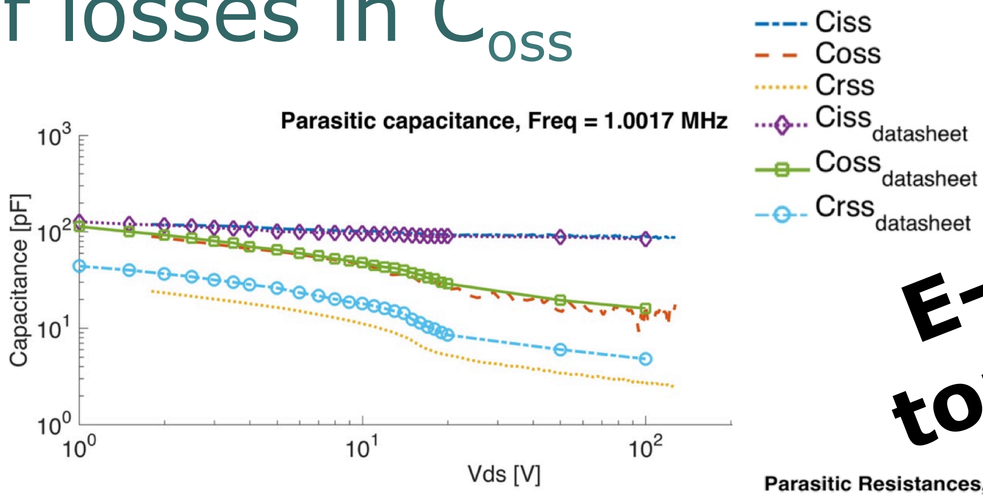




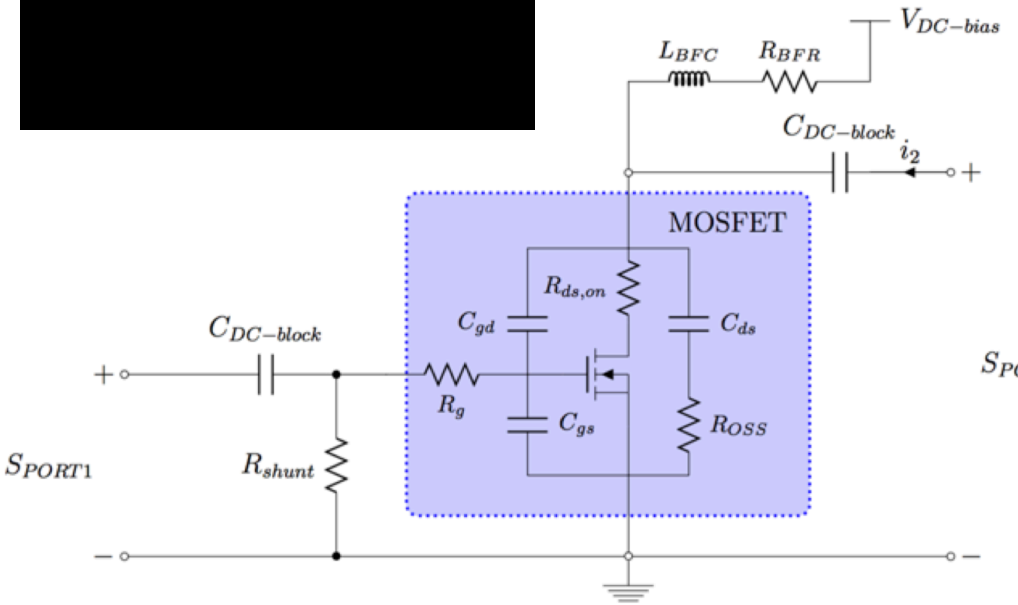


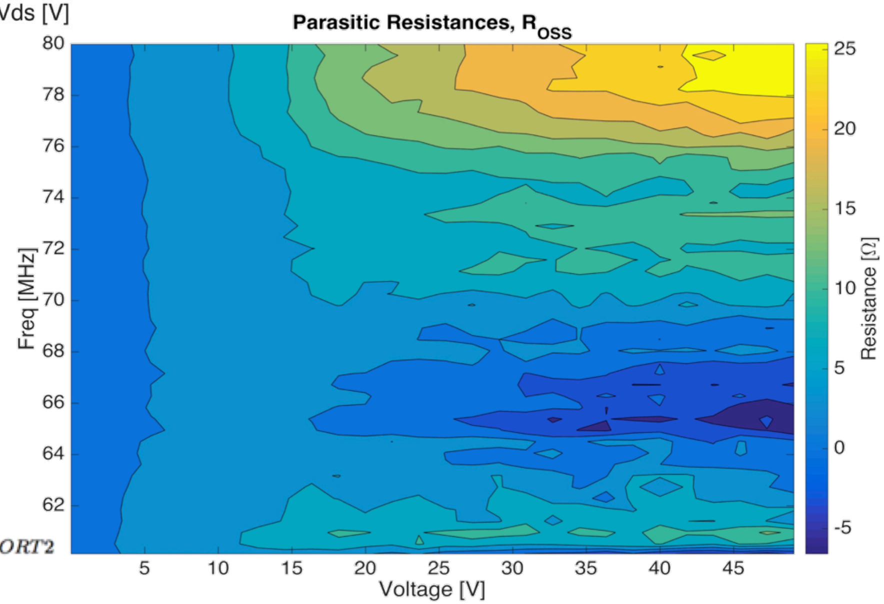
Modeling of losses in C_{oss}





E-poster tomorrow!

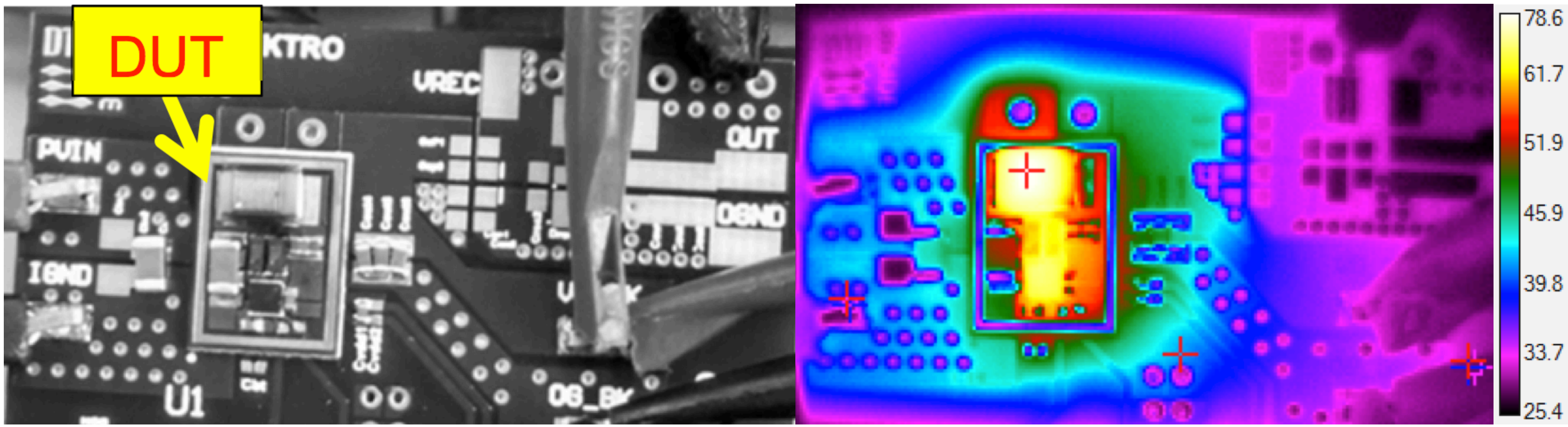




Discrete GaN design

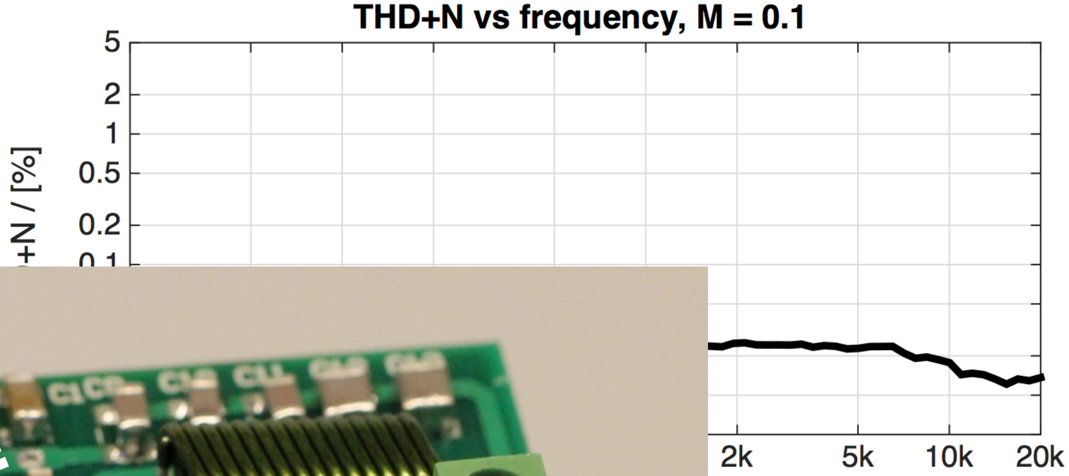
- V_{in} = 40 V, V_{out} = 10 V
- P_{out} = 12 W
- η_{peak} = 87 %
- P/Vol = 20 W/cm^3

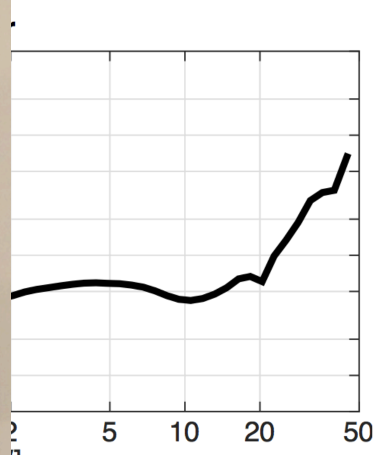
- More to come at APEC!

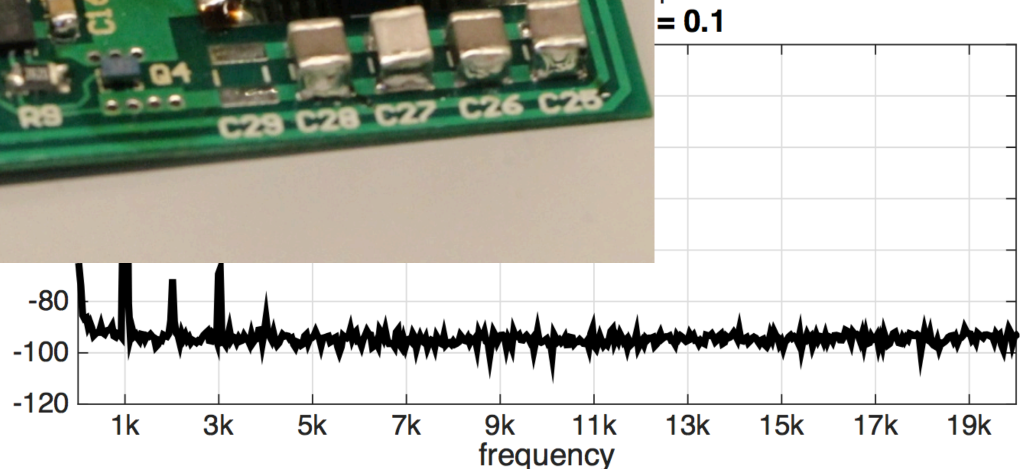


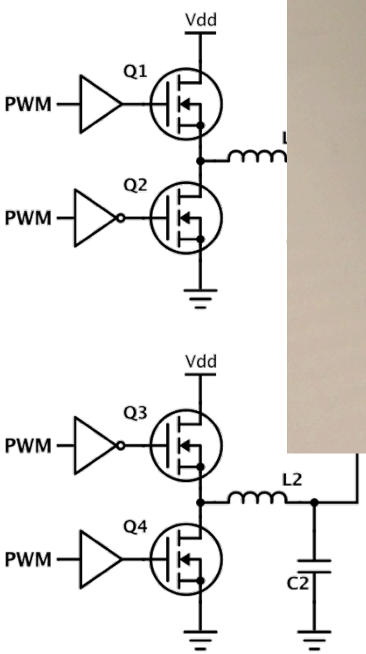
GaN-based audio power amplifers

- V_{in} = 40
- f_{sw} = 1 M
- P_{out} = 50
- EPC2016







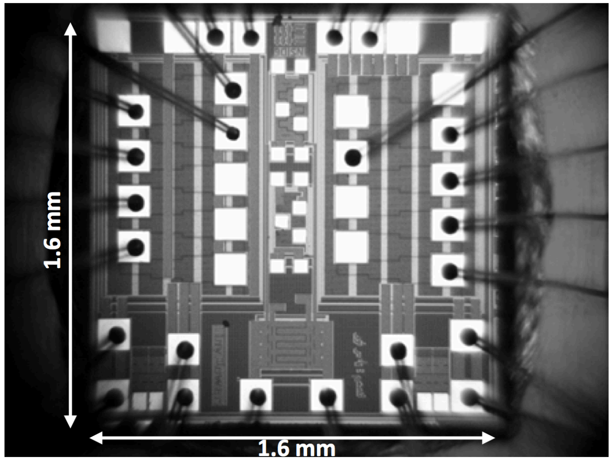


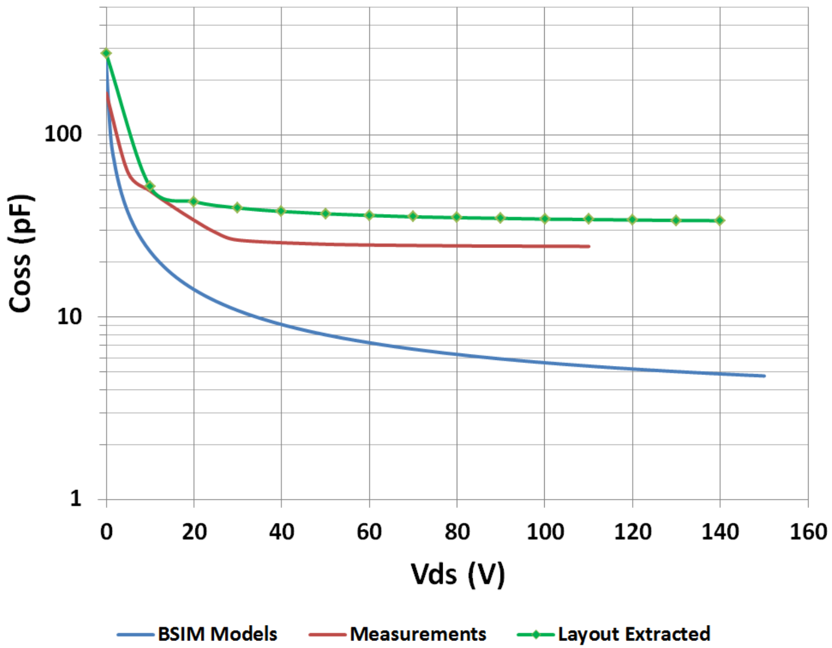
Amplification." *Audio Engineering Society Convention 138*. Audio Engineering Society, 2015.

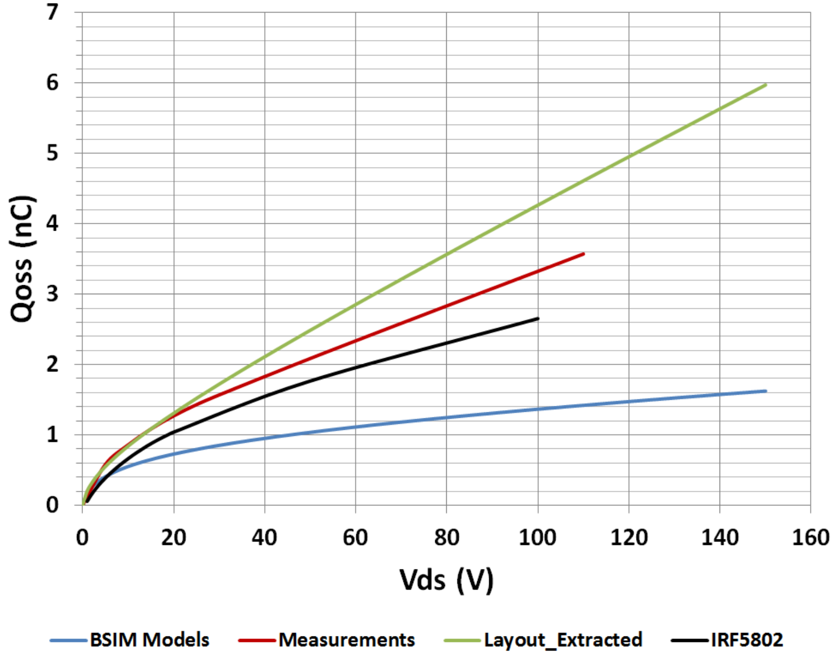
Si lateral power transistors

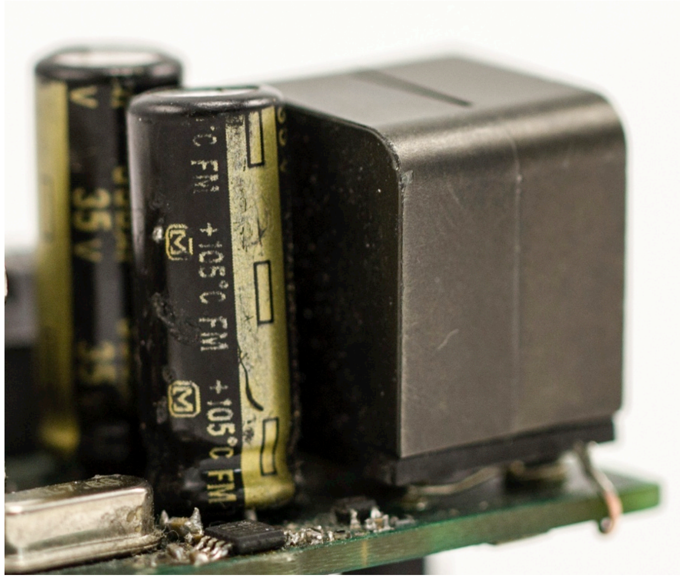
- "dual on die" electrically isolated super-junction lateral power transistors.
- 2 x 140 V, 1.2 Ω N-ch MOSFETs
- Using a 0.18 µm SOI process.

E-poster tomorrow!









Applications for PwrSoC

Enablers: semiconductors

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What's new on the architecture side?

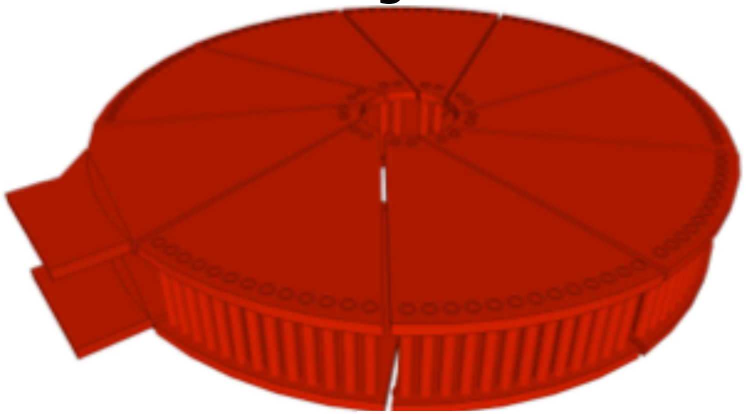
AGENDA

Passive components in PwrSoC

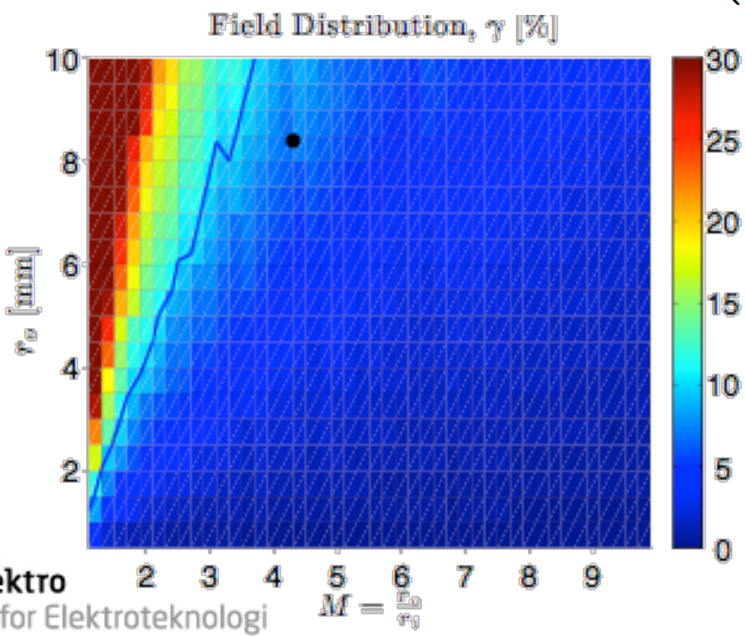
- PwrSoC:
  - lighter, cheaper, less material;
  - at mass production material amount is proportional to material cost
- so less material => less cost
- Therefore:
  - magnetic core manufacturers & capacitor manufacturers: Potentially loosing turn-over
- Main focus on inductors here
- Academia: trying hard with new materials
  - some go air-core approach

PCB toroids

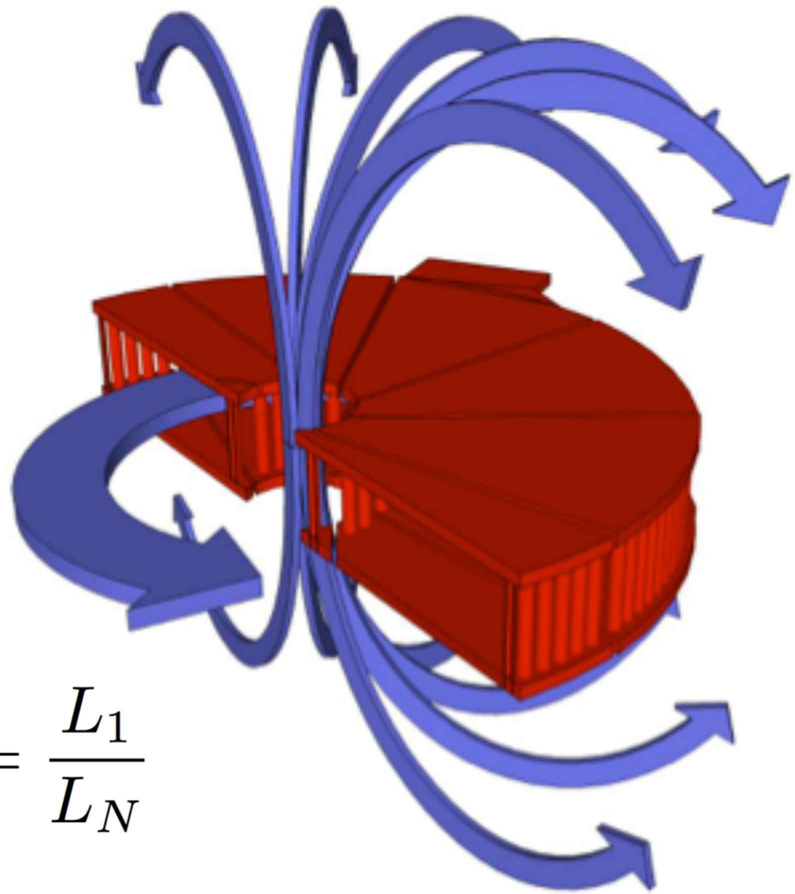
- Contained magnetic field



- Field ratios $L_N = \frac{N^2 h \mu}{2\pi} \ln\left(\frac{r_o}{r_i}\right)$



- Single turn field

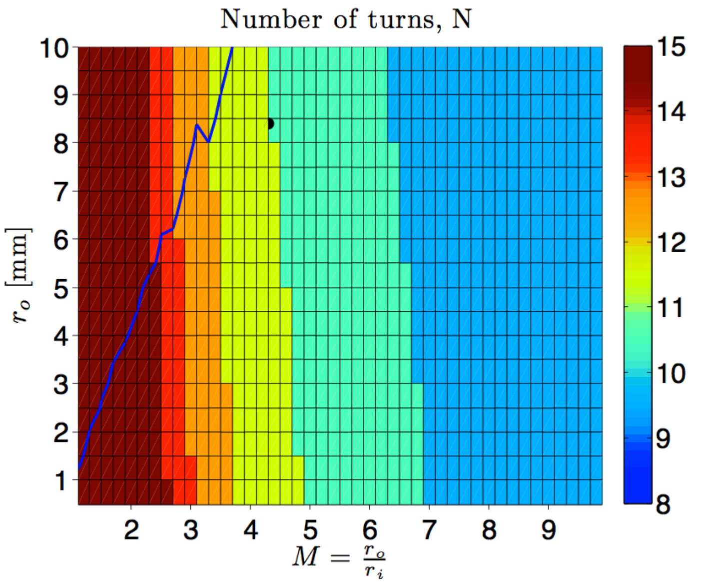


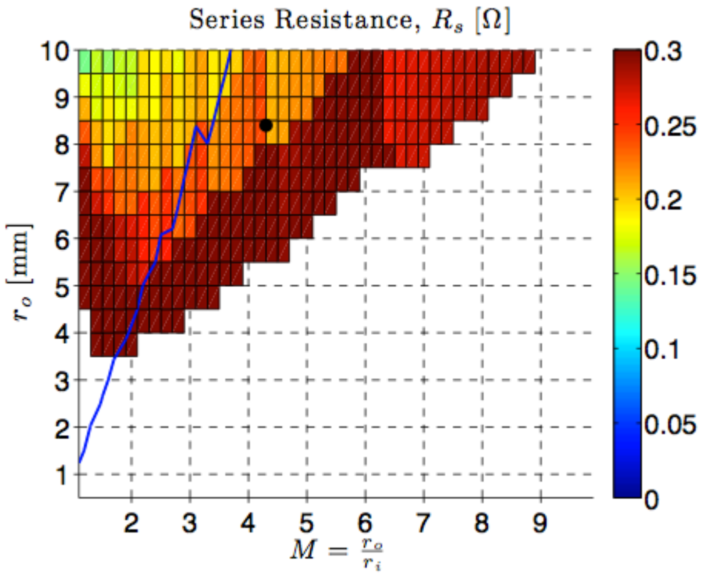
$$\gamma = \frac{L_1}{L_N}$$

$$L_1 = \frac{r_i + r_o}{2}\mu\left[\ln\left(8\frac{r_o + r_i}{r_o - r_i}\right) - 2\right]$$

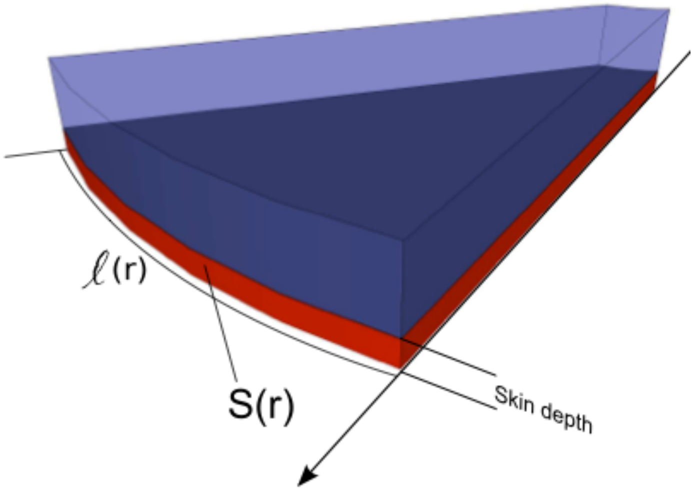
Design for inductance and losses

- N for 50 nH



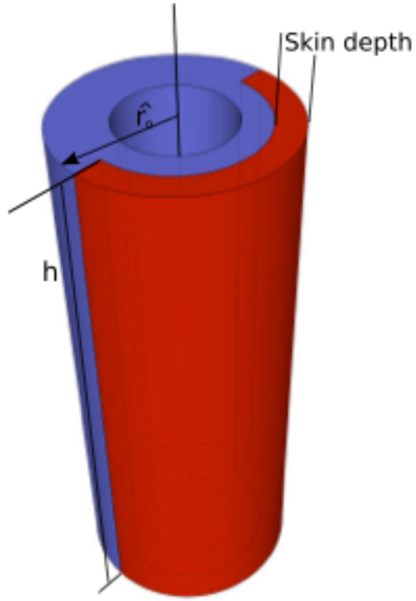


- Slab modelling



$$R_{\text{slab}} = \int_{r_i}^{r_o} \frac{\rho}{\delta\left(\frac{2\pi}{N}r - \alpha\right)}\,\mathrm{d}r = \frac{\rho N}{2\pi\delta}\ln\left(\frac{2\pi r_o - \alpha N}{2\pi r_i - \alpha N}\right) \quad \forall\ 2\pi r_i > \alpha N$$

- Via modelling



$$R_{\text{via}} = \frac{h\rho}{S} = \frac{2h\rho}{\pi\delta(2\hat{r_o} - \delta)}$$

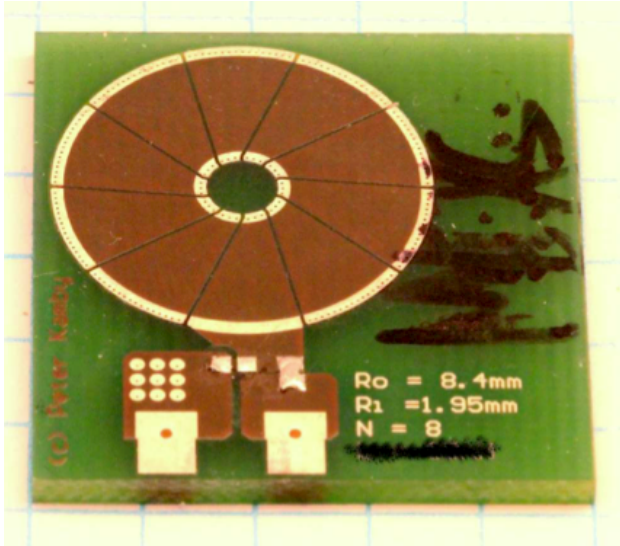
- Total resistance per turn

$$R'_w = 2R_{\text{slab}} + \frac{R_{\text{via}}}{n_i} + \frac{R_{\text{via}}}{n_o} = \frac{\rho N}{\pi\delta}\ln\left(\frac{2\pi r_o - \alpha N}{2\pi r_i - \alpha N}\right) + \frac{2h\rho\,(n_i + n_o)}{\pi\delta(2\hat{r_o} - \delta)n_i n_o}$$

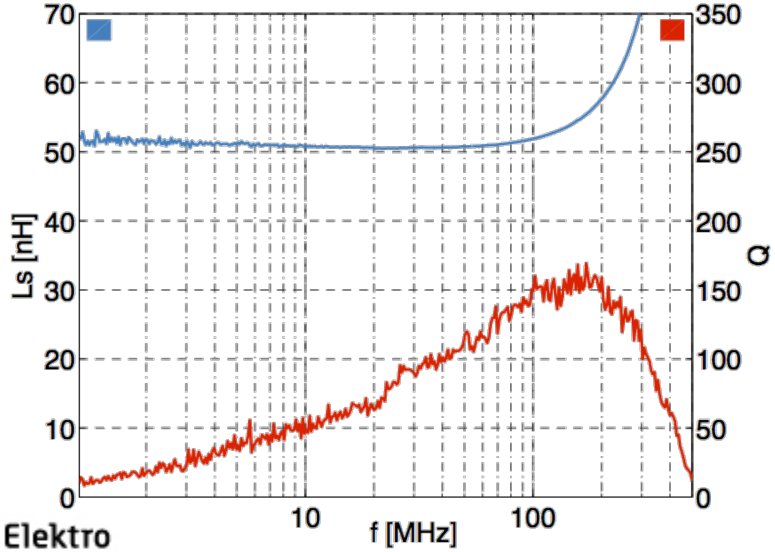
Experimental verification

- specification

Parameter	50 nH inductor
Inductance L	50.3 nH
Outer radius r_o	8.4 mm
Radius ratio M	4.3
Inner radius r_i	$\approx$ 1.95 mm
Toroid height h	1.6 mm
Number of turns N	8
Resulting total resistance R	209 mΩ
Field distribution factor γ	7.7 %



- measurement



- verification

	Design	Calculation	Measurement
Inductance L	50 nH	50.3 nH	52 nH
Series resistance R	—	209 mΩ	219 mΩ
Quality factor Q	—	151	149

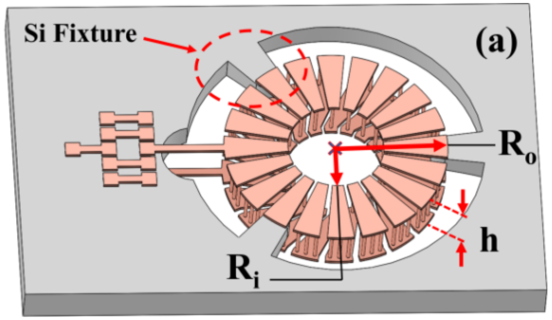
"Printed Circuit Board Integrated Toroidal Radio Frequency Inductors", Kamby, P.; Knott, A. ; Andersen, M.A.E., *IEEE Industrial Electronics Conference (IECON),* October 2012

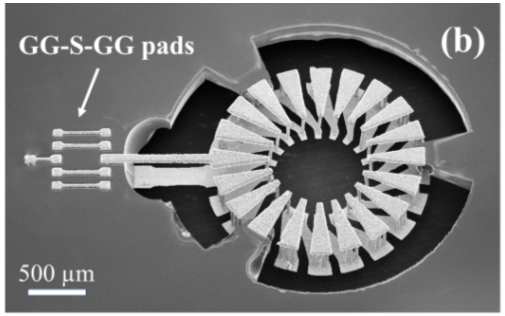
Integrated air core toroid

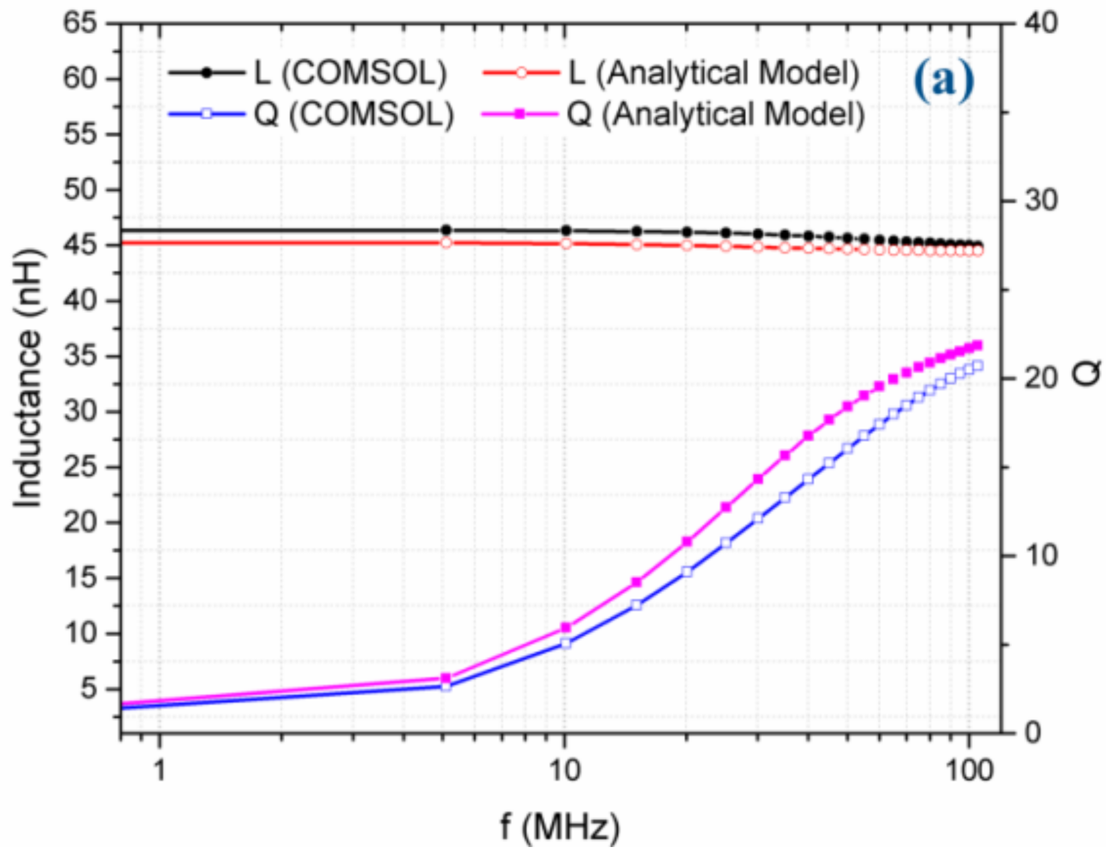
- L = 45 nH
- Q_{pk} = 21
- A = 4 mm^2

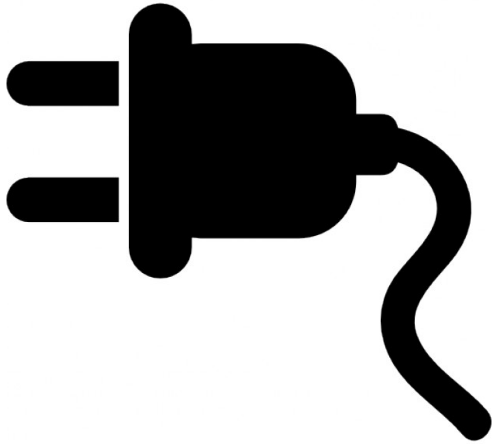
- More to come at APEC!

E-poster tomorrow!









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What's new on the architecture side?

AGENDA

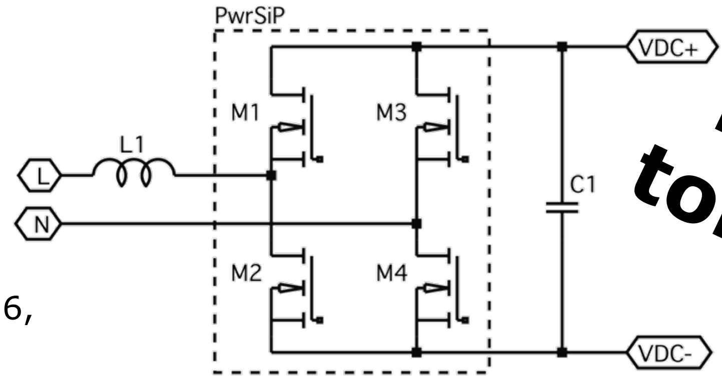
Architectures

- AC/DC interface
  - Rectifiers
  - Power combiner through switched cap
  - Ripple ports
    - Inductive based
    - Switched cap

- DC/DC through Very High Frequency (VHF, 30 MHz – 300 MHz)
  - Class E, Class Φ_2, Class DE
  - Stacking

Rectifiers

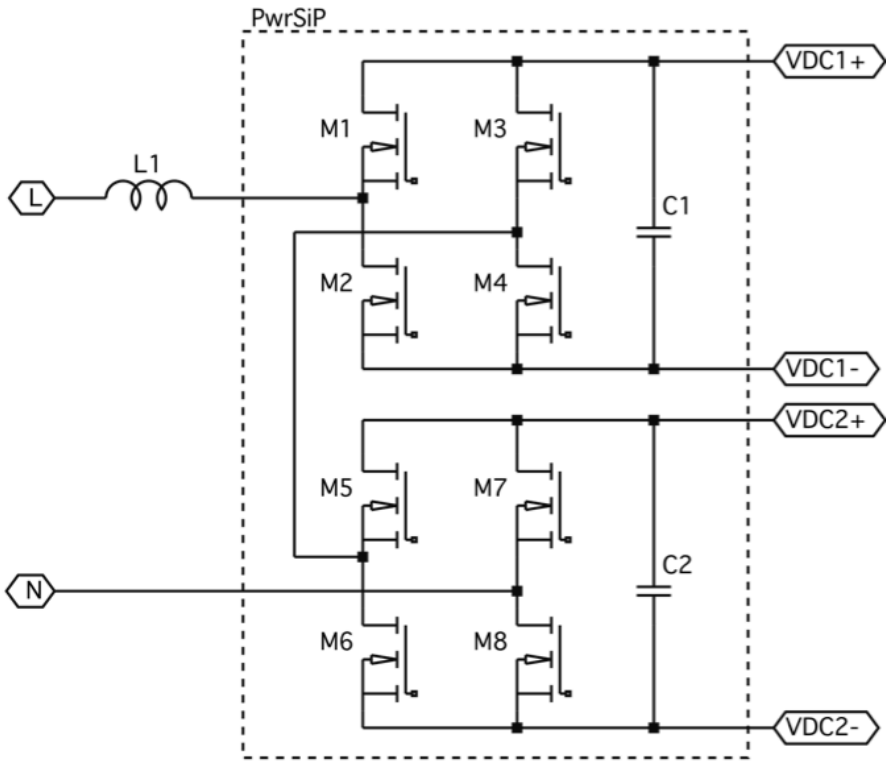
- Bridgeless Totem Pole
  (Infineon, ”GaN in a Silicon world: competition or coexistence”, APEC 2016, Industry Presentation, slide 17)

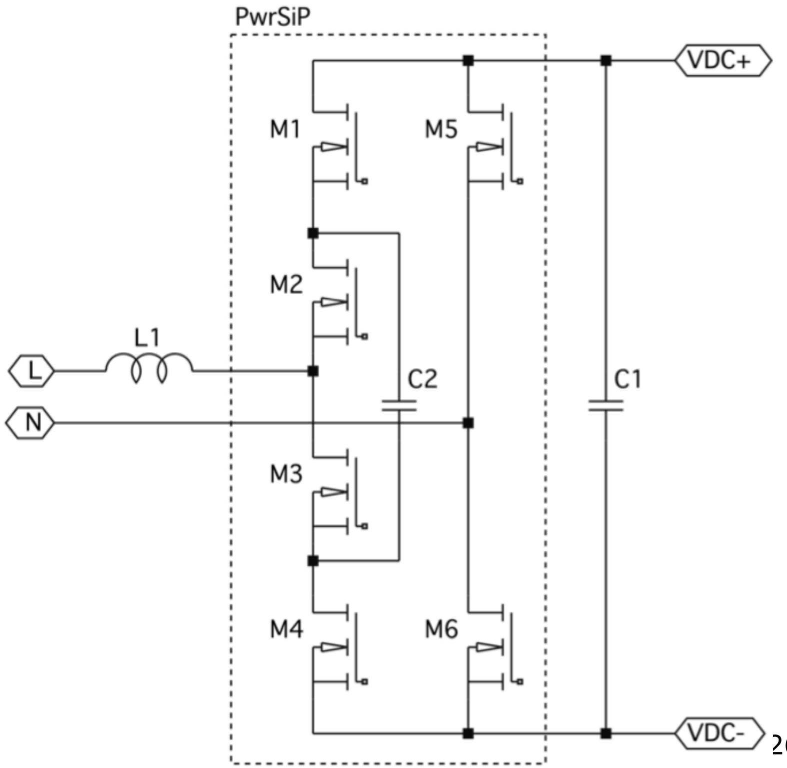


E-poster tomorrow!

- Cascaded multi-cell rectifier
  (Kasper, M., et al. "Hardware verification of a hyper-efficient (98%) and super-compact (2.2 kW/dm 3) isolated AC/DC telecom power supply module based on multi-cell converter approach." *APEC* 2015)

- Bridgeless Totem Pole Rectifier with Flying Capacitor
  (Vu, T., et. al, "Implementation of multi-level bridgeless PFC rectifiers for mid-power single phase applications." *APEC* 2016)

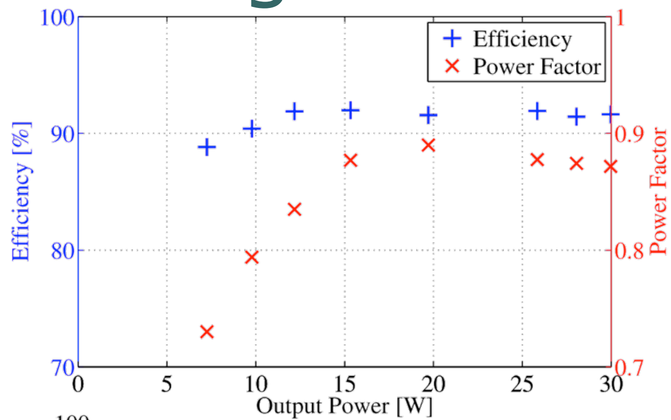


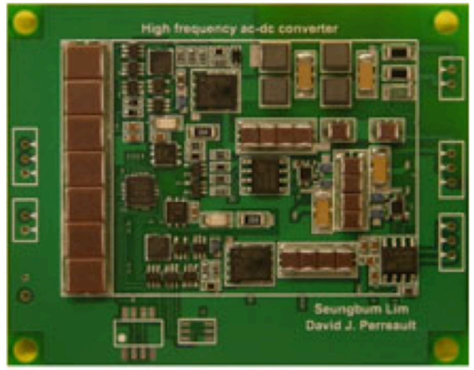


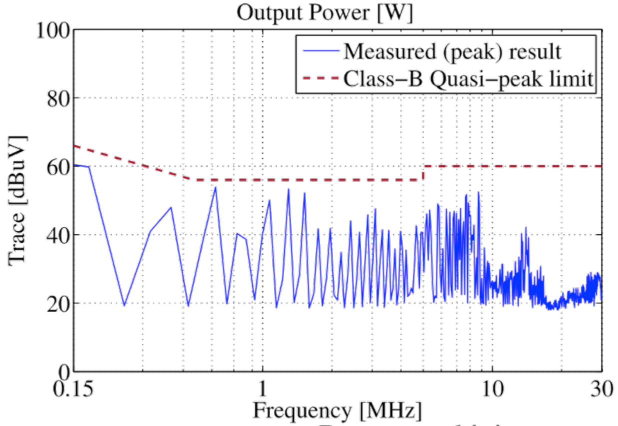
Power combiner through switched cap

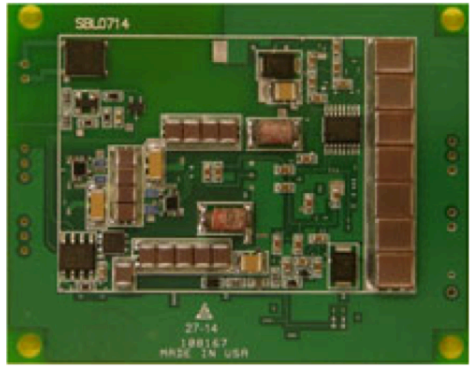
- US mains -> 35 V
- f_{sw} = 3 - 10 MHz
- η_{peak} = 92 %
- PF = 0,89
- P/Vol = 3,1 W/cm^3

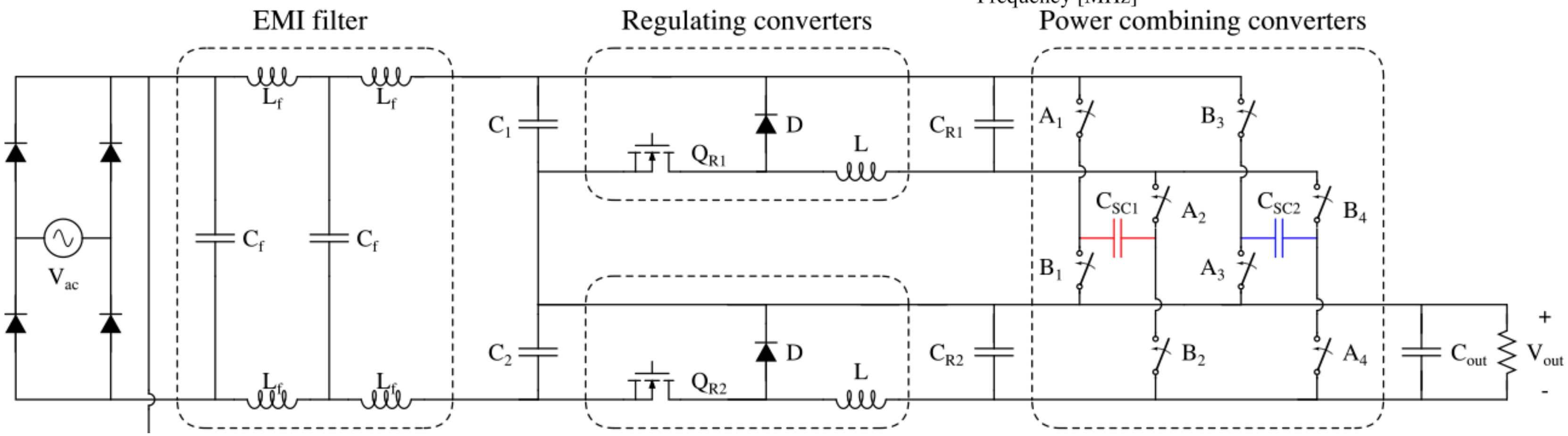
(Lim, S., et. al, "New AC–DC Power Factor Correction Architecture Suitable for High-Frequency Operation." *IEEE Transactions on Power Electronics* 31.4 (2016).)









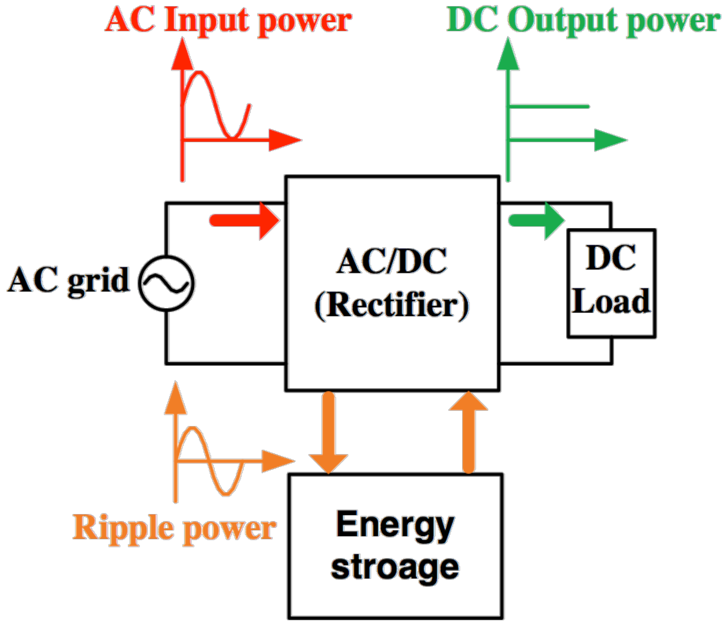


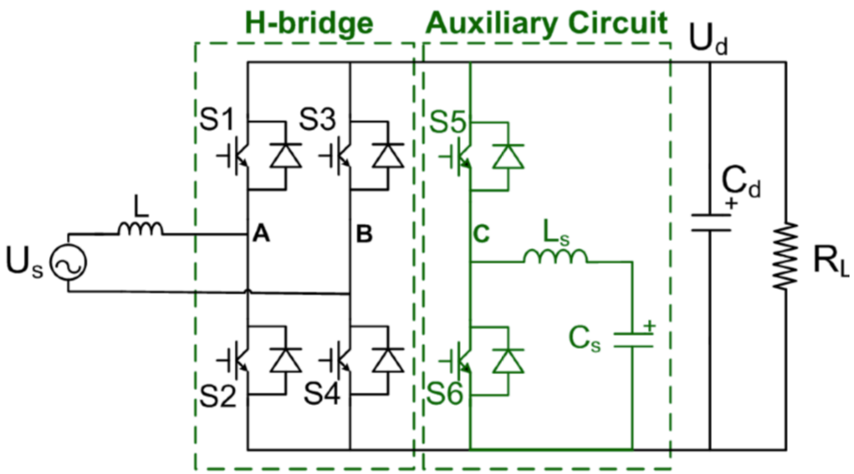
Inductive-based ripple port

- US-mains -> 42 V
- Output ripple:
  5 % * V_{out}

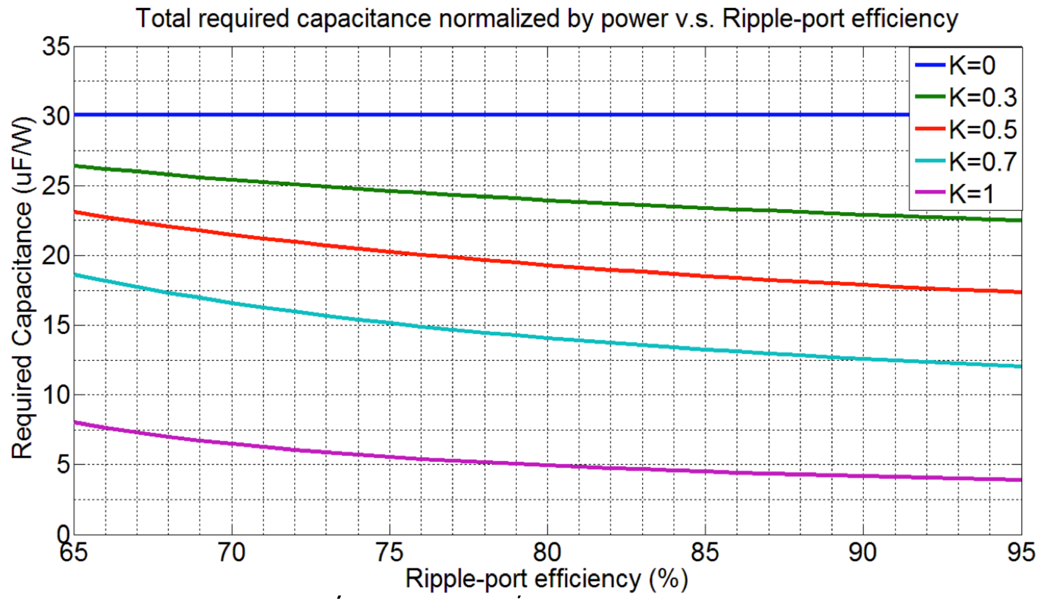
(Wang, R., et al. "A high power density singlephase PWM rectifier with active ripple energy storage." *APEC 2010*.)

(Tian, B., *A Single-phase Rectifier With Ripple-power Decoupling and Application to LED Lighting*. M.Sc. thesis. Texas A&M University, 2015.)

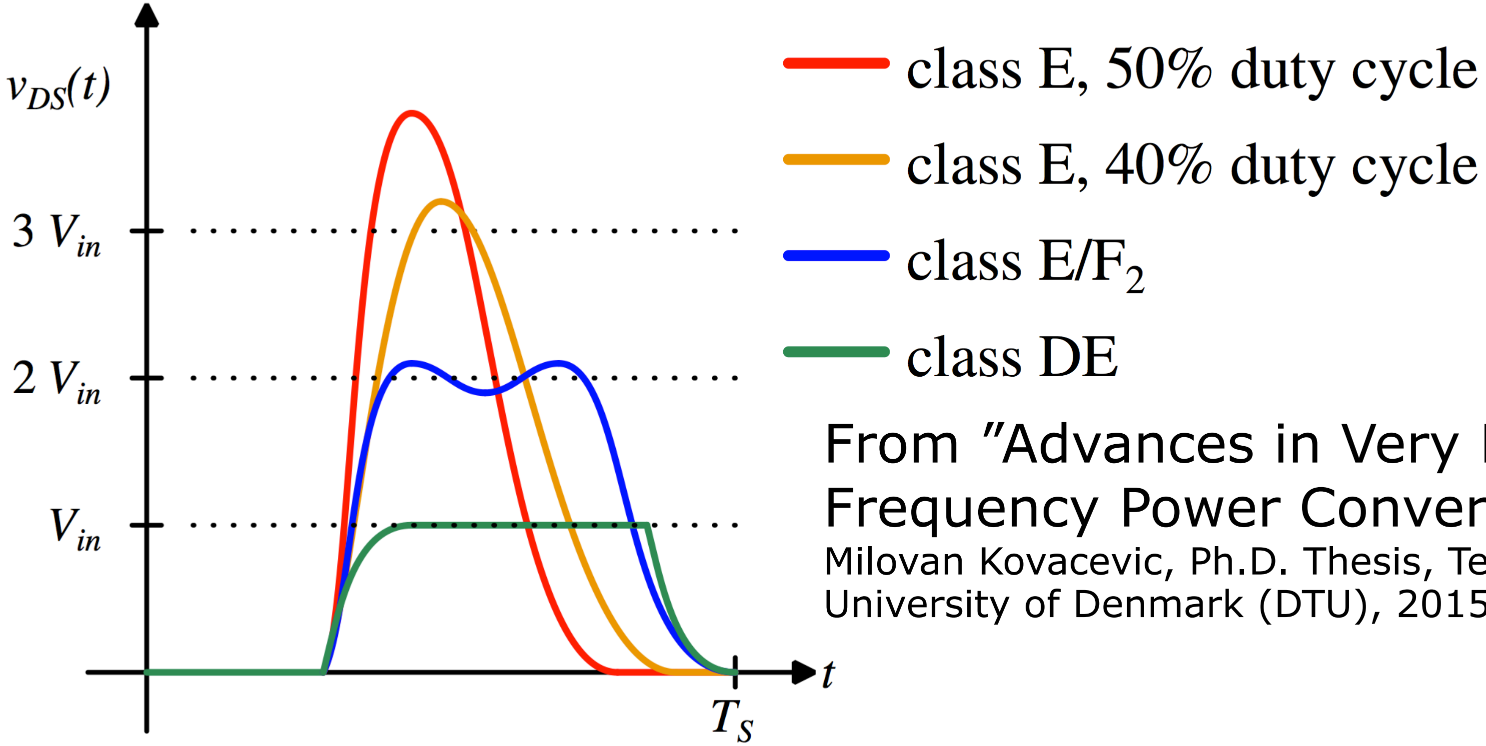




$$K = \frac{P_{rpp\_ripple}}{P_{LED} + P_{rpp\_loss}}$$



VHF DC-DC resonant converter topologies



From "Advances in Very High Frequency Power Conversion", Milovan Kovacevic, Ph.D. Thesis, Technical University of Denmark (DTU), 2015

High voltages

⇒bigger distances on semiconductor die

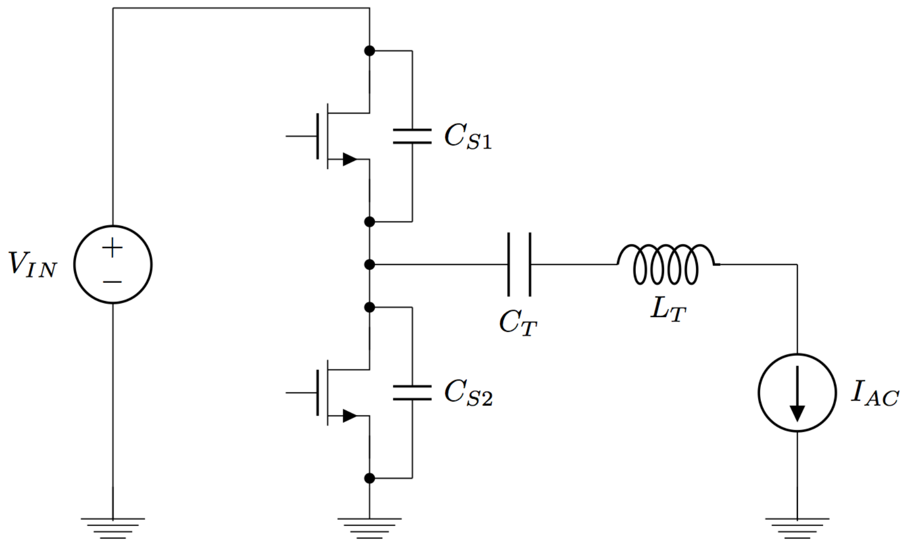
⇒therefore bigger parasitic "plates"

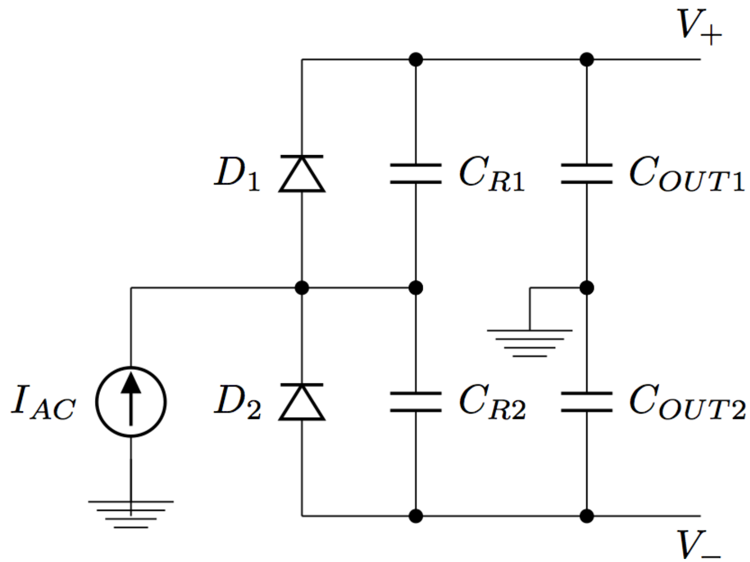
⇒Bigger capacitances

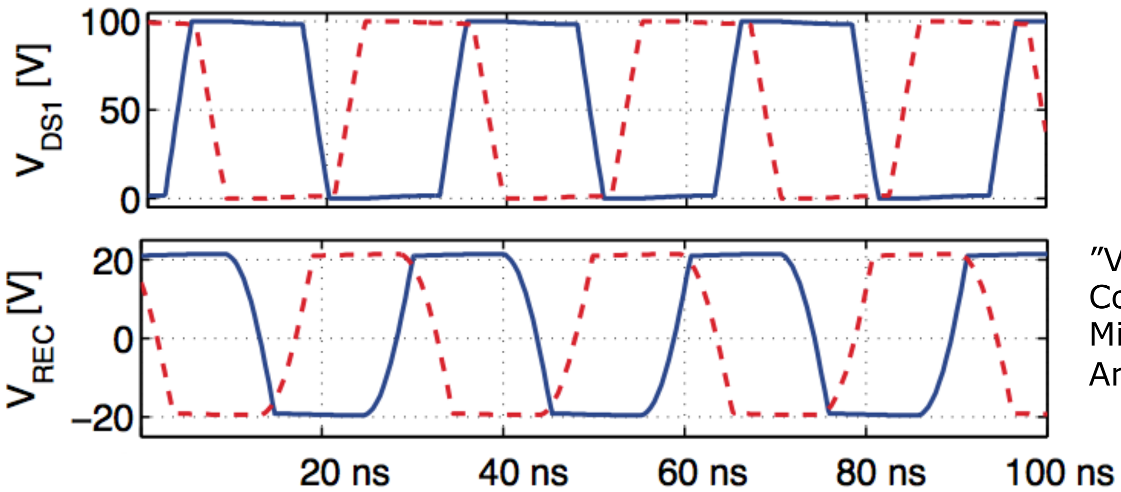
BUT: $$f_{max} = \frac{P_o}{2\pi^2 C_{oss} V_i^2}$$

"Radio Frequency Switch Mode Power Supplies", Toke M. Andersen, MSc. Thesis, Technical University of Denmark (DTU), 2010

Class-DE is reducing voltage stress

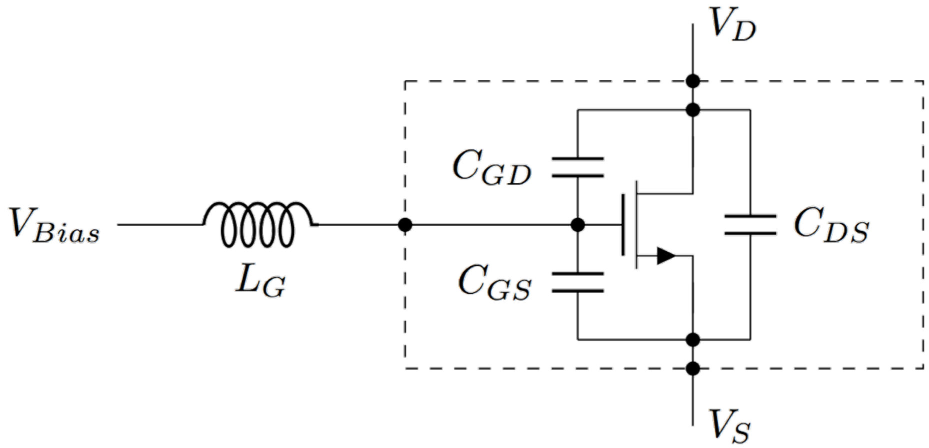




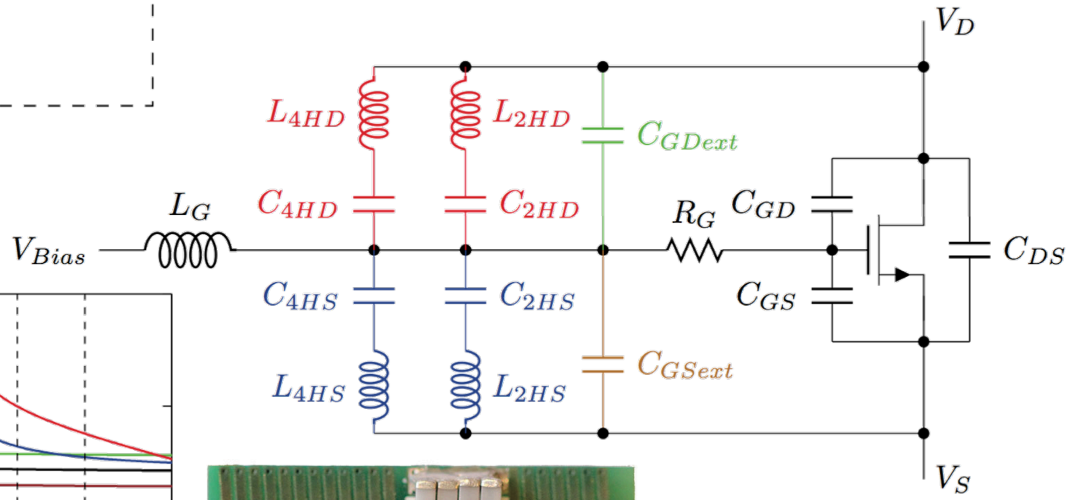


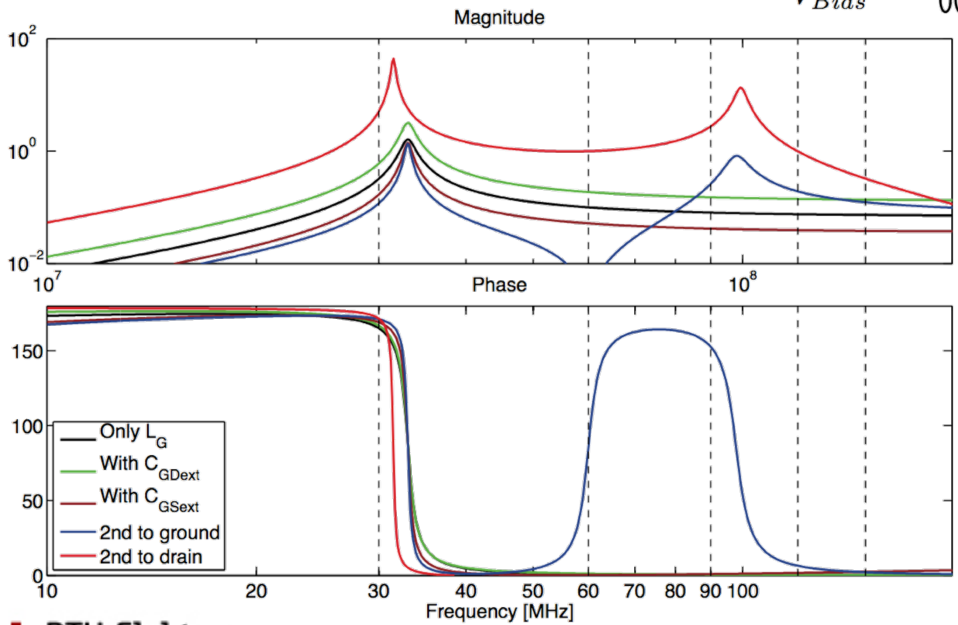
"Very High Frequency Half Bridge DC/DC Converter",
Mickey P. Madsen, Arnold Knott, Michael A.E. Andersen, APEC 2014

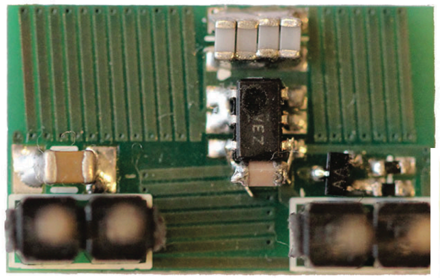
Gate Drive is the key

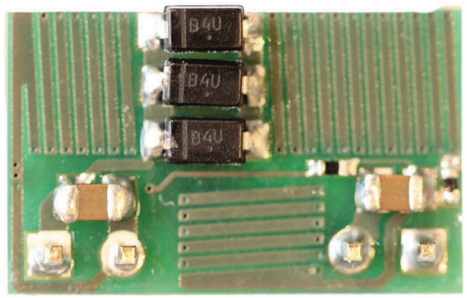


"Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components", Mickey P. Madsen, Jeppe A. Pedersen, Arnold Knott, Michael A. E. Andersen, APEC 2014









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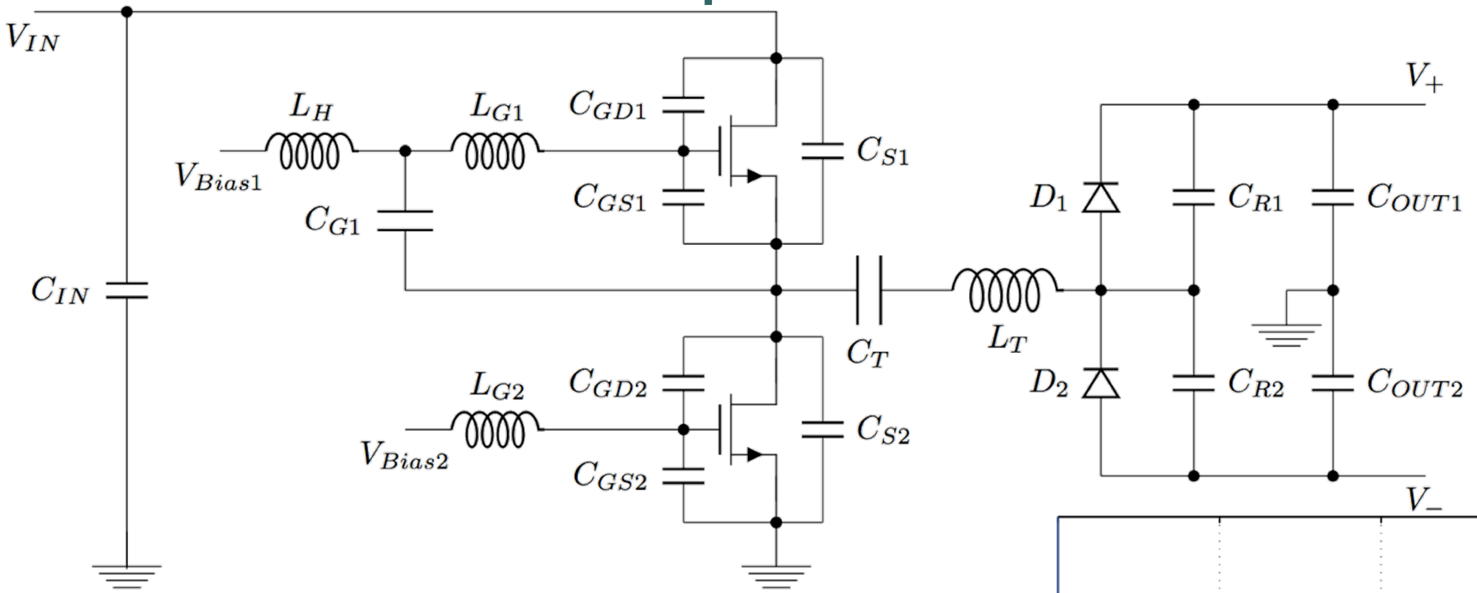
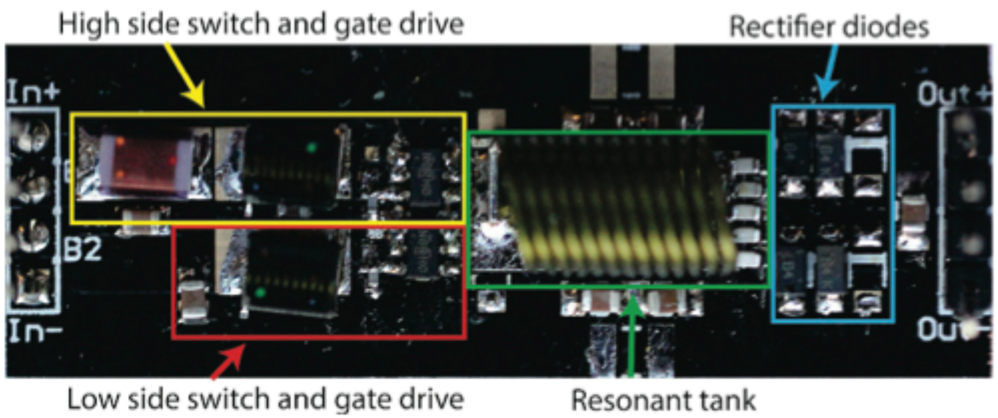
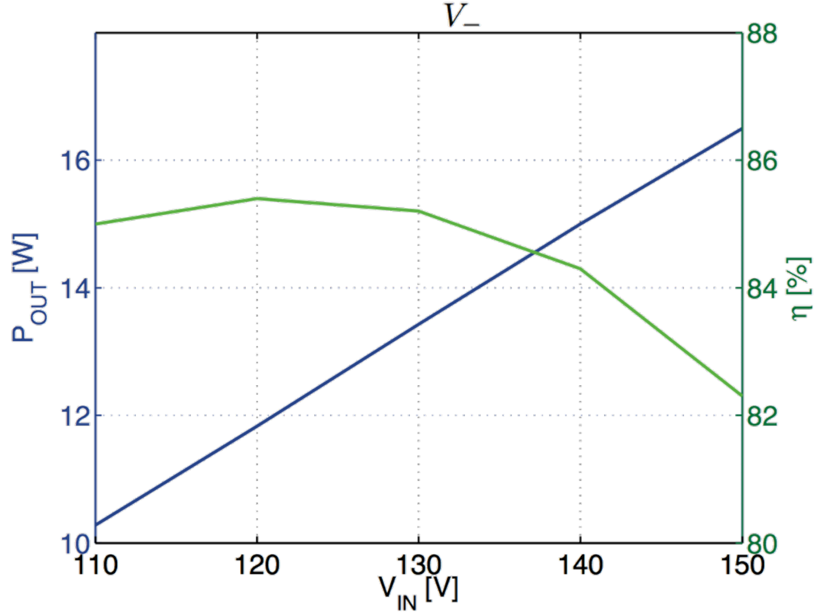
Class-DE final implementation





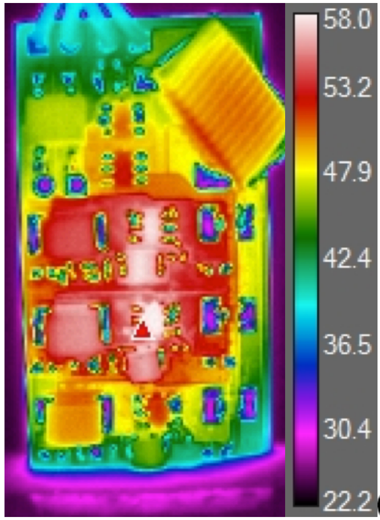


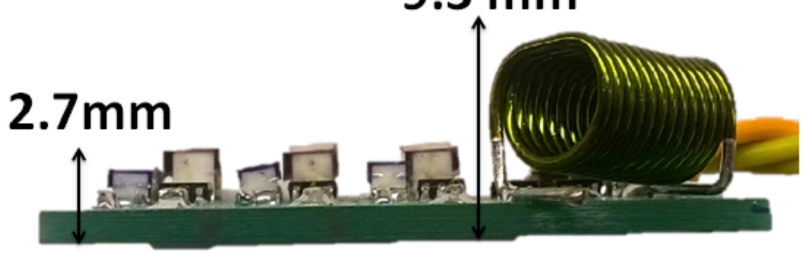
"Very High Frequency Half Bridge DC/DC Converter",
Mickey P. Madsen, Arnold Knott, Michael A.E. Andersen, APEC 2014

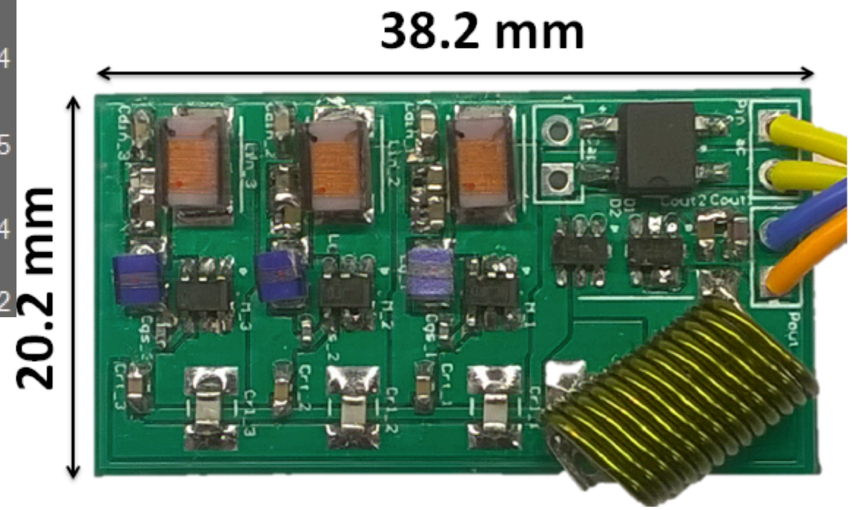
Stacking of VHF converters

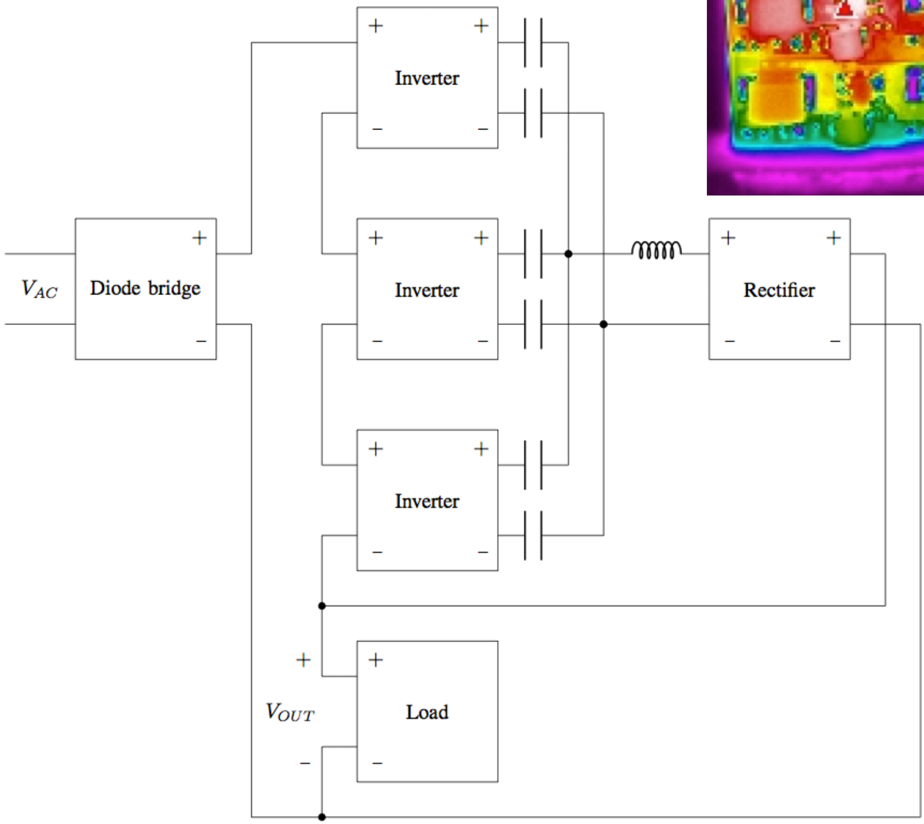
Pedersen, Jeppe A., et al. "US mains stacked Very High Frequency self-oscillating resonant power converter with unified rectifier." *APEC* 2016

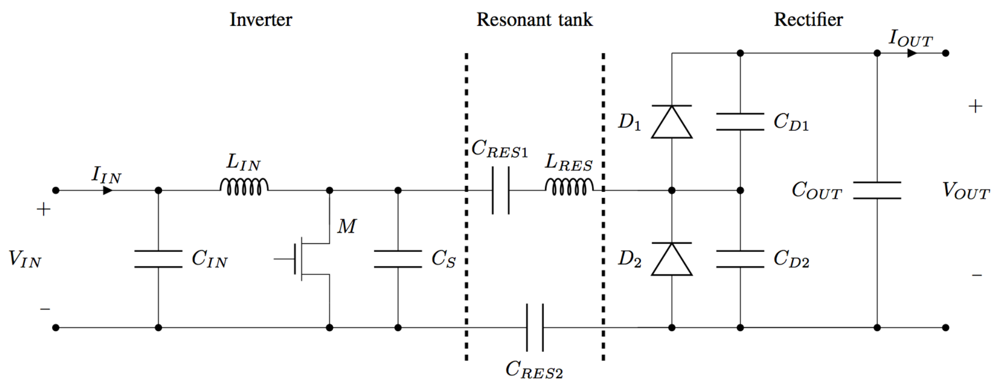
- US mains -> 60 V LED
- f_{sw} = 37 MHz
- η_{peak} = 89,4 %
- P/Vol = 2,1 W/cm^3











Conclusion on components

- PwrSoC:
  - smaller, lighter, less material (for passives) => cheaper
- Smaller passives (material volume ~ mass production cost):
  - magnetic core manufacturers & capacitor manufacturers: Potentially loosing turn-over
  - Unless we find new markets / applications, like LED drivers
- Bigger part of the cake goes to semiconductor companies
- Academia: trying hard with new materials, some go air-core approach

Conclusion on architectures

- Intensified research on AC/DC
  - mains interface
  - Ripple ports

- Intensified research on DC/AC
  - see google little box challenge

- Stacking in DC/DC
  - Galvanic isolation solutions found
  - Enables stacking for both
    inductor based and switched cap approaches

THANK YOU FOR THE INVITATION AND YOUR INTEREST!
PLEASE VISIT OUR E-POSTERS FROM

HOA THANH
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JENS PEJTERSEN
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