

Close supply chain collaboration enables easy implementation of chip embedded power SiP

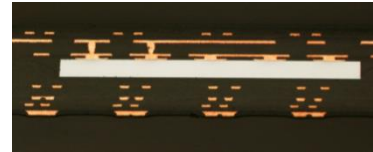
Gerald Weidinger,
R&D Project Leader, AT&S

Embedding Technology Industrialization

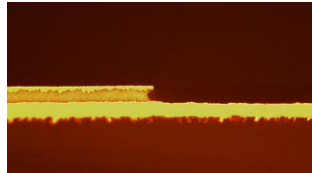
AT&S

History of embedded Die Technology

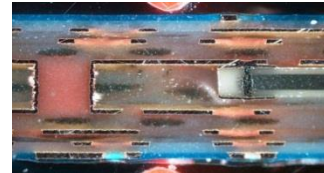
Embedded silicon



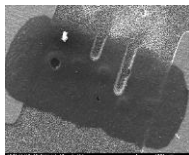
Printed capacitor



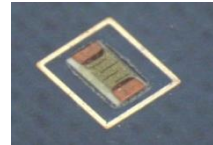
Discrete capacitor



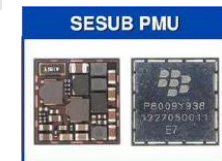
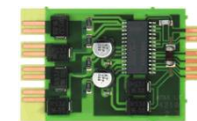
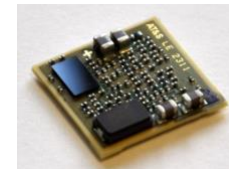
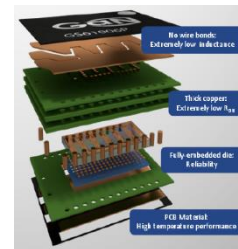
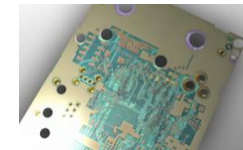
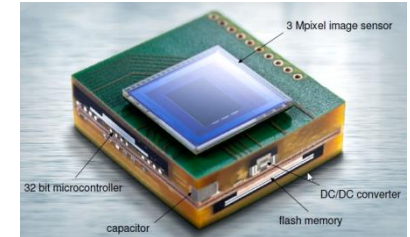
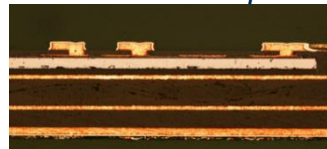
Printed resistor



Discrete resistor



Embedded Chip



1970

2000

2002

2004

2006

2008

2010

2012

2014

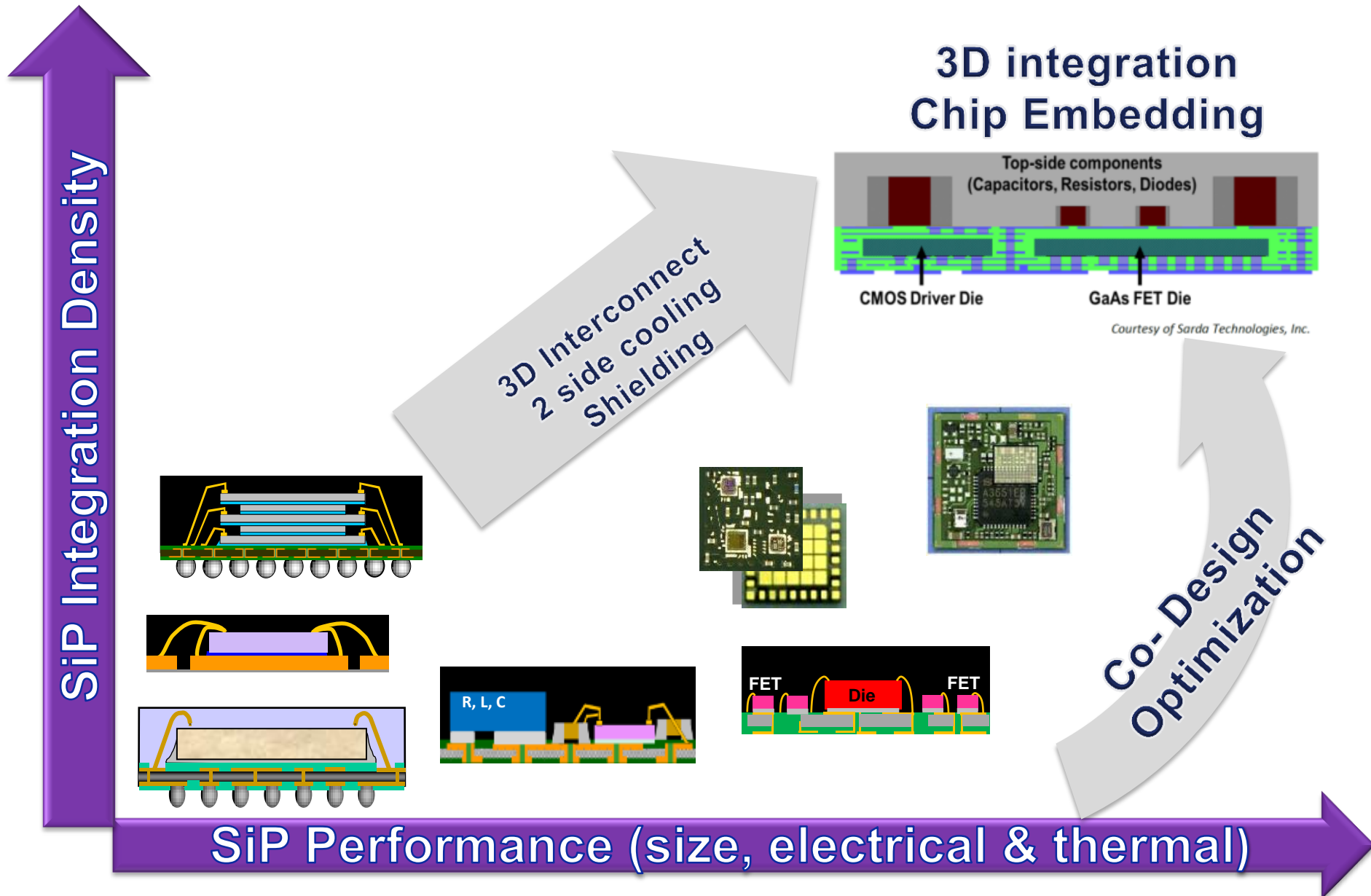
2016

Concepts

→ Research

→ Development Projects

→ Industrialization → Serial Production



Why Chip Embedding?

Unique Selling Propositions	... in detail
Miniaturization	<ul style="list-style-type: none">• Footprint reduction• Higher component integration (additional assembly layer)
Electrical performance	<ul style="list-style-type: none">• Improved signal performance (higher data rates)• Reduction of parasitic effects
Mechanical performance	<ul style="list-style-type: none">• Higher durability and reliability through copper-to-copper connections (copper filled microvias)• Package enables protective enclosure• High drop, shock and vibration tolerance
Thermal management	<ul style="list-style-type: none">• Improved heat dissipation through direct copper connection• Improved heat dissipation FR4 versus air (compared to SMD)
Additional functions <ul style="list-style-type: none">– Reduction of overall cost– EMI shielding	<ul style="list-style-type: none">• EMV shielding (partial or full shielding of a package)• Package is the housing → no additional molding required
ECP is supporting the trend towards modularization	<ul style="list-style-type: none">• Lower set-up costs compared to other packaging technologies (packaging versus PCB processes)• Customization of footprint and module versions can be done due to digital imaging - no separate tooling necessary (e.g. QFN)
Anti-Tamper and Security	<ul style="list-style-type: none">• Hidden electronics preventing reverse engineering and counterfeiting

Embedding Technology Industrialization

AT&S

Our collaboration enables customers success



- Global footprint
- Strong R&D focus
- High volume manufacturing experience , capacity and capability
- Brought product portfolio
- Strong customer base
- Long history in embedded technology



Alignment on

- Business processes
- Aligned technical capabilities
- Common focus on segments and applications



- Global footprint
- High volume manufacturing experience , capacity and capability
- Excellent testing capabilities
- Strong customer base
- Brought experience in backend processing of various applications

Supply Chain Offering

AT&S

Strategic supply chain collaboration is a key success factor

KGD test
RDL
Thin / Dice
Inspect / TnR



Substrate manufacturing
Embedded chip
Strip Test



SMT
Top FC / under fill
Cap or Mold
Solder Ball Attach
Package saw

Package level test
Reliability test

Co-
Design

Wafer
to Die

Substrate
embedded
chip

Package
assembly

Test



*Customer
Consigned
Option*



*Customer
Specs*



AT&S



April 2015 - Joint marketing / supply chain agreement
Between AT&S and UTAC for 3D SiP with embedded chip
technology. Collaboration press release April 2016.
AT&S over 5 years production embedding experience.

- Outsourced Semiconductor Assembly and Test services (OSAT) provider in support of Analog, Mixed-Signal, Logic, Power and Memory products.
- UTAC 2015 Revenue \$878M; Ranked 6th in the Top Ten OSATs
- Focus – Assy, Test and Full Turnkey; Test comprises 35% of sales in 2015.
- 1997 Established in Singapore
- Mfg Footprint - Singapore, Taiwan, Malaysia, Indonesia, Thailand, China.
- >260K M² Manufacturing Space and ~ 12K Employees Globally.
- Sales offices located worldwide.
- Markets: Mobile Phone, Automotive, Security, Wearable's, Industrial & Medical.





UTAC Dongguan, China (UDG)

[Since 1988, >500k sq ft, China Logistics, WW distribution]

BGA, LGA, QFN, Memory Cards, USB, SiP

3D SiP w/ Embedded chip



UTAC Thailand (UTL)

[Since 1973, 640k sq ft, Auto & Security certifications.]

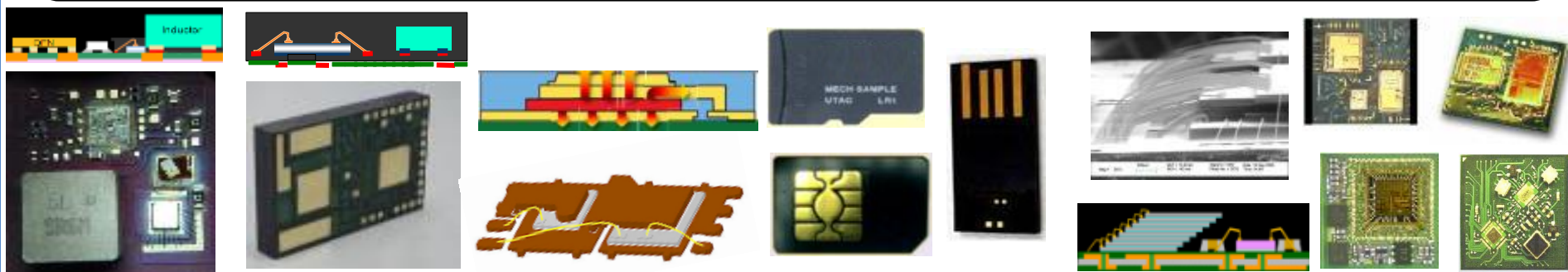
QFN, GQFN, LGA, MIS, MEMS, Power QFN with Cu Clip



UTAC Shanghai, China (USC)

[90k sq ft, WGQ Free trade zone, Focus - Asia customers]

QFN, FBGA, LGA, MIS



AT&S – a world leading high-tech PCB company

AT&S

High-End Interconnection
Solutions

for
Mobile Devices, Automotive,
Industrial, Medical Applications

Continuously
Outperforming
market growth

3

in High-End Technology
worldwide

€ 762.9m

Revenue in FY 2015/16,
5.2% organic growth

9,165
employees

One of the
most profitable
Players in the
Industry:

EBITDA margin of 22%
in FY 2015/16

1

manufacturer in Europe

Cost-competitive production
footprint with

6

plants in Europe and Asia

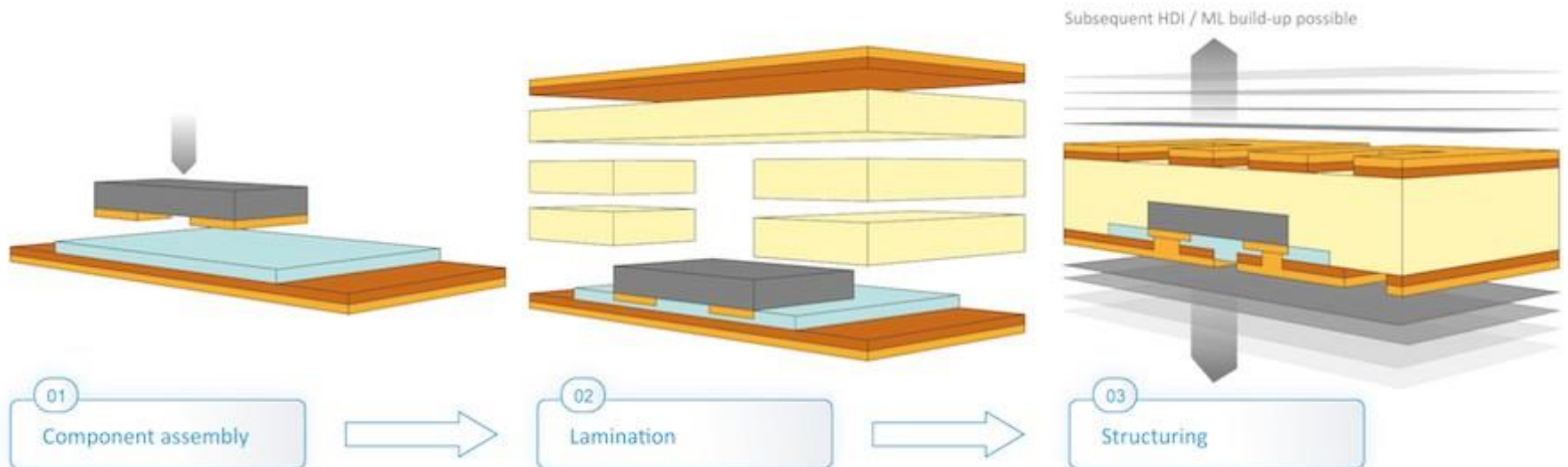
AT&S at a glance & global footprint

AT&S



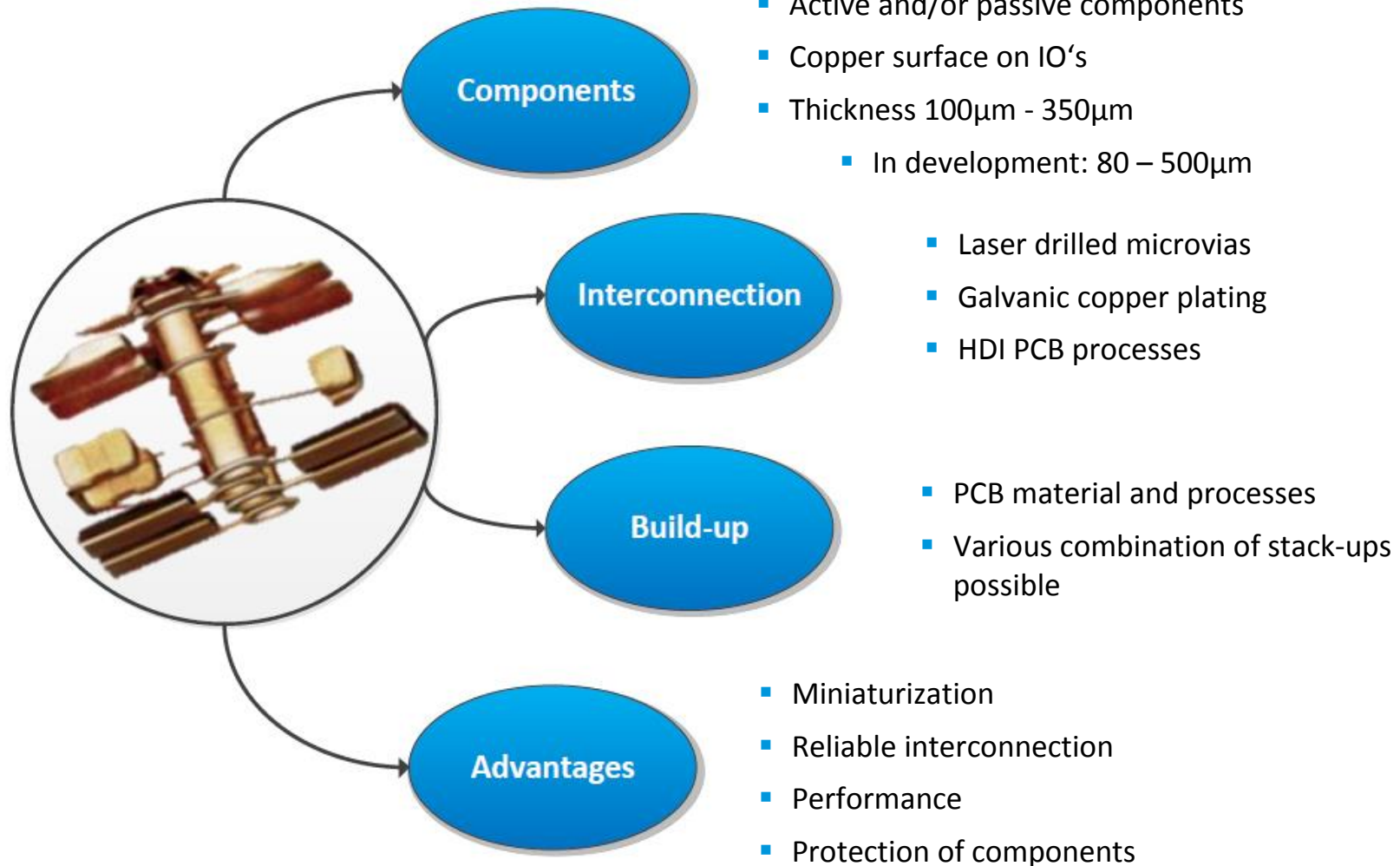
AT&S ECP® - Embedded Component Packaging

ECP® (**E**mbded **C**omponent **P**ackaging) uses the space in an organic, laminate substrate (Printed Circuit Board) for active and passive components integration

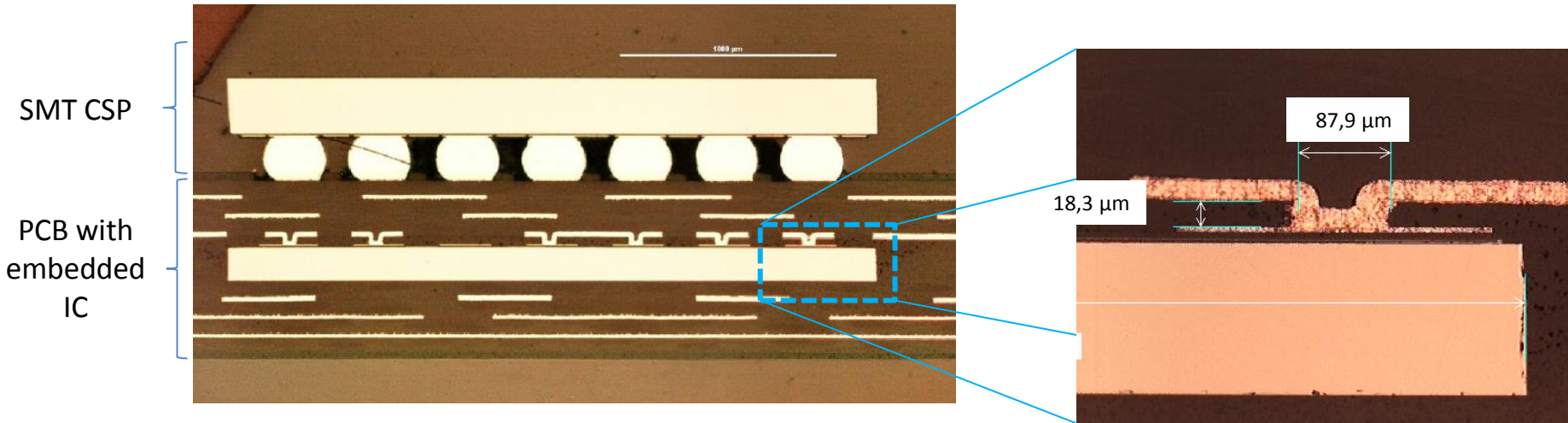


Components embedding into the PCB core with copper plated microvia connections

AT&S ECP® - Embedded Component Packaging

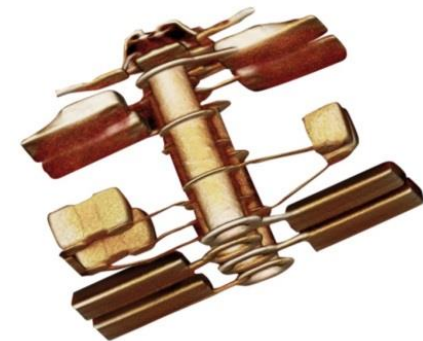
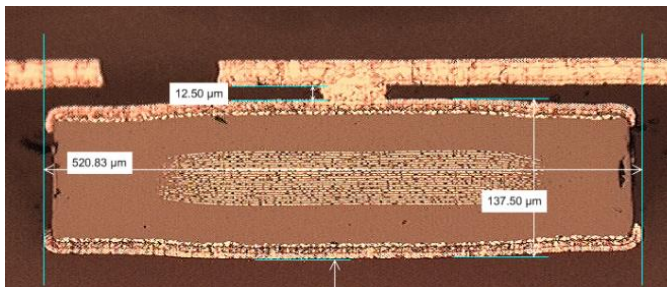


X-section of embedded devices



**For interconnection, same technology and processes
as for HDI/microvia PCBs!**

Embedded
passives

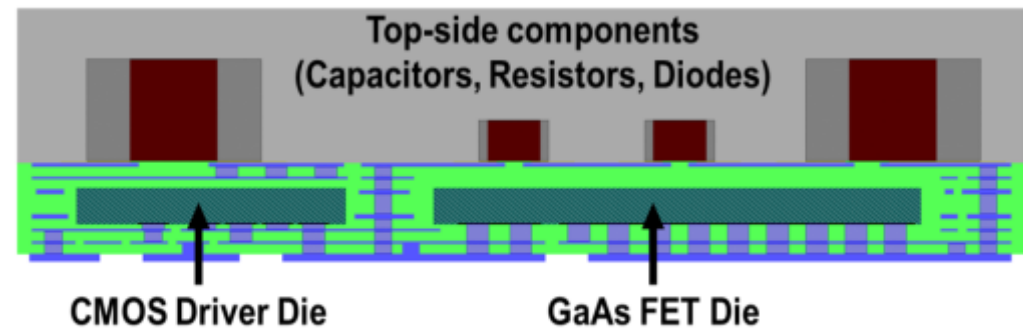
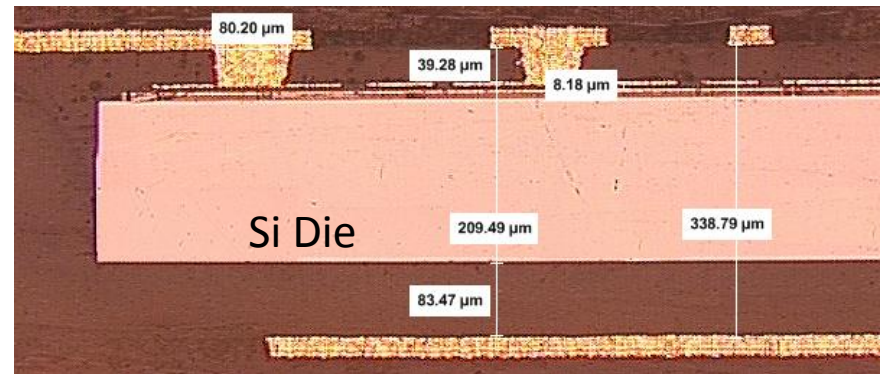
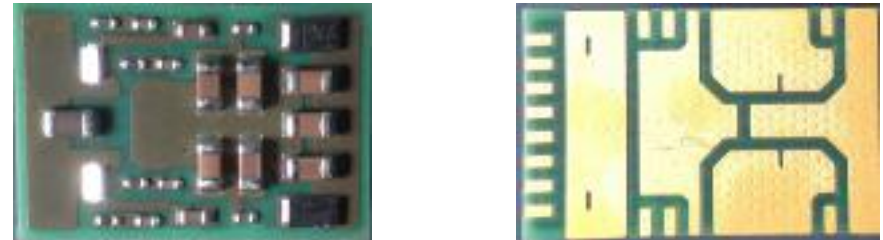


CT image of embedded caps in a 4 layer PTH board)

Package Type: 4.5 x 7.2mm LGA-SIP
Highlights: 2 embedded die + 24 passive components on substrate top side

Package size / Type	4.5 x 7.2 mm LGA-SIP
Substrate Thickness	560 $\mu\text{m} \pm 10\%$ 320 μm core
Die thickness	200 μm Max.
Surface finish (Die DAP)	Electrolytic Ni/AU
Surface finish (Land Pad)	Electrolytic Ni/AU
# of Passive Component (Top of substrate surface)	24ea Passive
Component Sizes	Passive 10ea 01005, 10ea 0402, 4ea 0201.
# of embedded chip	2
Strip Size	188x64mm
Substrate Metal layer	4 Layer

Assy Layout



Summary

- System in a package (SiP) is a strategic focus area for UTAC and AT&S
- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions
- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications
- Supply chain collaboration for emerging 3D SiP solutions with embedded chip technology will advanced the technology and provide full turnkey (FTK) supply solutions for customers.
- Flexible business models available to fit to customer requirements



AT&S first choice for advanced applications

Double sided PTH

IMS

ECP®

2.5D®

Thick Copper

HDI Any-Layer

NucleuS®

HSMtec

Multilayer

Flexible & Rigid Flexible

Metal Core

HDI Microvia

AT&S

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