AMD INSPIRES INNOVATION EVERYWHERE.

The world's top companies count on AMD.

Integrated Power Conversion Strategies across Laptop, Server and Graphics Products

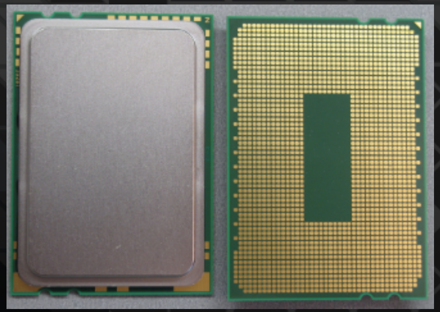
Sam Naffziger

AMD PRODUCTS

DIVERSE POWER DELIVERY CHALLENGES

- Laptop
  - 10W to 45W TDP
  - 3-4 high current (up to 40A) rails
  - 5-10 low current rails
  - Diverse IP

- Server
  - 65W to 165W TDP
  - 3 high current rails (up to 120A)
  - 2-3 low current rails



- Graphics
  - 10W to 300W TDP
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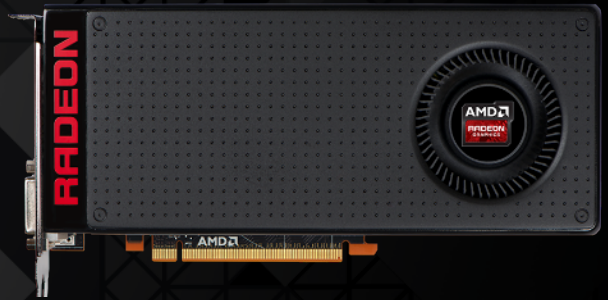
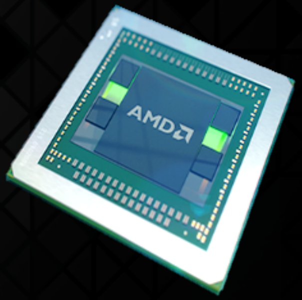
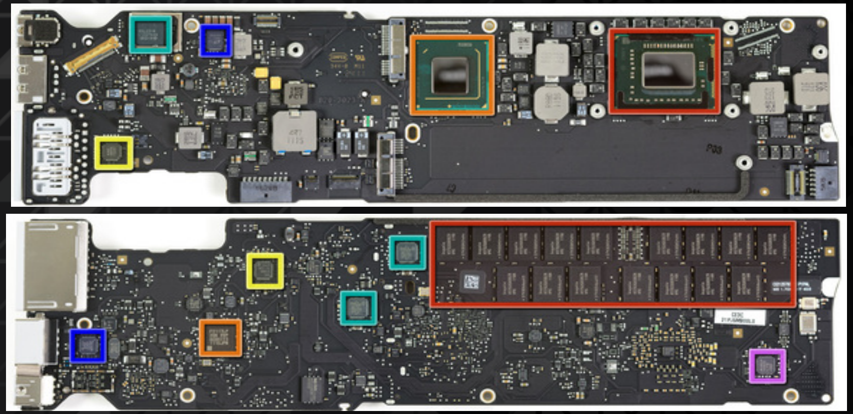


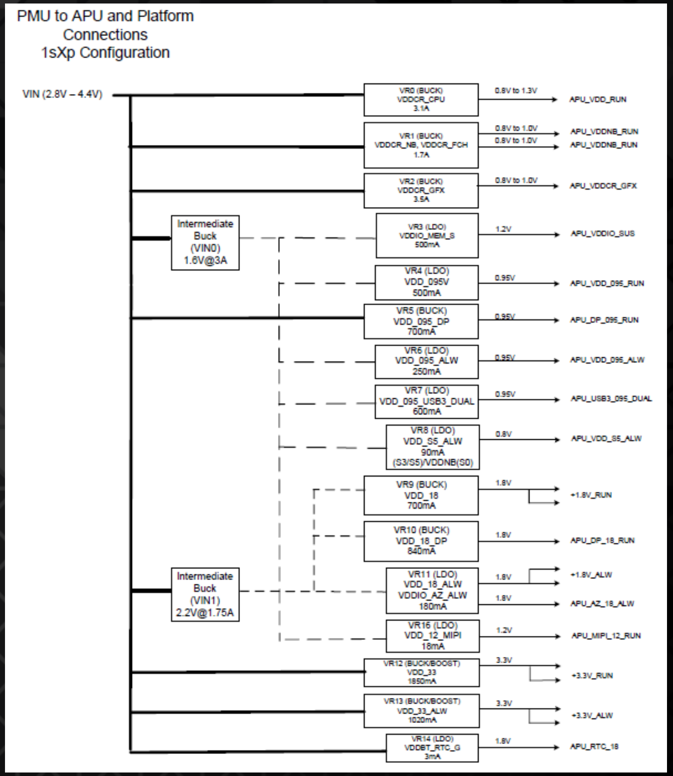


PRIMARY POWER CONVERSION AND DELIVERY CHALLENGES

AMD

- Minimize AC transients
- Accurate DC voltage
- Large size / weight of voltage regulator components
  - Exacerbated by high currents
- Regulator costs with the profusion of rails
  - Exacerbated by increasingly diverse integrated IP and high core counts

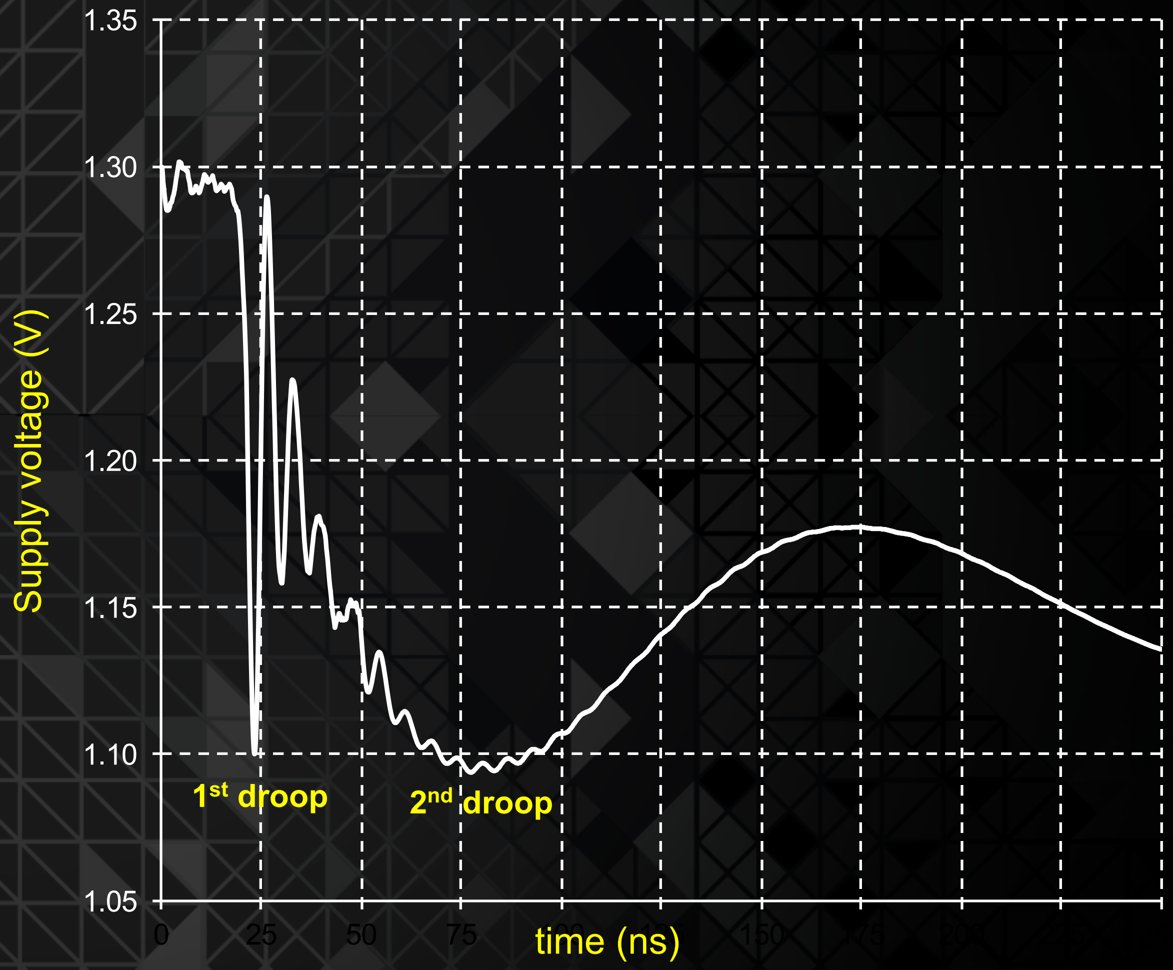




FOR ALL PRODUCTS: AC POWER SUPPLY NOISE IS AN ISSUE

INDUCED THROUGH HIGH CURRENT TRANSIENTS

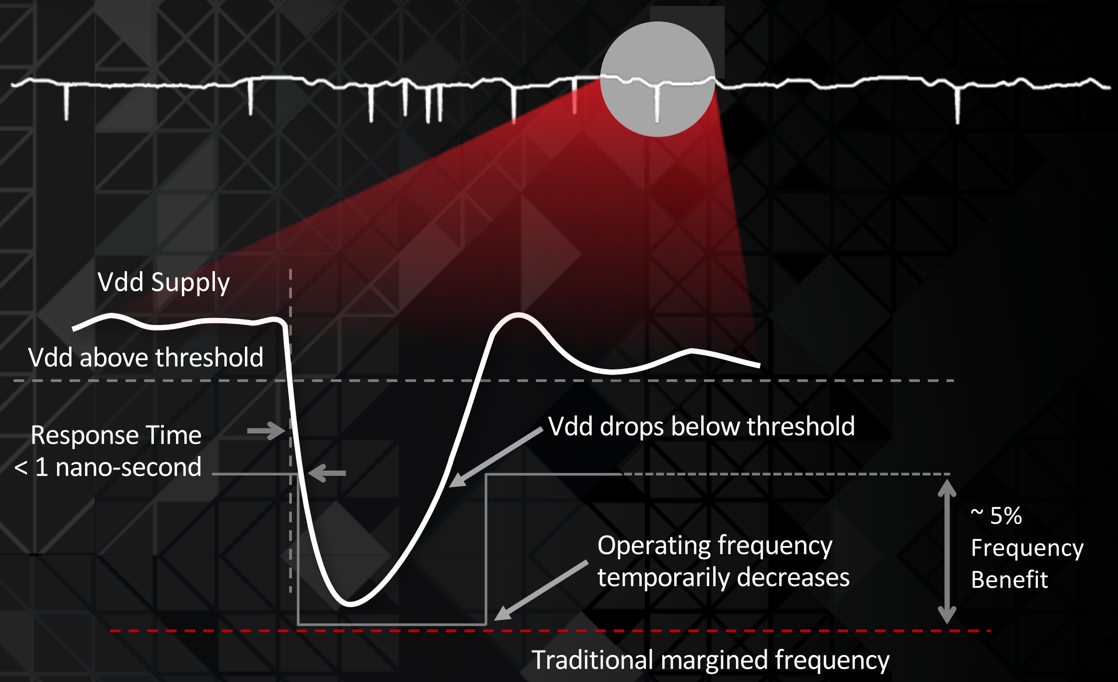
- CPUs, GPUs and APUs all operate at low voltages with high current – this creates a challenge for power supplies and packages to delivery a quality voltage
  - In this example the first droop has rung out prior to the trough of the second droop
  - However, workloads can exist which overlap the frequencies leading to an even larger drop in voltage
- It is costly to provide perfect power supply decoupling: have to make trade-offs
- The situation gets worse each generation
  - Finer power supply partitioning
  - More aggressive stuttering behavior
  - Reduced on-die decoupling capacitance with scaling
  - Improved fine grain clock gating

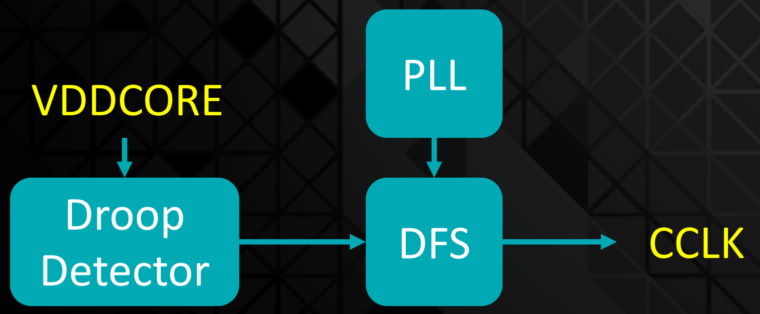


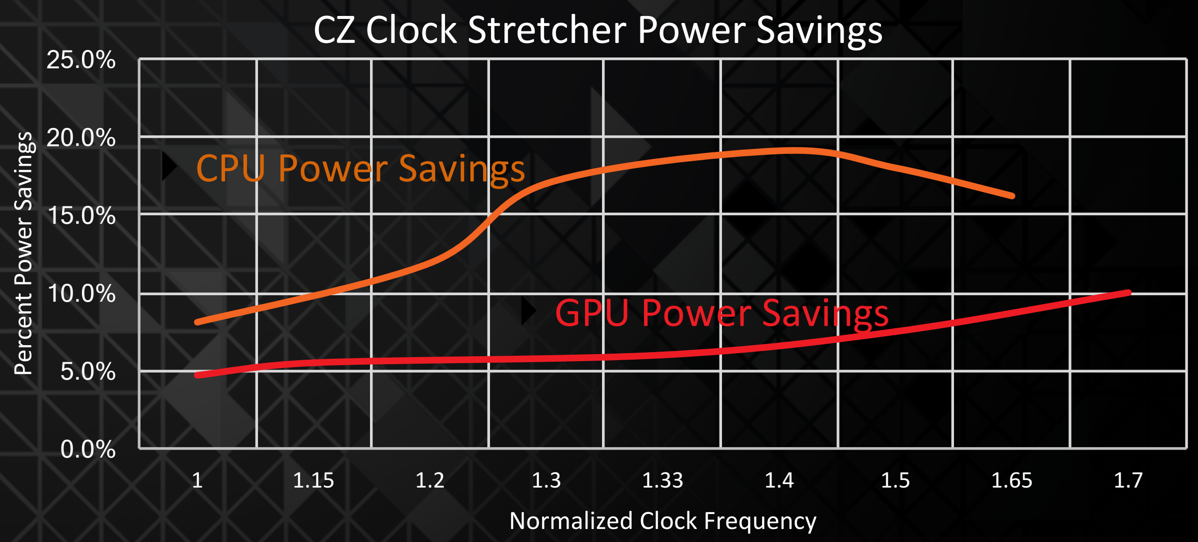
AMD'S CLOCK STRETCHER

ADAPT CLOCK FREQUENCY TO IN RESPONSE TO VOLTAGE DROOPS

- Detect the voltage is dropping
- Immediately slow down the clock so speed paths don't fail due to lower voltage
- Prevents rare events from increasing voltage margin
  - Typically see largest droops < 1% of the time
- Doesn't compensate for 100% of droop or eliminate need for good power delivery, but greatly mitigates the impact

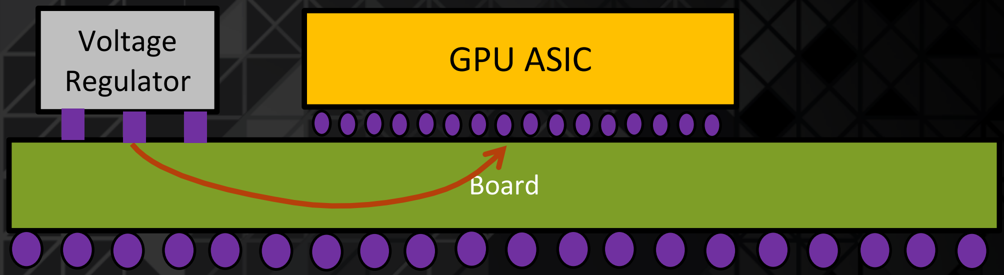


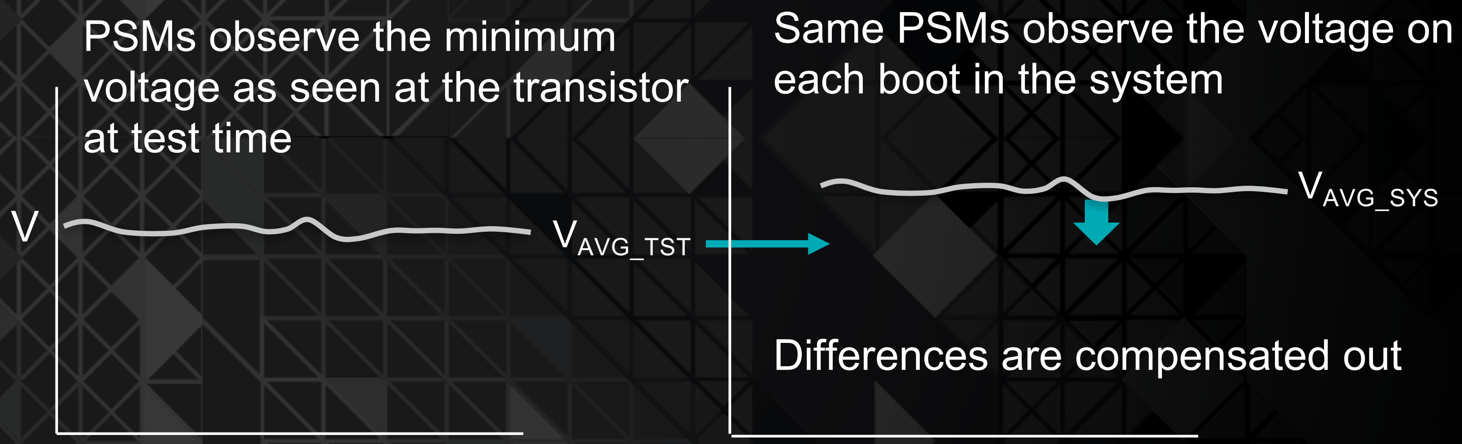




DEALING WITH DC VARIATIONS: BOOT TIME POWER SUPPLY CALIBRATION

- Run voltage analysis code on the tester when the part is tested and binned
  - Log the voltage as seen by the integrated power supply monitors
- On boot-up in whatever system and board the GPU is deployed, run that same code and observe the voltage
  - Dial the regulator to deliver the same AC voltage as observed on the tester for speed binning





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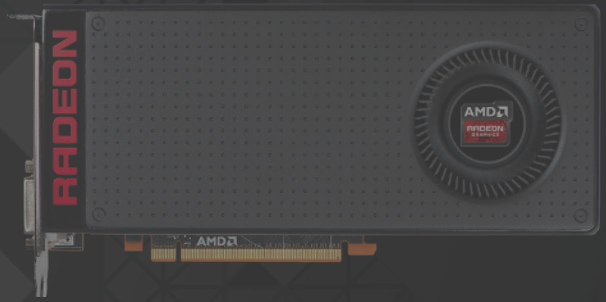
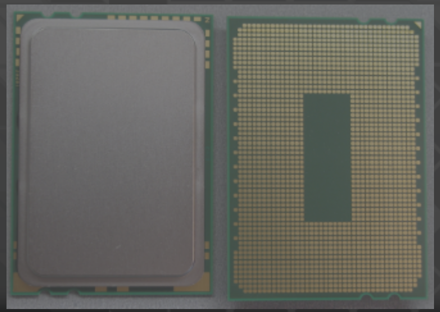
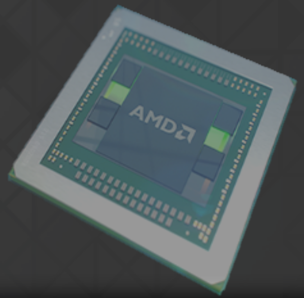


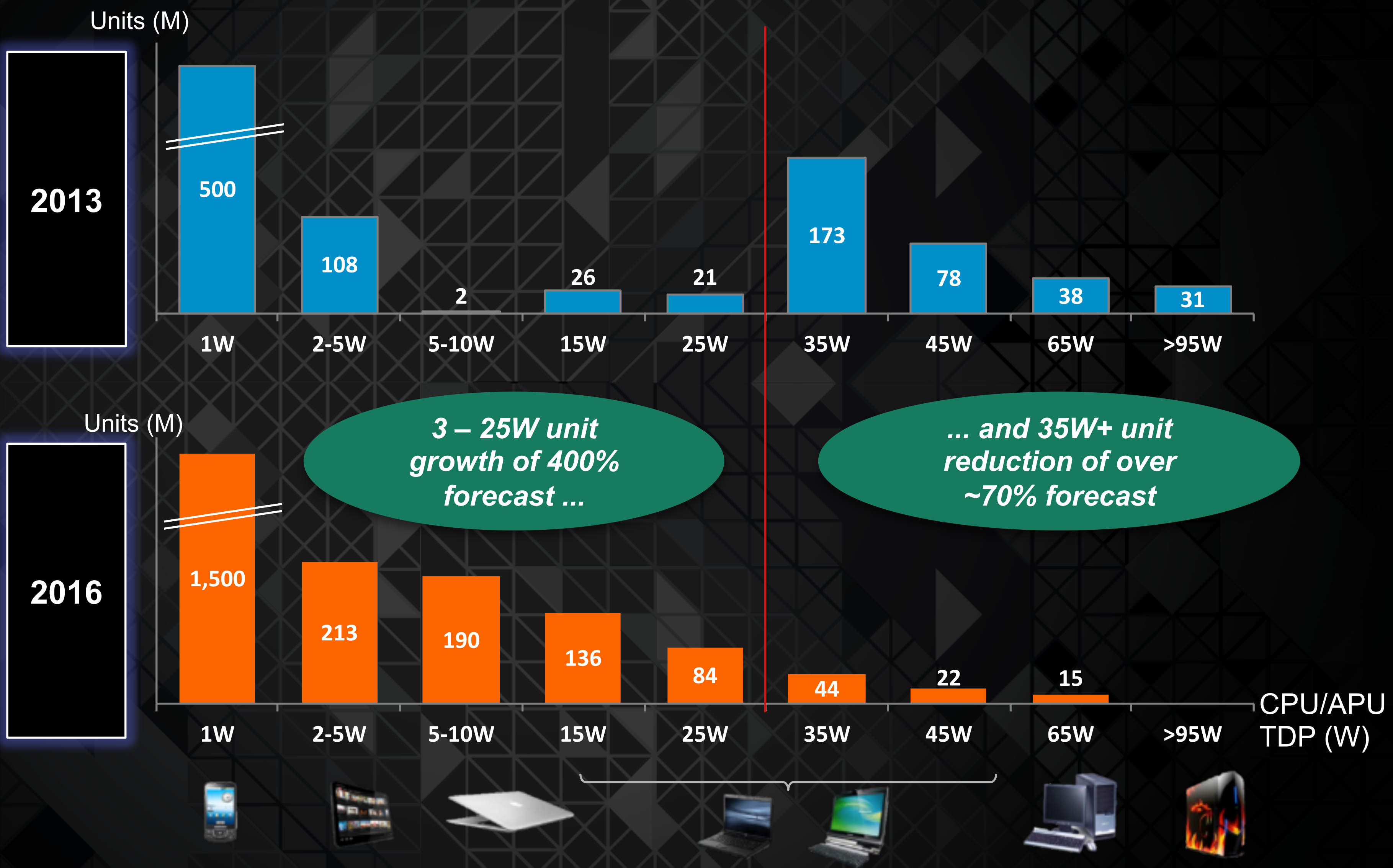




THE IMPORTANCE OF LOW POWER TO CLIENT

Laptop purchaser's #1 concern: Battery life

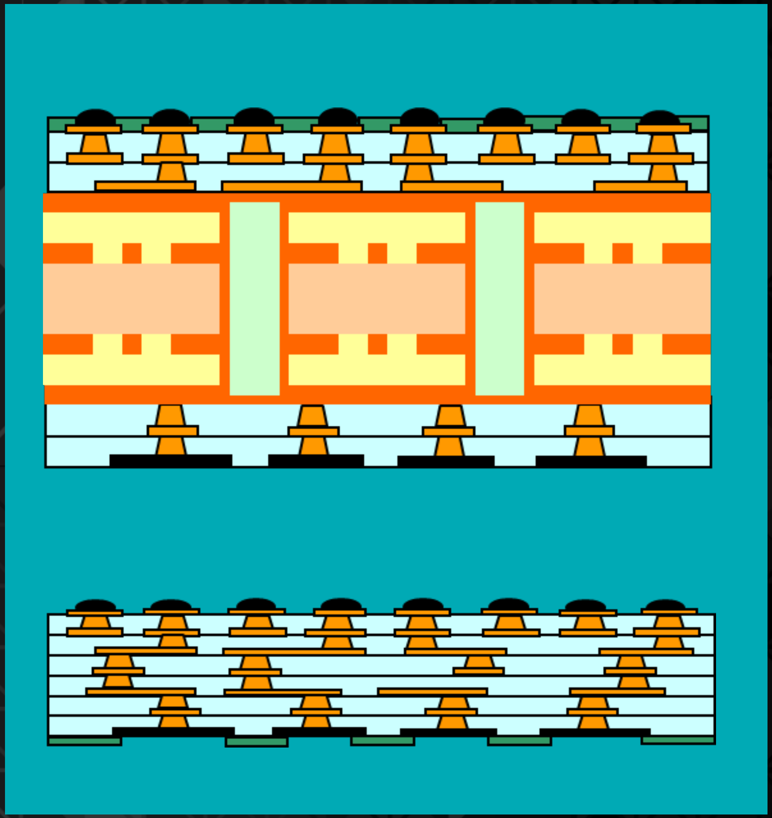
Market consistently moving to thinner, lighter form factors



Source: Mercury, PDCB , AMD LRP

THE RACE TO BE THIN

1.9mm → 1.8mm → Future: <1.3mm



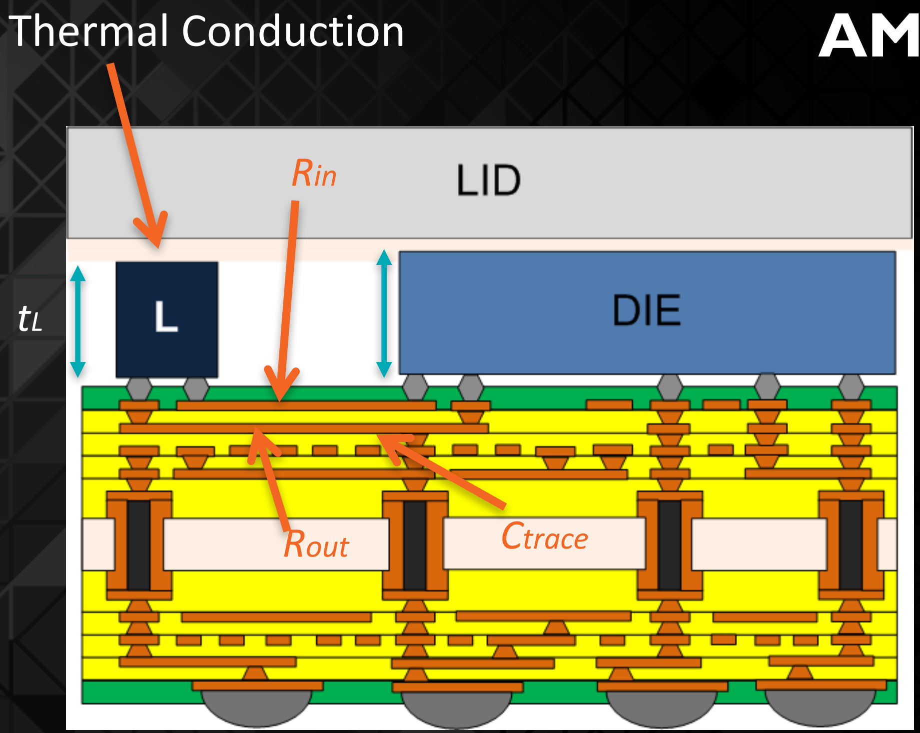
Standard Core

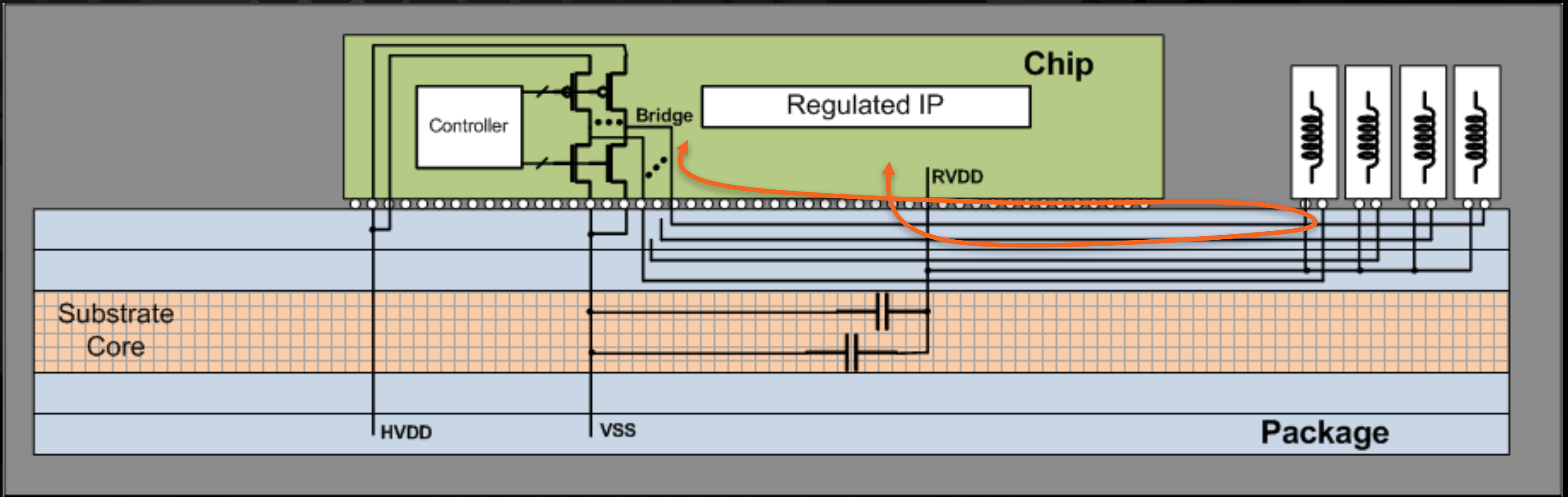
Coreless

- Standard core – 800um thick
- Thin core – 400um thick
- Ultra-thin core – Equal or less than 200um thick
- Coreless – No core (build-up only)

FOR INTEGRATED REGULATION, WE NEED DISCRETE INDUCTORS

- But they are big – at odds with the Z-height reduction
  - Silicon integration a possibility
- Package area is much more expensive than board area → moving power conversion on –package is expensive
- Silicon area is even more expensive than package – difficult to manage the cost of moving power FETs on die





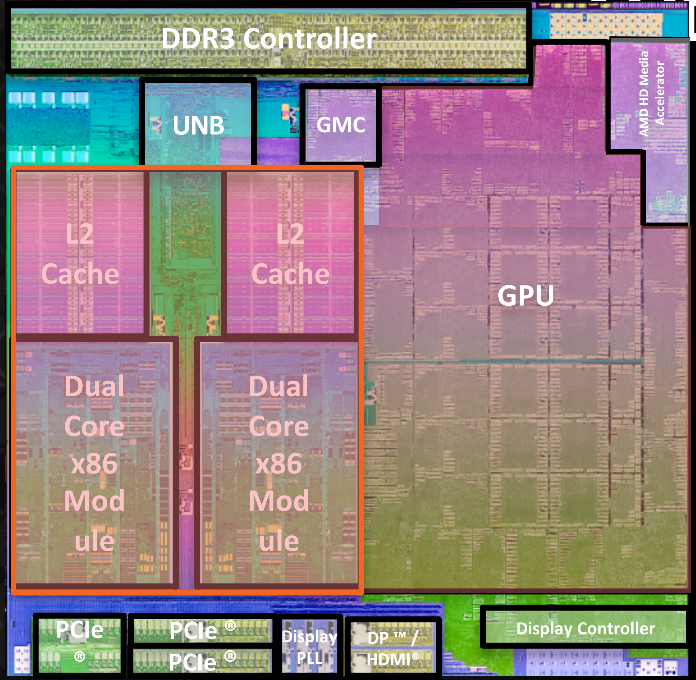
THE MANY RAILS REQUIRED IN LAPTOPS PRESENT CHALLENGES AND OPTIONS

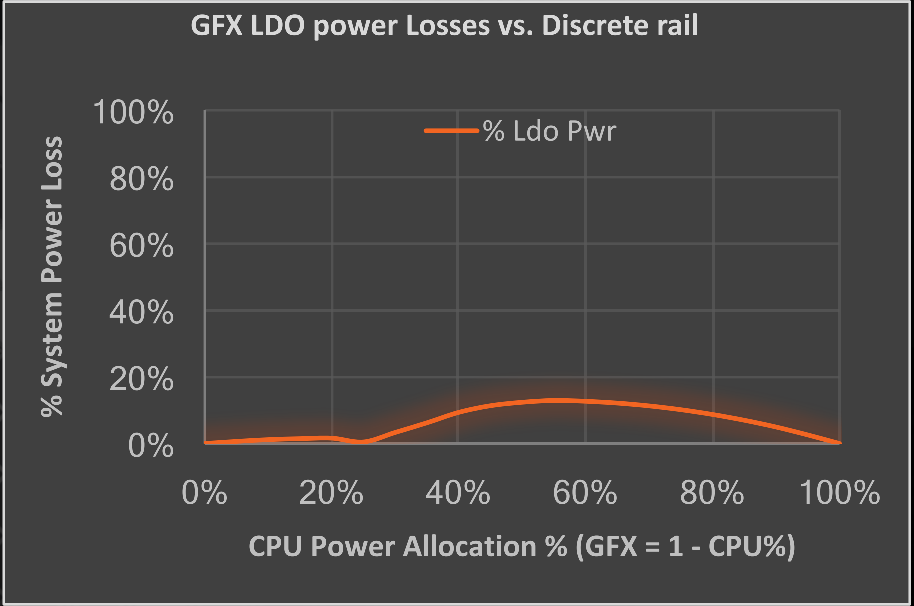
For TDP 35 W Carrizo part

Die Supply Name	Nominal voltage	TDC(A)
VDDCR_CPU	Variable .7V-1.5V	40
VDDCR_GFX	Variable .7V – 1.2V	30
VDDCR_NB	Variable .7V-1.2V	12
VDDCR_FCH	0.8	0.2
	1.5	3
VDDIO_MEM_S3	1.35	2.9
	1.25	2.8
VDDP	1.05	7
	0.95	7
VDDP_GFX	1.05	1.5
	0.95	1.5
VDDP_S5	1.05	0.8
	0.95	0.8
VDD_18	1.8	1.5
VDD_18_S5	1.8	0.5
VDD_33	3.3	0.2
VDD_33_S5	3.3	0.2
	1.8	0.2
VDD_AUDIO	1.5	0.2
VDDBT_RTC_G	1.8	4uA

Could combine high current rails

Can be discrete or aggregated into a Power Management IC (PMIC) on-board

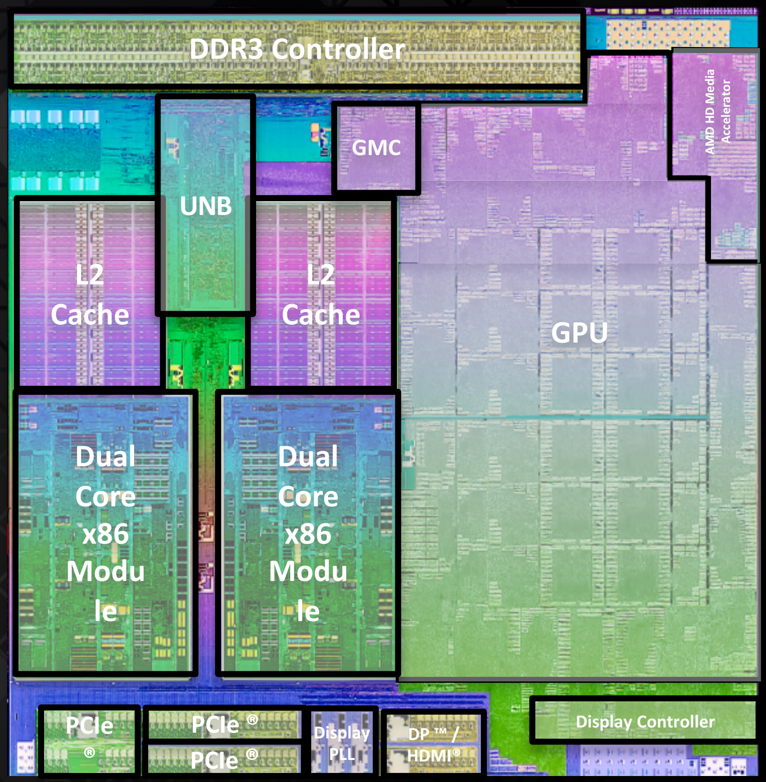




LAPTOP PRODUCT POWER INTEGRATION

CONCLUSIONS

- The trend is to low power so massive currents are not a motivator for integration
- Constant pressure on costs
  - Can’t increase silicon area or package area unless there are other substantial competitive advantages
- Z-height reductions to support thin form factors is a very high priority
  - Discrete inductors not viable
  - Silicon-integrated a possibility within cost constraints
- LDO’s can be used judiciously to reduce rail counts and costs



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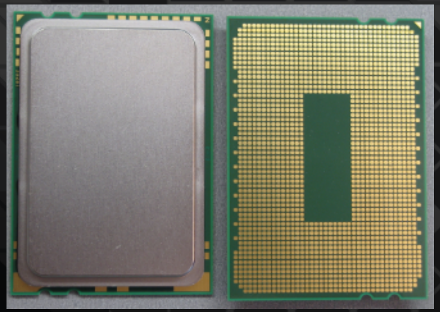

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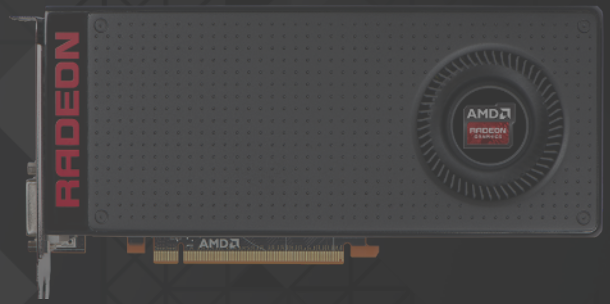
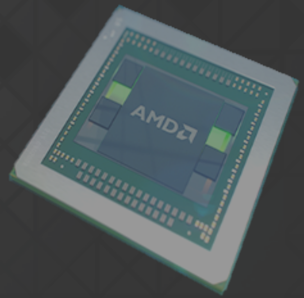
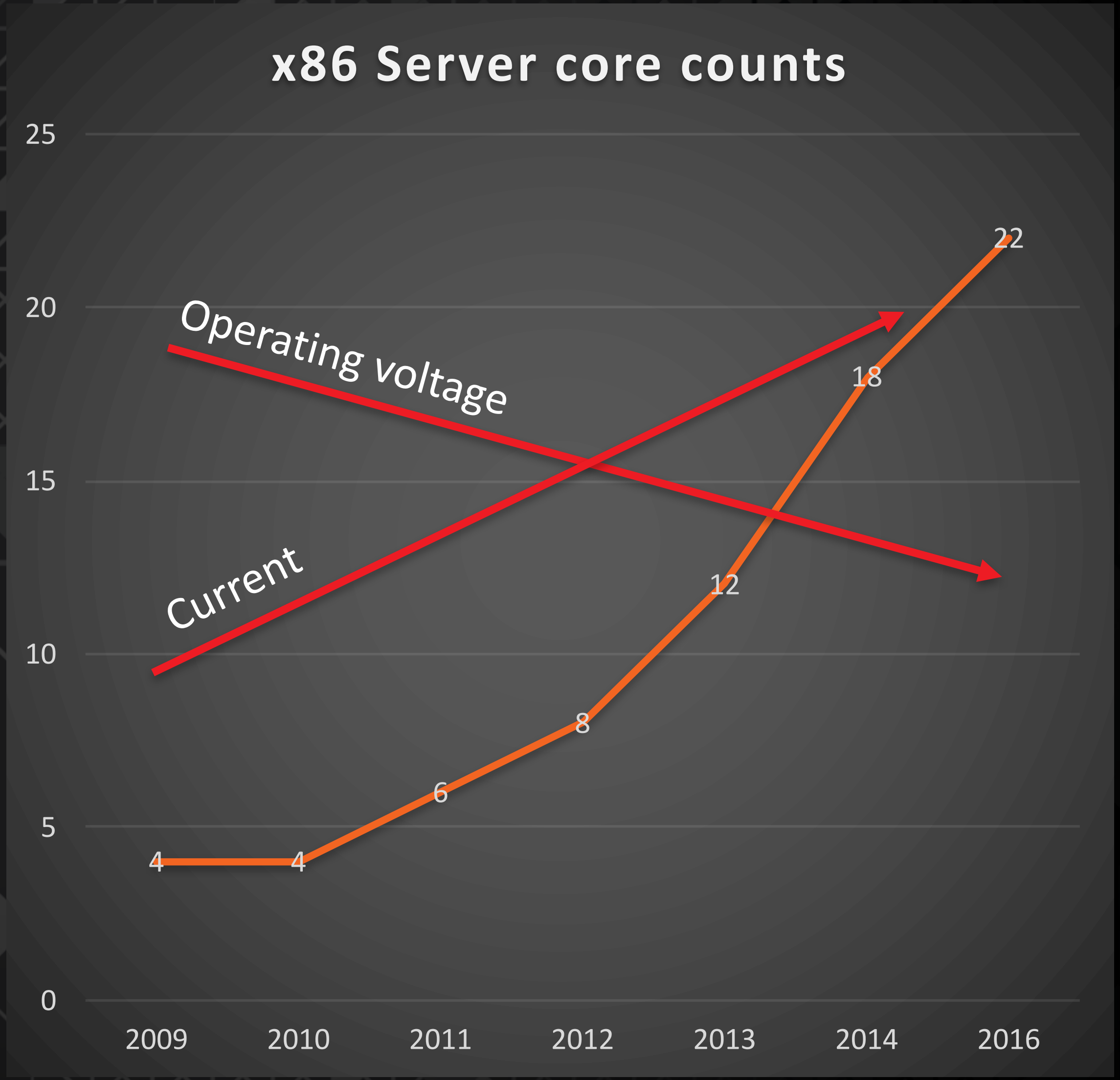




SERVER POWER DELIVERY

KEY POINTS

- The critical things are:
  - High efficiency – customers base purchase decisions on TCO which has a strong power component
  - Manage thermals – cooling is expensive
  - Support high currents – both process and performance trends are pushing currents much higher
  - Cost is still important – pricing pressure from the cloud and competition



PROCESSOR ELECTRICAL SPECS

A COUPLE OF DEFINITIONS

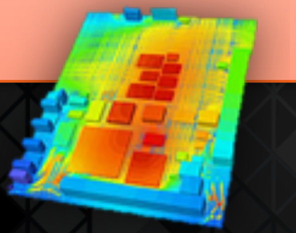
TDC: Thermal Design Current

a.k.a. Continuous Current

a.k.a. Max Continuous Current

a.k.a. Thermal Current

Amount of electrical current voltage regulator must supply and be thermally viable.



EDC: Electrical Design Current

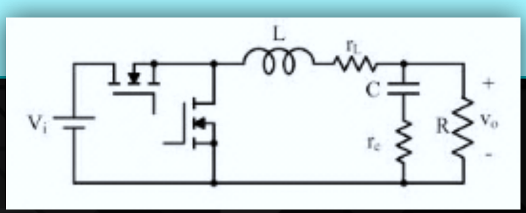
a.k.a. Peak Current

a.k.a. Max Current

a.k.a. Max Instantaneous Current

a.k.a. Imax

Amount of electrical current voltage regulator must supply without caring for thermals.



The EDC/TDC ratio is a function of maximum activity versus “typical” activity ➔ This is steadily increasing as IPC, core counts and boost frequencies increase

PROCESSOR EDC

INCREASING FASTER THAN TDP OR TDC

AMD

EDC: Electrical Design Current

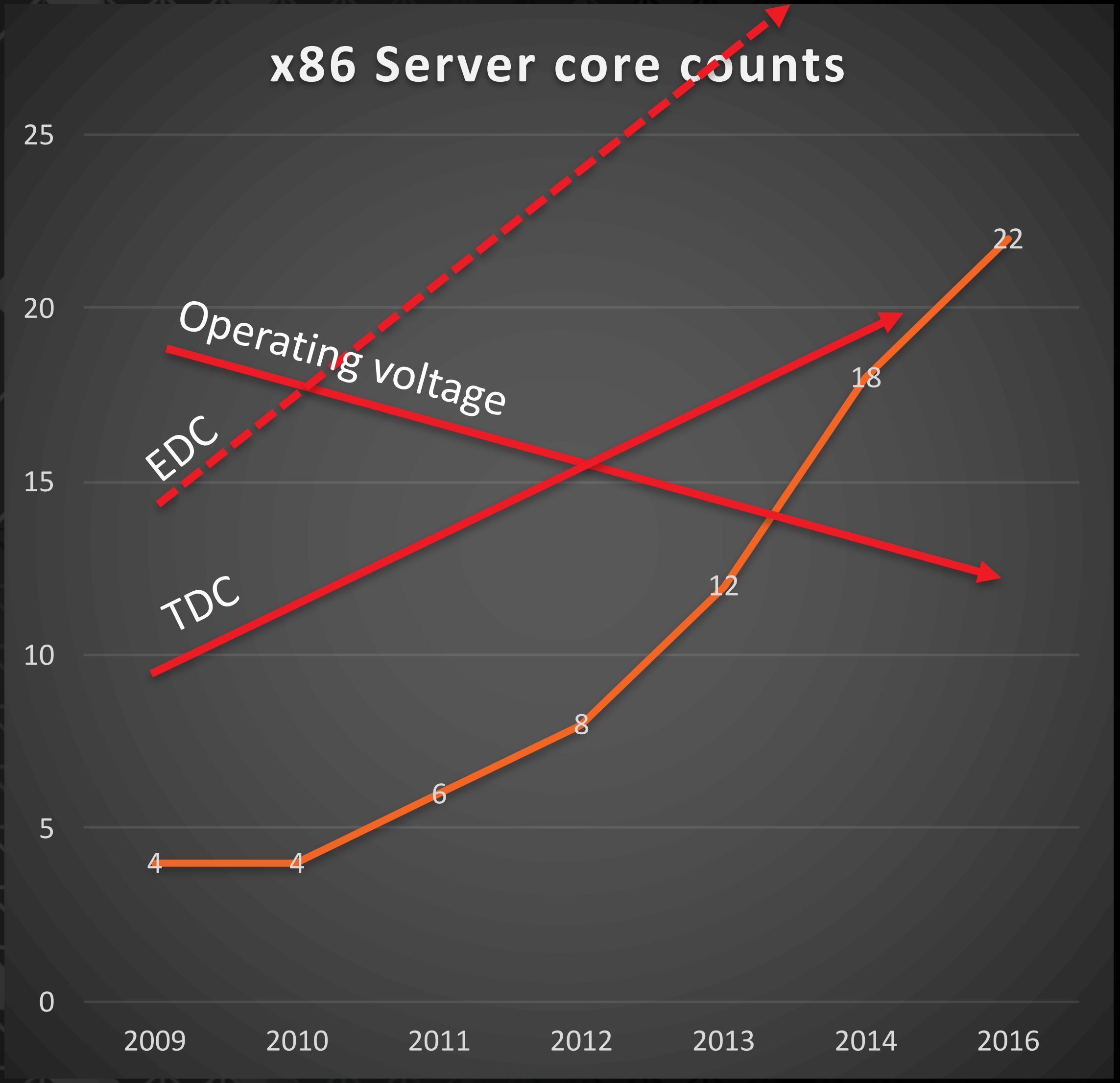
As we become more effective at reducing average power

While adding wider vector instructions and increasing IPC

and running higher frequencies for short term boost

The ratio of EDC to TDC is increasing from what used to be 1.3X to 1.5X and now well beyond that

- EDC is on track to become a first order limiter.
- Mitigations:
  - Reduce operating frequency (bad)
  - Increase phase and inductor counts for VR (expensive)
  - Power management approaches
  - Use IVR to reduce VR currents

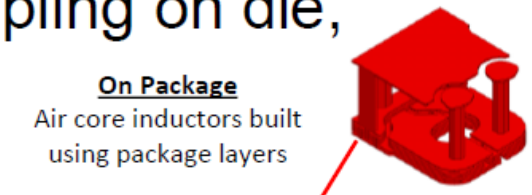


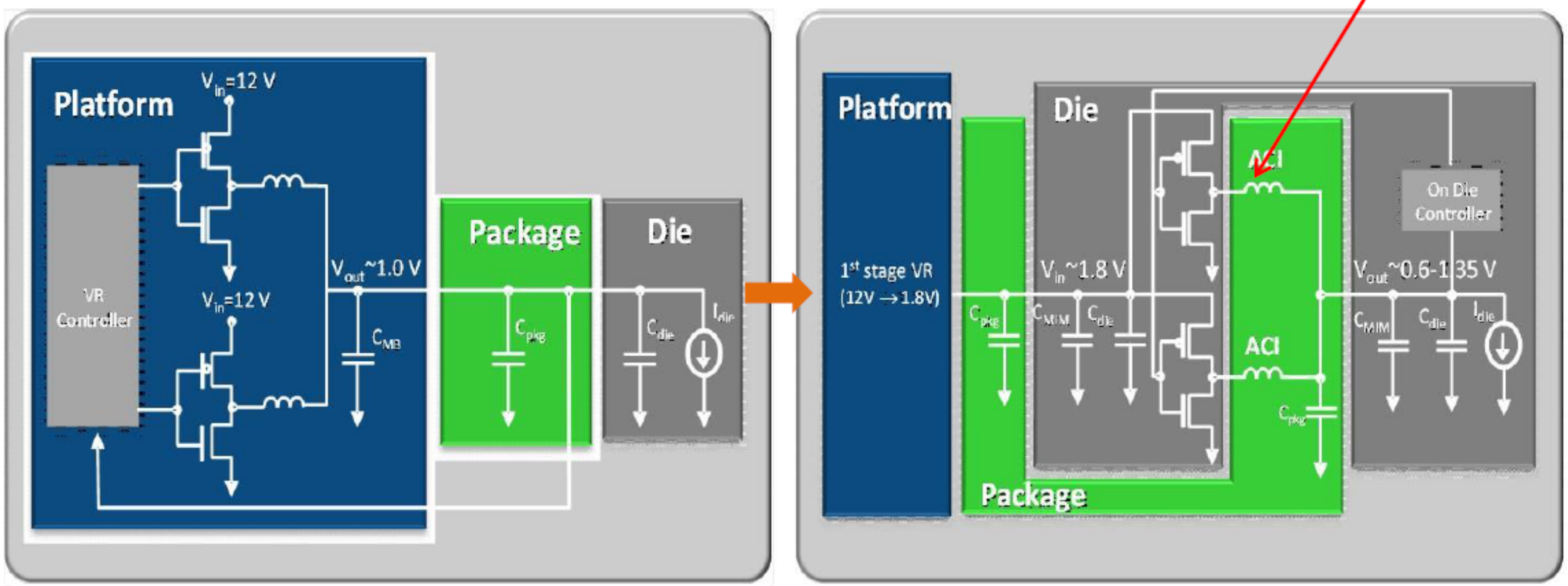
IVR CAN BE A GOOD FIT FOR SERVER

- High currents make package inductors viable
  - Lower cost and area solution

Fully Integrated Voltage Regulators

- FIVR = Fully Integrated Voltage Regulator
- Power delivered to the CPU from a single MBVR at elevated voltage (1.8V) reducing platform power loss
- Power FETs, control circuits and decoupling on die, inductors are on the package

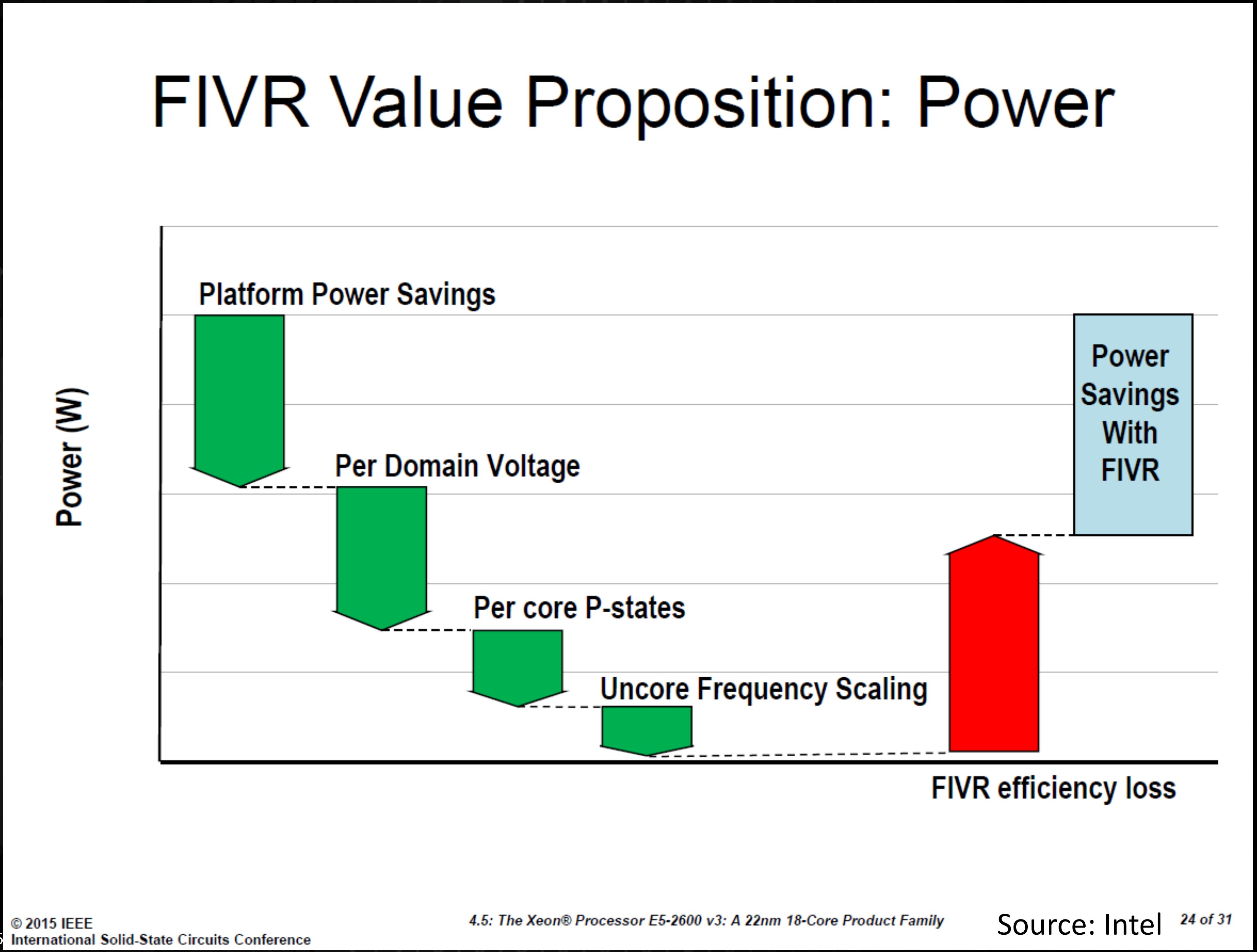




Source: Intel

IVR CAN BE A GOOD FIT FOR SERVER

- Thermal impact *may* be offset by power savings, but is workload dependent
- Impact of power density not accounted for here

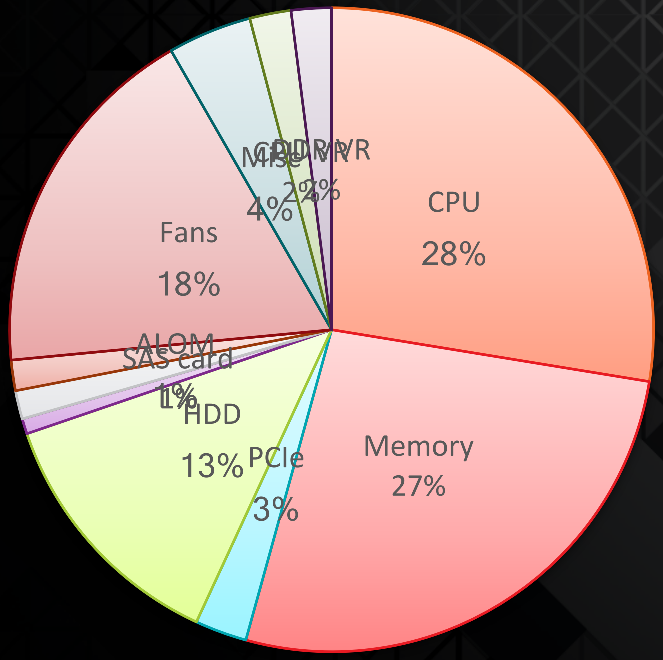


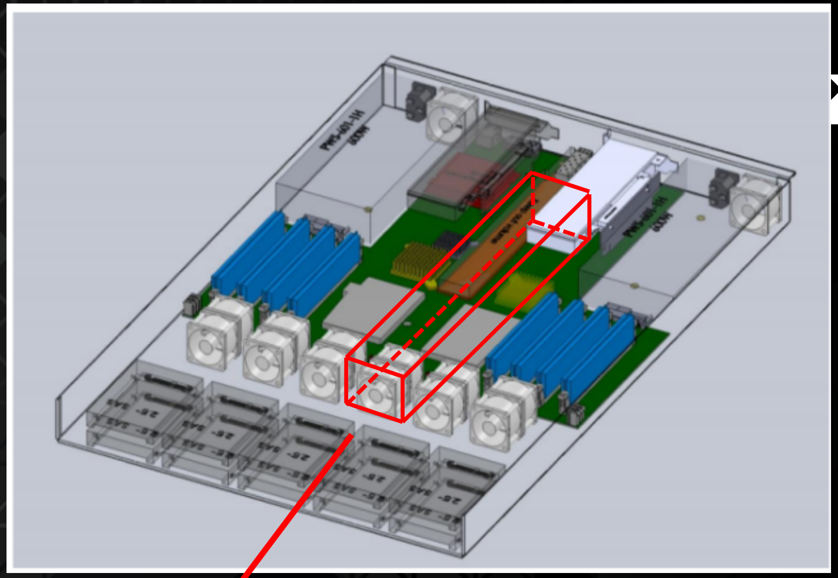
BUT THERMALS ARE VERY CHALLENGING

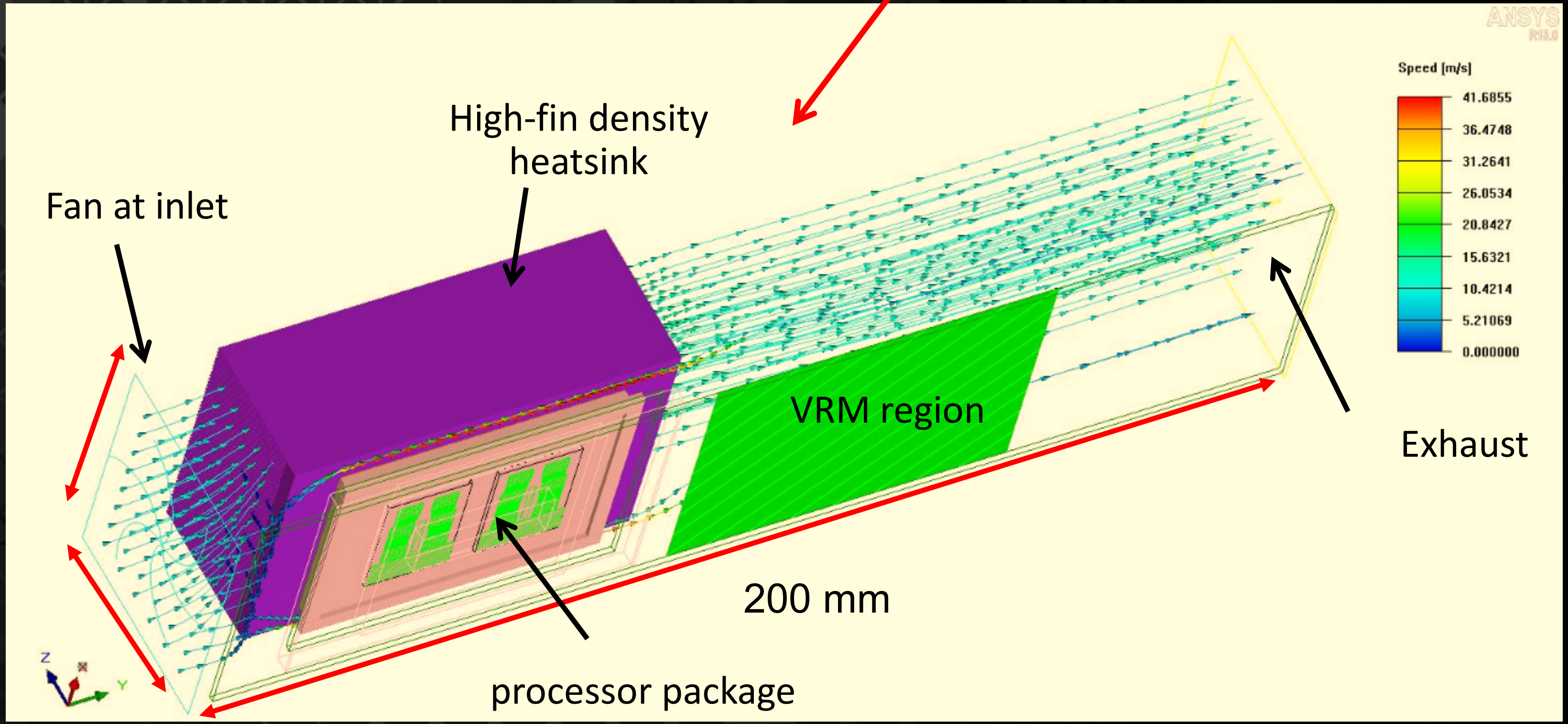
- Server and HPC system are typically thermally limited
- Fans are a large fraction of power and cost

➔ Increasing power density is expensive

Example system power breakdown





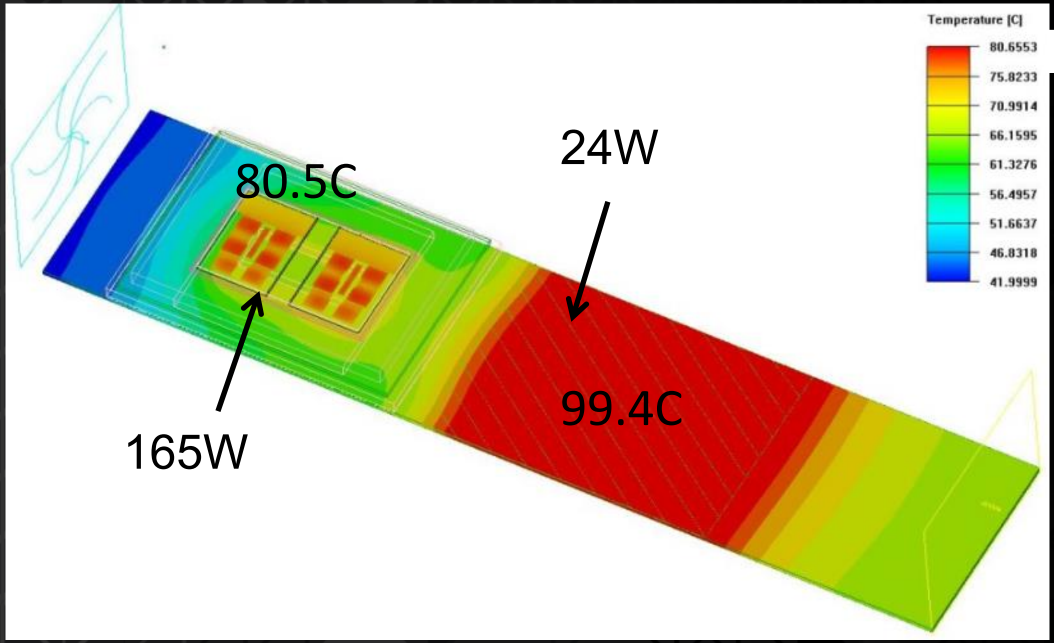


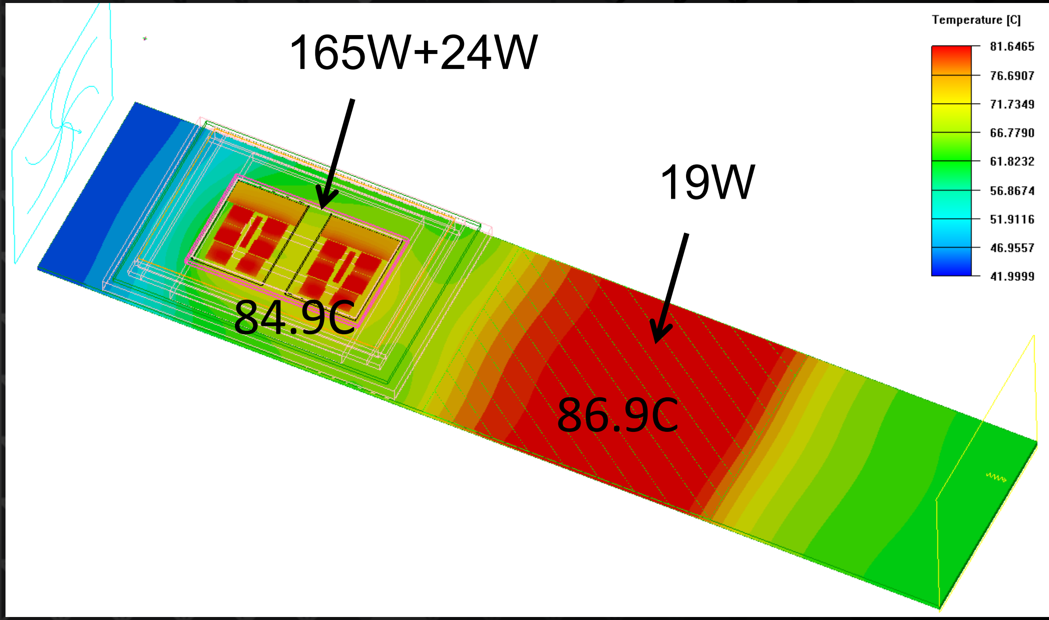
THERMAL SCENARIOS FOR VOLTAGE REGULATION

- Scenario 1: traditional VRM design
  - Per package TDP: 165W
  - VR Power loss: 24W (~87% efficiency)
  - Fan Speed: 30 CFM

- Scenario 2: VRM+IVR
  - Per package TDP: 165W
  - IVR Power loss: 24W (~87% efficiency)
  - Fan Speed: 30 CFM
  - All cores running at full speed (max P-state)
  - Extra heat uniformly distributed

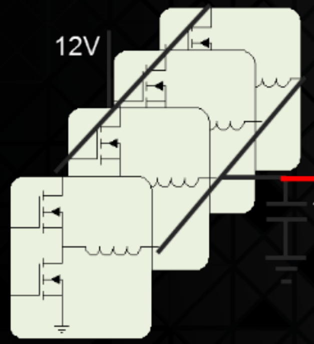
All else equal (i.e. reliability limits, heatsink, fans), the additional 5C for the processor must result in lower power and hence lower performance



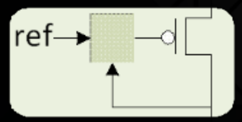


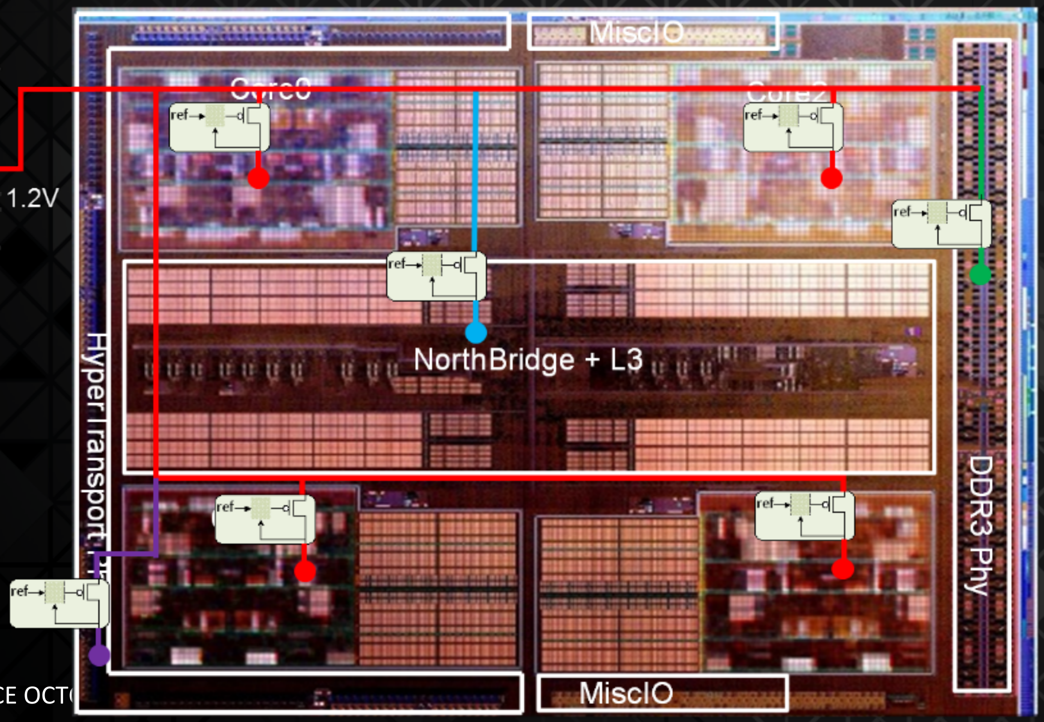
PER-CORE VOLTAGE A KEY IVR SERVER BENEFIT

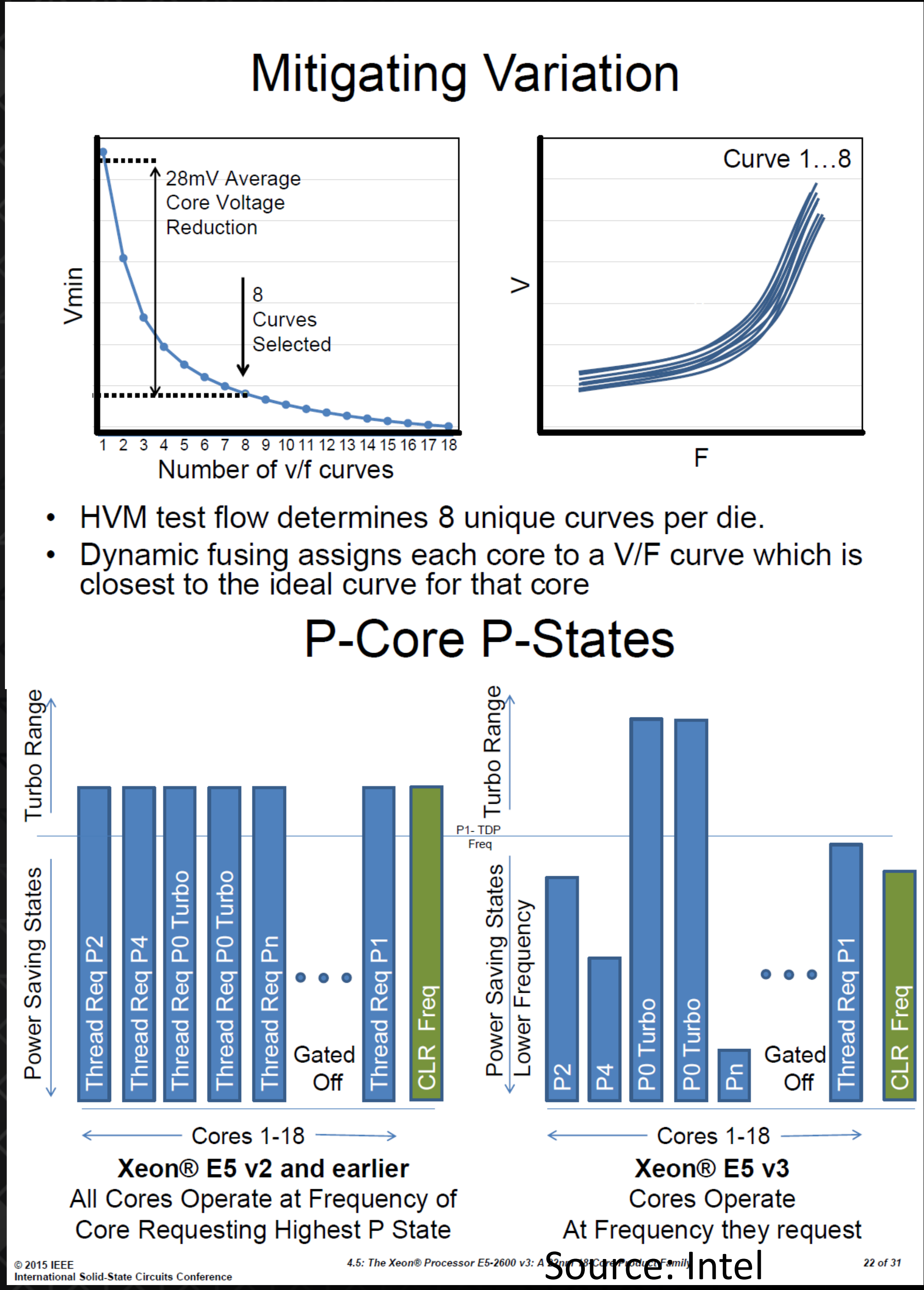
- Variation mitigation
  - 28mV on average ≈ 3% voltage
  - ➔ an LDO is higher efficiency
- Per-core P-states
  - For IVR to be a win over LDO, average drop-out must be >10%
  - Workload dependent and not necessarily the common case
    - System level



LDO CONCEPT



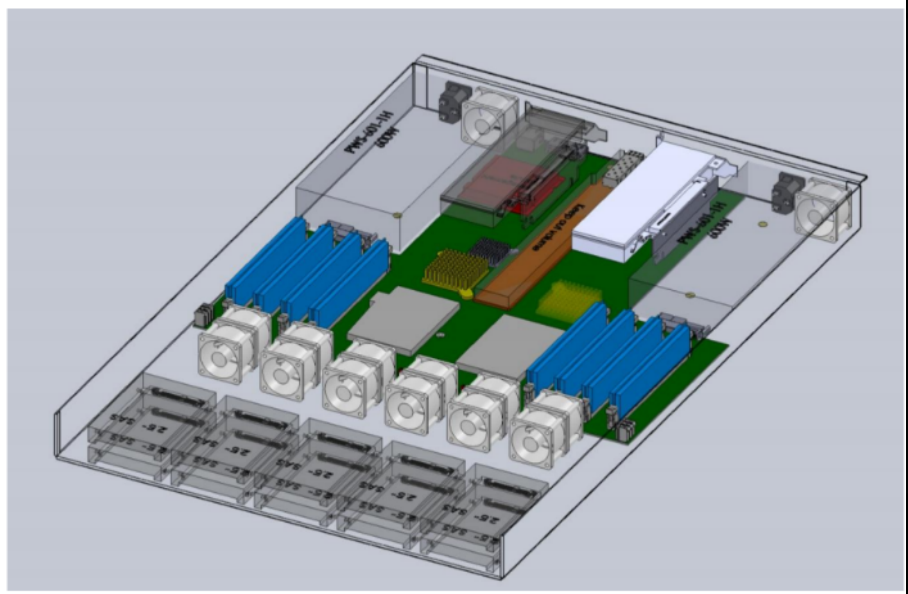




SERVER PRODUCT POWER INTEGRATION

CONCLUSIONS

- Thermal limitations are at the forefront and not easily dealt with
- Currents are increasing rapidly with each generation with max current or EDC, becoming a first order limiter
- Integrated voltage regulation solves some problems but creates new ones
  - Per-core voltage, EDC mitigation, platform BOM reduction
  - LDO’s versus IVR is a tradeoff that needs to be re-examined each generation
  - IVR conversion efficiency is the most important parameter



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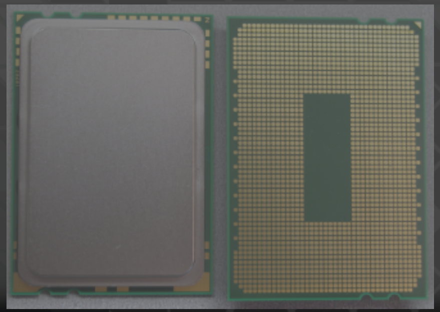
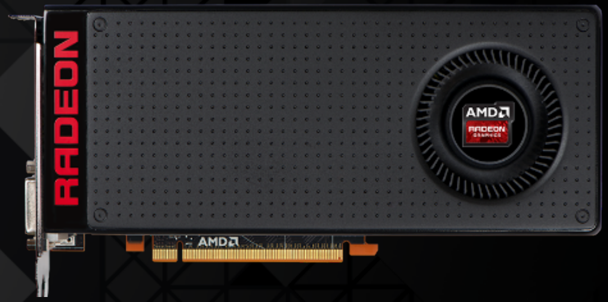
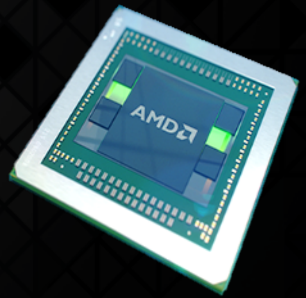


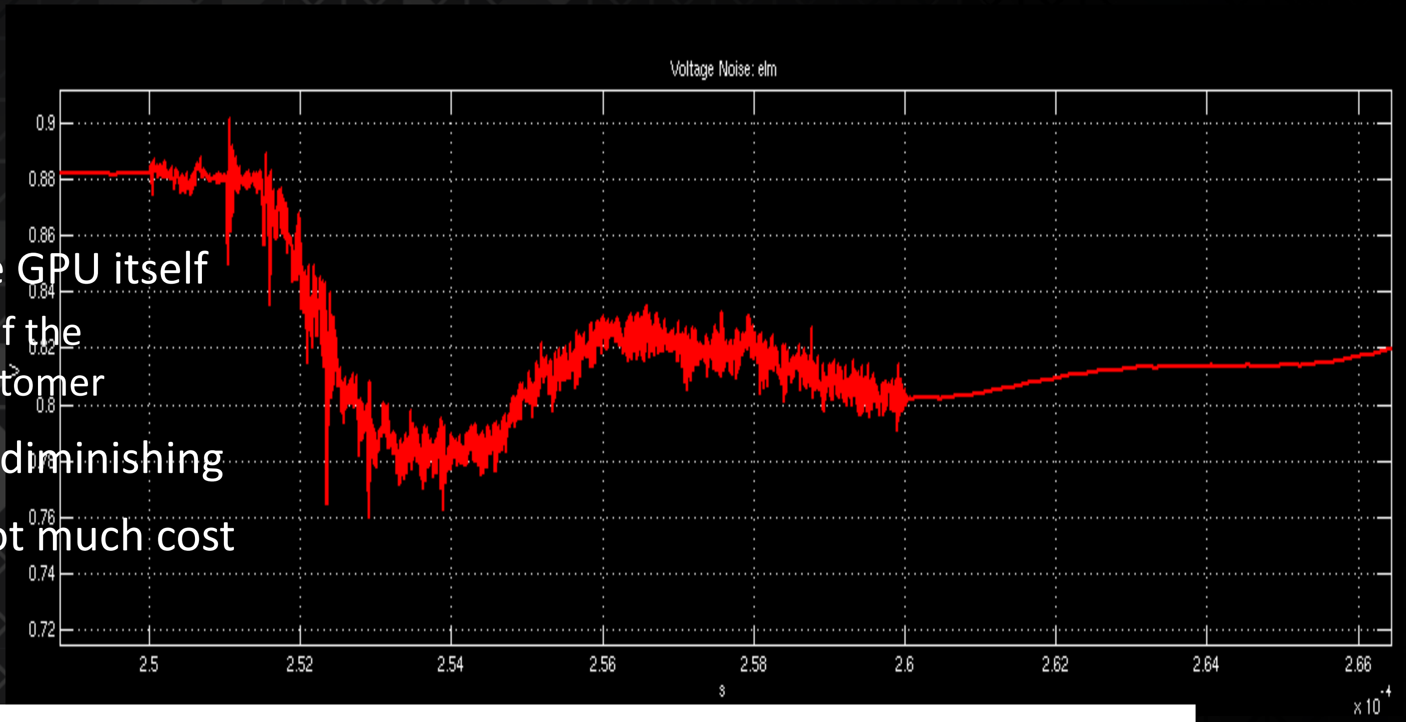


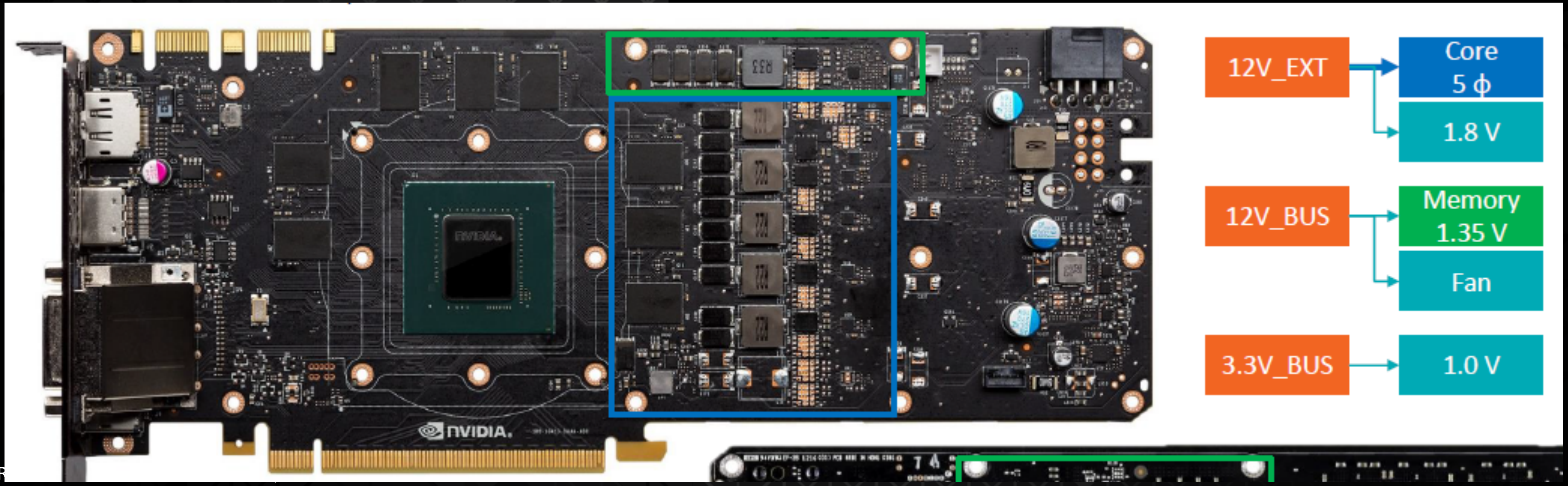


GRAPHICS POWER DELIVERY

KEY POINTS

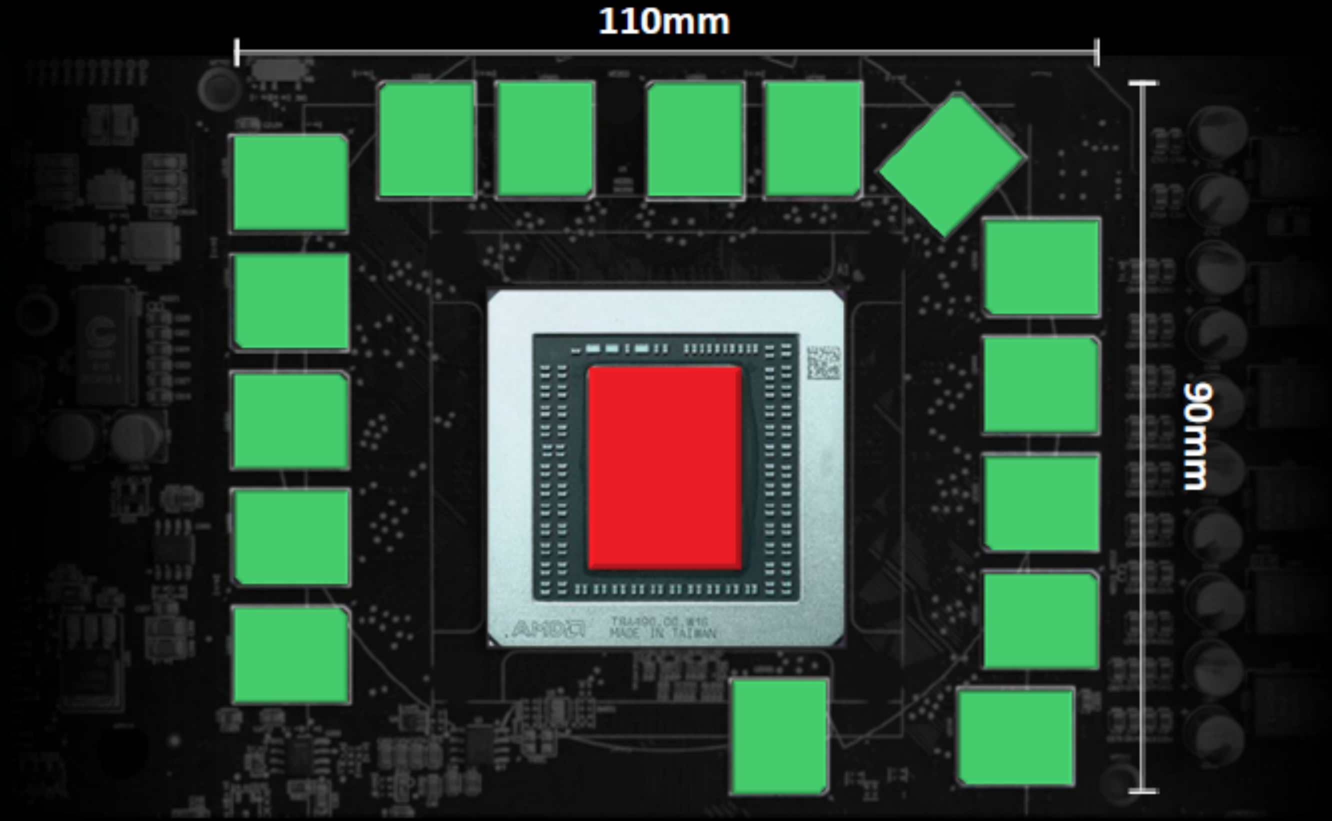
- The final product is the add-in board (AiB), not the GPU itself
  - Power conversion and delivery are the responsibility of the component vendor (i.e. AMD), not the OEM/ODM customer
- TDC and di/dt are very high, and show no signs of diminishing
- Prices are generally fixed by market segment so not much cost flexibility



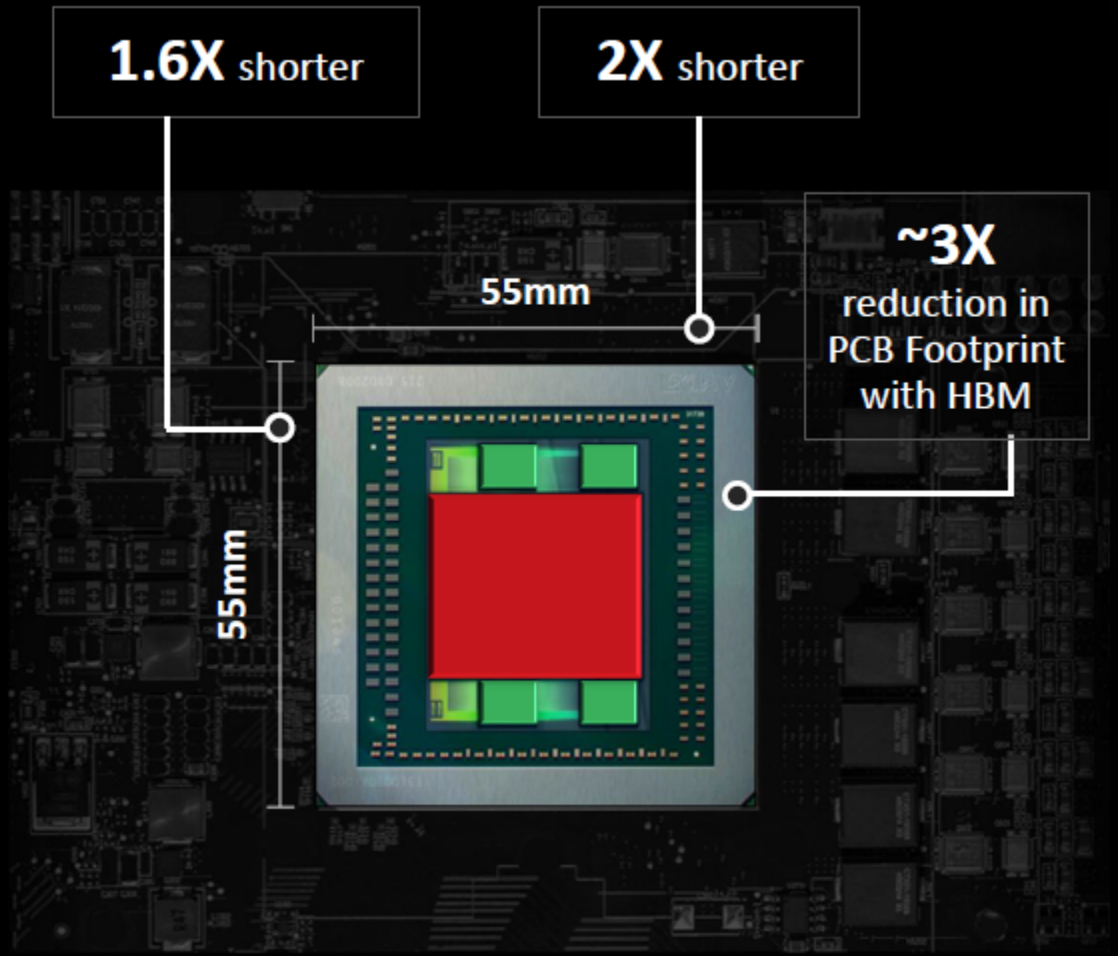


POWER DELIVERY CASE STUDY WITH FURY X

VR'S CAN MOVE CLOSER TO THE LOAD WITH HBM



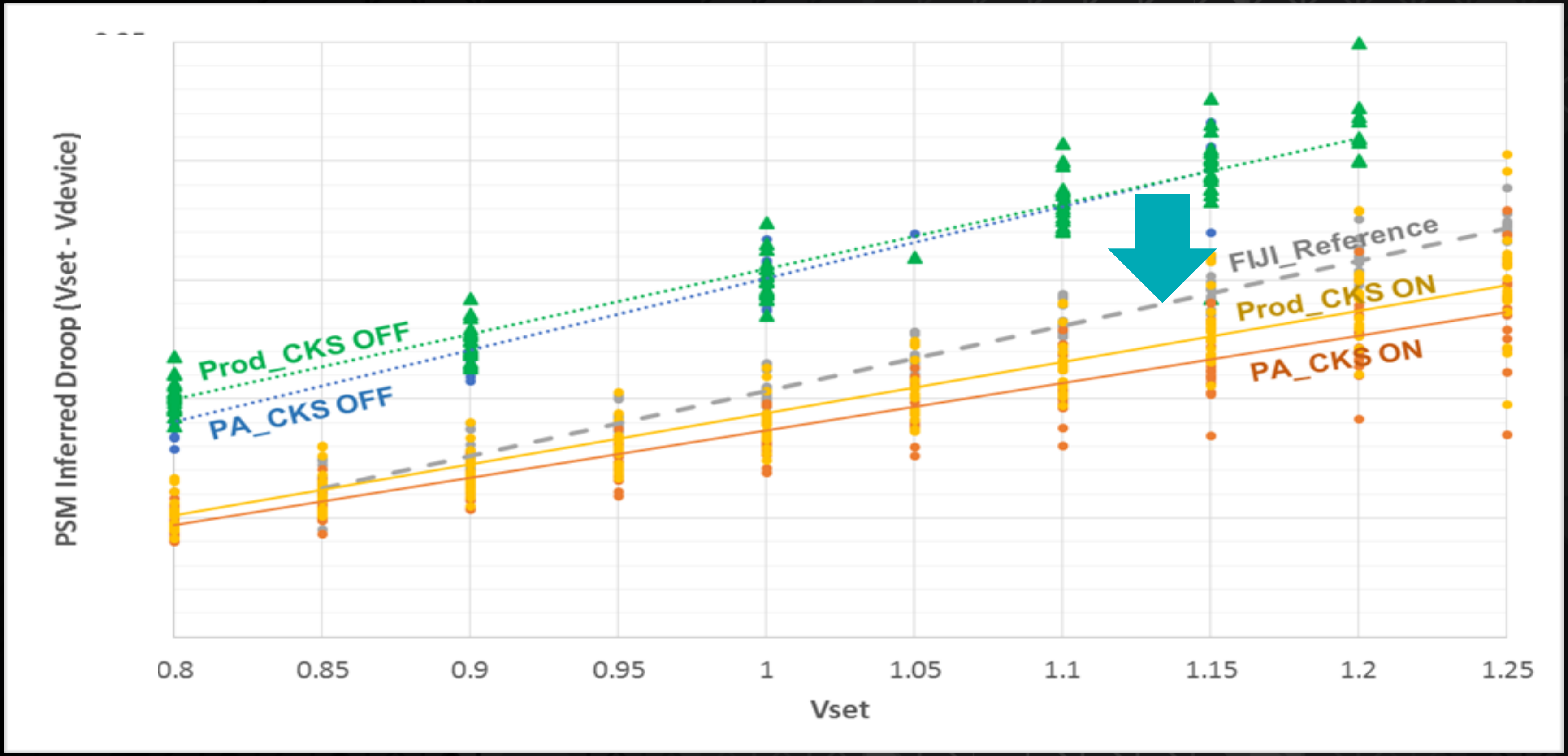
PCB area occupied by ASIC + Memory (Radeon™ R9 290X)

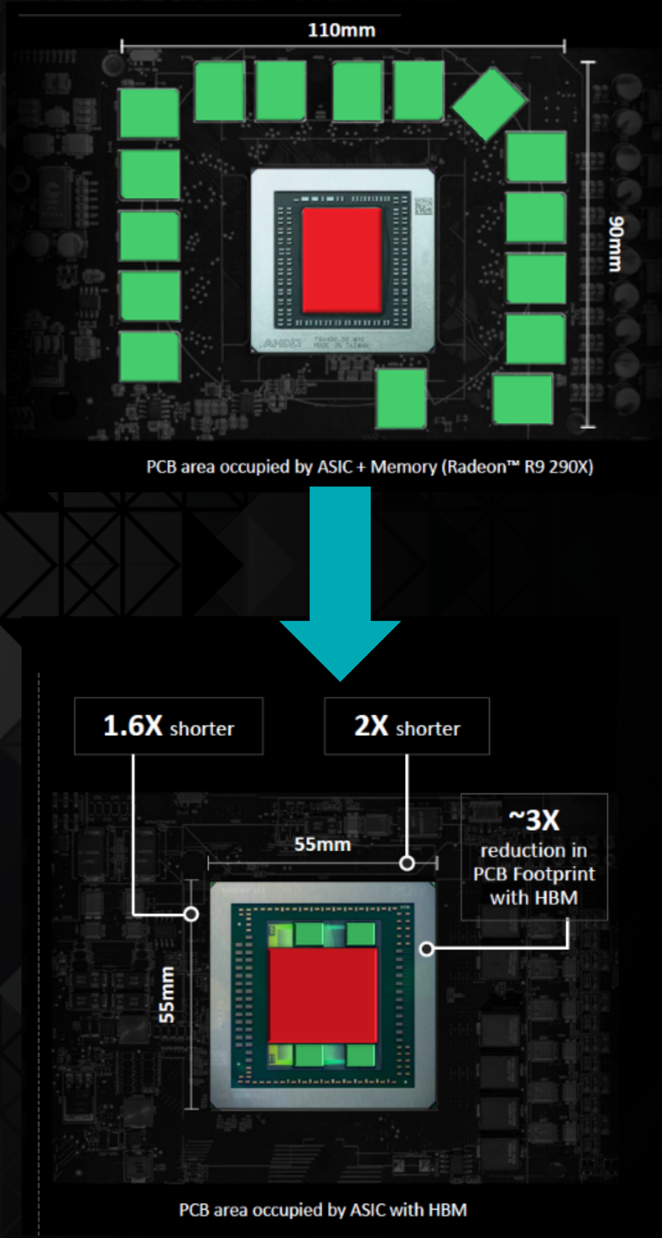


PCB area occupied by ASIC with HBM

VOLTAGE DROOP MEASUREMENTS

ADAPT CLOCK FREQUENCY TO IN RESPONSE TO VOLTAGE DROOPS



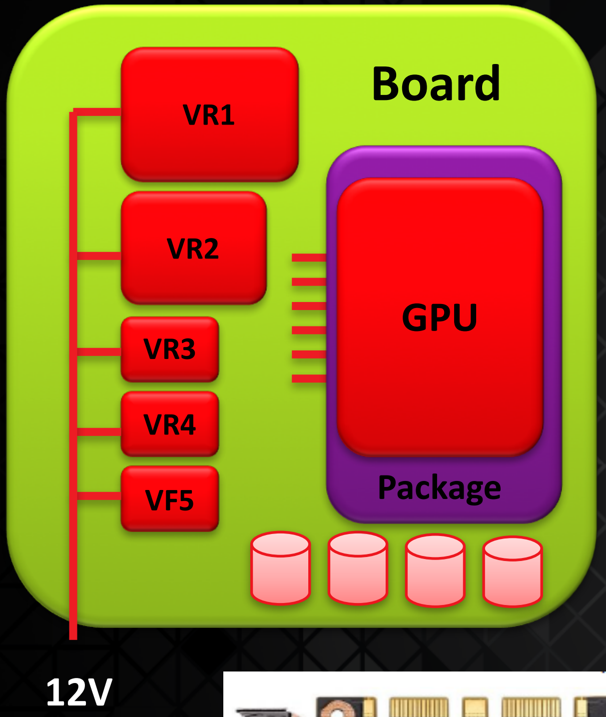


- Clock stretching cuts droop about in half for a traditional memory board
- The HBM board (called Fiji here), has almost the same voltage without clock stretching

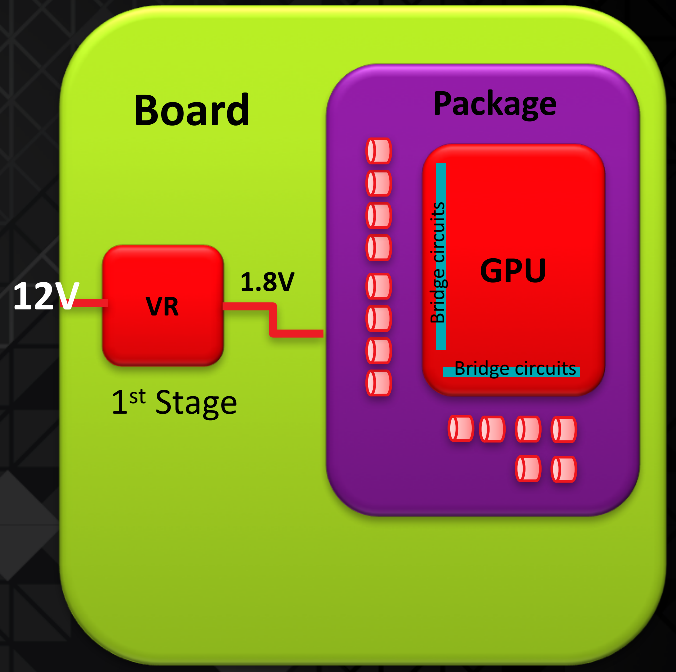
POWER CONVERSION INTEGRATION

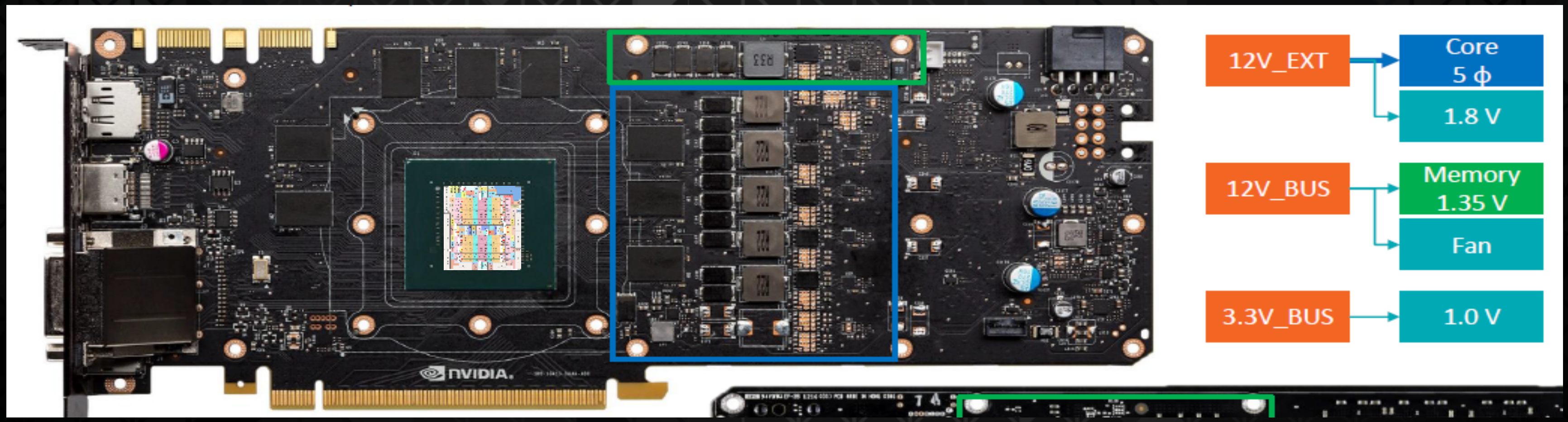
TARGET: IMPROVE AC AND DC VOLTAGE IMPACTS, REDUCE COSTS

Employs package discrete passive components (L, C)



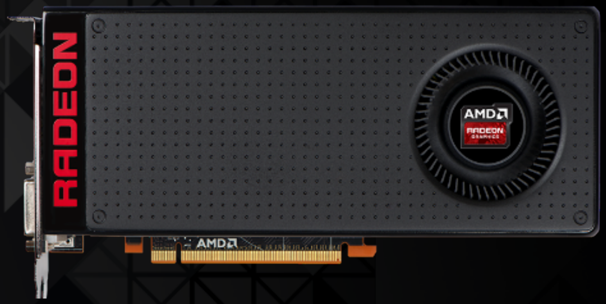
- High frequency switchers can definitely improve AC transients
  - Question is how big the gain is after clock stretching is accounted for
- For cost reduction, we've grown the expensive package and silicon while reducing commodity VRD components
  - Benefit depends on a tight, miniaturized IVR design
  - Increased power density likely to impact cooling solution cost



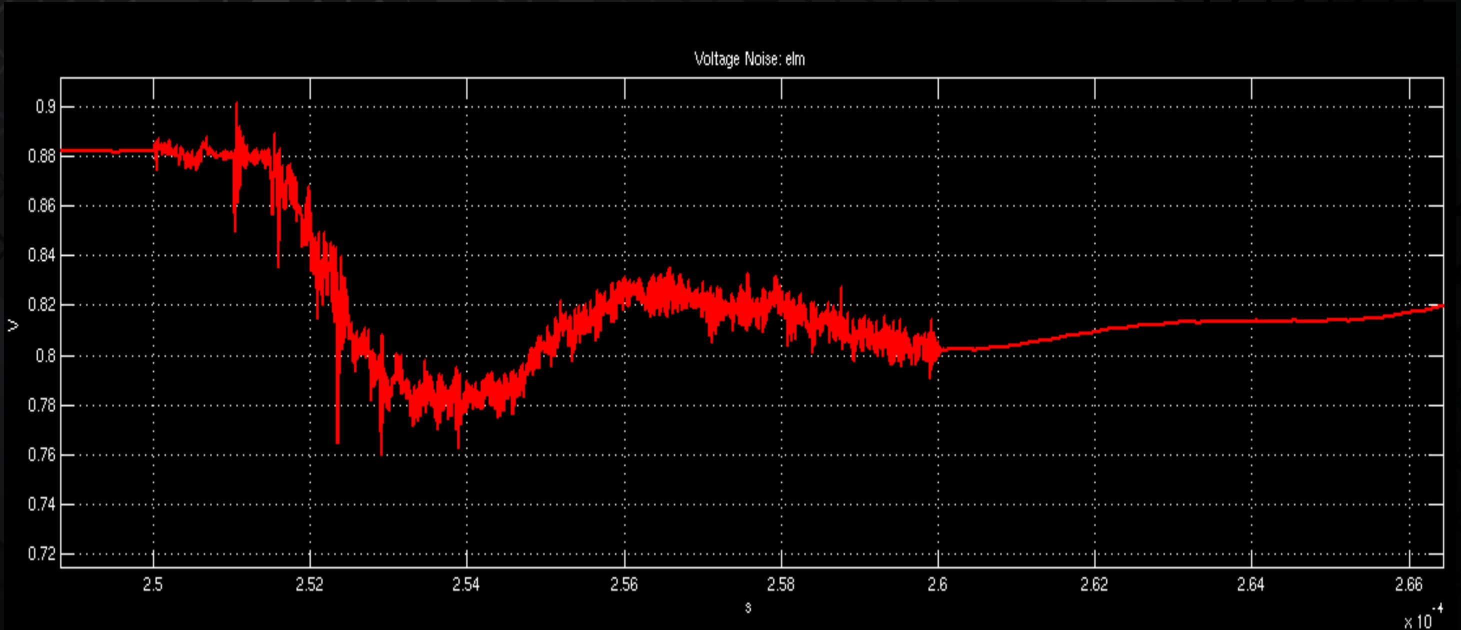


GRAPHICS PRODUCT POWER INTEGRATION

CONCLUSIONS



- Adaptive techniques like clock stretchers and boot time calibration are mitigating AC and DC power delivery losses that would otherwise motivate integration
- Some AC droop impact remains and can be targeted by integration
- BOM cost reduction is another motivator, but the cost equation is challenging, requiring minimal impact to package size and silicon area
  - Reductions in capacitors from better AC response and simplified board design can potentially offset

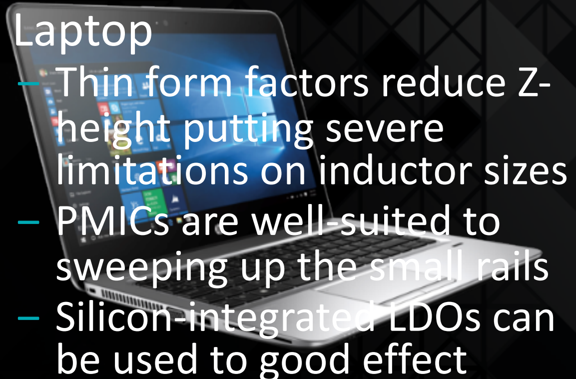


INTEGRATED POWER CONVERSION

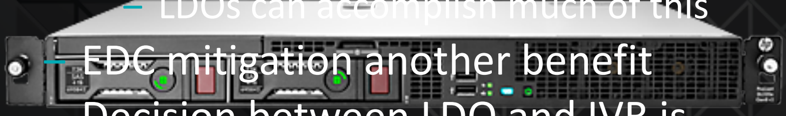
SUMMARY

AMD

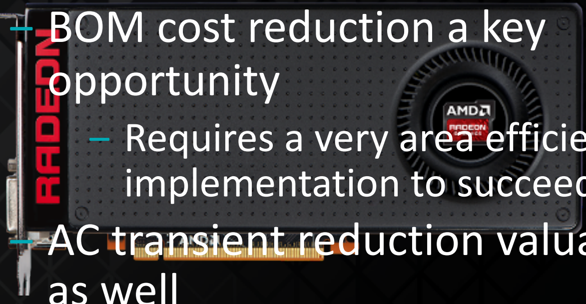
	Product Line Sensitivity			Integration Approach Impact		
IVR benefit / challenge	**Laptop**	**Server**	**Graphics**	**IVR**	**LDO**	**PMIC**
Thermals	Mid	High	Mid	High	Mid-Low	Low
Cost reduction	High	Mid	High	High	Low	Low
EDC mitigation	Mid	High	Mid	High	Low	Low
AC+DC loss mitigation	High	High	High	High	Mid	Low
Per-IP/per-core voltage	High	High	Low	High	High	Mid
Form factor reduction	High	Low	Low	Low	Mid	High



- Laptop
  - Thin form factors reduce Z-height putting severe limitations on inductor sizes
  - PMICs are well-suited to sweeping up the small rails
  - Silicon-integrated LDOs can be used to good effect



- Server
  - Increasing power density impacts thermals
  - Per-core voltage is a key benefit
    - LDOs can accomplish much of this
  - EDC mitigation another benefit
  - Decision between LDO and IVR is very product specific



- Graphics
  - BOM cost reduction a key opportunity
    - Requires a very area efficient implementation to succeed
  - AC transient reduction valuable as well