Monolithic Capacitive Power Converters Towards Higher Voltage Conversion Ratios

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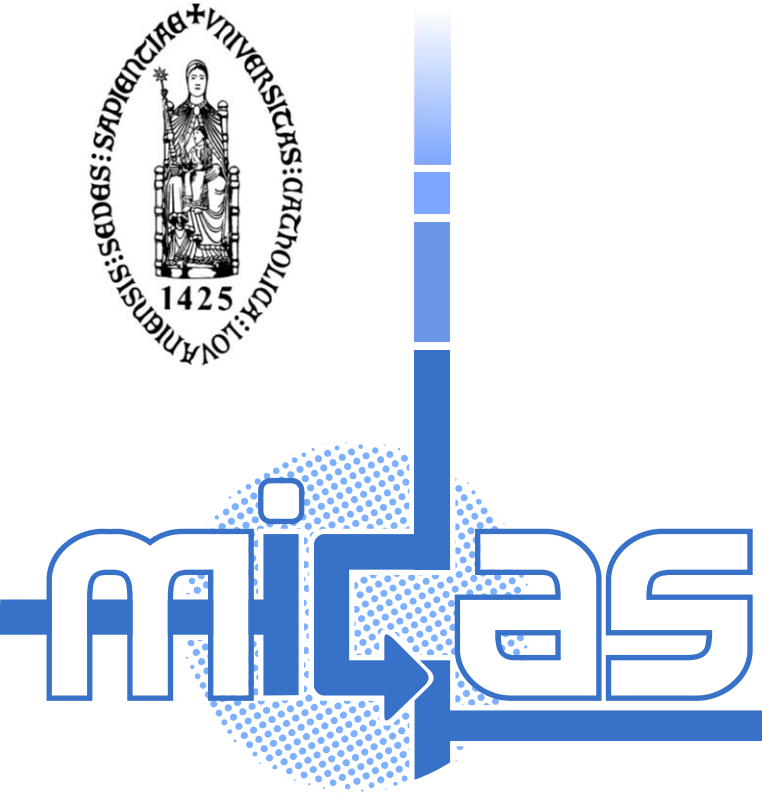

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Overview

- ***Introduction & Motivation***
- Capacitive AC-DC Step-Down Approach
- High Voltage Conversion Ratio DC-DC Approach
- Conclusions

Problem & Facts

Although **standby power** of individual mains connected appliances is low (<1 W), it represent a **significant fraction of global electricity consumption** due to the large amount of devices

Consumers:

- TV, VCR, Set-top, Stereo
- Computer
- Kitchen appliances
- External power supplies
- Ceiling fans

Consumption:

Annual Domestic Percentage

- France 2000: 7%
- UK 2004: 8%
- Other: up to 13%

Problem & Facts

Although **standby power** of individual mains connected appliances is low (<1 W), it represent a **significant fraction of global electricity consumption** due to the large amount of devices

Consequence:

- Emissions: International Energy Agency attributes 1% of 2007 global CO_2 emissions to vampire power
  - ⇔ 3% CO_2 due global air traffic
  - CO_2 ⇨ Global warming
  - SO_2 ⇨ Acid rain
- Fire risk : Heat dissipation

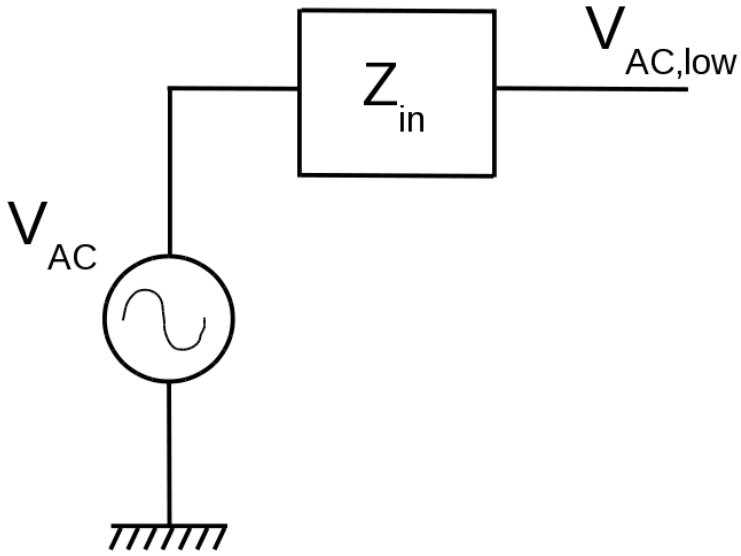
Goal

- Provide low power from the mains with an **auxiliary power supply** enabling a **low loss standby power consumption**
  - Main power supply fully off
  - Low cost
  - Low volume
  - Low input power
  - Optimal power throughput

Large Voltage Conversion Ratio Required

Bridging the voltage gap

1. Series impedance
   - Resistor
     - Very lossy due to high voltage ratio
   - Series capacitor
     - Lossless in ideal case
     - Large impedance as result of low mains frequency
2. Direct mains connection
   - Stacked voltage domains (high VCR / Extensive stacking)



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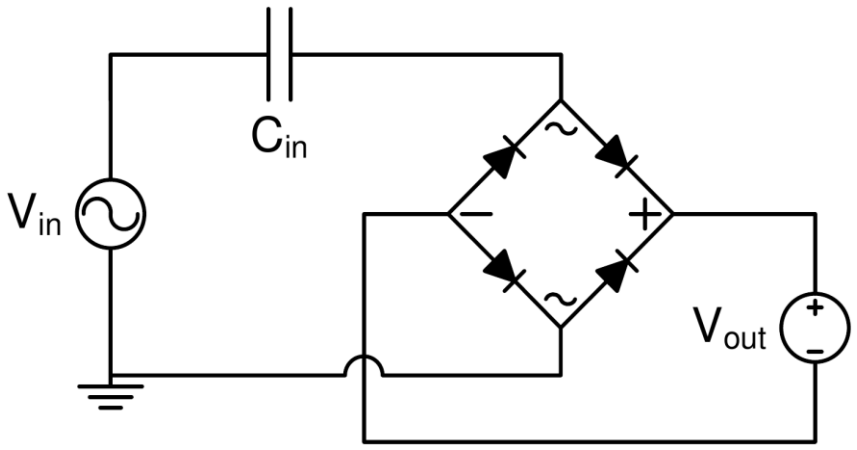
A Capacitive AC-DC Step-Down Converter

- Ideal model
  - $P_{out} = f(V_{out}, C_{in}, f_{mains}, V_{in})$
  - f_{mains}, V_{in} fixed



$$V_{in}(t) = \sqrt{2} V_{in} sin(2\pi f_{mains} t)$$

$$V_{C_{in}}(t) \approx (\sqrt{2} V_{in} - V_{out}) sin(2\pi f_{mains} t)$$

$$i_{C_{in}}(t) = C_{in} \frac{dV_{C_{in}}}{dt}$$

$$= C_{in} (\sqrt{2} V_{in} - V_{out}) cos(2\pi f_{mains} t)$$

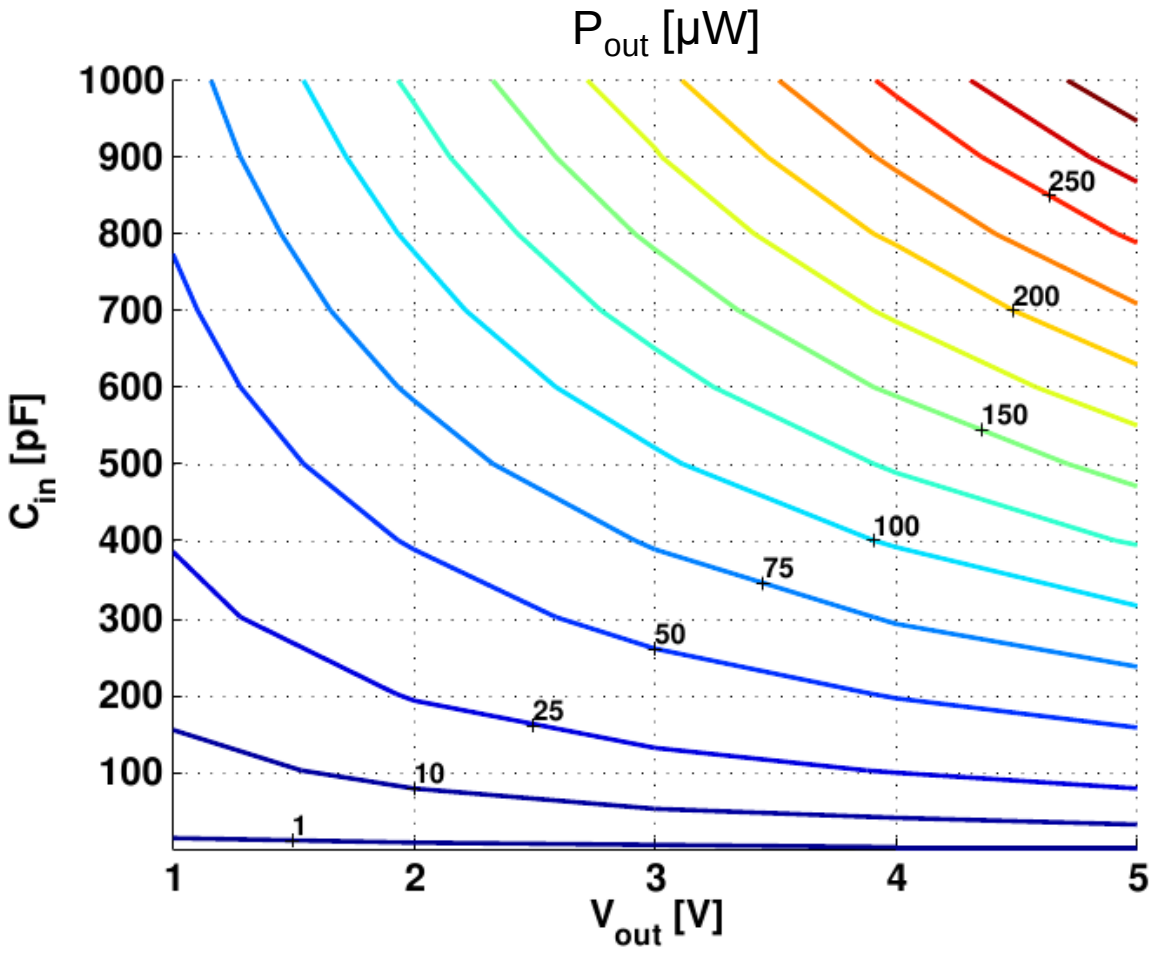
$$2\pi f_{mains}$$

$$< |i_{C_{in}}| > = 4 f_{mains} C_{in} (\sqrt{2} V_{in} - V_{out})$$

$$P_{out} = < |i_{C_{in}}| > V_{out}$$

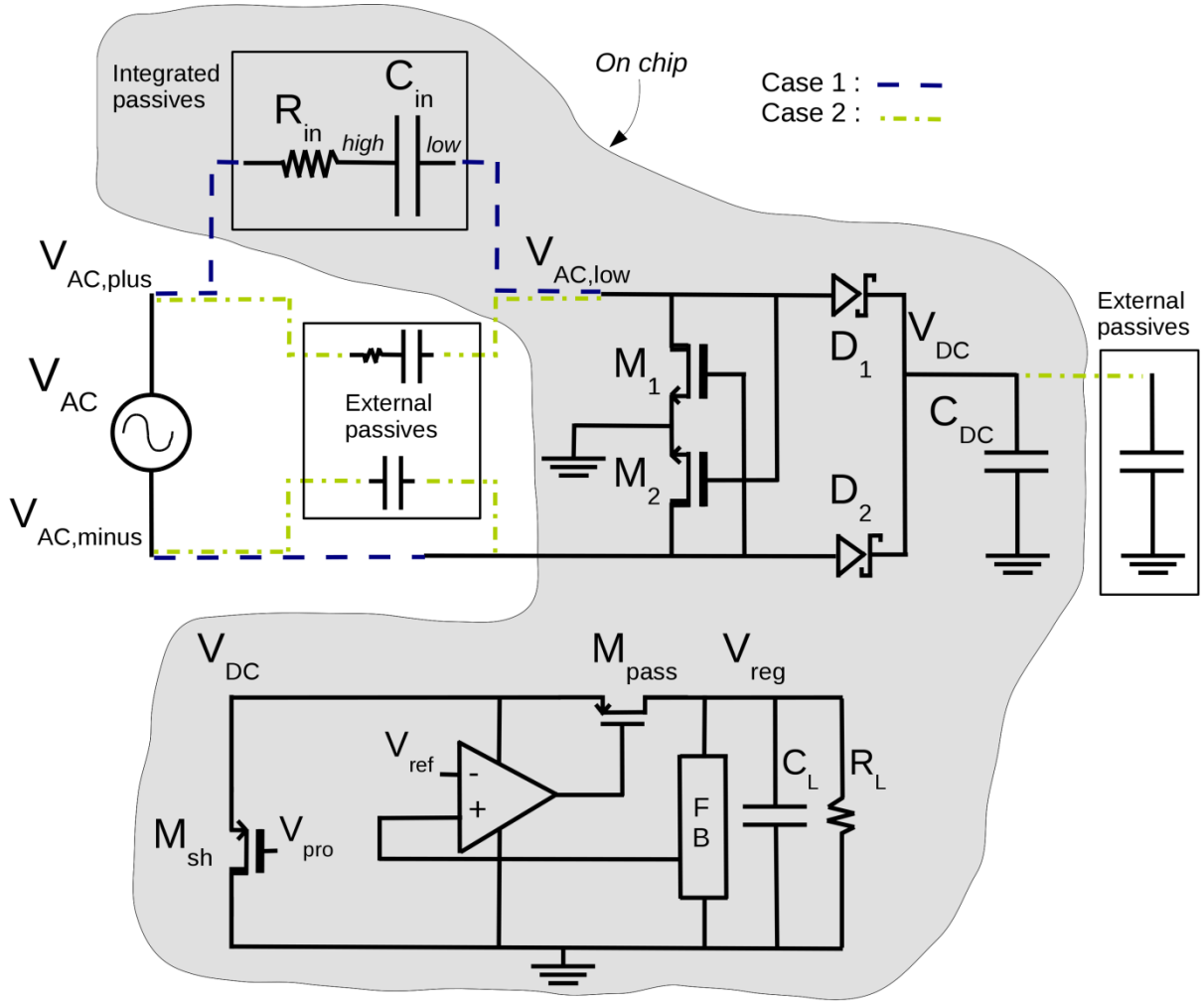
Modeling result

- $P_{out}(C_{in})$ linear
- $P_{out}(V_{out})$ linear for low V_{DC}



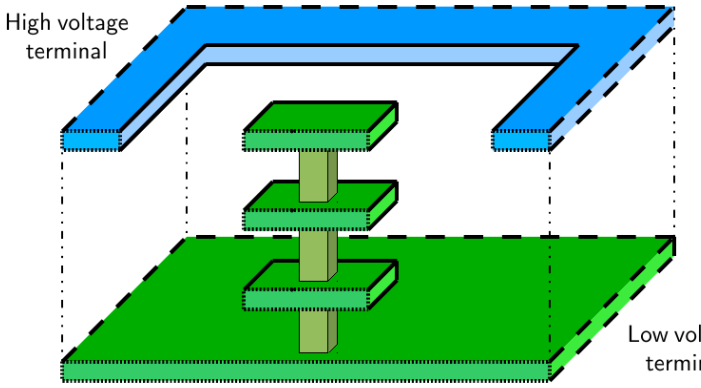
Circuit implementation

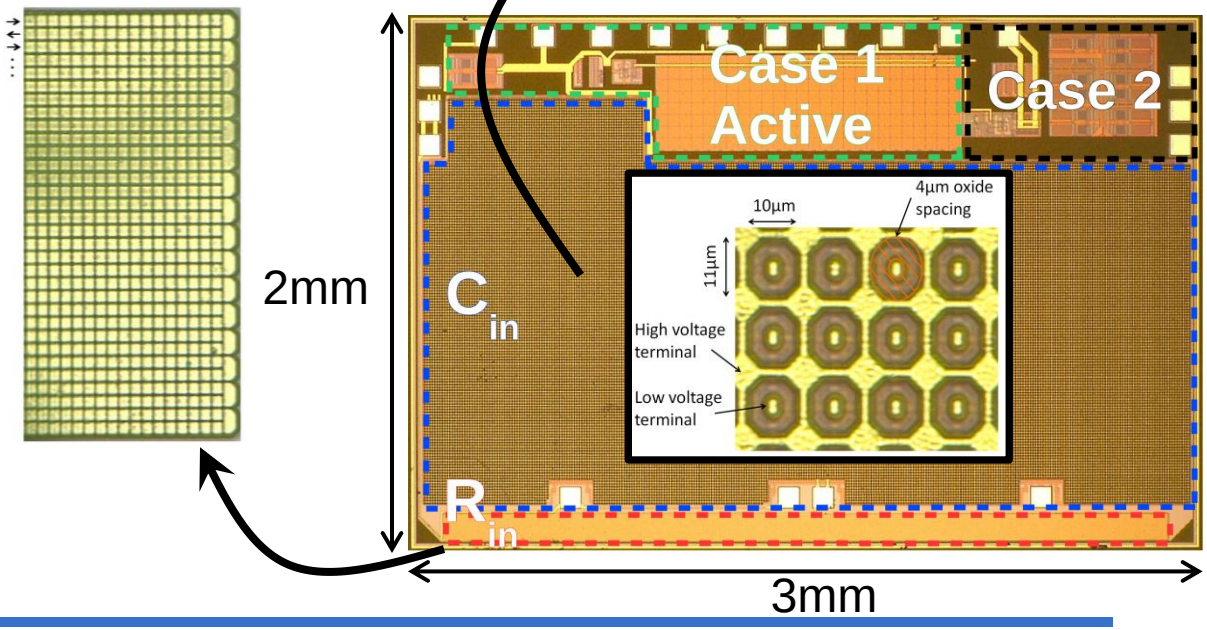
- 2 cases: Fully integrated (µW's), Highly Integrated (mW's)



Chip implementation

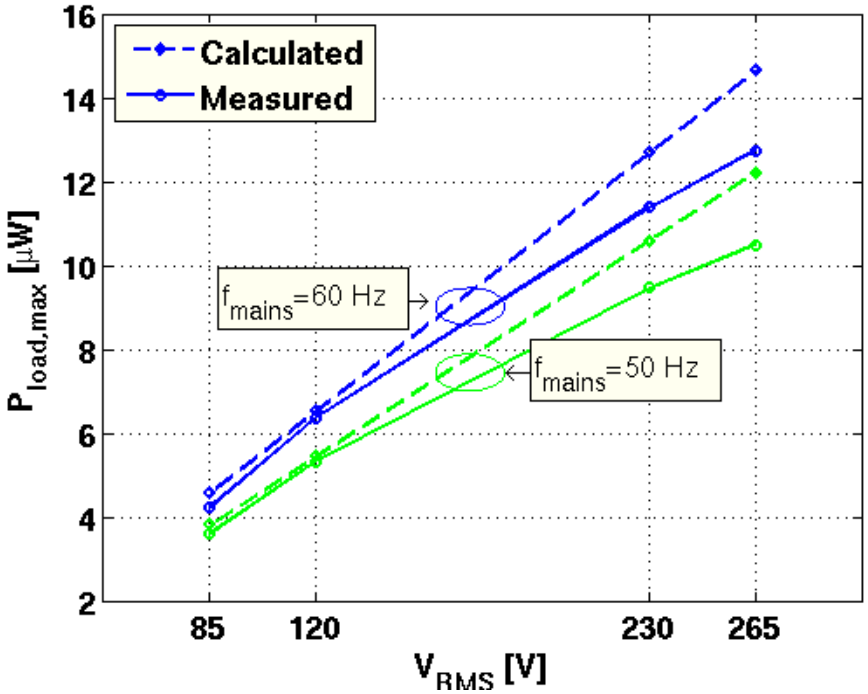
- Capacitor
  - Metal-metal capacitor
  - High voltage plate in top metal
  - 4µm spacing
  - 50 pF
- Resistor
  - 6µm to substrate
  - Top metals
  - Vias
  - 36 kΩ

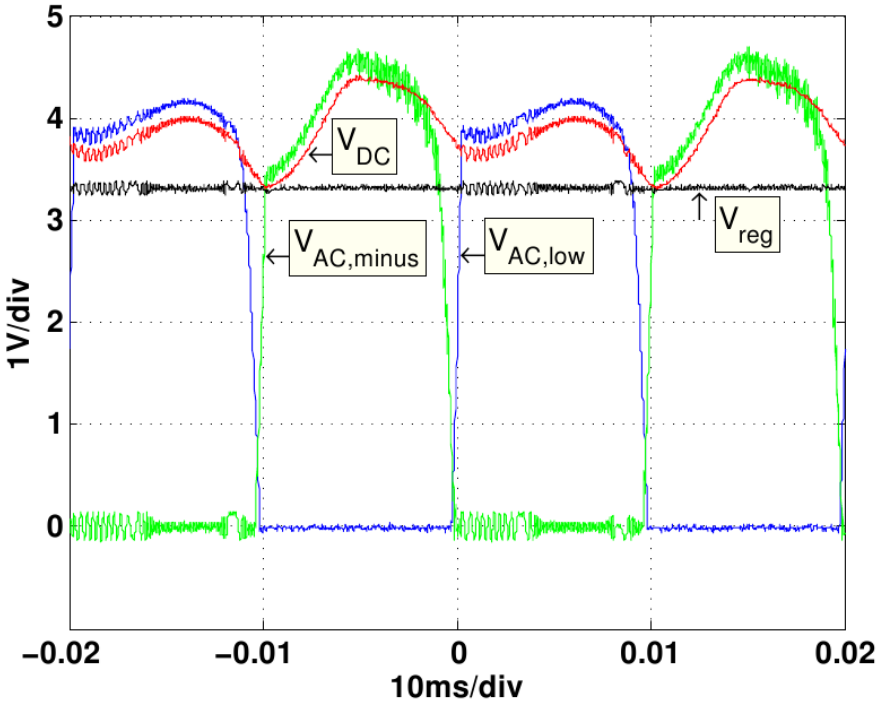




Measurements

- Universal mains
  - 85-265V_{rms}
  - 50-60Hz
- C_{in}: 50pF
- US: 6.4 µW
- EU: 9.5 µW

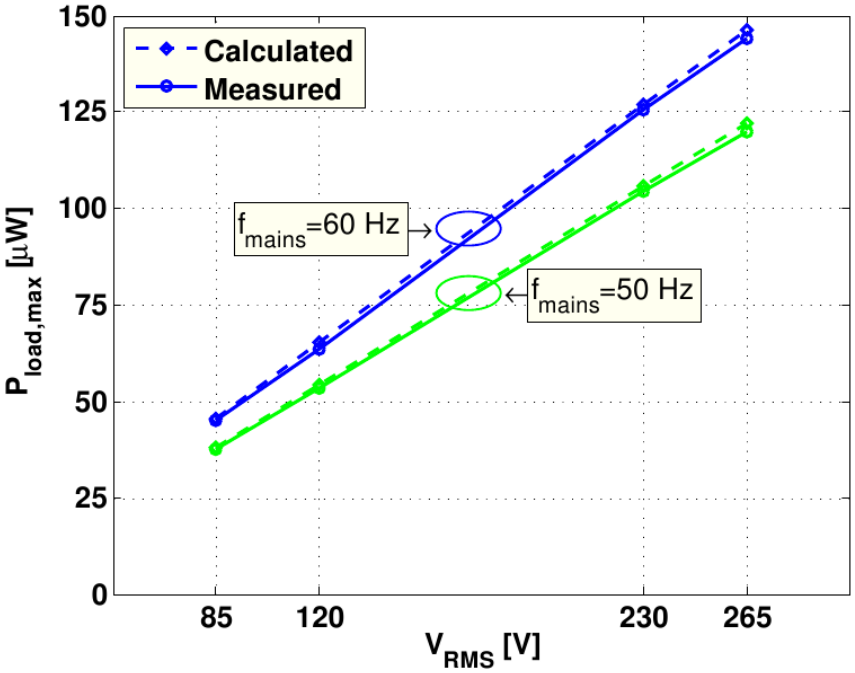


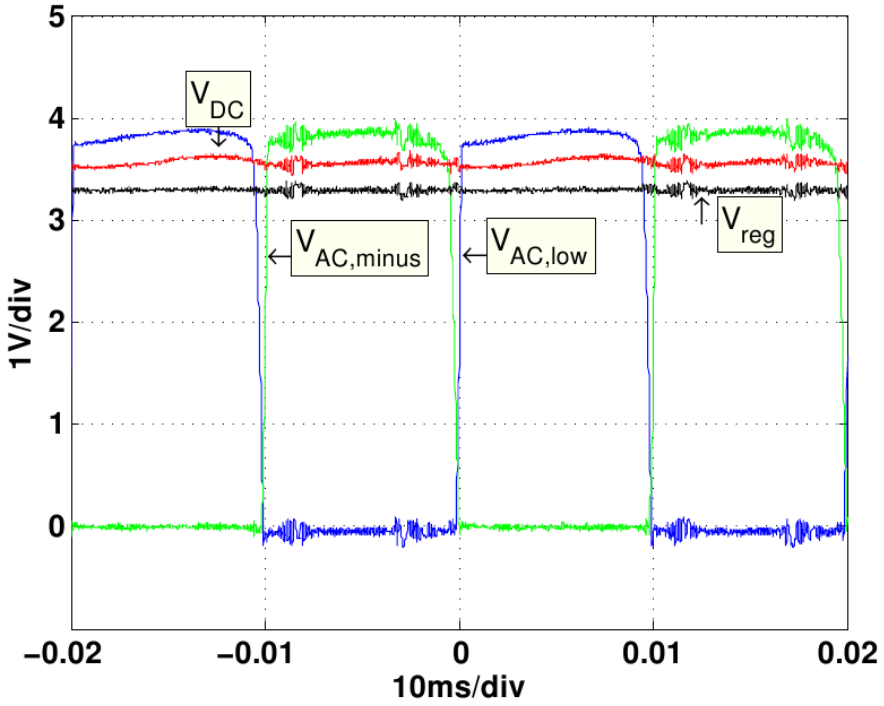


Measurements

- Universal mains
  - 85-265V_{rms}
  - 50-60Hz

- C_{in}: 2x 68nF
- US: 4.2 mW
- EU: 7 mW





Measurements

Reference	[Tamez, Esscirc'10]	Case 1		Case 2 (2x68nF)	
Tech node	$0.13\mu m$	$0.35\mu m$			
V_{RMS}	120V	120V	230V	120V	230V
f_{mains}	60Hz	60Hz	50Hz	60Hz	50Hz
Power/area	$0.43\mu W/mm^2$	$1.06\mu W/mm^2$	$1.58\mu W/mm^2$	-	-
V_{reg}	$4V$	$3.3V$			
$t_{on,diode}$	48%	91%	93.5%	91%	93.5%
$P_{out,max}$	$1.5\mu W$	$6.4\mu W$	$9.5\mu W$	$4.2mW$	$7mW$

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Concept & Goal

- ***High voltage conversion ratio*** *from a* ***high input voltage*** *with a* ***monolithic IC***

Switched Capacitor approach?

➡ ***Duty cycle 50%***

⟷ ***Inductive DC-DC converter : PWM***

✚ ***Monolithic integration***

✚ ***Voltage domain stacking/serialization***

➡ **Investigate SC DC-DC potential for Monolithic Very High VCR DC-DC**

Problem considerations

- What do we *need* to make a high VCR converter?
  - VCR is topology dependant
    - Min #capacitors set by Fibonacci Limit (Makowski)
    - Higher VCR requires more components
  - Switches & Capacitors
    - Voltage ratings set by topology
  - Control
    - Getting signals from start to finish throughout voltage domains

Problem considerations

- What do we *have* to make a high VCR converter?

	Impact
– Switches	
▪ Low voltage: GO1, GO2, (GO3)	'high' f_{sw} Ok
▪ High voltage: DMOS	'low' f_{sw} only
– Capacitors	
▪ Low voltage: GOX cap, (MIM cap)	'low' density
▪ High voltage: Fringe cap	'very low' density

➡ It will be impractical to use DMOS devices since low f_{sw} and very low density capacitors are not a good match

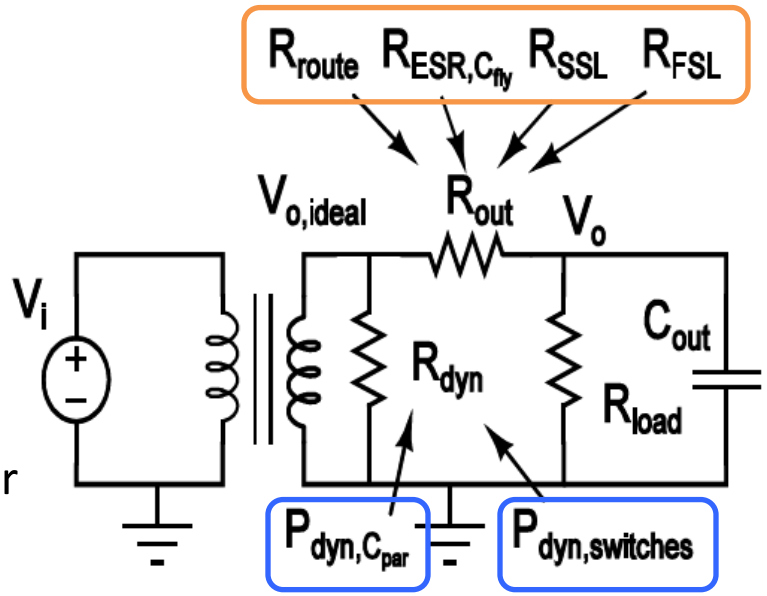
Problem considerations

- What do we need to pay attention to in a monolithic high VCR converter?
  - How does VCR influence component requirement?
    - Component rating
    - Component utilization
  - Parasitics related to components
    - Ex. parasitic capacitor coupling to substrate with $V_{c,rated}$

➡ Where are the loss contributions coming from?

CMOS considerations

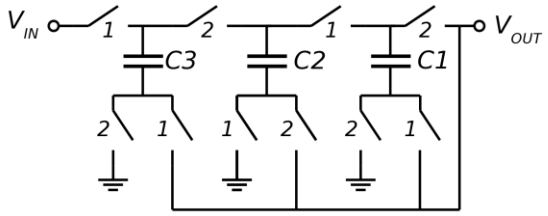
- Where are the loss contributions coming from?
  - Intrinsic losses
    - R_{out} related
  - Extrinsic losses
    - R_{dyn} related
      - Parasitic capacitor coupling factor
      - Parasitic capacitor swing
        - $M_{sw}=\sum a_{c,i}\ V_{Cpar,swing,i}^{2}$



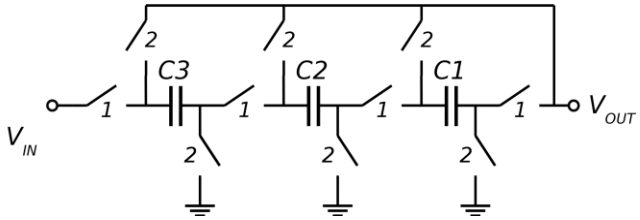
Investigated topologies

- Known to have efficient capacitor utilization

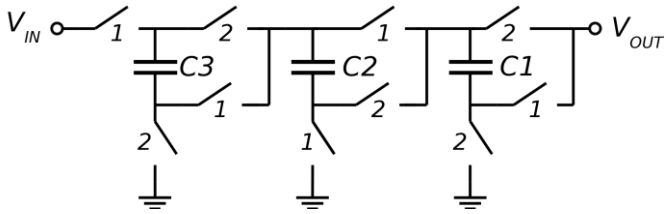
(a) Dickson Star 4:1



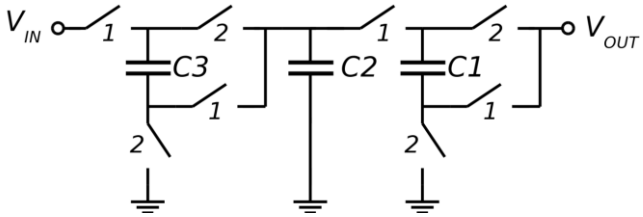
(b) Series parallel 4:1



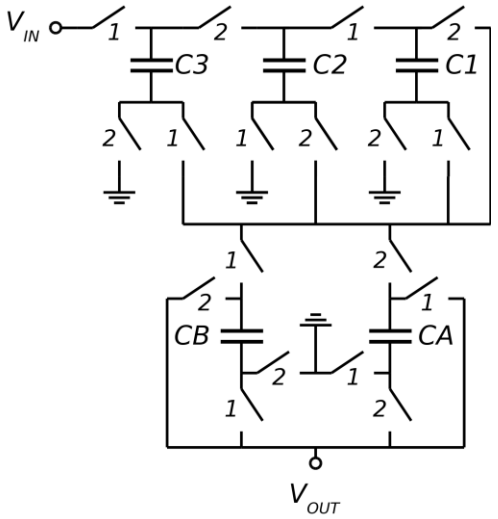
(c) Fibonacci 5:1



(e) Doubler 4:1



(d) Dickson Star Embedded Cascade 8:2:1



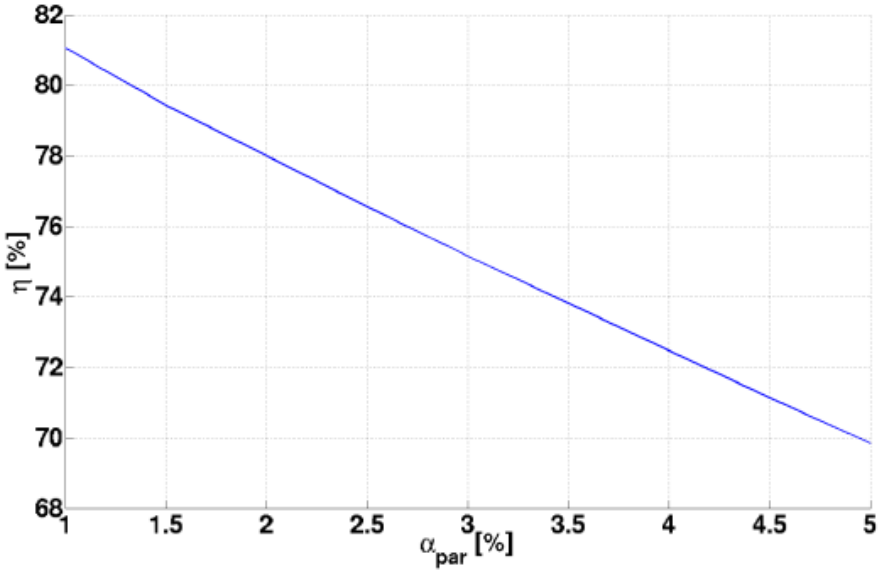
Topology results

	Dickson Star	Series Parallel	Fibonacci	Dickson Star Embedded Cascade	Doubler
# columns = k	$k = N - 1$	$k = N - 1$	$Fib_{k+2} = N$ [a]	$k = \frac{N}{2} - 1$ [b]	$k = 2log_2(N) - 1$
k_c	$[\frac{1}{N} \dots \frac{1}{N}]$	$[\frac{1}{N} \dots \frac{1}{N}]$	$[Fib_1 \dots Fib_k]$	$[\frac{1}{N} \dots \frac{1}{N}\ \frac{1}{4}\ \frac{1}{4}]$ [b]	$[\frac{1}{2}\ \frac{1}{2^2}\ \frac{1}{2^2}\ \frac{1}{2^3}\ \frac{1}{2^3} \dots \frac{1}{2^N}\ \frac{1}{2^N}]$
$V_{C,rated}$ $[V_{out}]$	[1 2 3 ... N-1]	[1 ... 1]	$[Fib_2 \dots Fib_{k+1}]$	[2 4 6 ... $(\frac{N}{2} - 1)$ 1 1] [b]	$[1\ 2\ 2\ 4\ 4 \dots \frac{N}{2}\ \frac{N}{2}]$
V_{sw} $[V_{out}]$	[1 ... 1]	[1 2 3 ... N-1]	$[Fib_1 \dots Fib_k]$	[2 ... 2 1 1] [b]	$[1\ 2^1\ 0\ 2^2\ 0 \dots 2^{log_2(N)}\ 0]$
M_{sw}	$\frac{N-1}{N}$	$\frac{1}{N}\sum_{i=1}^{N-1} i^2$	$\frac{1}{N}\sum_{i=1}^{k}(Fib_i)^3$	$2.5 - \frac{4}{N}$	$\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{i-1}$
$K_c = (\sum_{i=1}^{N} \lvert k_{c,i} \rvert)^2$			$(\frac{N-1}{N})^2$		$(\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{-i})^2$
$K_c,\ N = \infty$			1		2.25
$M_{sw},\ N = 2$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$
$M_{sw},\ N = 4$	$\frac{3}{4}$	3.5	–	1.5	1.5
$M_{sw},\ N = 8$	$\frac{7}{8}$	17.5	4.62	2	3.5
$M_{sw},\ N = 16$	$\frac{15}{16}$	77.5	–	2.25	7.5
$M_{sw},\ N = 64$	$\frac{63}{64}$	1333.5	$N = 55 - 89$ 220.6 – 578	2.375	31.5
$M_{sw},\ N = \infty$	1	∞	∞	2.5	∞

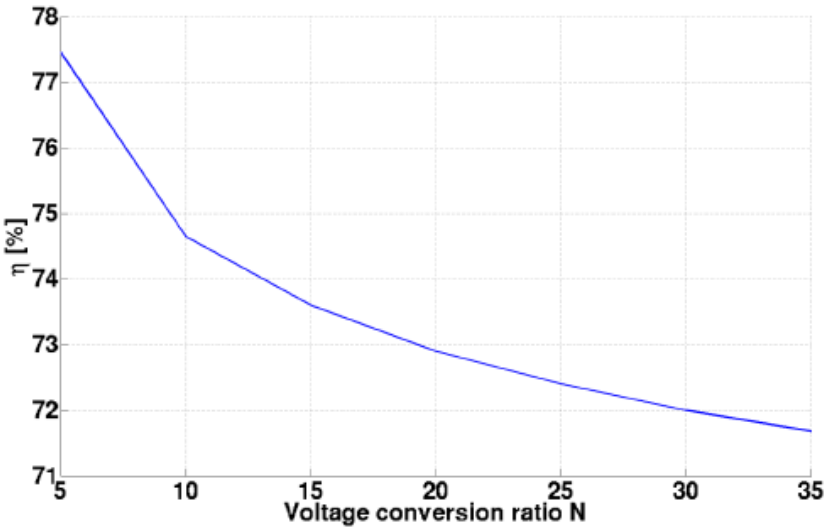
[a] $Fib_1 = 1, Fib_2 = 1$ [b] $N > 2$ and N even and $\frac{N}{2}$ even

Topology Simulations

- Validation of Dickson Star: η[α], η[VCR]



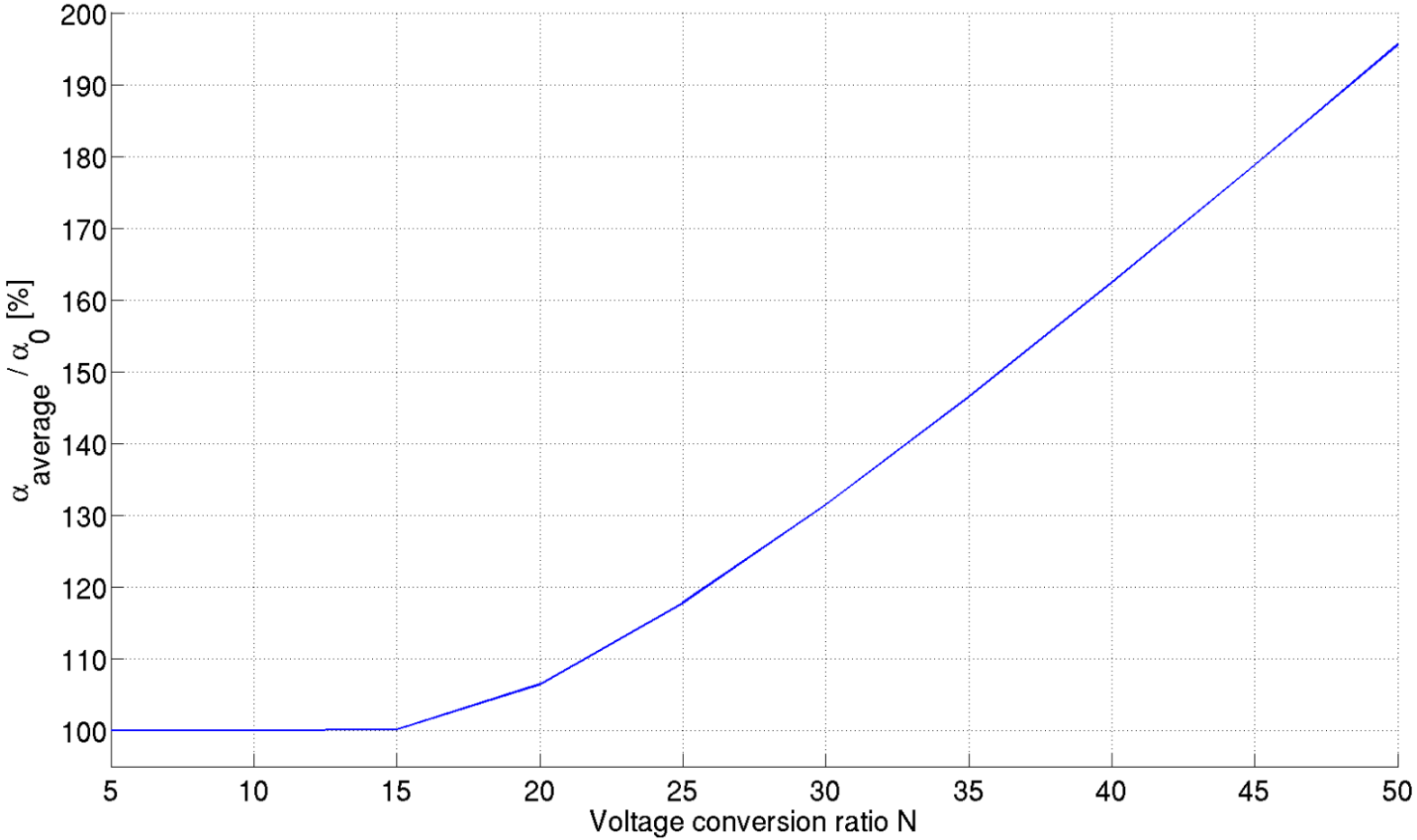
(a) Dickson Star topology with parasitic reduction at VCR=11, $f_{sw} = 10\text{MHz}$, $V_{in} = 41.7V$, $V_{out} = 3.3V, P_{out} = 40\text{mW}$, $C_{tot} = 2.9nF$



(b) Evolution of the converter efficiency with rising voltage conversion ratio, $f_{sw} = 10\text{MHz}$, $\alpha_{par} = 3\%$, $V_{out} = 2.5V, P_{out} = 20\text{mW}$, $C_{tot}/V_{in} = 1.94nF/19V$ for N=5 to $2.86nF/100.5V$ for N=35

Inclusion of practical C_{fly} voltage rating

- Variable VCR; V_{out}=1.8, γ=0.88, f_{sw}=15MHz, P_{out}=20mW



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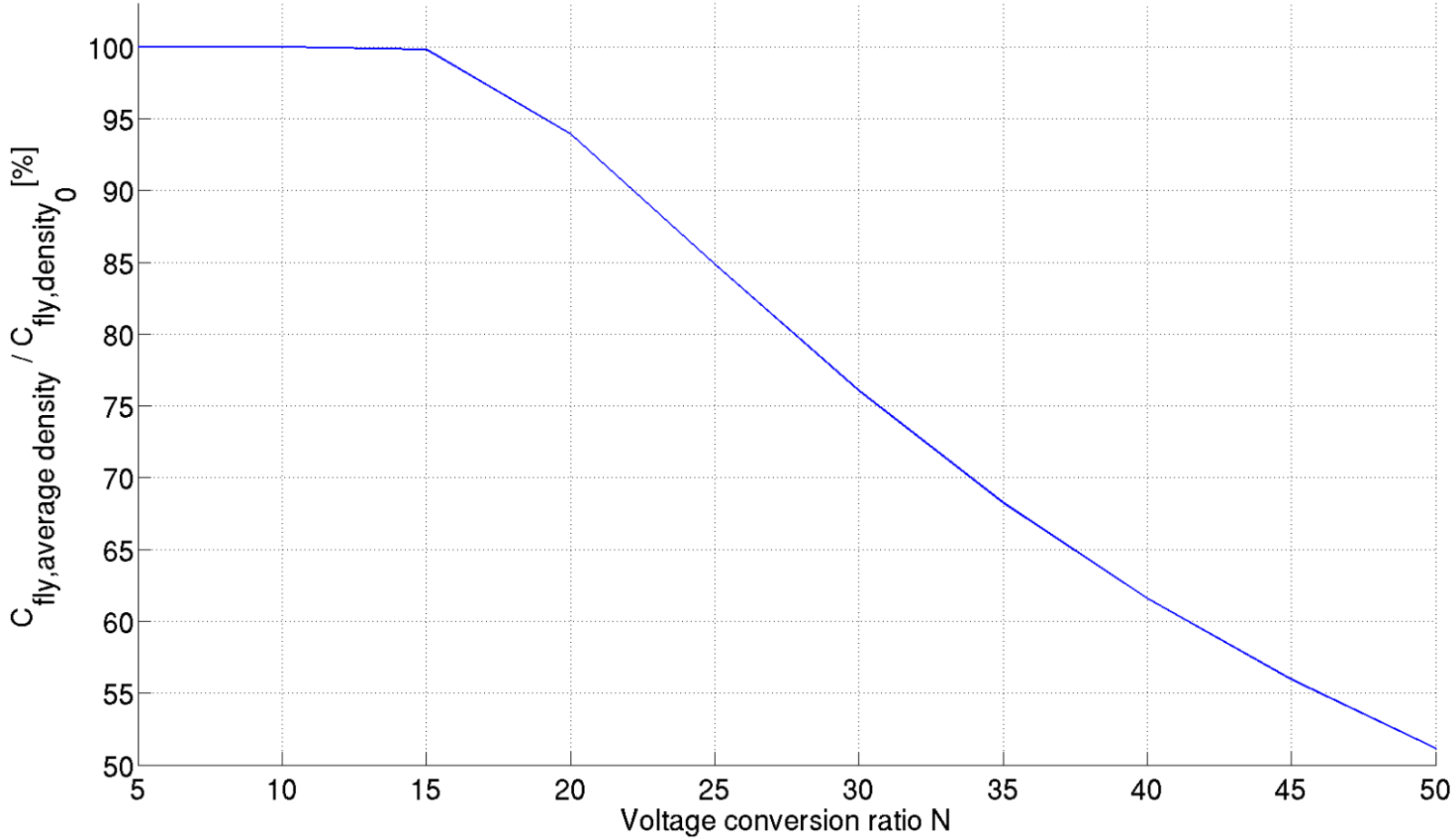

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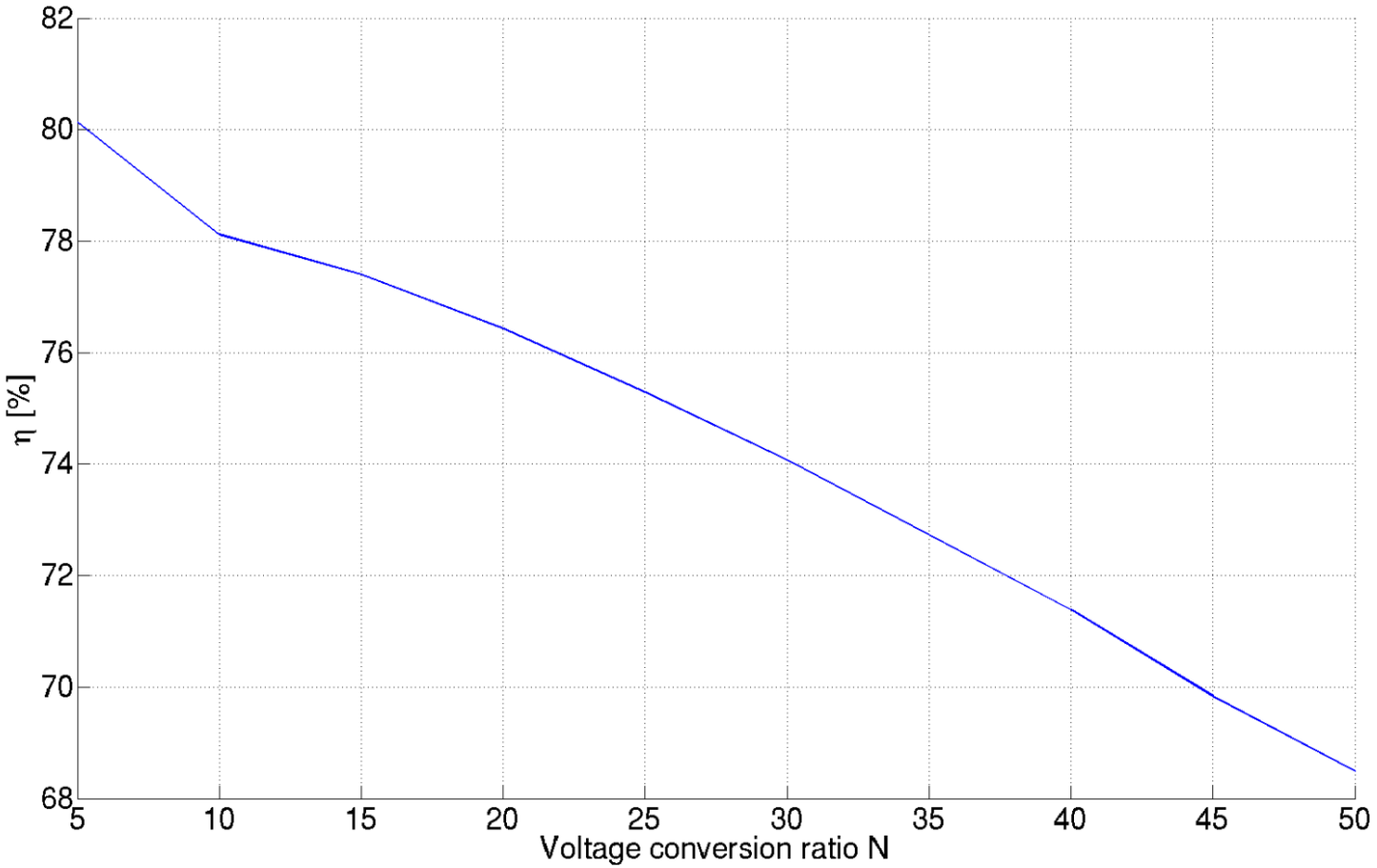

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High VCR topology conclusion

- M_{sw} highly volatile over investigated topologies
  - Dickson Star clearly differentiates and outperforms
    - Highest possible capacitance utilization
    - Lowest possible M_{sw} metric *(converges!)*
    - Good match for CMOS implementation

Decreasing η drop with increasing VCR

- Embedded D* Cascade not better than D*
  - Even though it is a single stage conversion

Conclusions

- ***High VCR*** AND ***Monolithic integration***
  - $\boldsymbol{\alpha_{par}}$ and $\boldsymbol{V_{Cpar,swing}}$ have *large* impact on solution space
  - **Dickson Star** topology very *promising*:
    - Converging f_{ac}
    - Converging M_{sw}
  - Large **component count** *no issue*

Thank you!

QUESTIONS?