Distributed Power Conversion - An answer to Power Delivery Challenges in SoCs?

Rinkle Jain, Jim Tschanz, Vivek De

October 8 2014

Circuit Research Lab, Intel Corporation

Hillsboro, OR

Acknowledgements

- Vaibhav Vaidya
- Stephen Kim
- Seth Sanders
- Krishnan Ravichandran
- Chai Sutantavibul
- Trang Ngyuen
- Chung-ching Peng
- Tri Huynh
- Ken Ikeda
- Carlos Tokunaga
- Muhammad Khellah
- Rick Forand

This research was, in part, funded by the U.S. Government (DARPA). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Government.

Outline

Motivation for fully integrated VRs

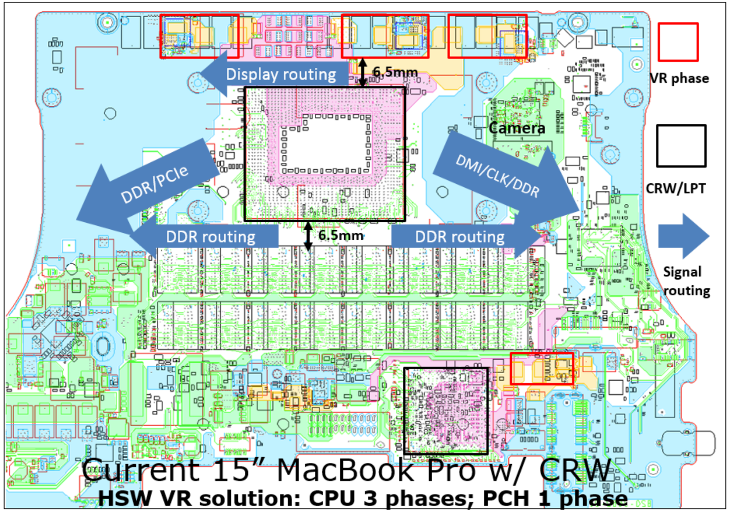
Capability of Switched Capacitor Voltage Regulator (SCVR)

DVFS enabler with minimum area-power overhead

Co-design with load

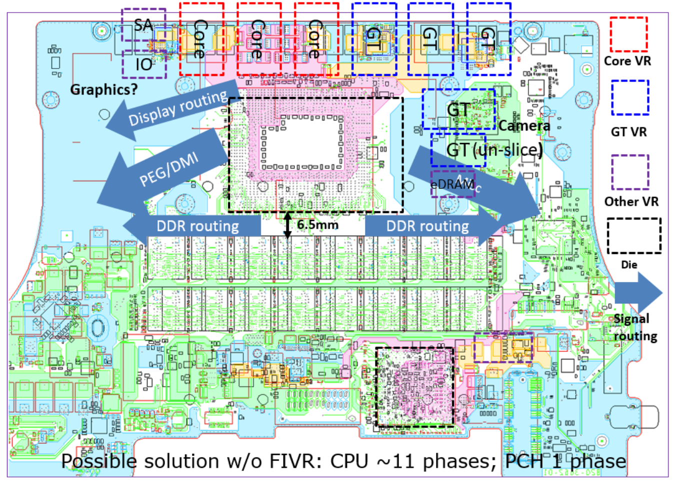
Summary and Conclusion

The Platform Perspective



Courtesy: S. Soman, A. Uan-zo-li; Intel

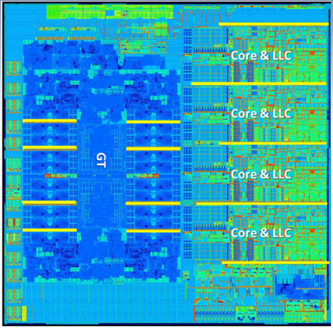
The Platform Perspective

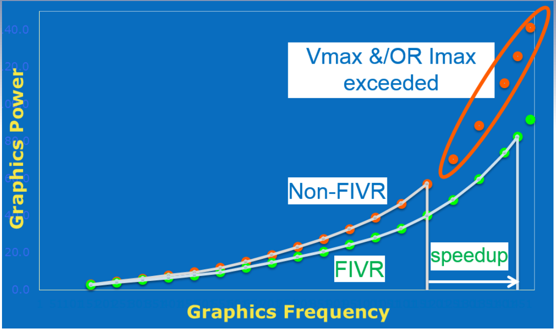


SoCs inherently require several voltage rails

Input rail consolidation simplifies power delivery significantly

The Die Side of the Story



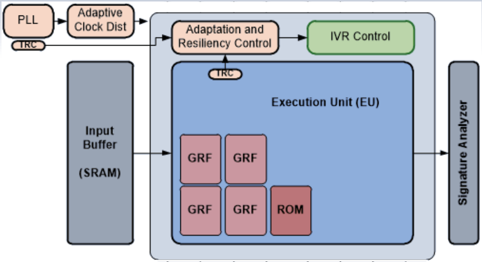


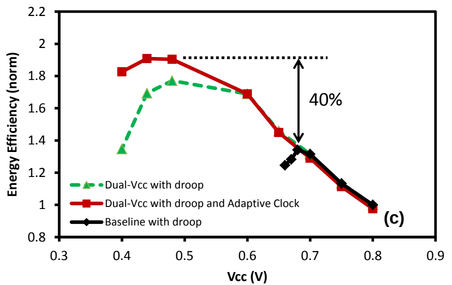
[Burton et.al APEC '14]

[Kurd et.al ISSCC '14]

- Faster state transitions by 25%, higher performance per watt
- Overall idle power slashed by 20x, battery life improvement by $> 50\%$
- Proliferation of Integrated voltage regulators in latest technology node

Finer Grain Voltage Domains



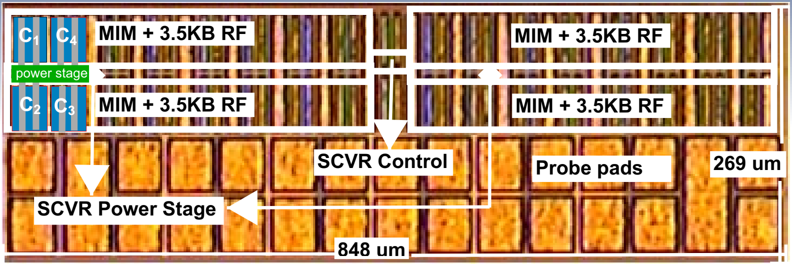


[Tokunaga et.al ISSCC '14]

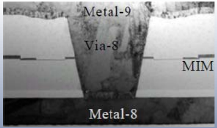
Measured data

- Vmin reduction through many voltage domains
- Necessary level shifters incorporated here with 0 area penalty

Switched Capacitor VR with MIM



High density MIM

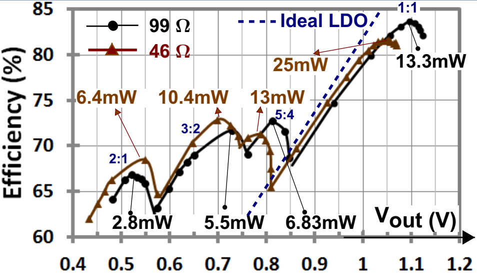


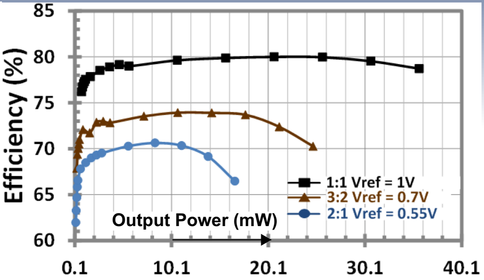
TEM *[C.-H. Jan et.al.; IEDM 2012]*

Technology	22nm Tri-gate CMOS
Passive Type	High Density MIM
MIM Area	99450 μm^2
Power Stage Area	3240 μm^2
Control Area	420 μm^2
Total Active Area	3660 μm^2
Total RF Area	101376 μm^2
Test Interface	Membrane probe

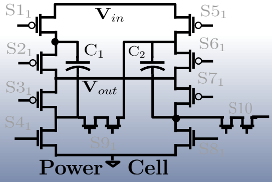
[R. Jain et.al.; JSSC 2014]

Conversion Efficiency Measurements



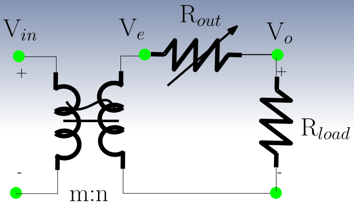


- 84% peak and 63% minimum efficiency
- Lower peaks in other modes due to larger switch size
- Flat efficiency down to << 10% rated load with PFM



[R. Jain et.al.; JSSC 2014]

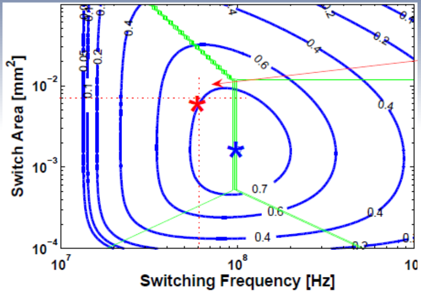
Motivation for Conductance Modulation



$V_e = V_{in} n/m$

$R_{out} = f(R_{fsl} \propto \frac{r_{dson}}{d}, R_{ssl} \propto \frac{1}{C f_{sw}})$

Averaged Model



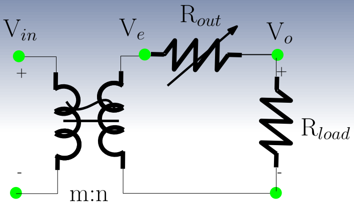
Efficiency Contours

Limitations of simple frequency modulation

- Lower-than-optimal conversion efficiency at lower voltages
- Increased output ripple and associated power loss at light loads
- Input noise coupling. EMI/RFI due to impulsive current draw

Other knobs: 1/r$_{dson}$ (conductance), C (fly capacitance), d(duty)

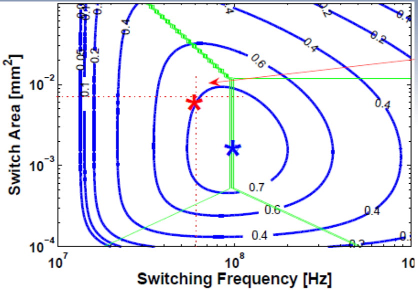
Motivation for Conductance Modulation



$V_e = V_{in} n/m$

$R_{out} = f(R_{fsl} \propto \frac{r_{dson}}{d}, R_{ssl} \propto \frac{1}{C f_{sw}})$

Averaged Model



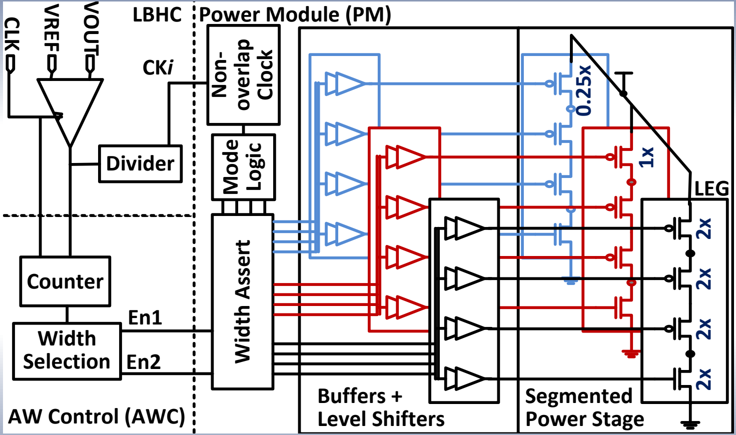
Efficiency Contours

Limitations of simple frequency modulation

- Lower-than-optimal conversion efficiency at lower voltages
- Increased output ripple and associated power loss at light loads
- Input noise coupling. EMI/RFI due to impulsive current draw

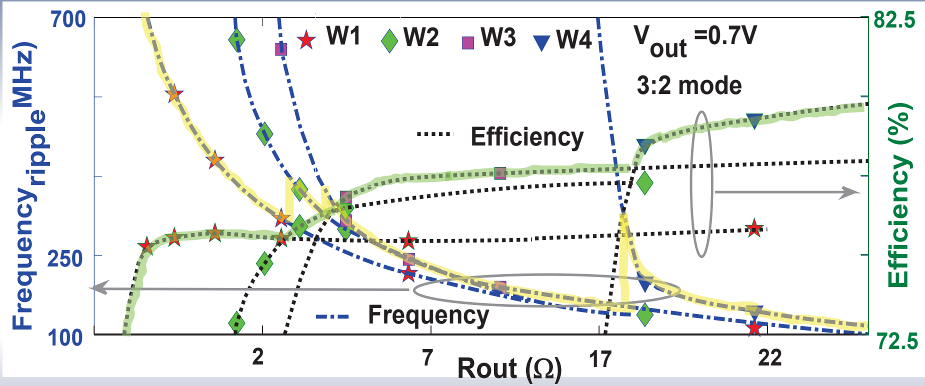
Other knobs: $1/r_{dson}$ (conductance), C (fly capacitance), d(duty)

Adaptive Widths Architecture



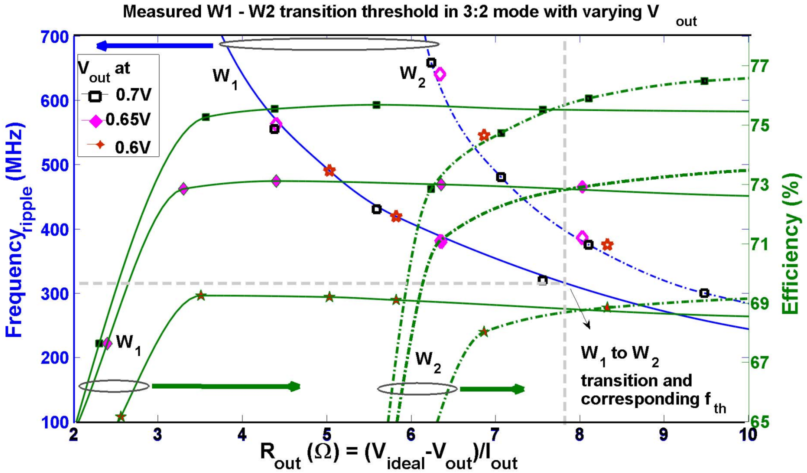
- Total transistor size implemented as 3 weighted banks (ratio 2:1:0.25)
- 8 way interleaving, 2GHz input cloc; 2 bits for width selection

AW Measurements at Constant V_{ref}



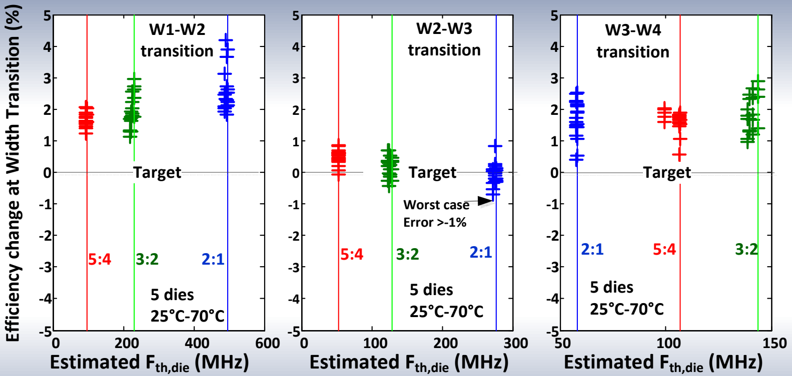
- fsw < $Fth_W = \frac{bW'}{a}$ implies higher efficiency at W' (W'=W/n)
- fsw is a good indicator of low voltage and light load conditions

AW Measurements at different V_{ref}



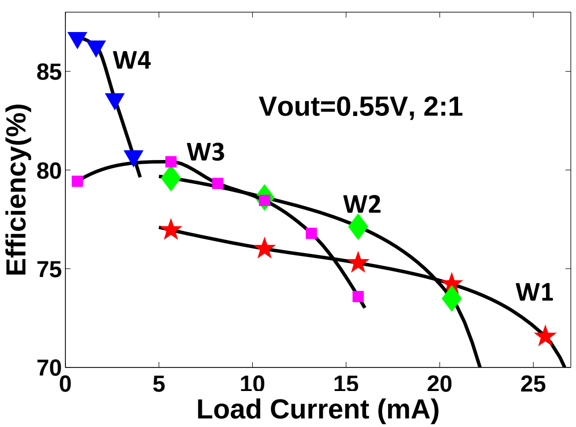
- Rout uniquely defines the optimal width

AW control law: Measurements



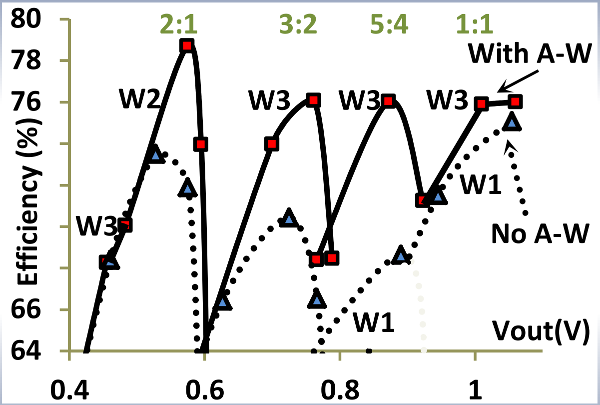
- F_{th} for each width computed from two open loop measurements
- Results show that proposed transition is effective

AW Conversion Efficiency Measurements



- All three major loss mechanisms scale with load (more than linearly)
- Nearly 15% improvement in 2:1 mode

AW Conversion Efficiency Measurements



- Constant resistance load
- All modes show optimal efficiency peaks

Capability Summary

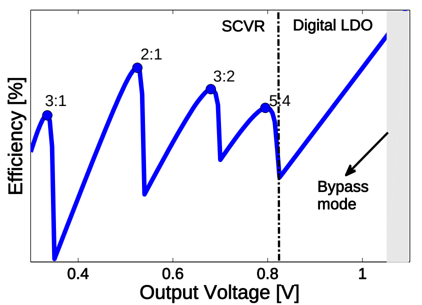
Reference	2	3	5	This work
Process	45nm SOI	45nm	32nm SOI	22nm trigate
Passives type	Deep trench	Gate Oxide SOI	Gate Oxide	MIM
Maximum frequency	100MHz	30MHz	225MHz	250MHz
Input Voltage	2V	1.8V	2V	1.23V
Output	0.95V/2.7mA	0.8-1V/8mA	0.4-1.1V/0.28A	0.45-1V, 88mA
Power Efficiency %	90	69	81	70@0.55V,84@1.1V
Response time	Unregulated	120-200ns	Unregulated	3-5ns
Droop	-	250mV	-	$\leq$25mV
Current density A/mm^2	2.3	0.050	0.73	0.88
Area Overhead	13%	6x	41%	3.6%

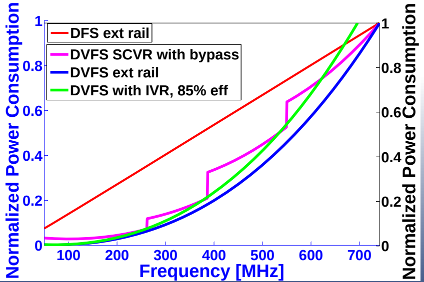
- All-digital multi-mode SCVR in 22nm tri-gate CMOS using high-density MIM
- Wide voltage range, good conversion efficiency across load
- Low area overhead of 3.6%, comparison assumes 30mA, 0.1mm^2 load
- Fast $<$ 5ns response times
- Max VR current density of 400(880) mA/mm^2 in 1:1(2:1) modes

Application

Current capability

- At 1V, 2:1 mode: 1.2-1.6A/mm^2 (22nm)
- Atom at 2.5A/mm^2, Graphics at 1.25 A/mm^2
- Worst case di/dt: atom at 2A/ns , Graphics at 150mA/ns
- Vin=Vccmax feasible, downconversion is not a must
- Reuse power gates, hybrid solution with LDO
- Minimum active power and area overhead





Physical Design Constraints

Practical issues: Co-design with load

- Graphics: large area, lower power density
- lots of signals traverse x and y and $x<y$
- Highly automated design, push button SoC Methodology (unlike core)
- Shared metal resources, IR drop on weak grids

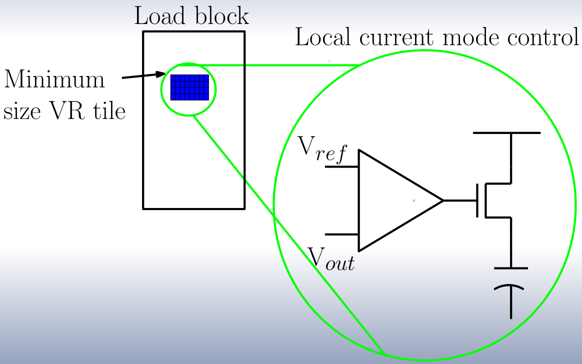
Need for distribution

- One contiguous VR block $\Rightarrow$ large keep-out-regions in APR
- A stand-alone minimum-size VR tile desired, custom-laid out ok
- VR tile should be reuse-able across loads of any size, aspect ratio

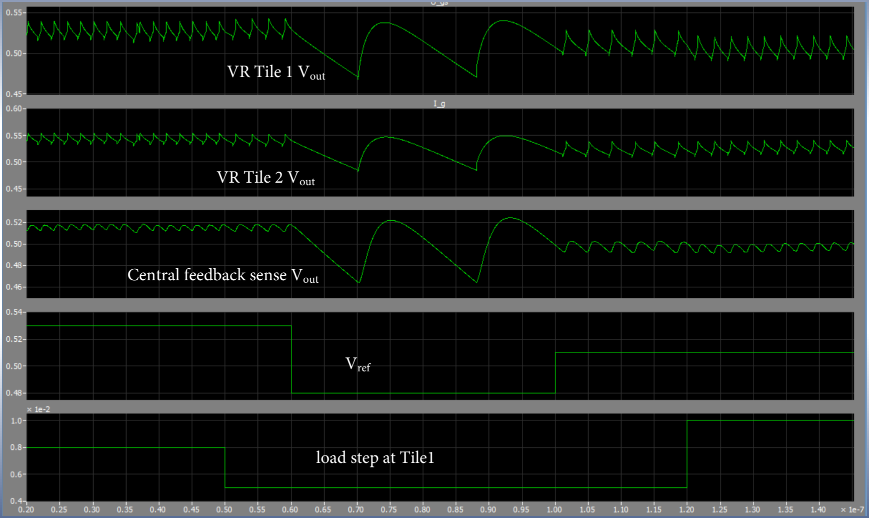
Active Ripple Control Enabling Distribution

Proposed solution

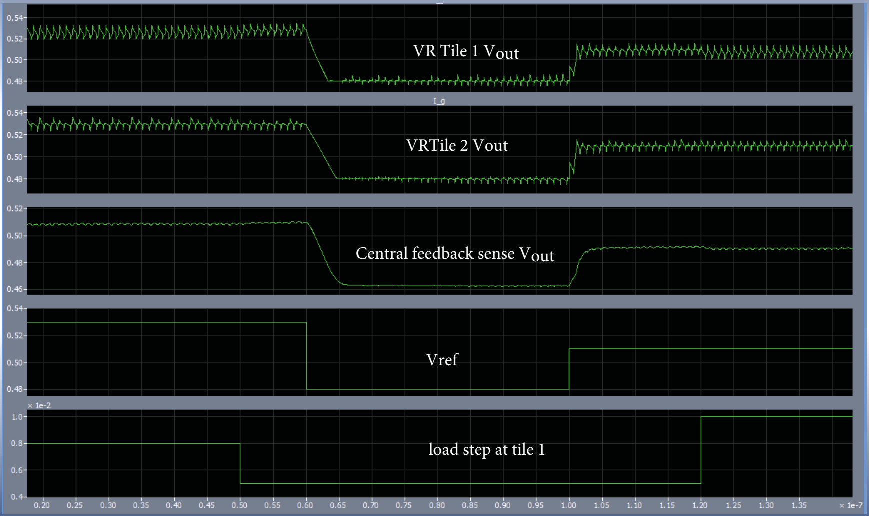
- Distributed standalone tiles
- Minimal interleaving
- Local current mode control
- Central PFM to drive all tiles



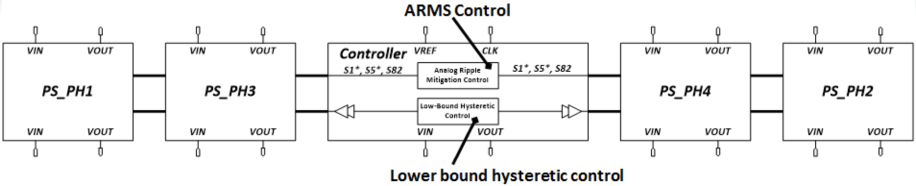
Active Ripple Control Enabling Distribution



Active Ripple Control Enabling Distribution



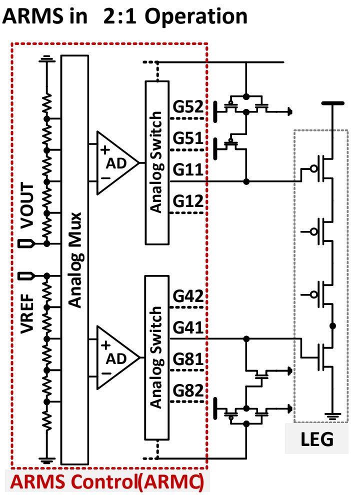
Active Ripple Mitigation Scheme (ARMS)

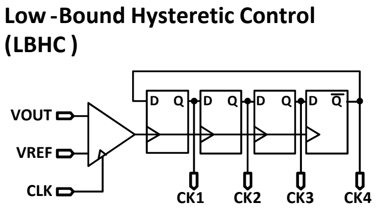


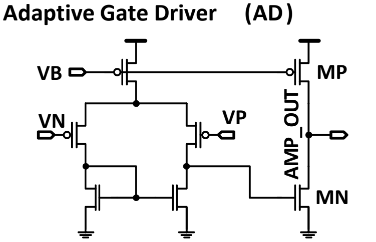
- Gate voltage of select transistors controlled using diff amplifier
- Ideally switch currents match load currents on a cycle by cycle basis

Objective: A frugal design that works across all conversion modes

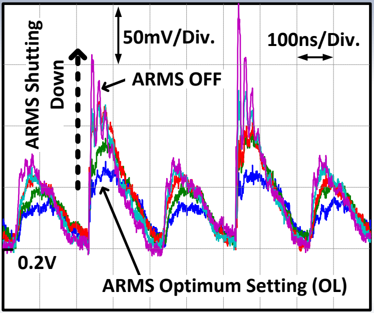
Active Ripple Mitigation Scheme (ARMS)

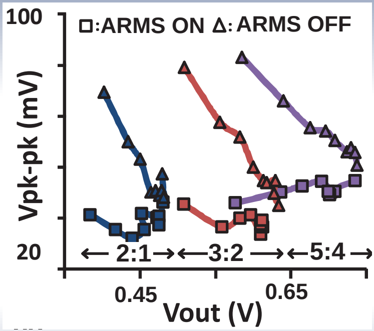






ARMS Ripple Measurements





- Load, V_{out} independent ripple
- Minimum size VR tile

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements ⇒ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements ⇒ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations. (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dictate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations, (ii) high di/dt, tighter impedance requirements $\Rightarrow$ step down IVR

Higher current density VR solutions for small domains are needed!

Thank you for your attention!