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CAD tool to optimize the design of a PowerSoC converter: Powerswipe design case

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POLITÉCNICA

Introduction

CEI UPM

CAD Tool

SEVENTH FRAMEWORK PROGRAMME

Tyndall National Institute

Consortium Leader
Magnetics on Silicon

Power SWIPE

Ampere

IC Design
200MHz LV PMIC

infineon

IFAT Villach
IC Design / Architecture
IFX Regensburg
Chip/Package Co-Design

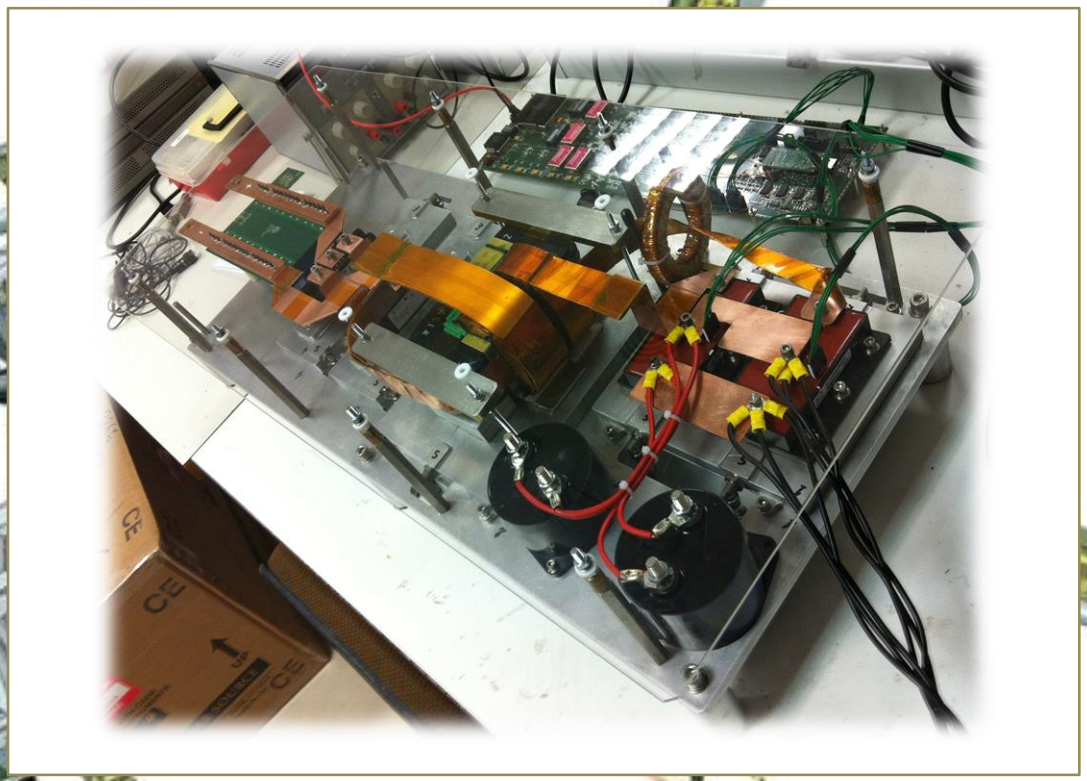
ipdia
The 3D Silicon Leader

Capacitors
Integration
Interposer

BOSCH

Gasoline engine ECU
System requirements

10^6 x factor



Part of this knowledge is needed in PowerSoC

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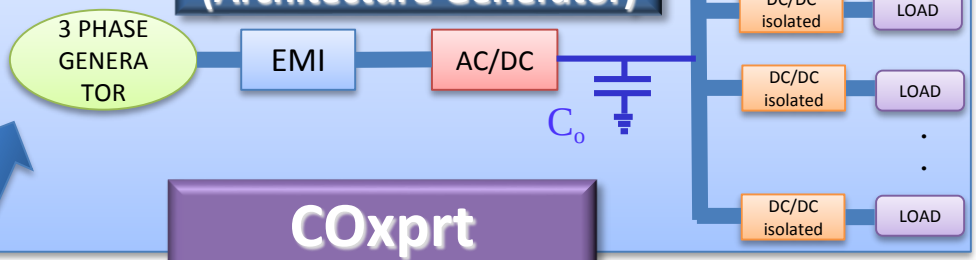
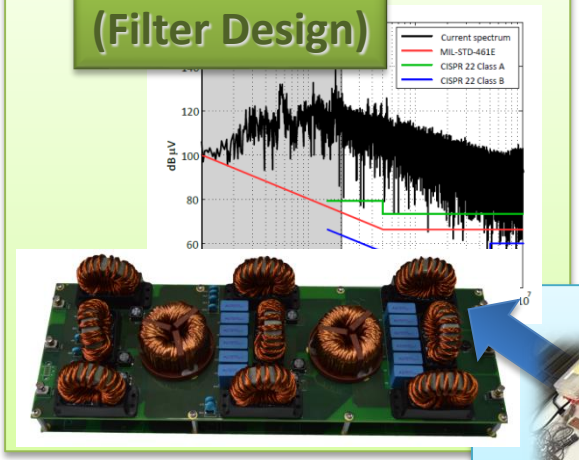
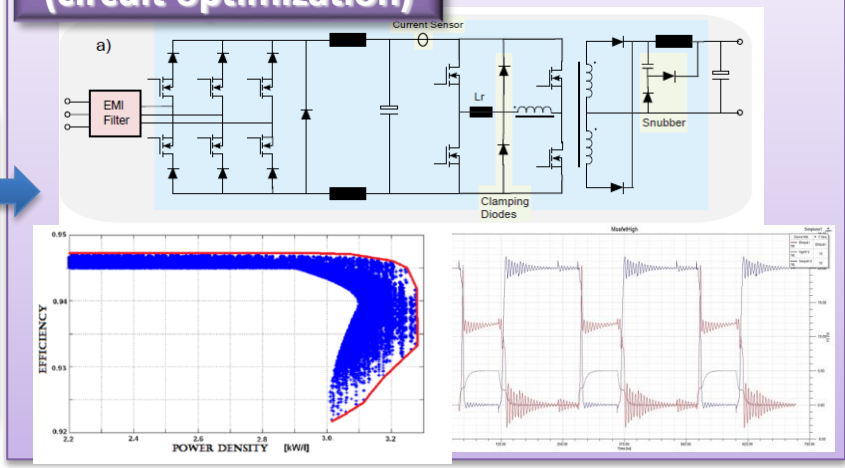
AGxprt (Architecture Generator)



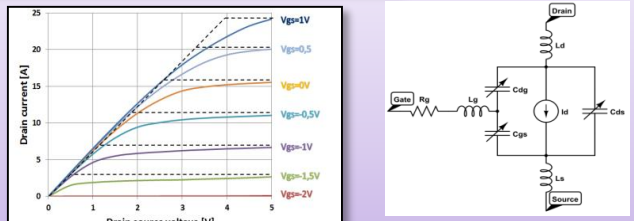
FDxprt (Filter Design)



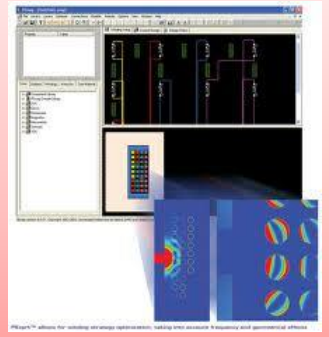
COxprt (circuit optimization)



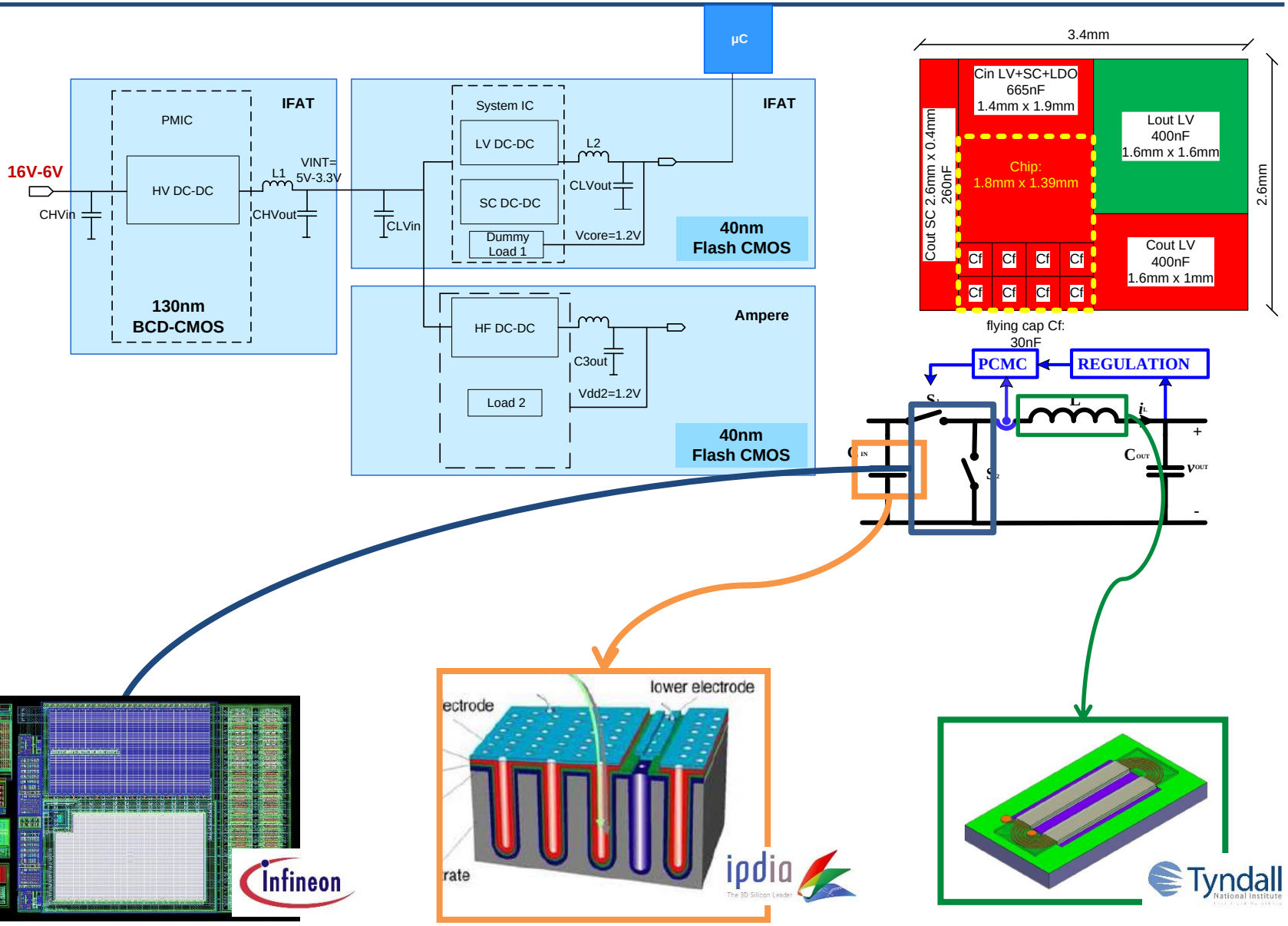
ChTool (Characterization Tool)



PExprt (Magnetic components)

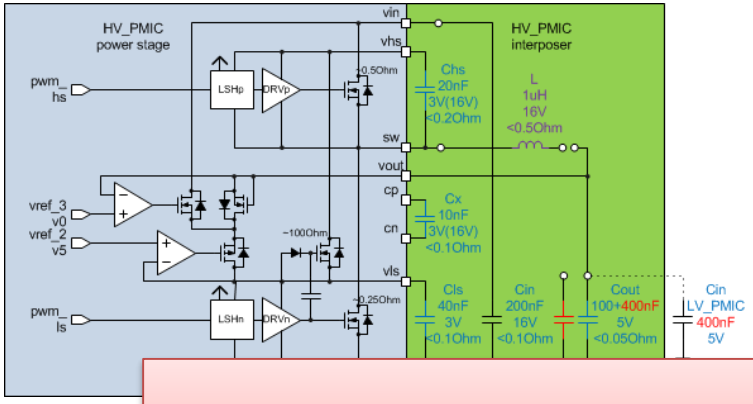


The need of an integrated multi-domain tool

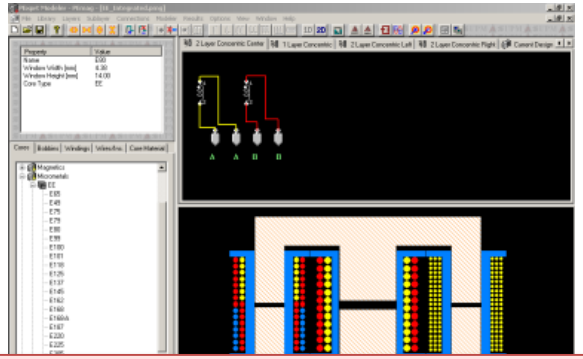


CAD Tools available

Circuit Level Simulators



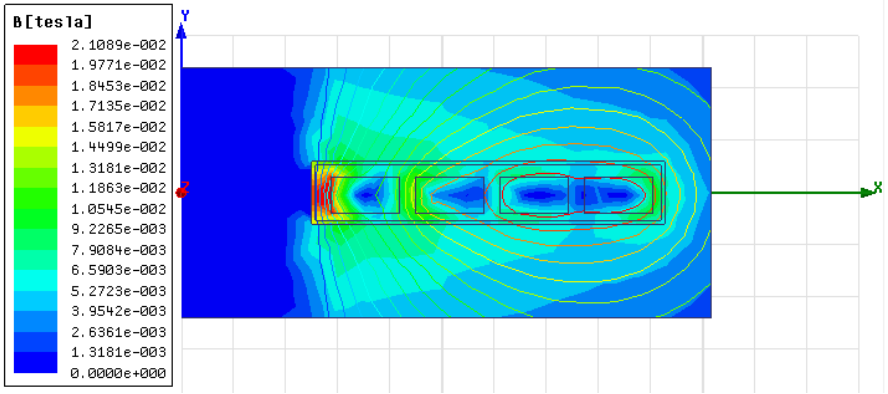
Magnetic Component Optimization Tools



PEXprt-Pemag developed by UPM

lack of integrated design environment for Power Systems on Chip

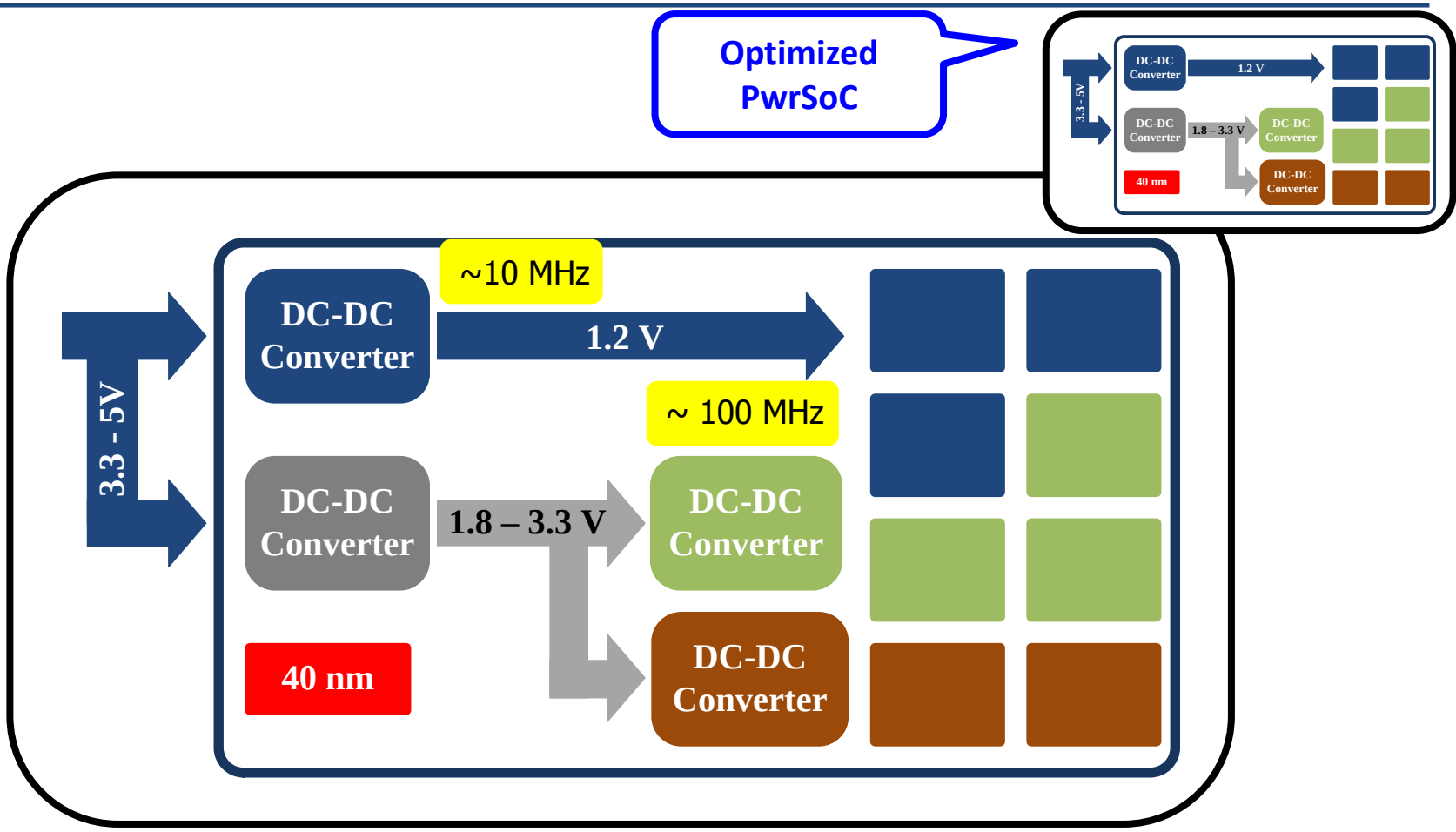
Finite Element Analysis Tools



General Purpose Math Tools

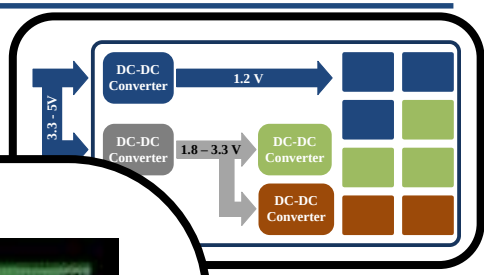
MathWorks

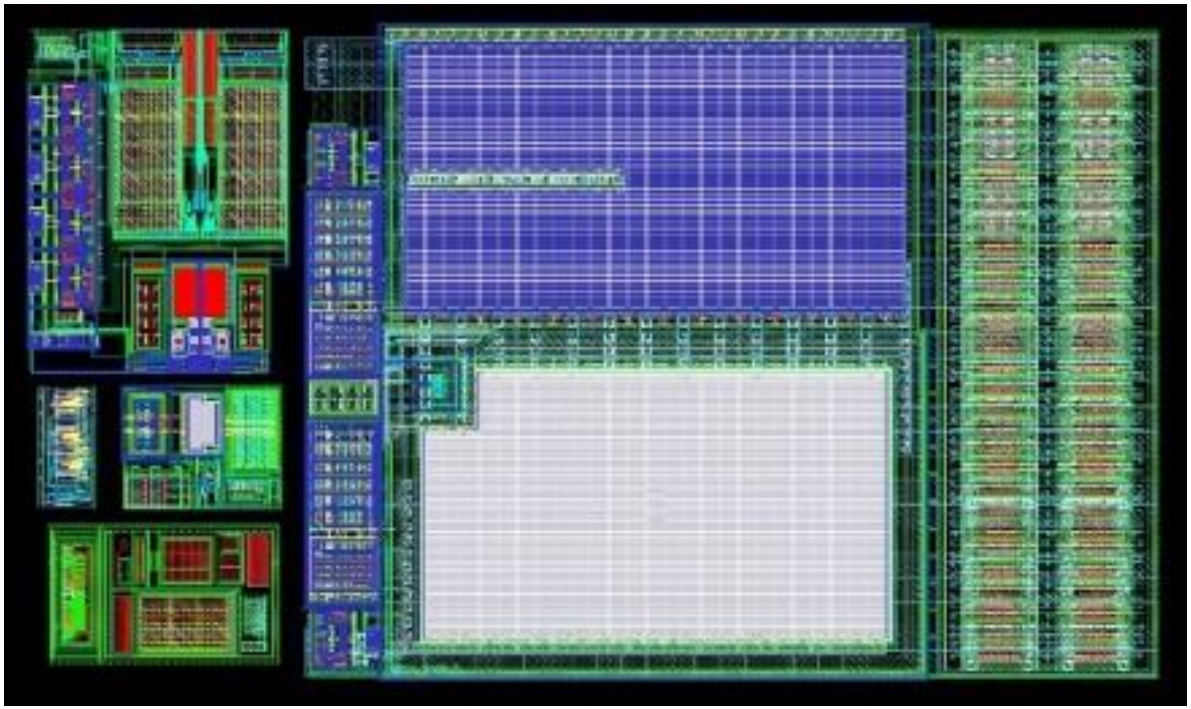
IC perspective

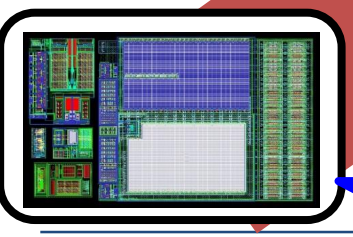


IC perspective

Optimized PwrSoC

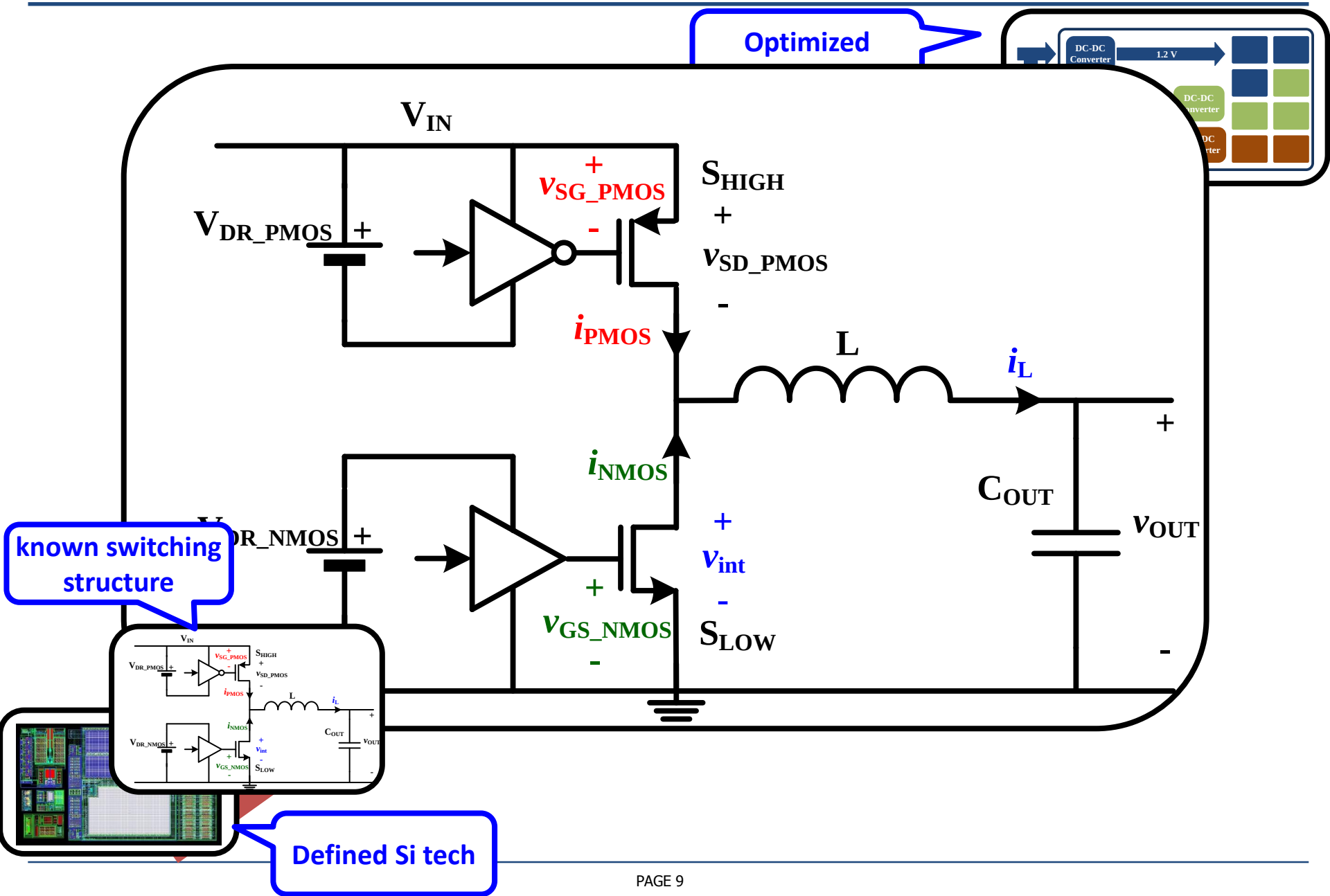




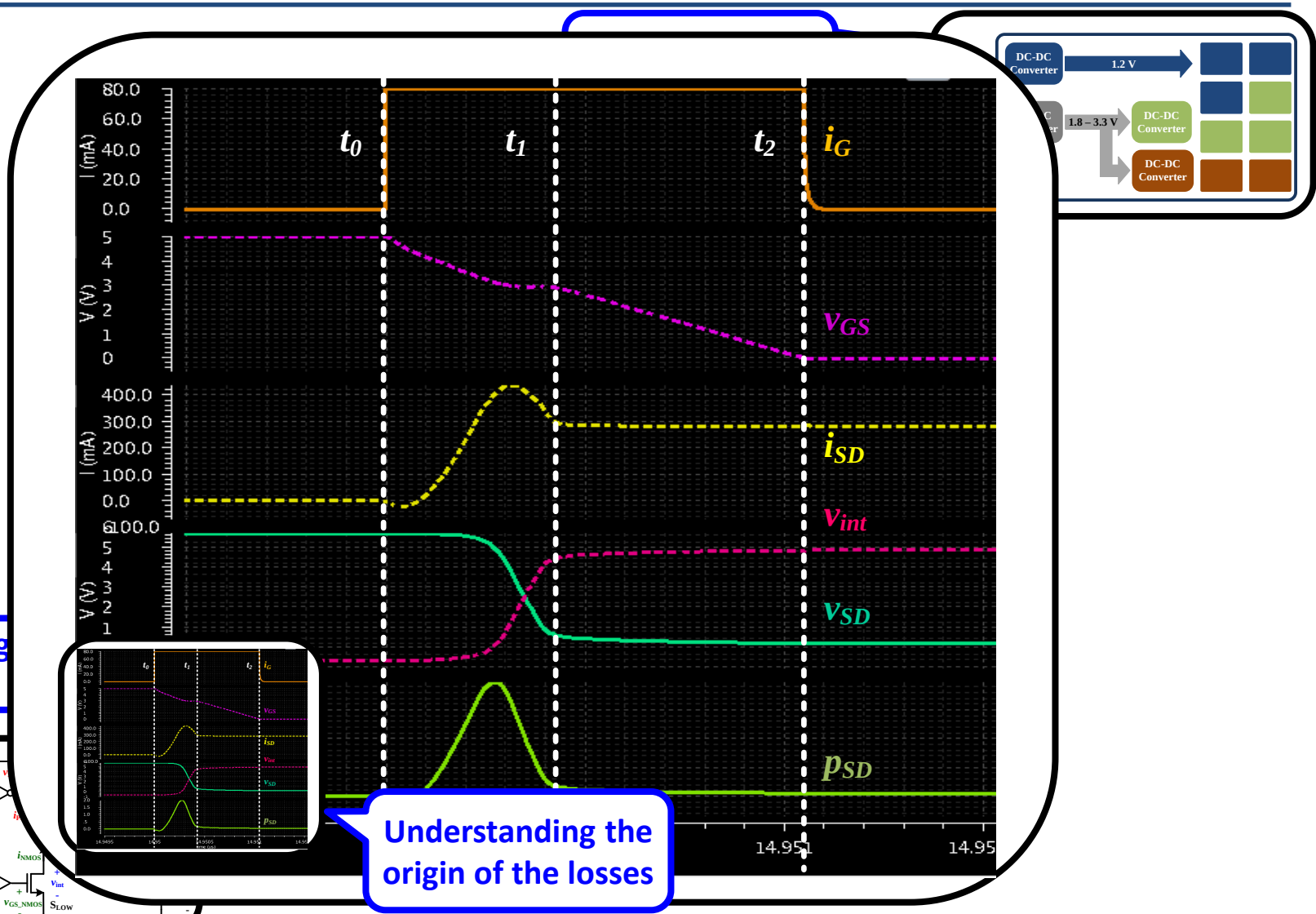


Defined Si tech

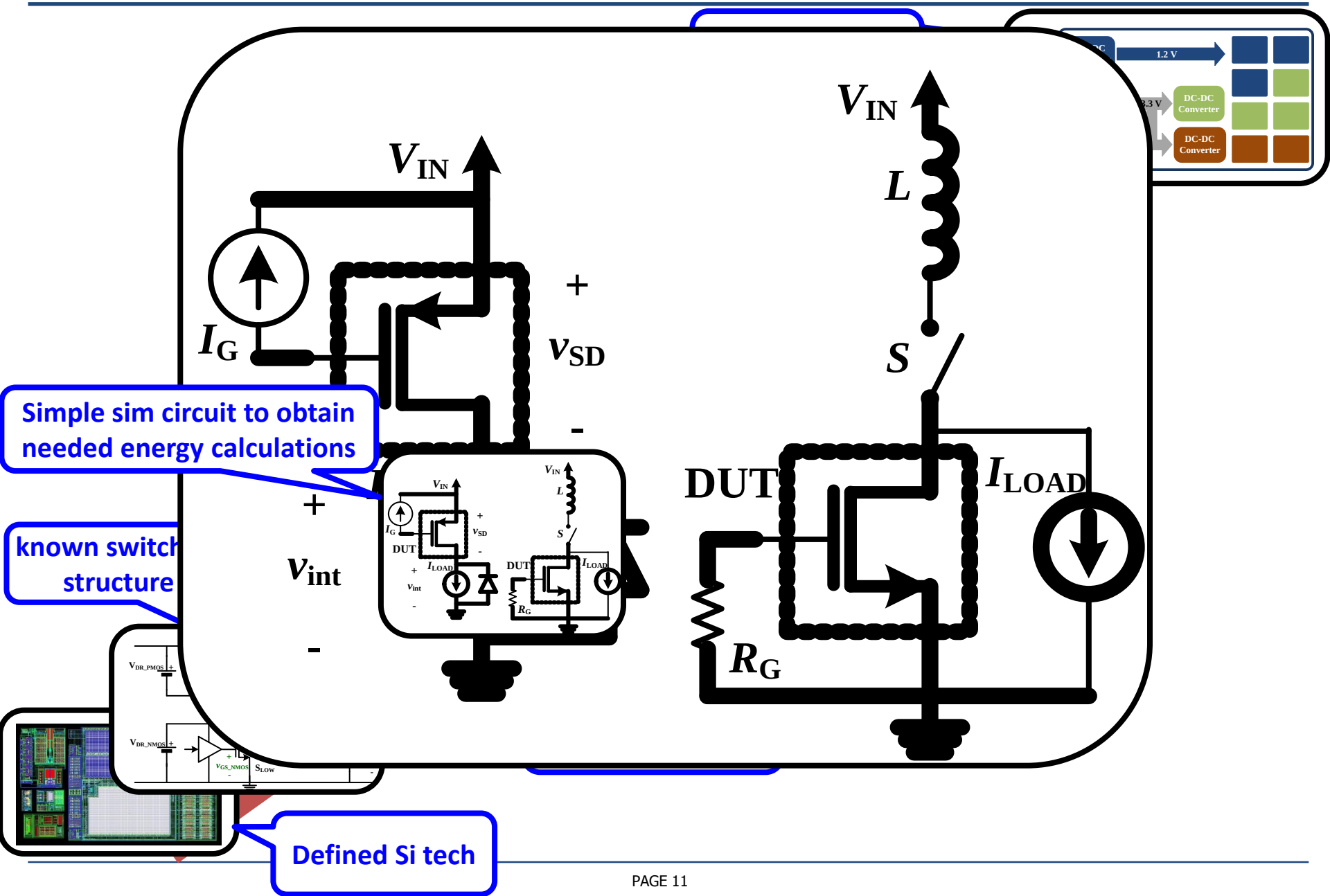
IC perspective



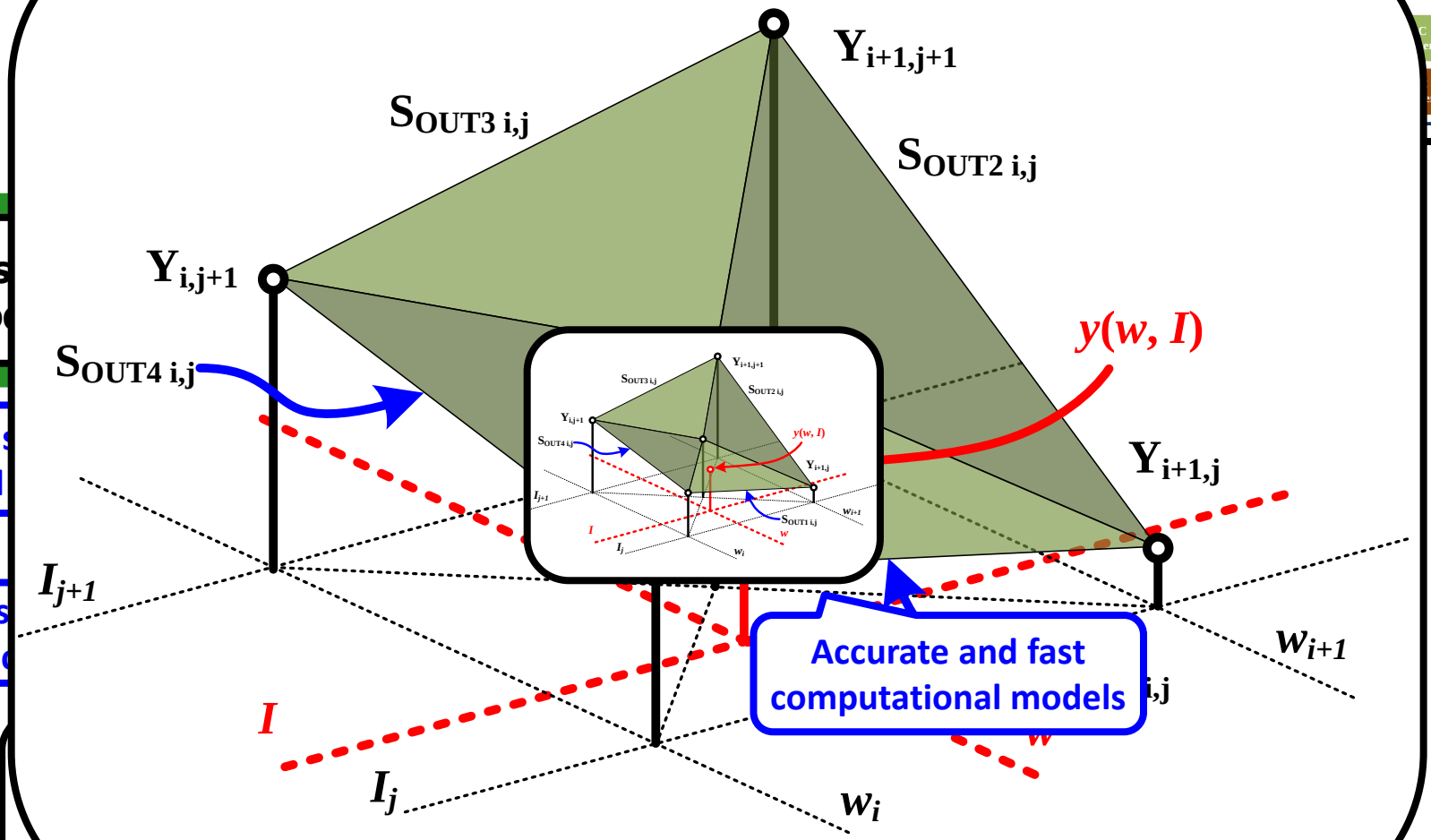
IC perspective



IC perspective



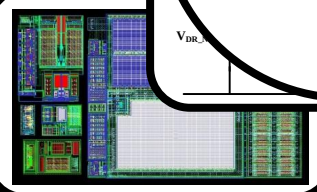
IC perspective



Pass
mo

Simple
needed

known
stru



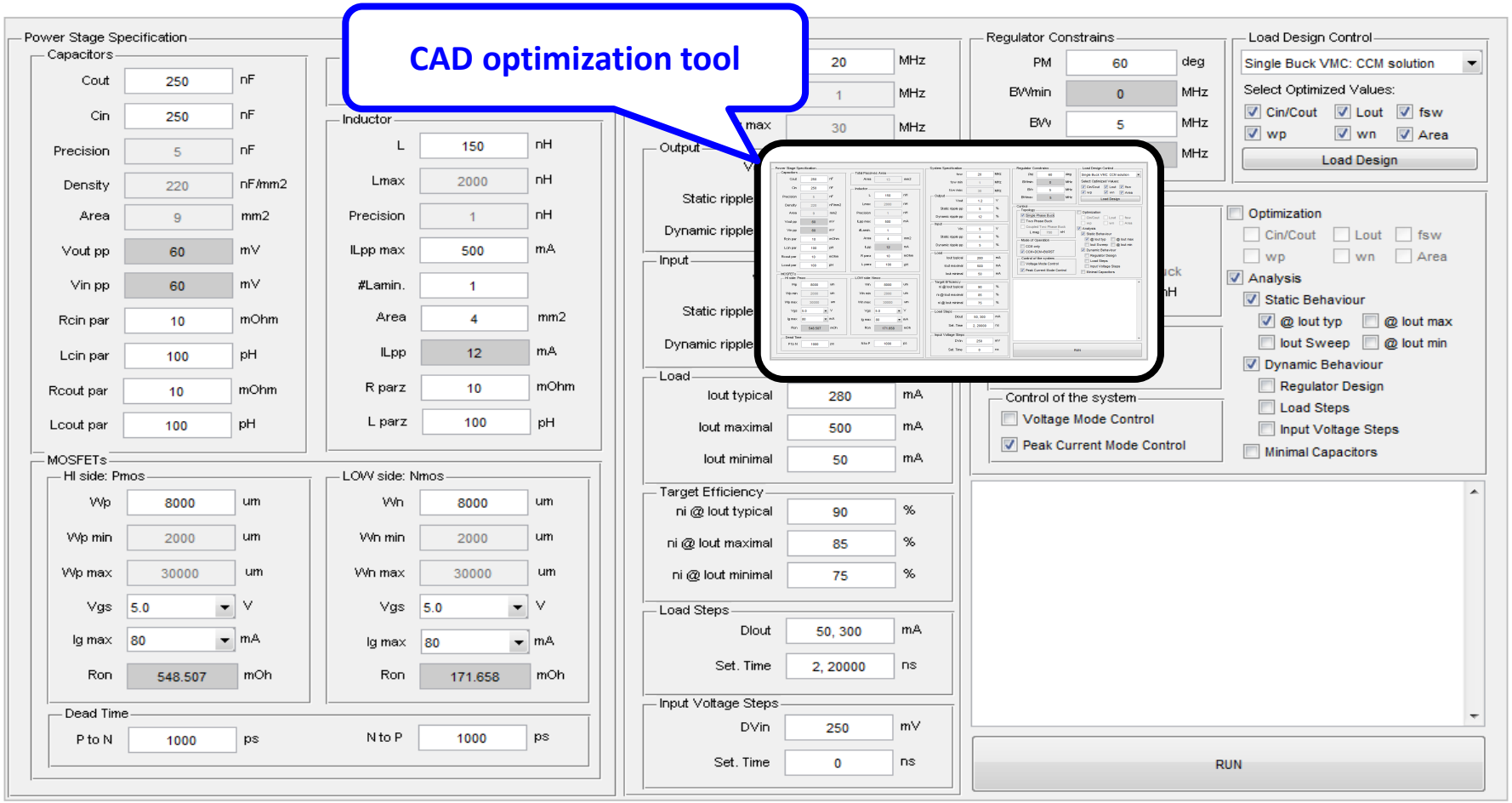
Defined Si tech

Control

PowerSoC perspective

Optimized

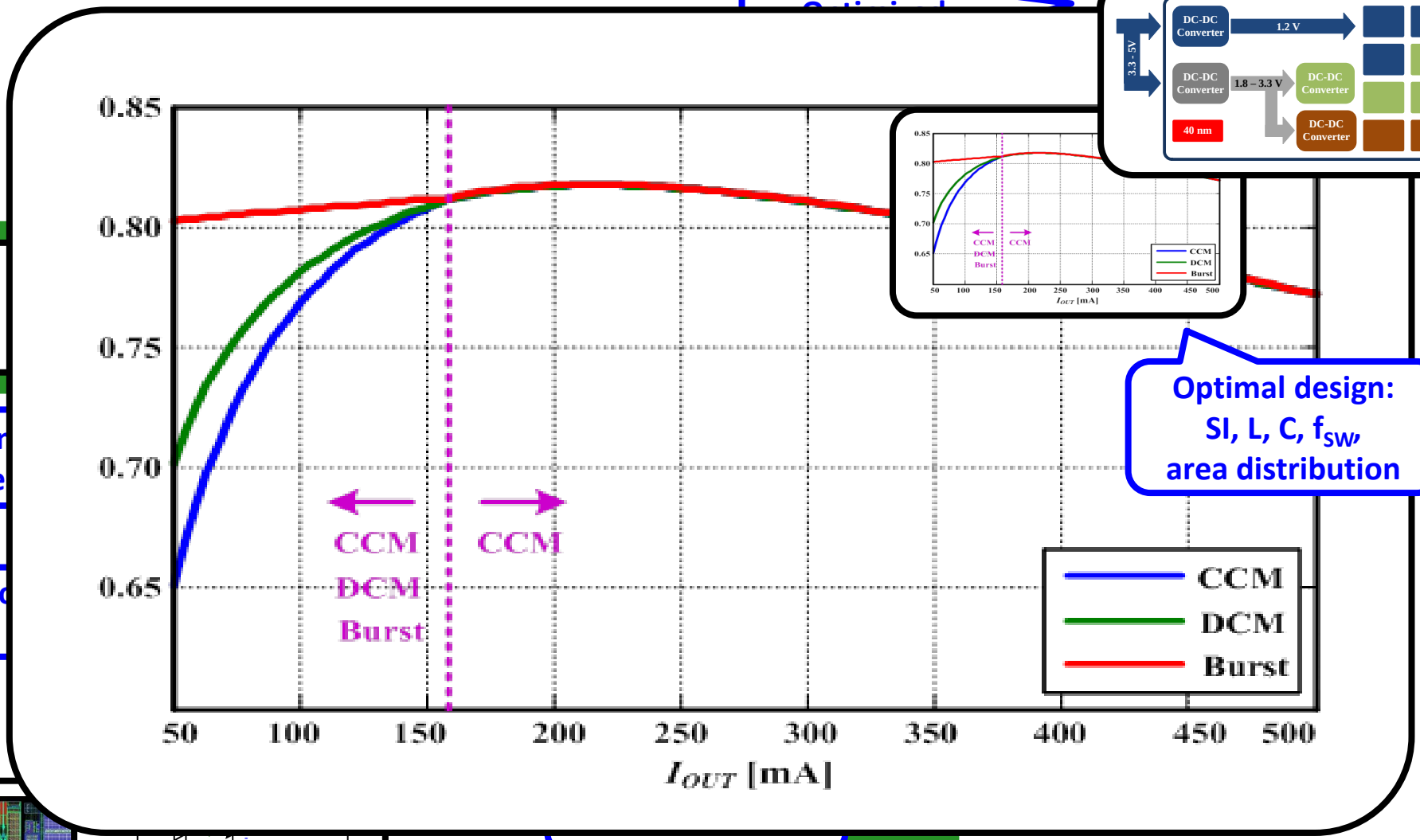
CAD optimization tool



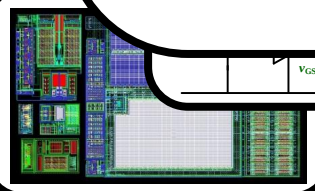
Defined Si tech

Control

PowerSoC perspective



Optimal design: SI, L, C, f_{SW}, area distribution

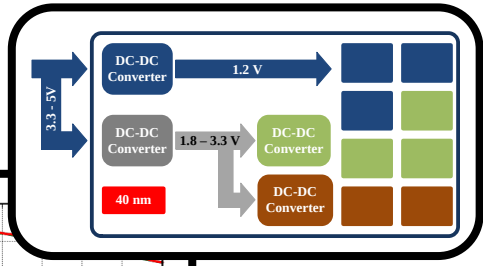


Defined Si tech

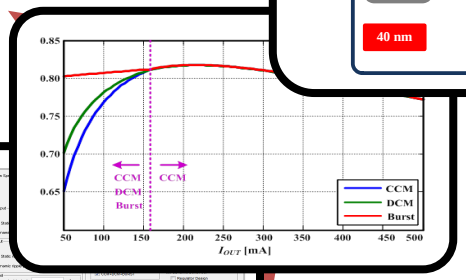
Control

PowerSoC perspective

Optimized PwrSoC



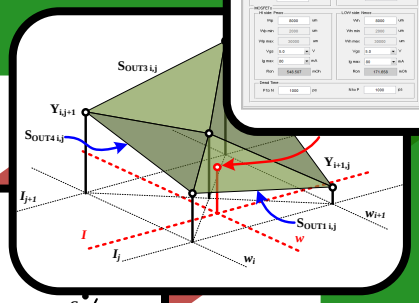
CAD optimization tool

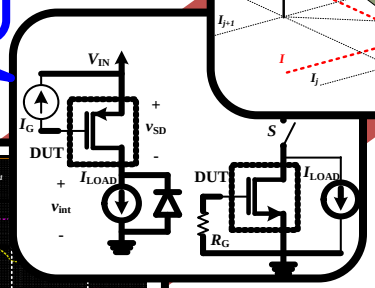


Passives models

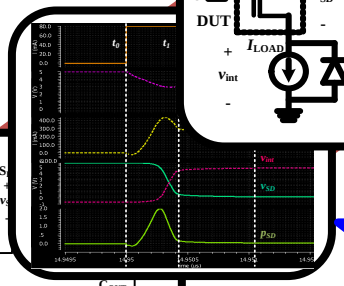
Optimal design: SI, L, C, f_{SW}, area distribution

Simple sim circuit to obtain needed energy calculations



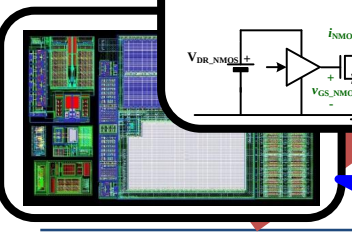


known switching structure



Accurate and fast computational models

Understanding the origin of the losses



Defined Si tech

Control

PowerSoC "design flow": Designer options

Specification

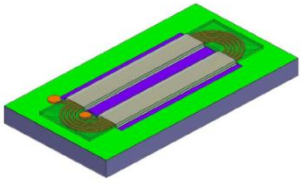
Technology

Topology

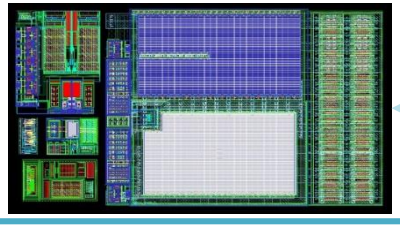
Control

Modes of operation

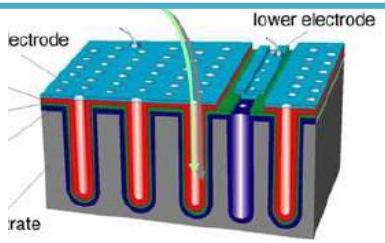
Inductor



Semiconductors



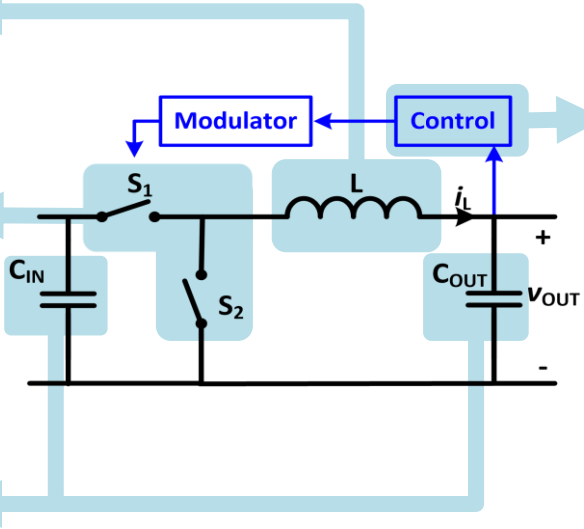
Capacitors



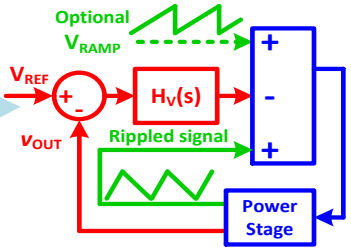
1-phase Buck converter
2-phase Buck converter
2-phase coupled Buck converter

Voltage mode
Current mode
Ripple-based

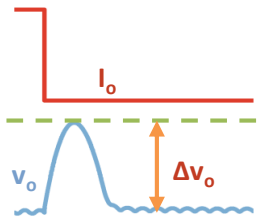
Modulation strategy
CCM
DCM
Light-load mode



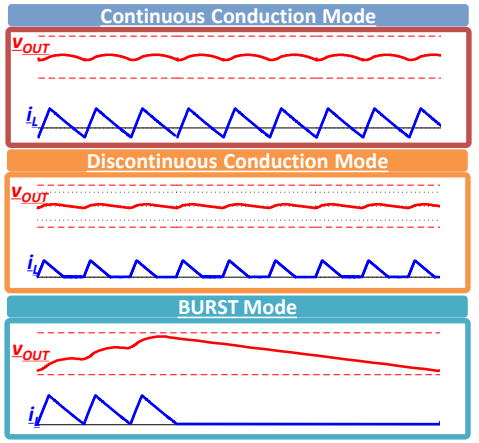
Ripple-based



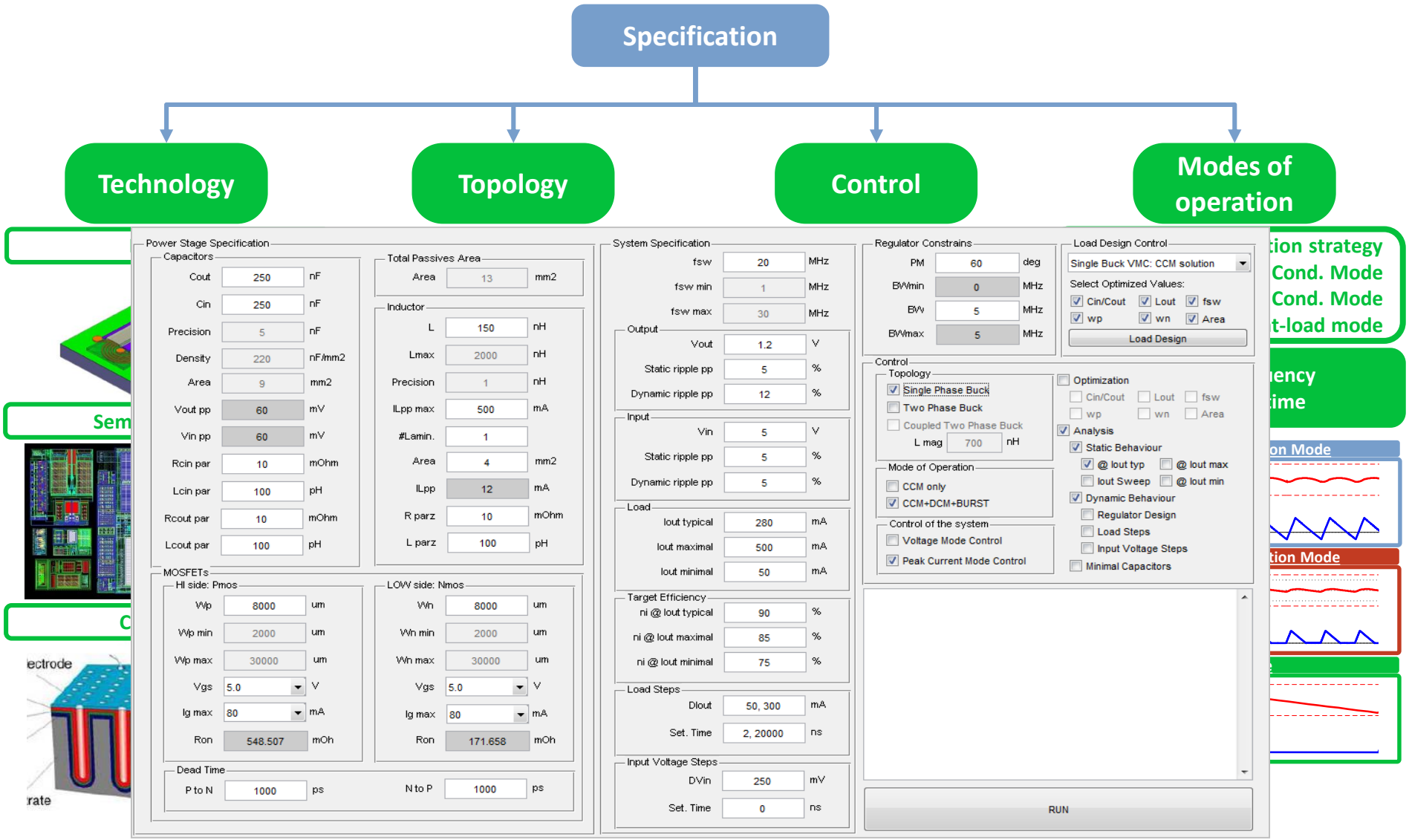
Load-steps



Constant frequency
Constant on-time



PowerSoC "design flow": Designer options

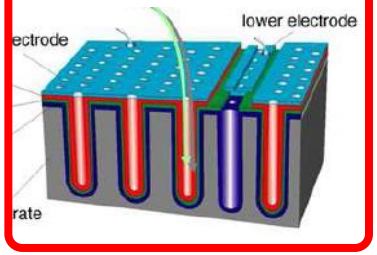


CAD GUI

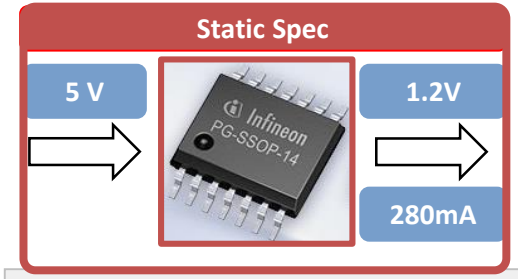

Power Stage Specification
Capacitors
Cout 250 nF
Cin 250 nF
Precision 5 nF
Density 220 nF/mm2
Area 9 mm2
Vout pp 60 mV
Vin pp 60 mV
Rcin par 10 mOhm
Lcin par 100 pH
Rcout par 10 mOhm
Lcout par 100 pH
Total Passives Area
Area 13 mm2
Inductor
L 150 nH
Lmax 2000 nH
Precision 1 nH
ILpp max 500 mA
#Lamin. 1
Area 4 mm2
ILpp 12 mA
R parz 10 mOhm
L parz 100 pH
MOSFETs
HI side: Pmos
Wp 8000 um
Wp min 2000 um
Wp max 30000 um
Vgs 5.0 V
Ig max 80 mA
Ron 548.507 mOh
LOW side: Nmos
Wn 8000 um
Wn min 2000 um
Wn max 30000 um
Vgs 5.0 V
Ig max 80 mA
Ron 171.658 mOh
Dead Time
P to N 1000 ps
N to P 1000 ps
System Specification
fsw 20 MHz
fsw min 1 MHz
fsw max 30 MHz
Output
Vout 1.2 V
Static ripple pp 5 %
Dynamic ripple pp 12 %
Input
Vin 5 V
Static ripple pp 5 %
Dynamic ripple pp 5 %
Load
Iout typical 280 mA
Iout maximal 500 mA
Iout minimal 50 mA
Target Efficiency
ni @ Iout typical 90 %
ni @ Iout maximal 85 %
ni @ Iout minimal 75 %
Load Steps
Dlout 50, 300 mA
Set. Time 2, 20000 ns
Input Voltage Steps
DVin 250 mV
Set. Time 0 ns
Regulator Constrains
PM 60 deg
BWmin 0 MHz
BW 5 MHz
BWmax 5 MHz
Load Design Control
Single Buck VMC: CCM solution
Select Optimized Values:
Cin/Cout Lout fsw
wp wn Area
Load Design
Control
Topology
Single Phase Buck
Two Phase Buck
Coupled Two Phase Buck
L mag 700 nH
Mode of Operation
CCM only
CCM+DCM+BURST
Control of the system
Voltage Mode Control
Peak Current Mode Control
Optimization
Cin/Cout Lout fsw
wp wn Area
Analysis
Static Behaviour
@ Iout typ @ Iout max
Iout Sweep @ Iout min
Dynamic Behaviour
Regulator Design
Load Steps
Input Voltage Steps
Minimal Capacitors
RUN

CAD GUI

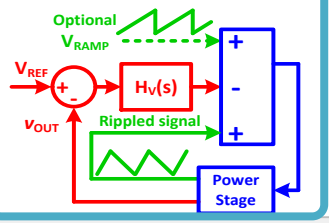
Capacitors



Static Spec

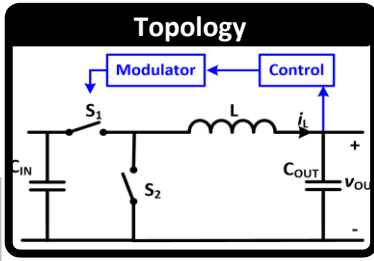


Regulator Constraints

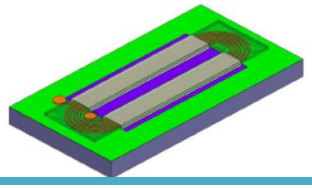


Load Design

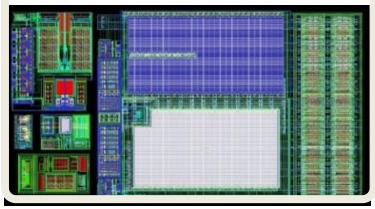
Topology



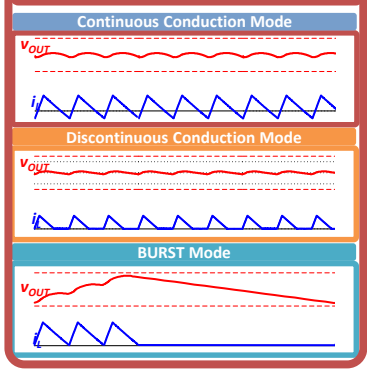
Inductor



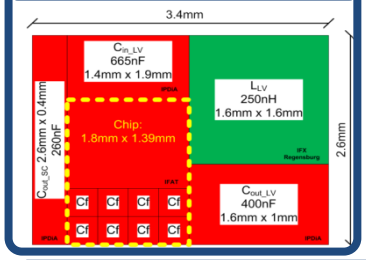
Semiconductors



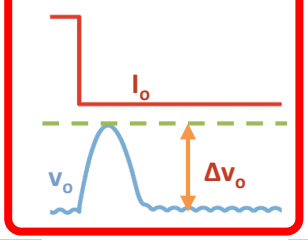
Operating Mode



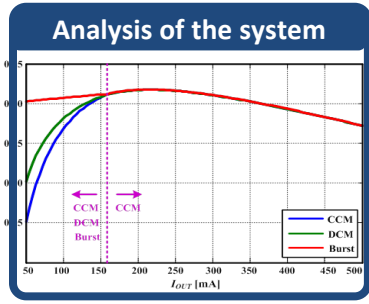
Total Area



Dynamic Spec

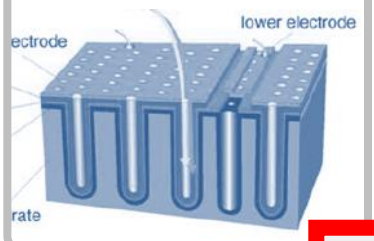


Analysis of the system

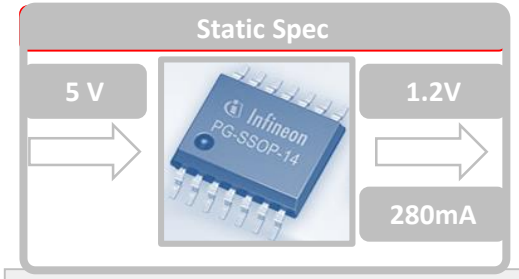


CAD GUI

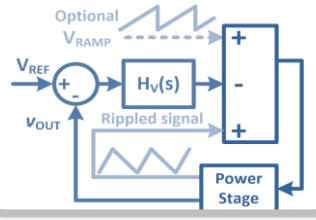
Capacitors



Static Spec

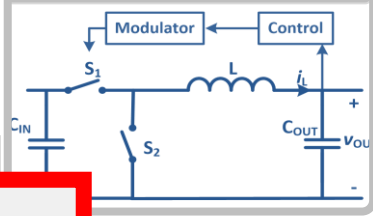


Regulator Constraints

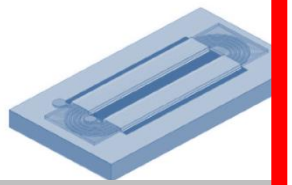


Load Design

Topology



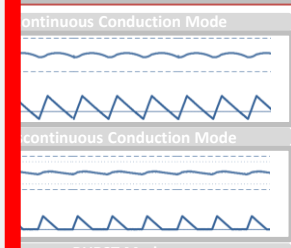
Inductor



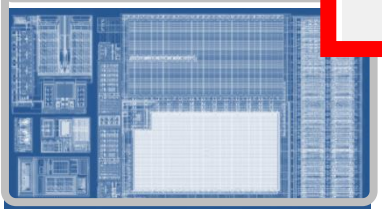
Optimization

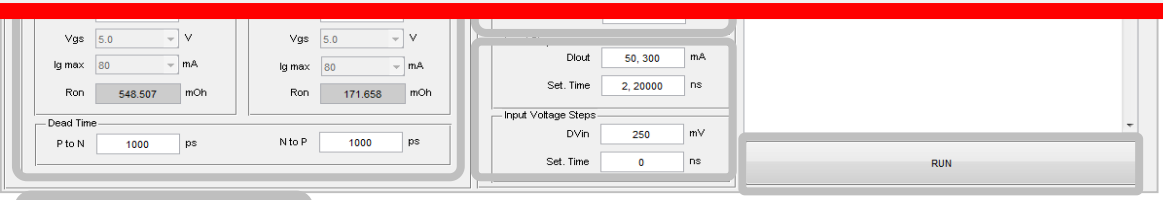
- Optimization
- Cin/Cout
- Lout
- fsw
- wp
- wn
- Area

Operating Mode

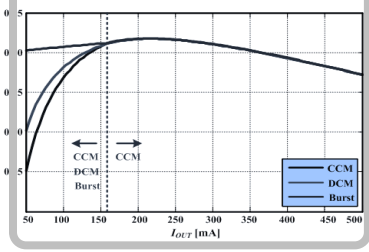


Semiconductors

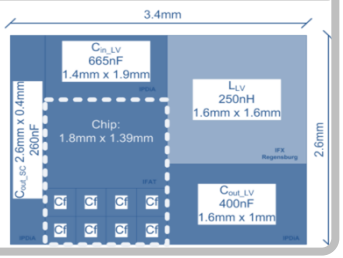




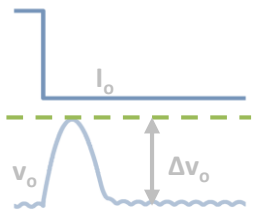
Analysis of the system

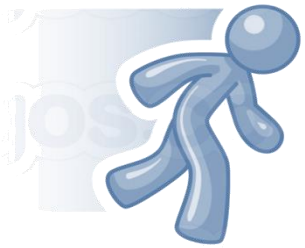


Total Area

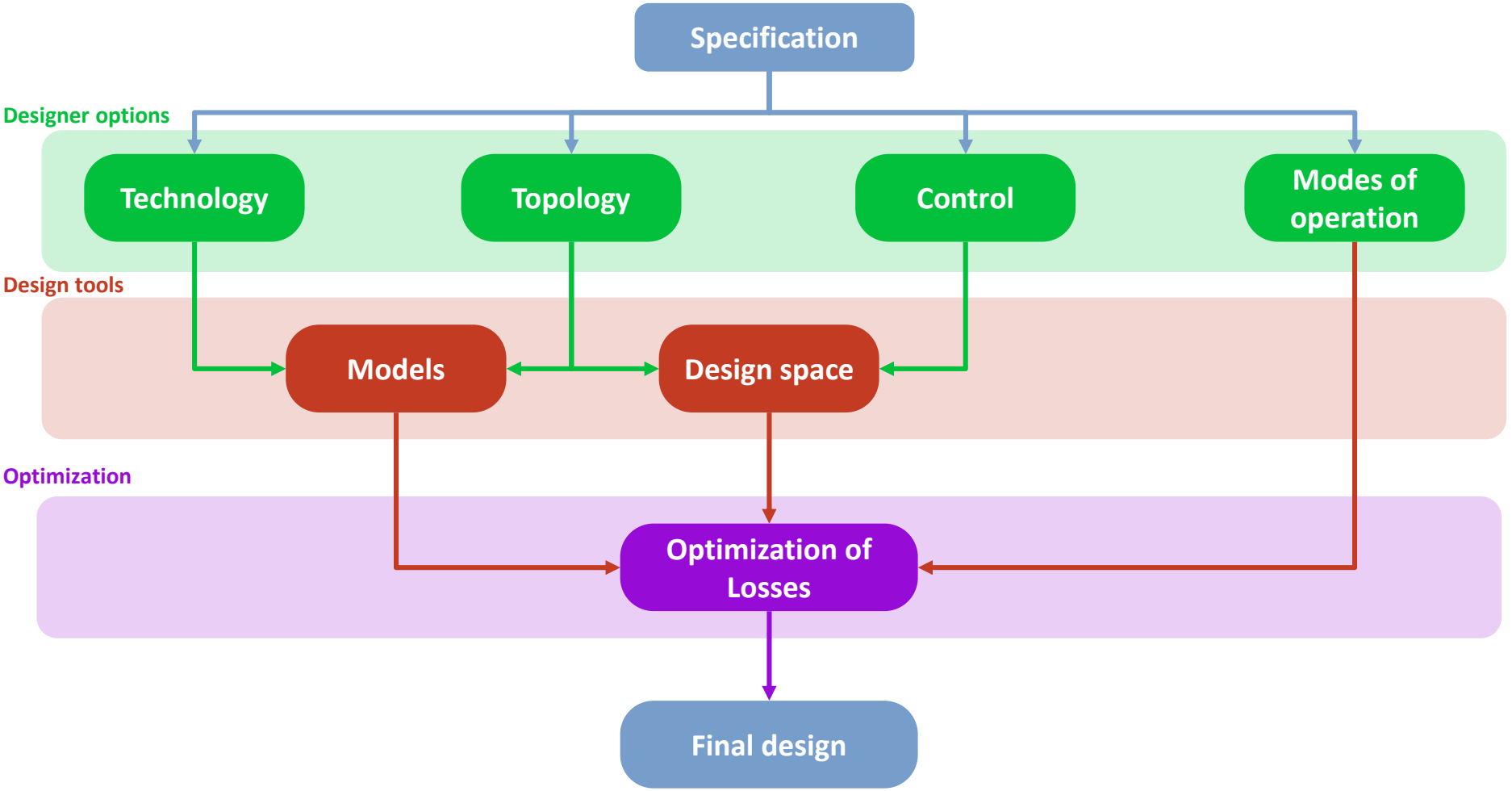


Dynamic Spec

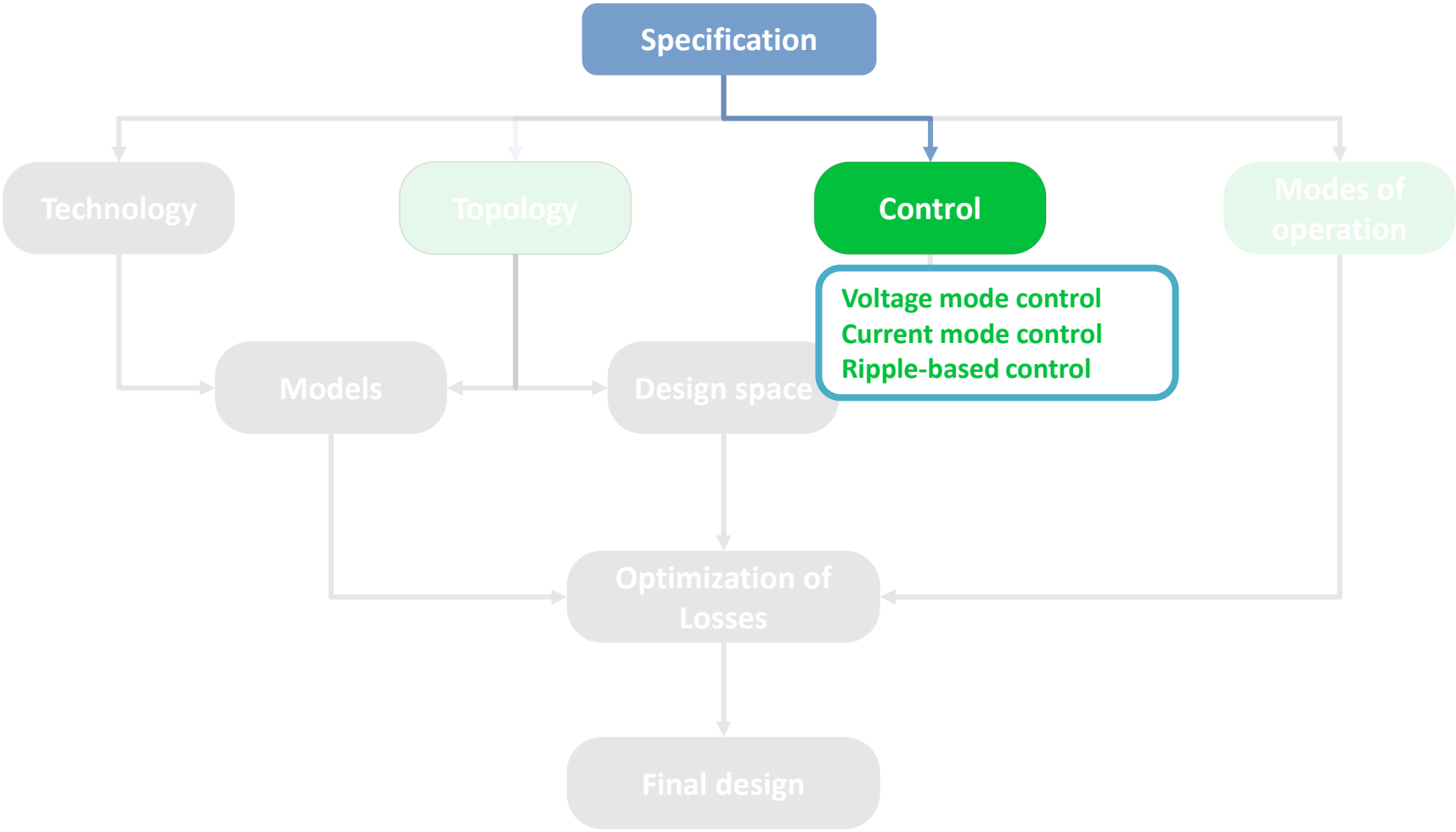




Design Flow

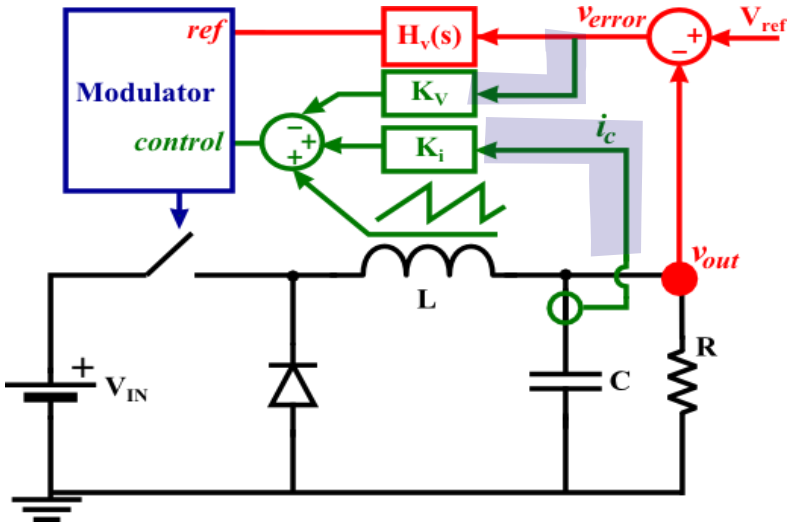

Specification
Designer options
Technology
Topology
Control
Modes of operation
Design tools
Models
Design space
Optimization
Optimization of Losses
Final design

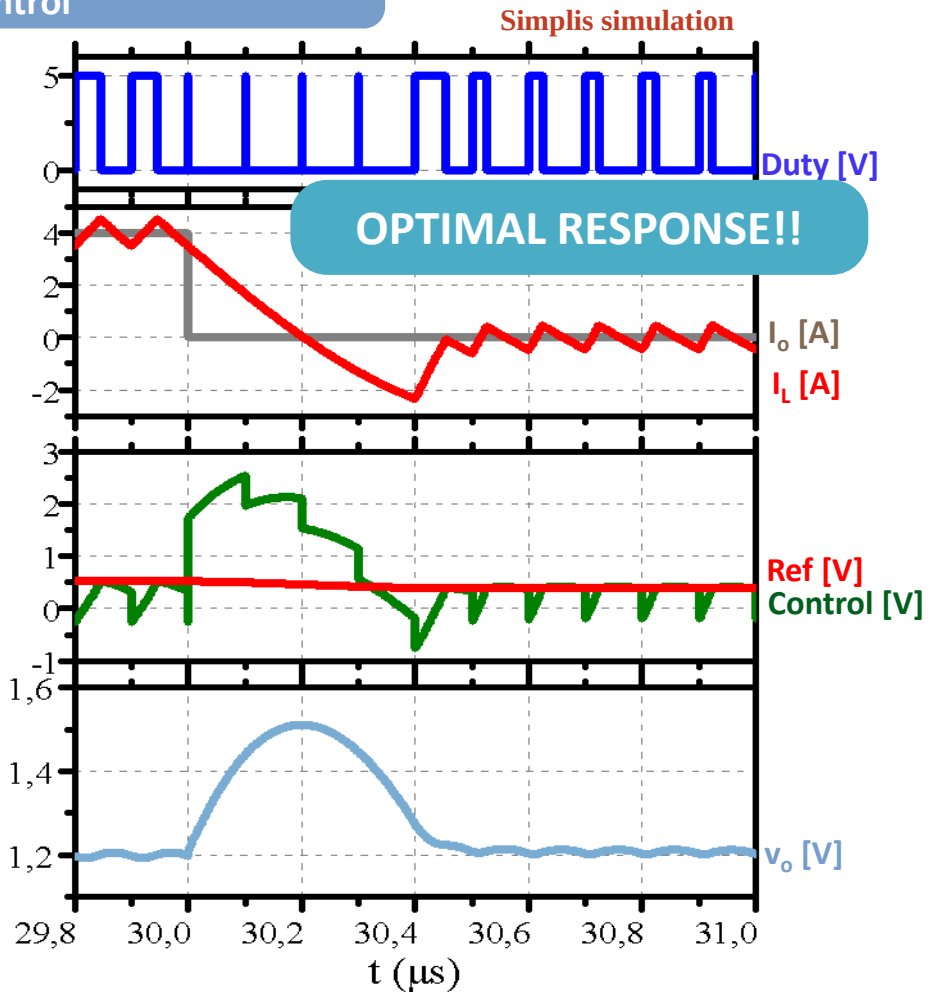
Design Flow


Specification
Technology
Topology
Control
Modes of operation
Voltage mode control
Current mode control
Ripple-based control
Models
Design space
Optimization of Losses
Final design

Ripple based Control

V^2I_c control





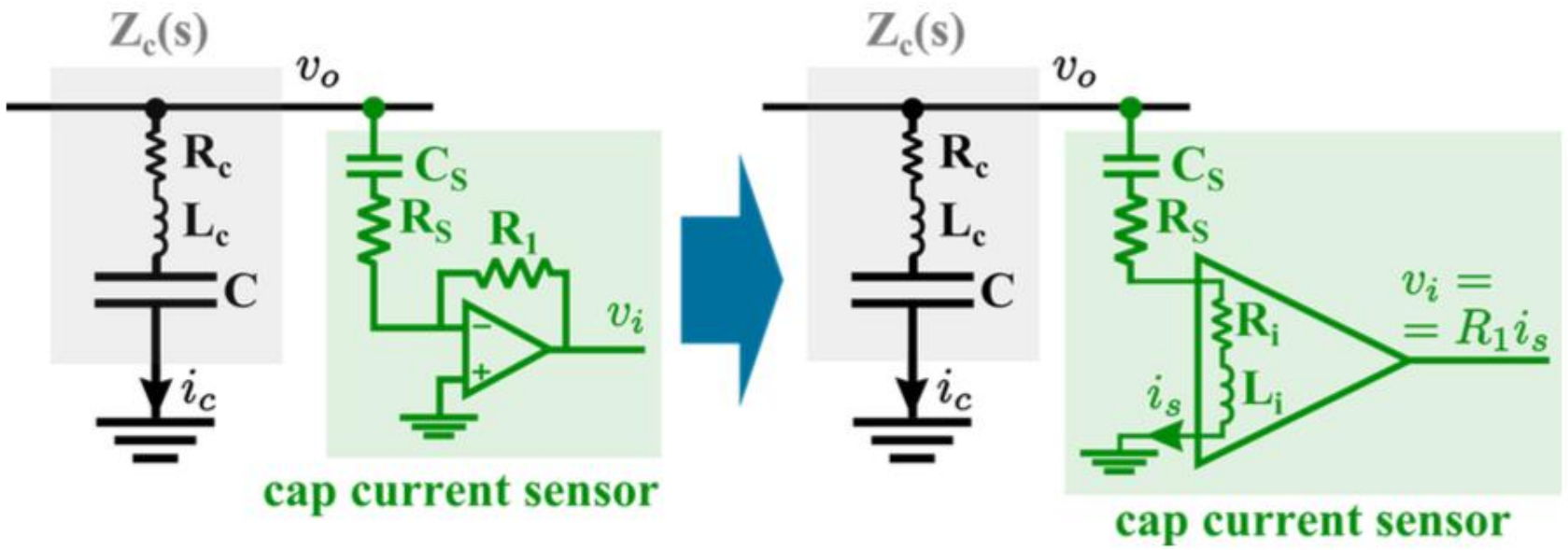
✓ Very fast even with low ESR caps

Feedforward of:
- Output current
- Voltage reference

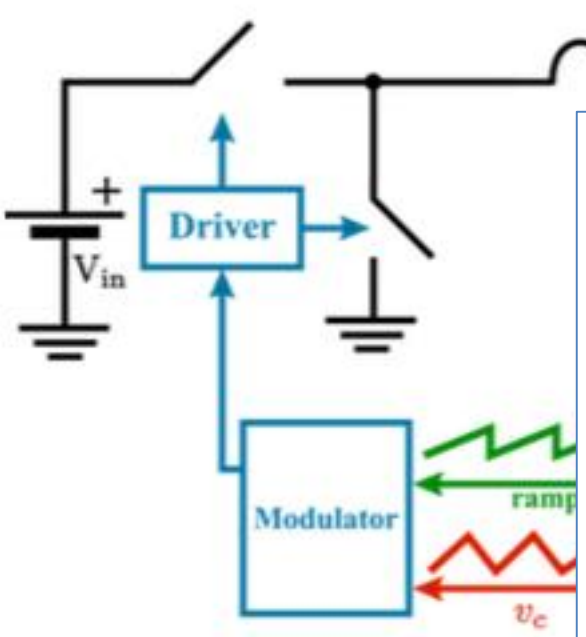
✗ Complex analysis, SIMPLE implementation

Del Viejo, M.; Alou, P.; Oliver, J.A.; Garcia, O.; Cobos, J.A., "V^2IC control: A novel control technique with very fast response under load and voltage steps," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.231,237, 6-11 March 2011

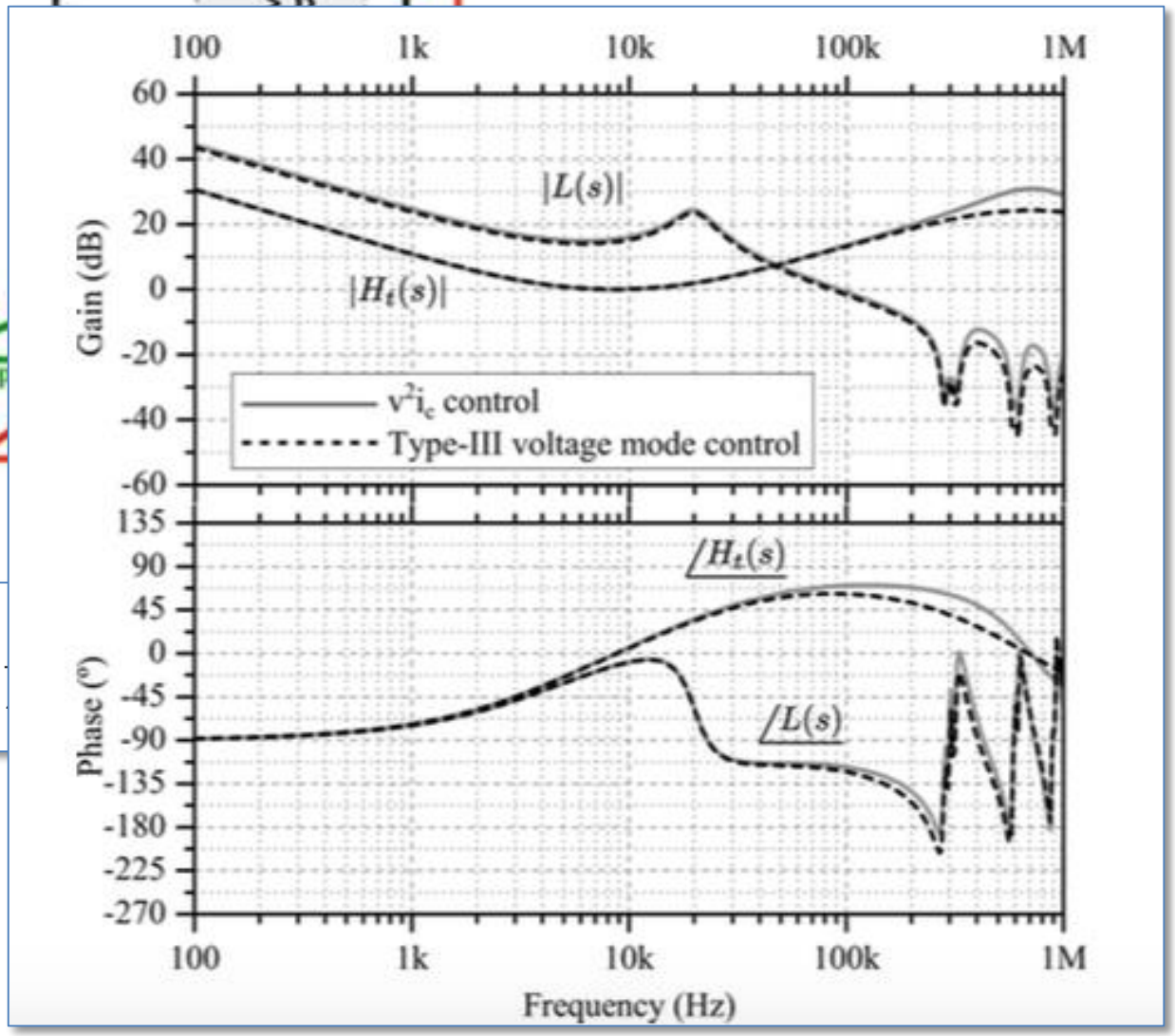
EASY implementation



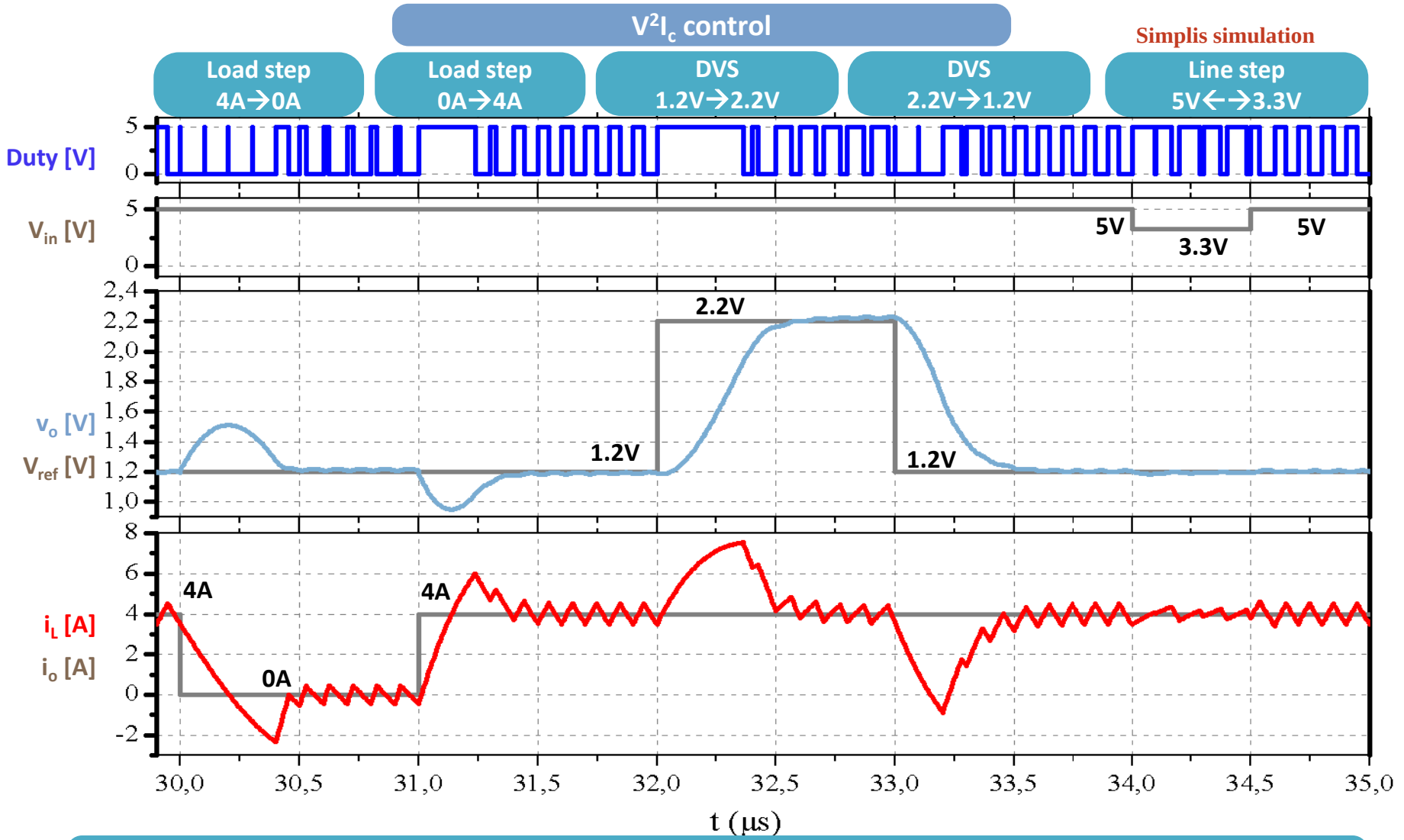
V^1 concept



$$H_t(s) = A_0/s + K_v + K_i$$

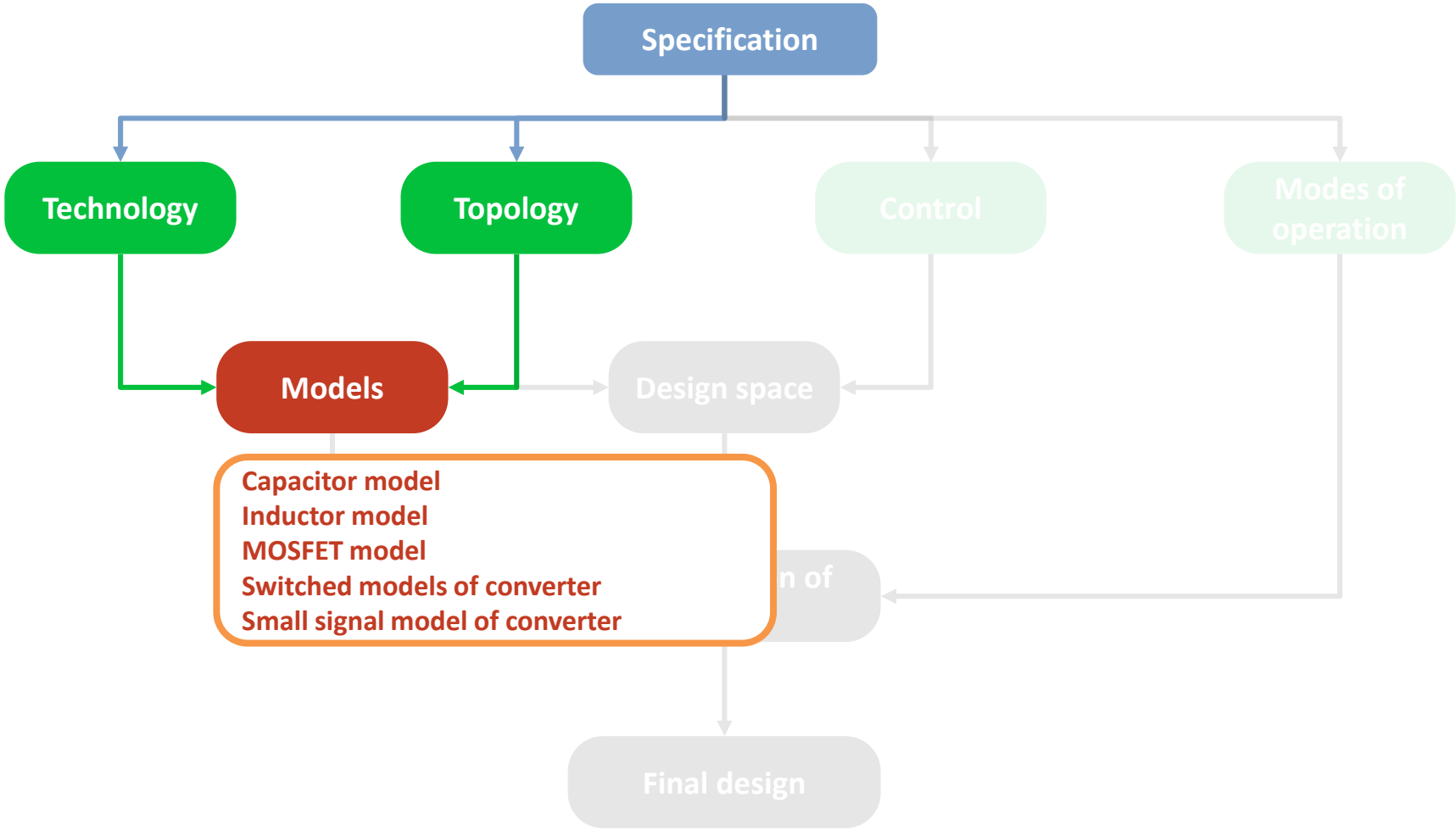


Control: V^2I_c

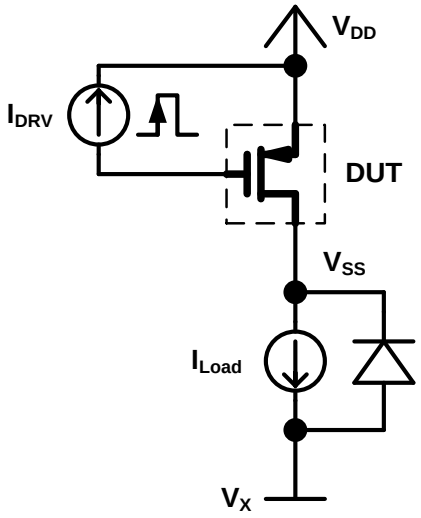


ALMOST OPTIMAL RESPONSES IN ALL TRANSIENTS

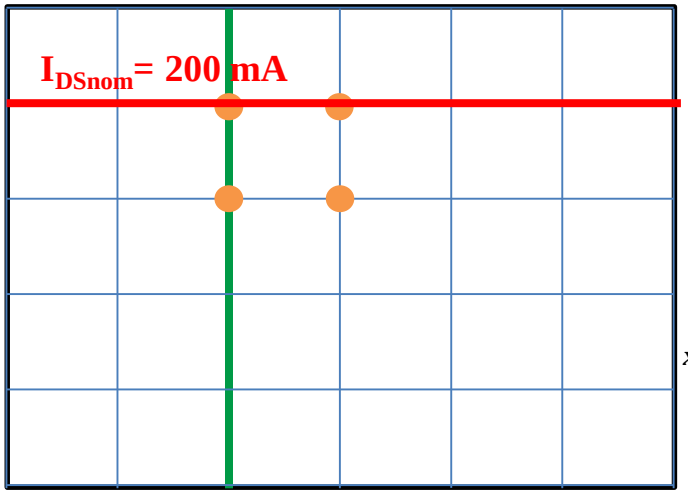
Design Flow


Specification
Technology
Topology
Control
Modes of operation
Models
Design space
Capacitor model
Inductor model
MOSFET model
Switched models of converter
Small signal model of converter
Final design

Models: MOSFETS

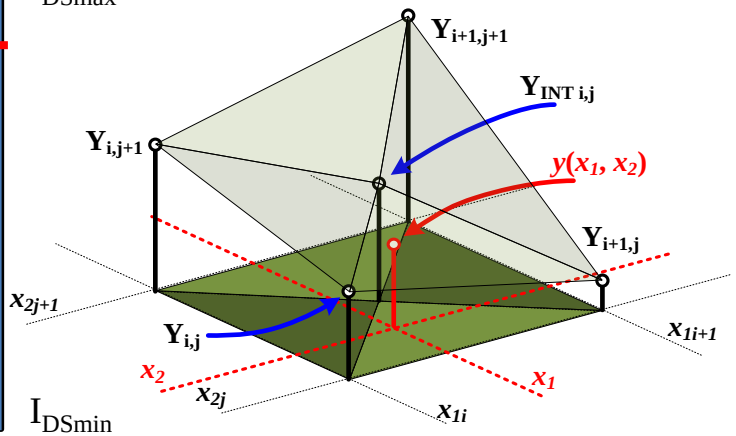


Optimization requires
"Low computational cost" model
based on accurate CADENCE simulations,
mapping the whole design space



I_{DSmax}

I_{DSmin}

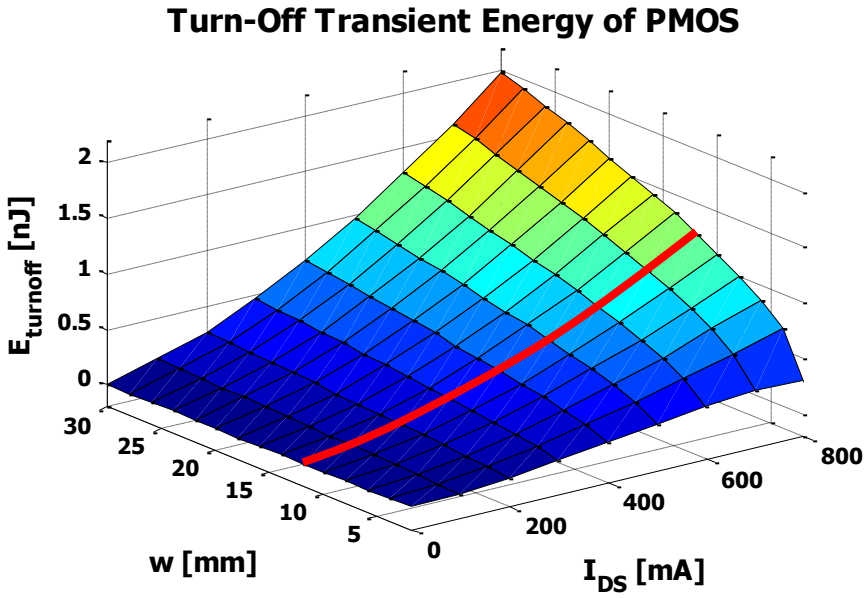


(w_{Pmin}, w_{Nmin}) (w_{Pmax}, w_{Nmax})

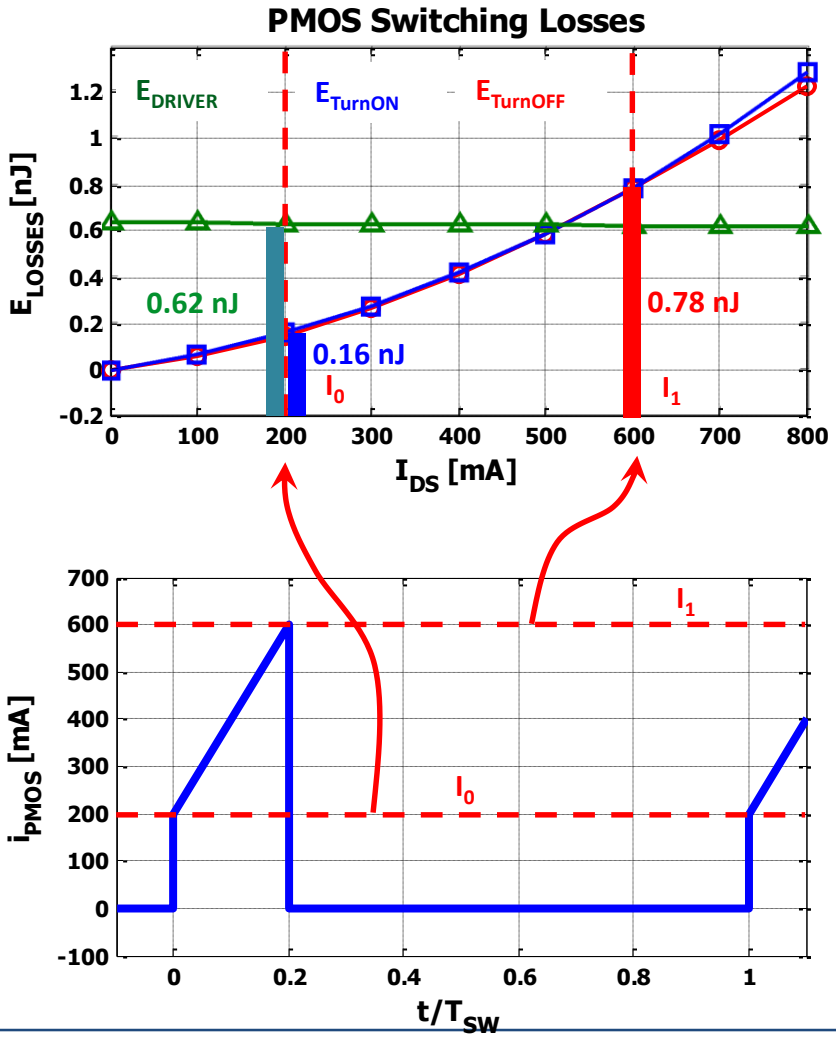
w_{Pnom}=10.6mm
w_{Nnom}=10.8mm

Svikovic, V.; Cortes, J. ; Alou, P. ; Oliver, J. ; Cobos, J.A. ; Maderbacher, G. ; Sandner, C.
"Energy-Based switches losses model for the optimization of PwrSoC buck converter", COMPEL 2014

Example: HI-Side



Circuit waveform to quickly calculate losses in the optimization algorithm



f_{SW} = 10 MHz

$P_{TurnOFF}$ = 7.86 mW

P_{TurnON} = 1.6 mW

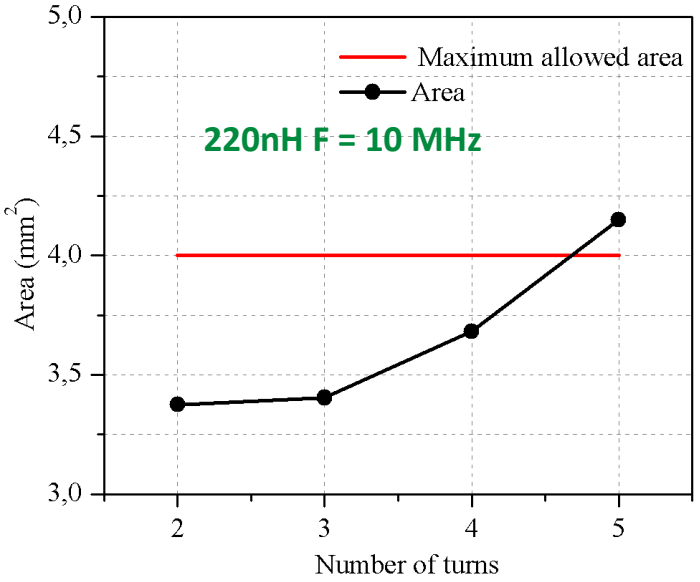
P_{Driver} = 6.25 mW

$I_{PMOSrms}$ = 186.2 mA

R_{PMOSon} = 410 mΩ

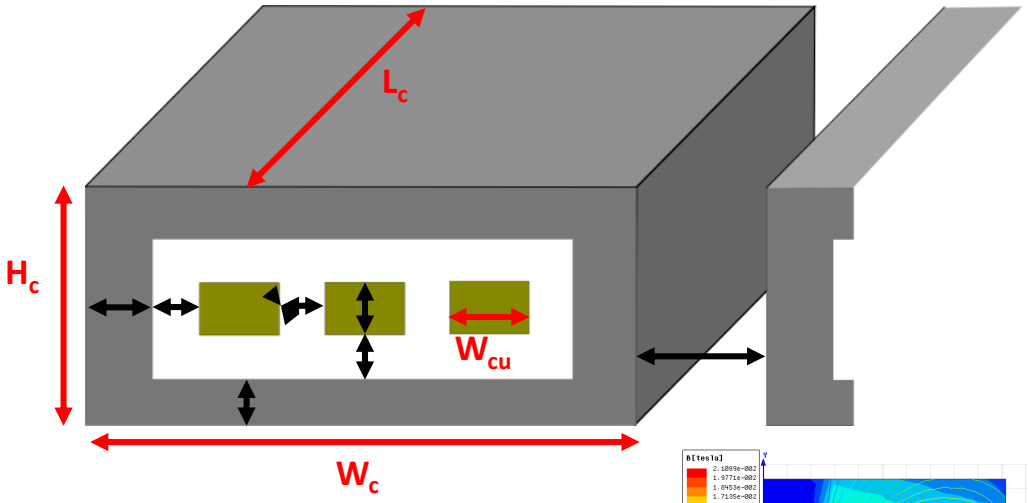
P_{COND} = 14.2 mW

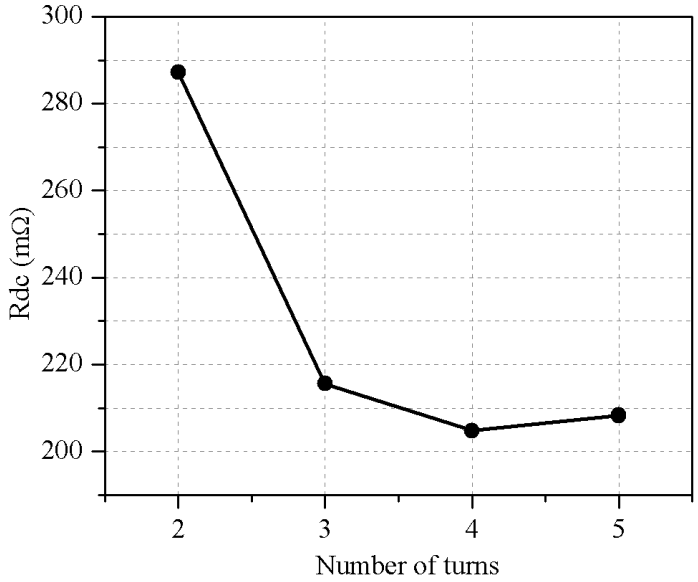
Inductor Optimization

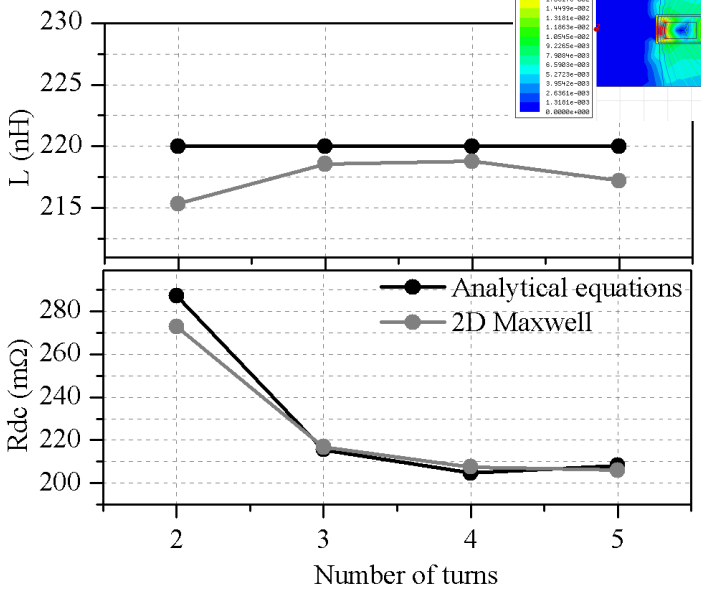


— fixed dimensions

— degrees of freedom





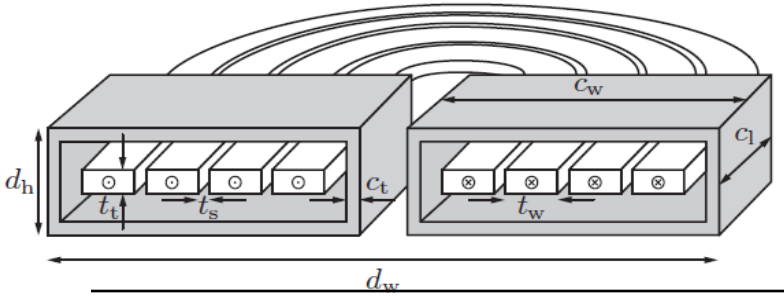


Models: Inductors

Racetrack inductor

Geometry design

Core inductance
Self inductance of wires



Symbol	Description
N	Number of turns
t_w	Winding width
c_t	Winding thickness
c_s	Winding spacing
c_w	Core width
c_t	Core thickness
c_l	Core length
d_h	Device height
d_w	Device width
d_l	Device length

Losses calculation

Copper losses
Hysteresis losses
Eddy current losses

T.M. Andersen, C.M. Zingerli, F. Krismer, J.W. Kolar, Ningning Wang and C.O. Mathuna, "*Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip*," Power Electronics, IEEE Transactions on , vol.28, no.9, pp.4422,4430, Sept. 2013

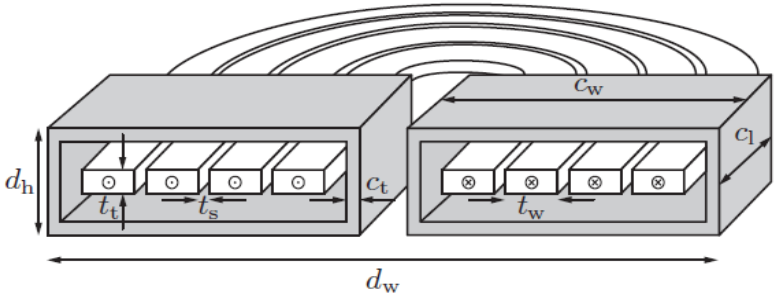
Tyndall National Institute | ETH zürich

Models: Inductors

Geometry design

Geometry design

Core inductance
Self inductance of wires



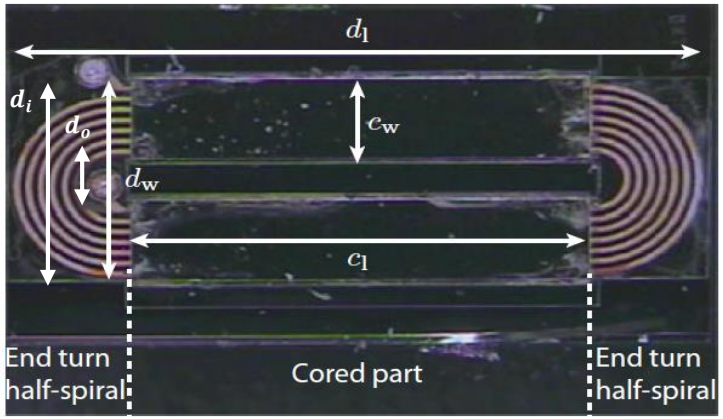
Core inductance

$$L_{core} = 2\frac{\mu_o \mu_c N^2 A_c}{l_m} = \frac{\mu_o \mu_c N^2 c_t c_l}{c_w + d_h}$$

Self-inductance of wires

$$L_{t,self} \approx 0.2 c_l \left[\ln\left(\frac{2c_l}{t_w + t_t}\right) + \frac{1}{2}\right]$$

Inductance of core-less spirals



$$L_{t,spiral} \approx \frac{\mu_o N^2 d_{avg}}{2} 0.2 c_l \left[\ln\left(\frac{2.46}{p}\right) + 0.2p^2\right]$$

Average diameter

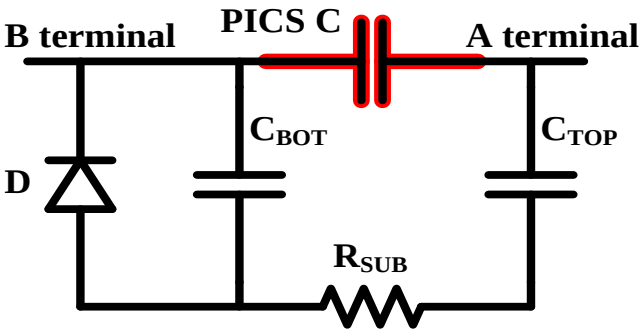
$$d_{avg} = \frac{d_o + d_i}{2}$$

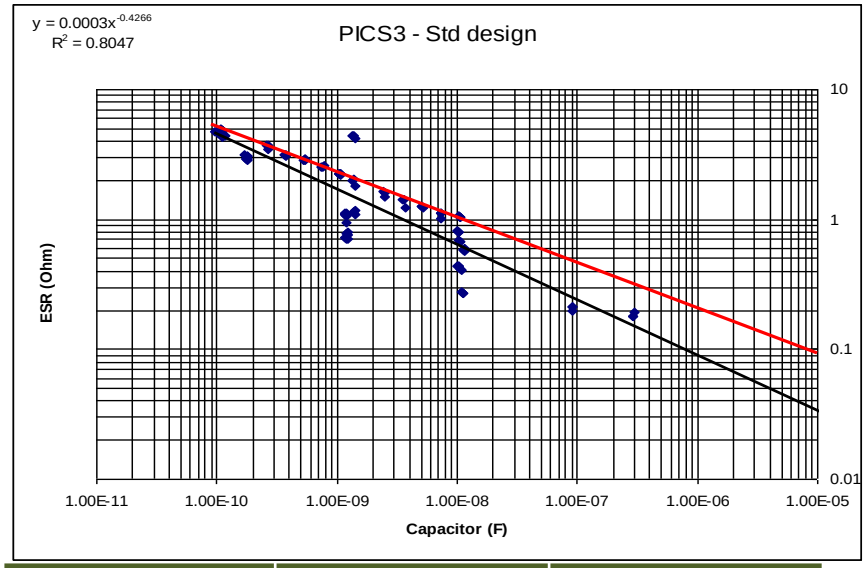
Fill factor

$$p = \frac{d_o - d_i}{d_o + d_i}$$

$$L = L_{core} + L_{t,self} + L_{t,spiral}$$

Models: Capacitors – Spice Model

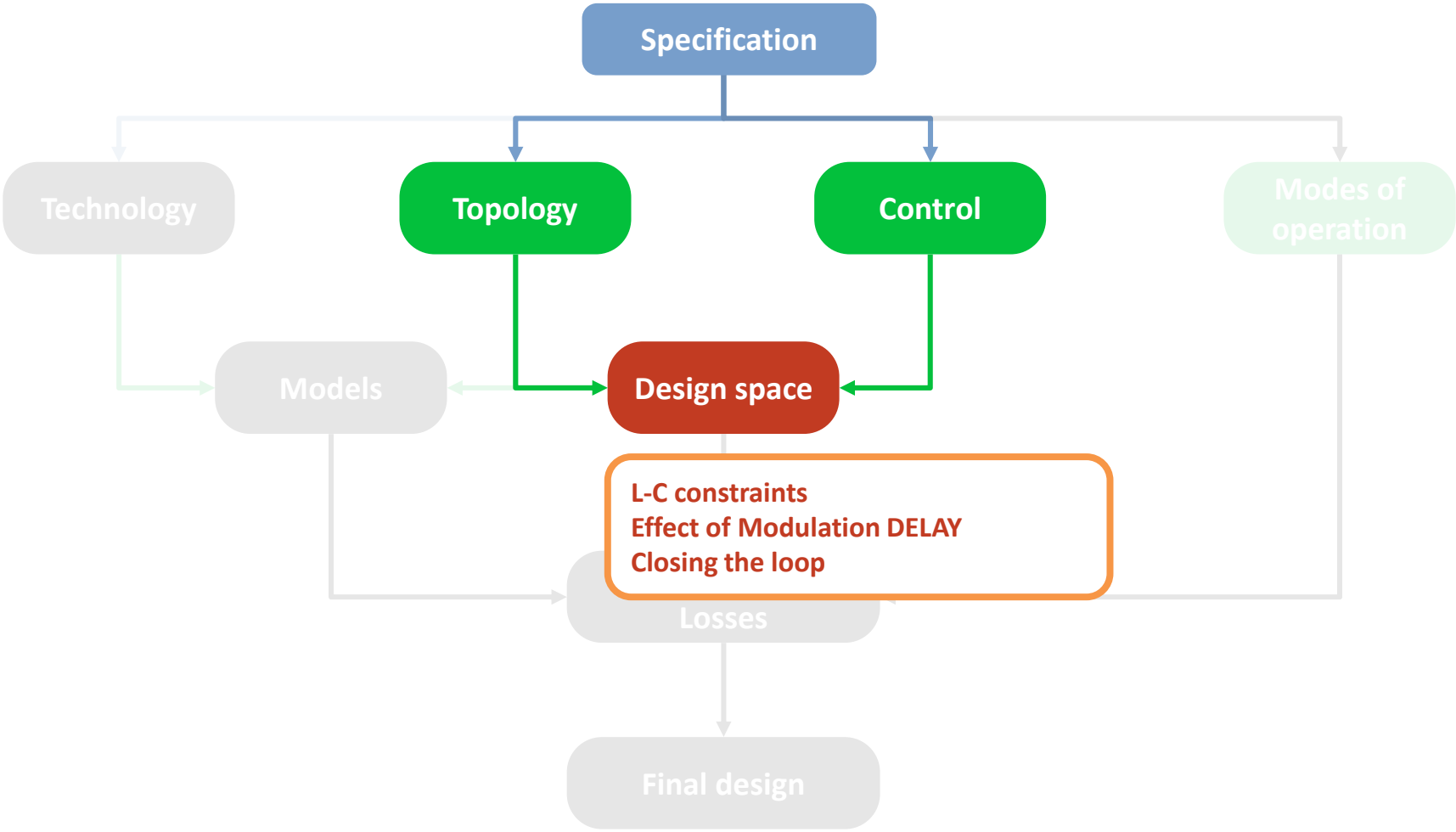




	Parameters	min	typical	max
Capacitors	Pits Capacitance [nF/mm²]	200	250	300
	Planar capacitance [nF/mm²]	4	5.4	6.8
	Metal M1 to metal M2 [pF/mm²]	76	80	84
	Metal M1 to substrate [pF/mm²]	75	100	125
DIODE	Parameters			
	BV [V]	30		
	IS [A]	1.83e-16*perimeter + 2.9e-15 * surface		
	IBVL	2 * IS		
	M	0.3		
	CJ0 [pF/mm²]	10		
	EG [eV]	1.11		

Defined by

Design space



Design space: constraints

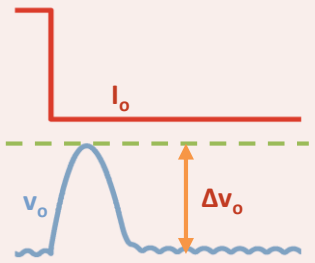
BUCK CONVERTER

Design decisions:

- Output capacitor
- Inductor filter
- Switching frequency
- Control
- Single-phase / Multi-phase

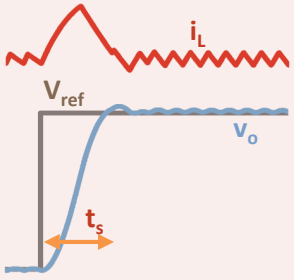
Constraints

Load transients



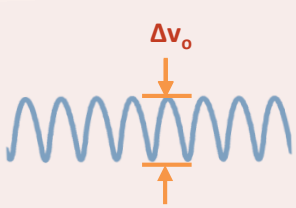
$$\Delta v_o \sim cte \cdot \frac{L}{C}$$

Voltage reference tracking



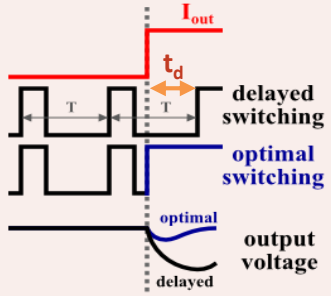
$$t_s \sim cte \cdot \sqrt{LC}$$

Static ripple



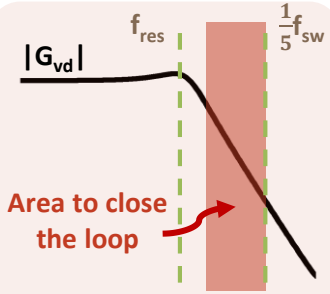
$$\Delta v_o \sim cte \cdot \frac{1}{f_{sw}} \cdot \frac{1}{LC}$$

Modulation delays



$$t_d \sim cte \cdot \frac{1}{f_{sw}}$$

Filter resonance in Voltage mode

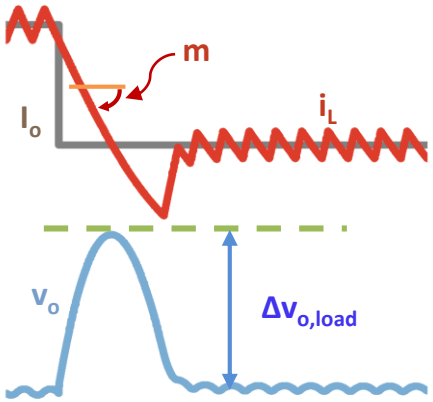


$$f_{res} \sim cte \cdot f_{sw} \cdot \frac{1}{\sqrt{LC}}$$

Design space: load transient

Constraints

Load transients | Voltage reference tracking | Static ripple | Modulation delays | Filter resonance in Voltage mode

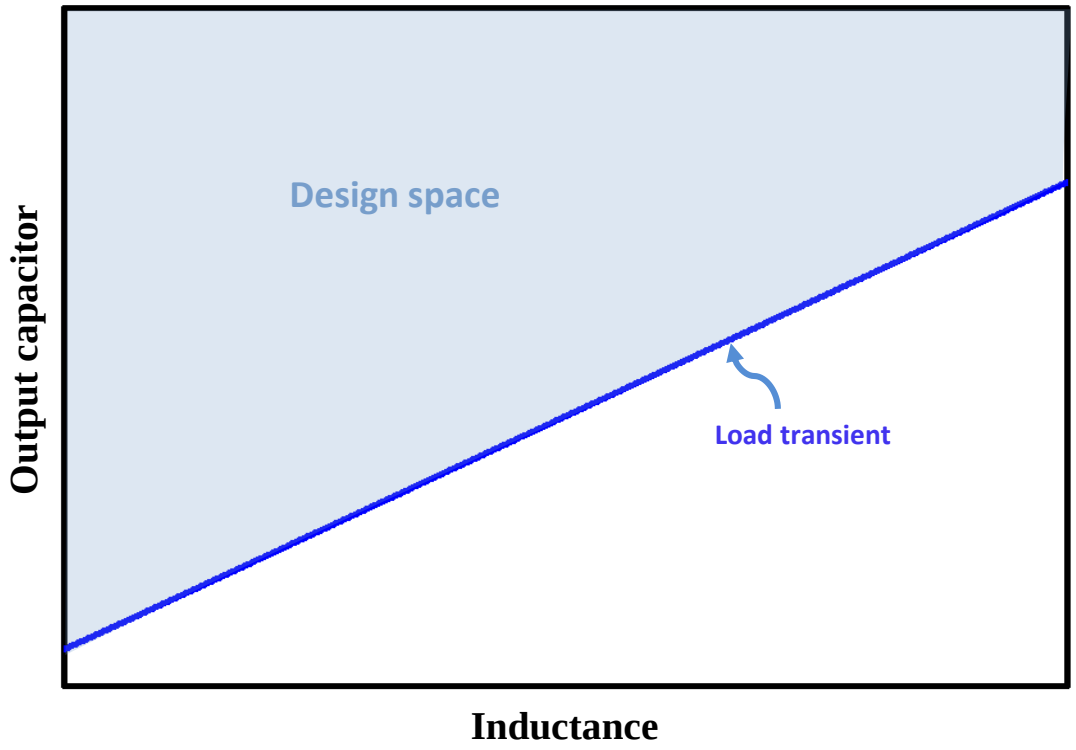


$$\Delta v_{o,load}^{min} = \frac{1}{2C}\left((C \cdot ESR)^2 m + \frac{\Delta I_o^2}{m}\right)$$

Loading $\quad m = \frac{V_{in} - v_o}{L}$

Unloading $\quad m = \frac{v_o}{L}$

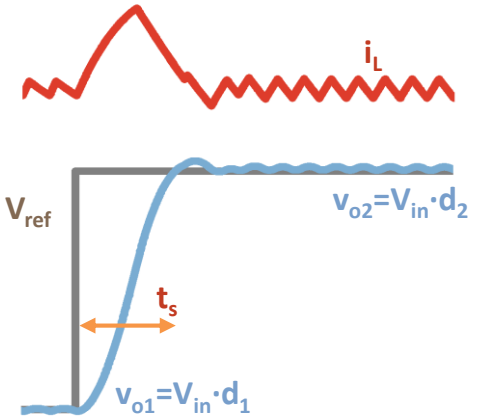
$$\Delta v_{o,load} \sim cte \cdot \frac{L}{C}$$



Design space: voltage reference tracking

Constraints

Load transients | **Voltage reference tracking** | Static ripple | Modulation delays | Filter resonance in Voltage mode

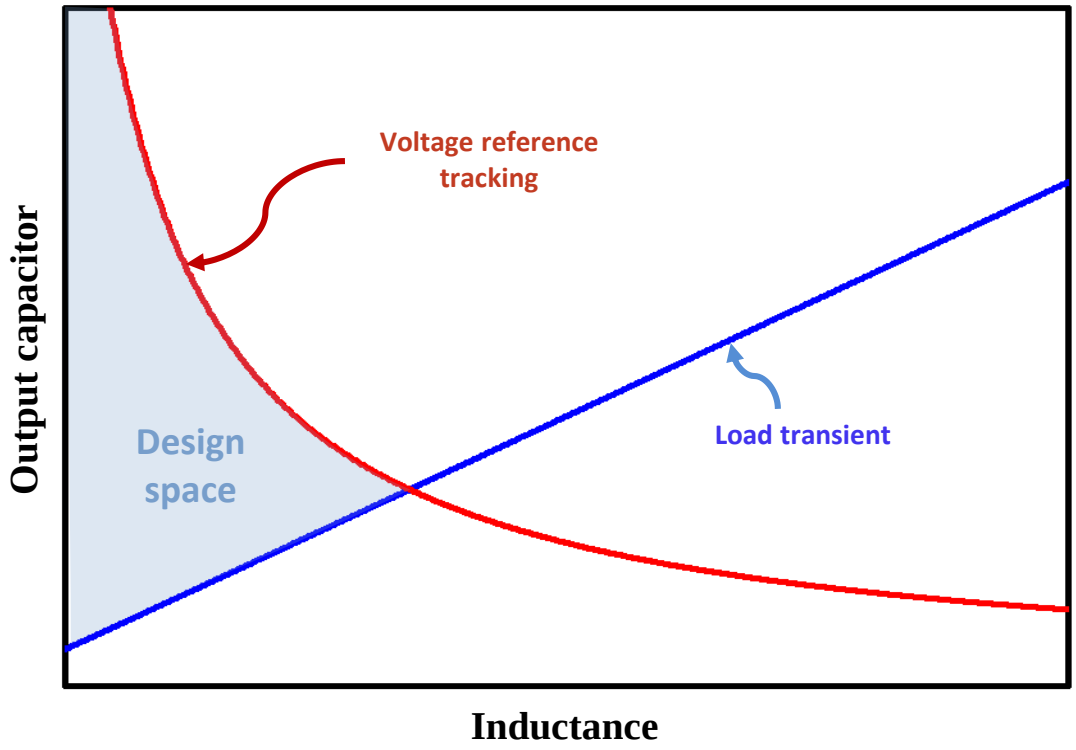


$$t_s^{min} = \sqrt{\frac{2 \cdot L \cdot C}{d_m(1-d_m)\left(\frac{1}{\Delta d}+\frac{1}{2}\right)}}$$

$$d_m = \frac{d_1 + d_2}{2}$$

$$\Delta d = |d_2 - d_1|$$

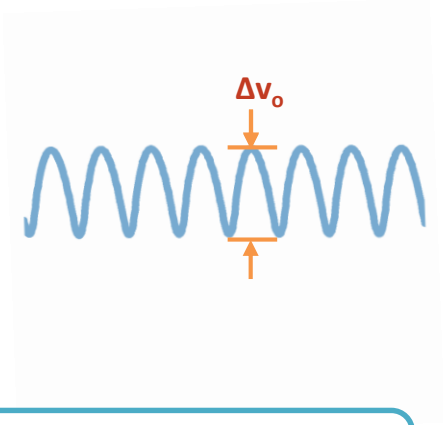
$$t_s \sim cte \cdot \sqrt{LC}$$



Design space: static ripple

Constraints

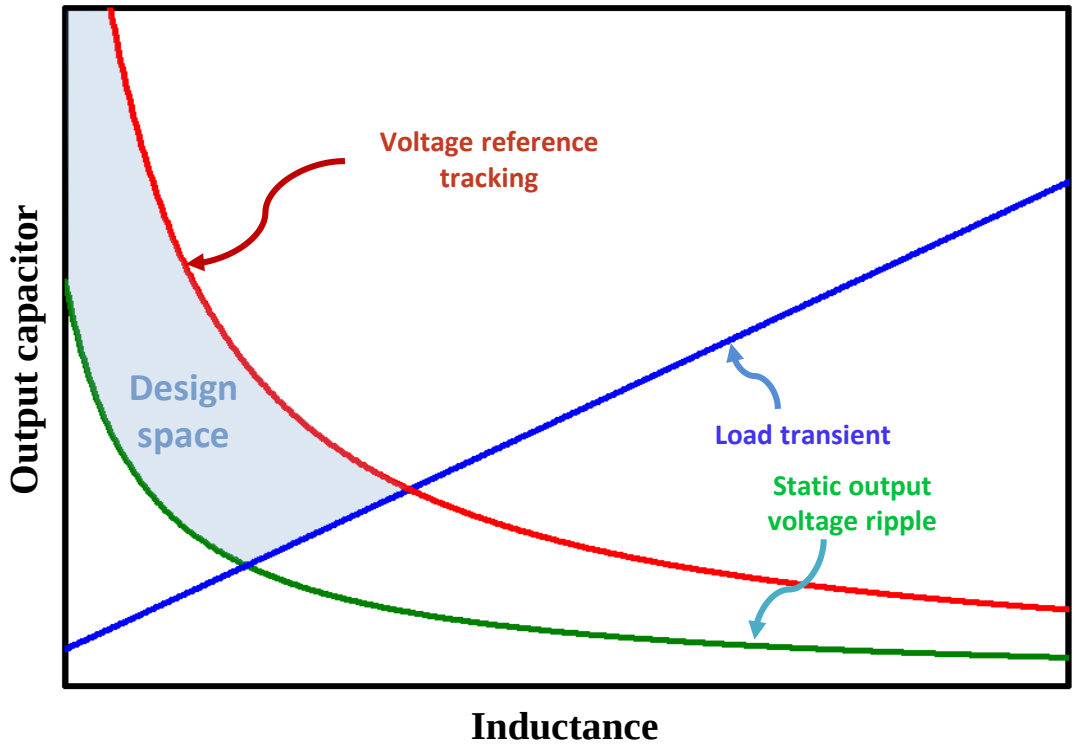
Load transients | Voltage reference tracking | **Static ripple** | Modulation delays | Filter resonance in Voltage mode



$$\Delta v_{o,pp}^{min} \approx \Delta i_L \left(\frac{1}{8 C f_{sw}} + ESR \right)$$

$$\Delta i_L = \frac{V_{in} - v_o}{L} \frac{d}{f_{sw}}$$

$$\Delta v_{o,pp} \sim cte \cdot \frac{1}{f_{sw}^2} \cdot \frac{1}{LC}$$

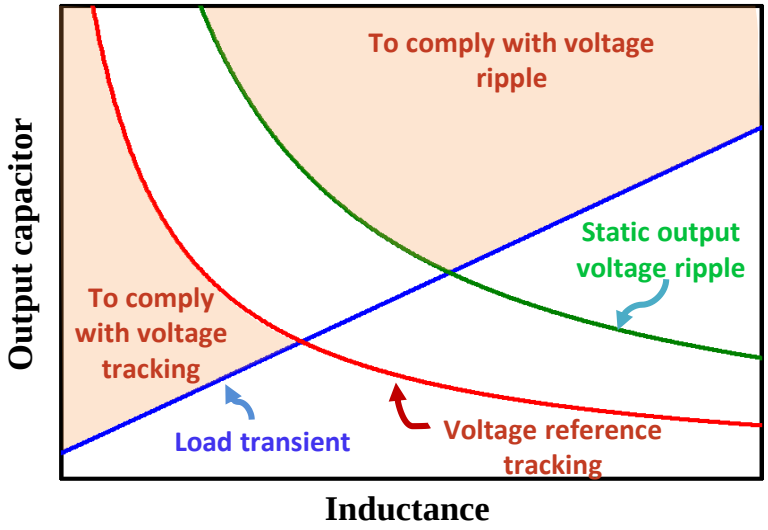


Design space: static ripple

Constraints

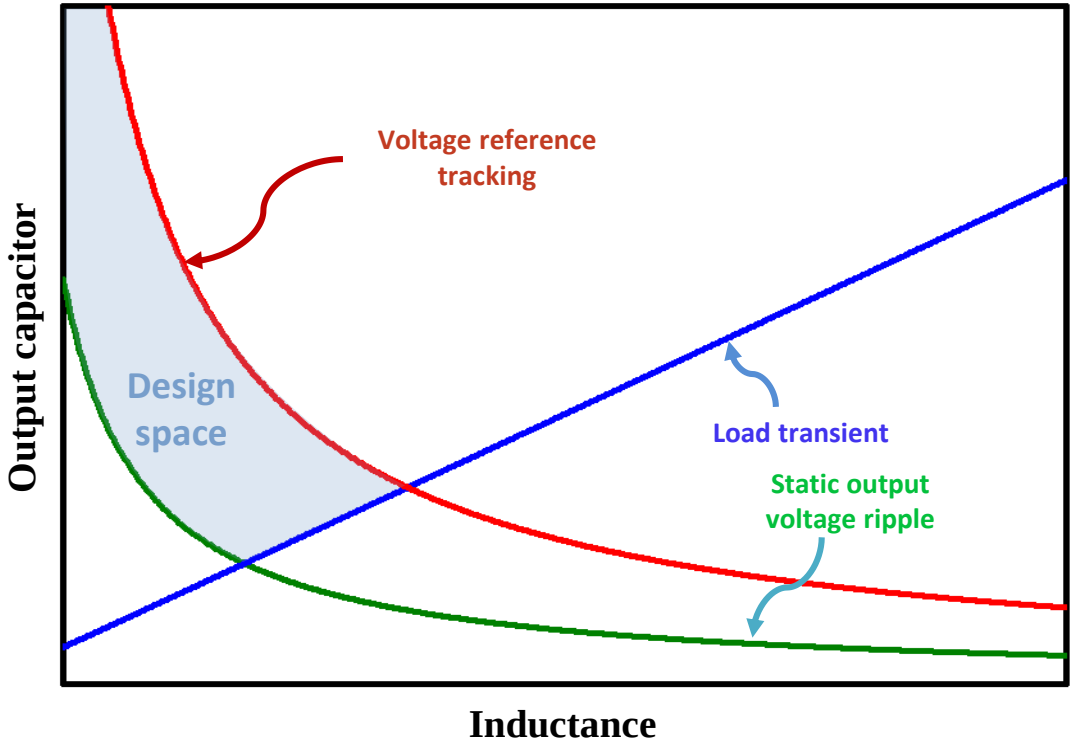
Load transients | Voltage reference tracking | **Static ripple** | Modulation delays | Filter resonance in Voltage mode

What if there is no solution in the design space??

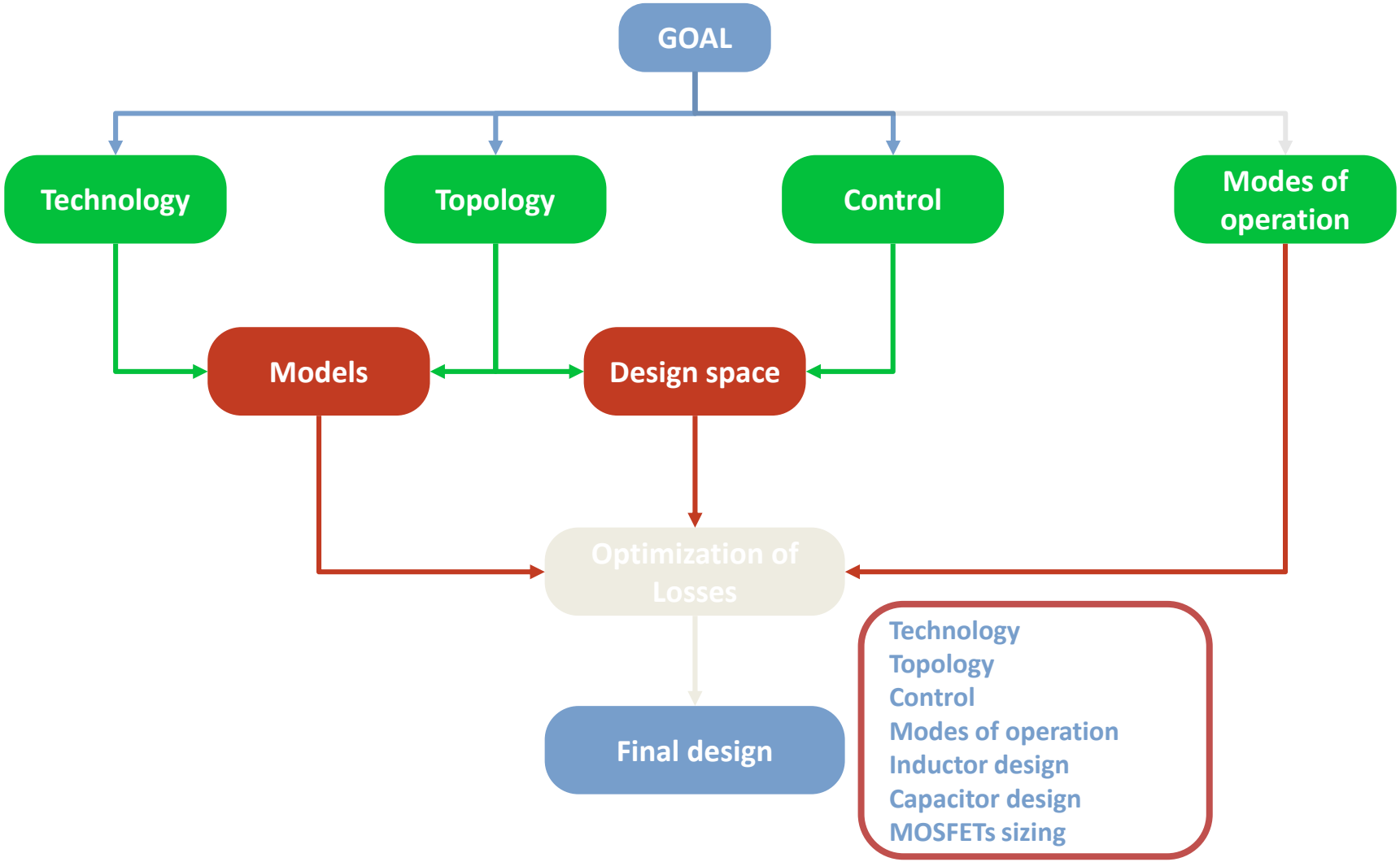


The solution is to decrease output voltage ripple by other means

- Use multi-phase topology
- Increase switching frequency



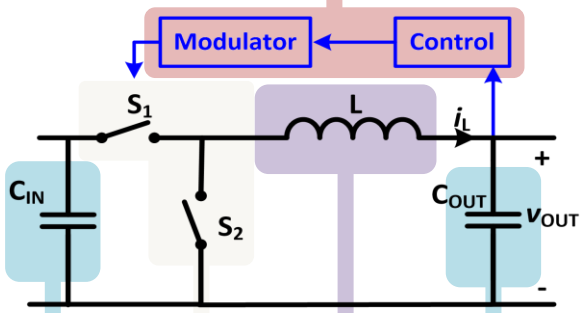
Design Flow


GOAL
Technology
Topology
Control
Modes of operation
Models
Design space
Optimization of Losses
Final design
Technology
Topology
Control
Modes of operation
Inductor design
Capacitor design
MOSFETs sizing

Specifications

Control specs

- Peak current mode
- CCM/DCM/Burst
- $\Delta B < f_{sw}/7$
- PM = 60º
- $f_{sw,min}$ = 1MHz
- $f_{sw,max}$ = 30MHz



Input specs

Static
- V_{in} = 5V
- $\Delta V_{in,max}$ = 250mV

Dynamic
- $\Delta V_{in,max}$ = 600mV
- $\Delta V_{in,trans}$ = 250mV@0ns

Output specs

Static
- V_{out} = 1.2V
- $\Delta V_{out,max}$ = 60mV
- $I_{out,typical}$ = 280mA
- $I_{out,max}$ = 500mA
- $I_{out,min}$ = 50mA

Dynamic
- $\Delta V_{out,max}$ = 144mV
- $\Delta i_{out,trans}$ = 300mA@2µs
- $\Delta i_{out,trans}$ = 50mA@2ns

MOSFET specs

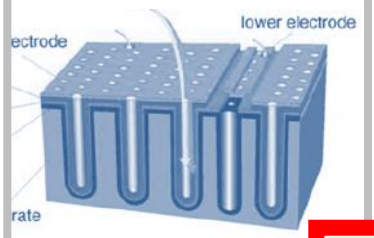
Common for p-MOS and n-MOS
- w_{min}= 2mm
- w_{max} = 30mm
- V_{gs} = 5V
- $I_{g,max}$ = 80mA
- Dead time p→n = 1ns
- Dead time n→p= 1ns

Inductor specs
- L_{max} = 2µH
- $\Delta I_{L,max}$ = 500mA
- R_{par}=10mΩ
- L_{par}=100pH

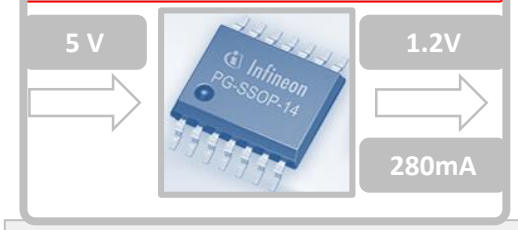
Capacitor specs
- C_{min} = 50nF
- $\sigma_{cap,ensity}$ = 220nF/mm²
- R_{par}=10mΩ
- L_{par}=100pH

CAD GUI

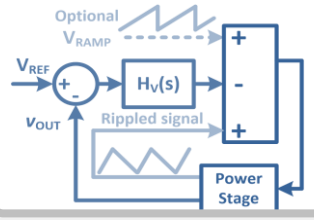
Capacitors



Static Spec

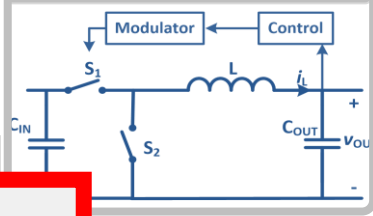


Regulator Constraints

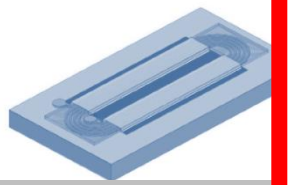


Load Design

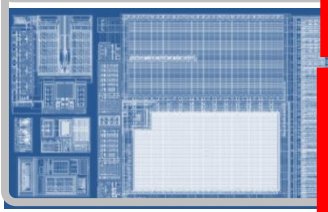
Topology



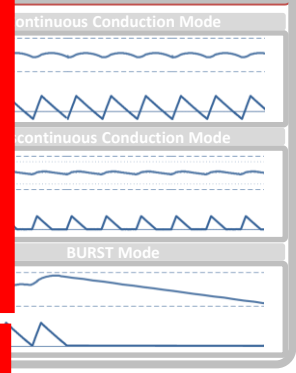
Inductor



Semiconductors



Operating Mode



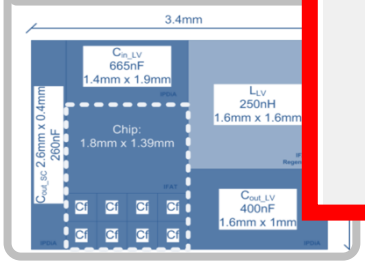
Optimization

- Cin/Cout
- Lout
- fsw
- wp
- wn
- Area

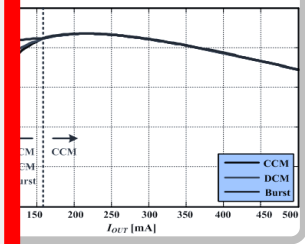
Results of the optimization process

175 nF / 245 nF	201 nH	11.7 MHz
12 mm	14.1 mm	9.9 mm^2

Total Area

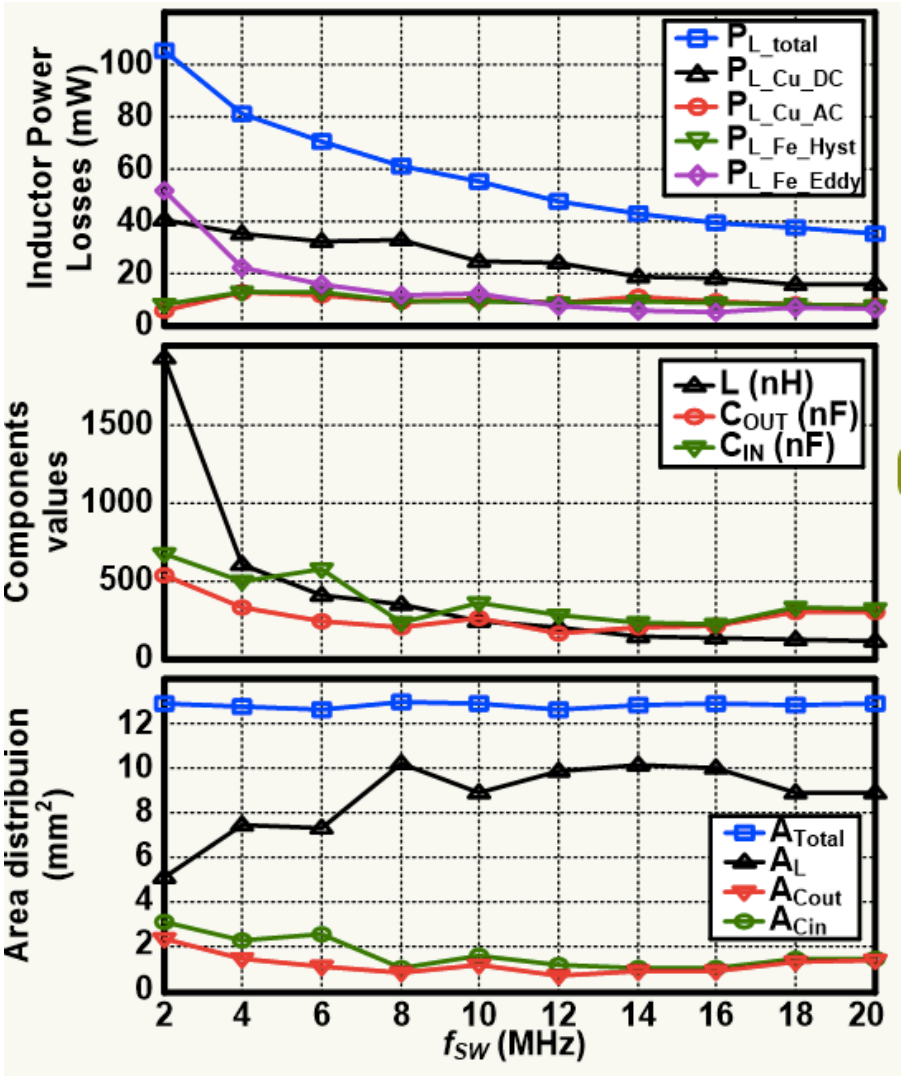


alysis of the system

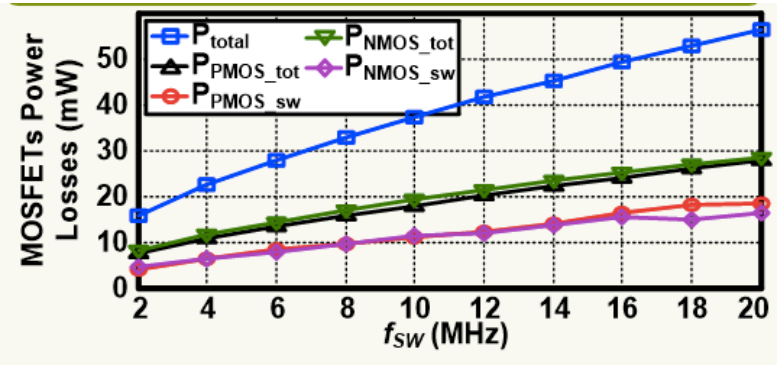


Results (& "what if" analysis)

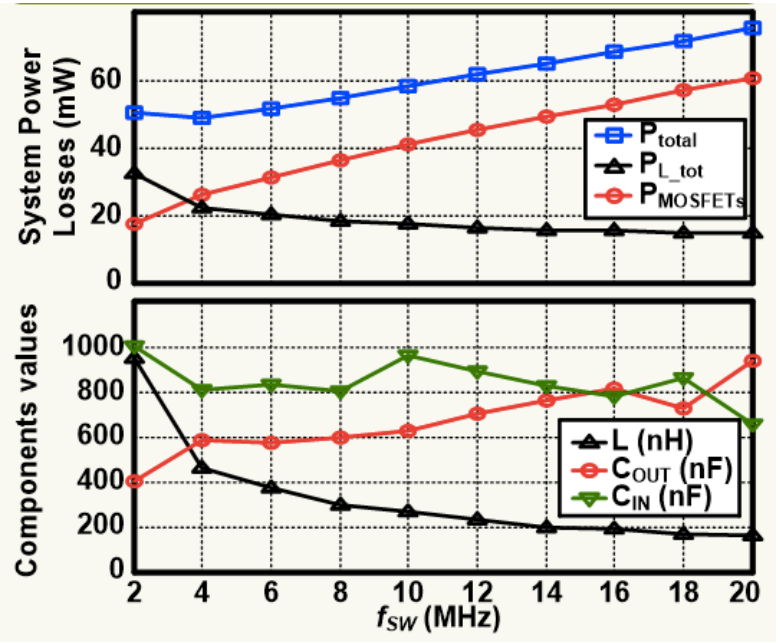
Ideal MOSFETs – Real Inductor



Real MOSFETs – Ideal Inductor

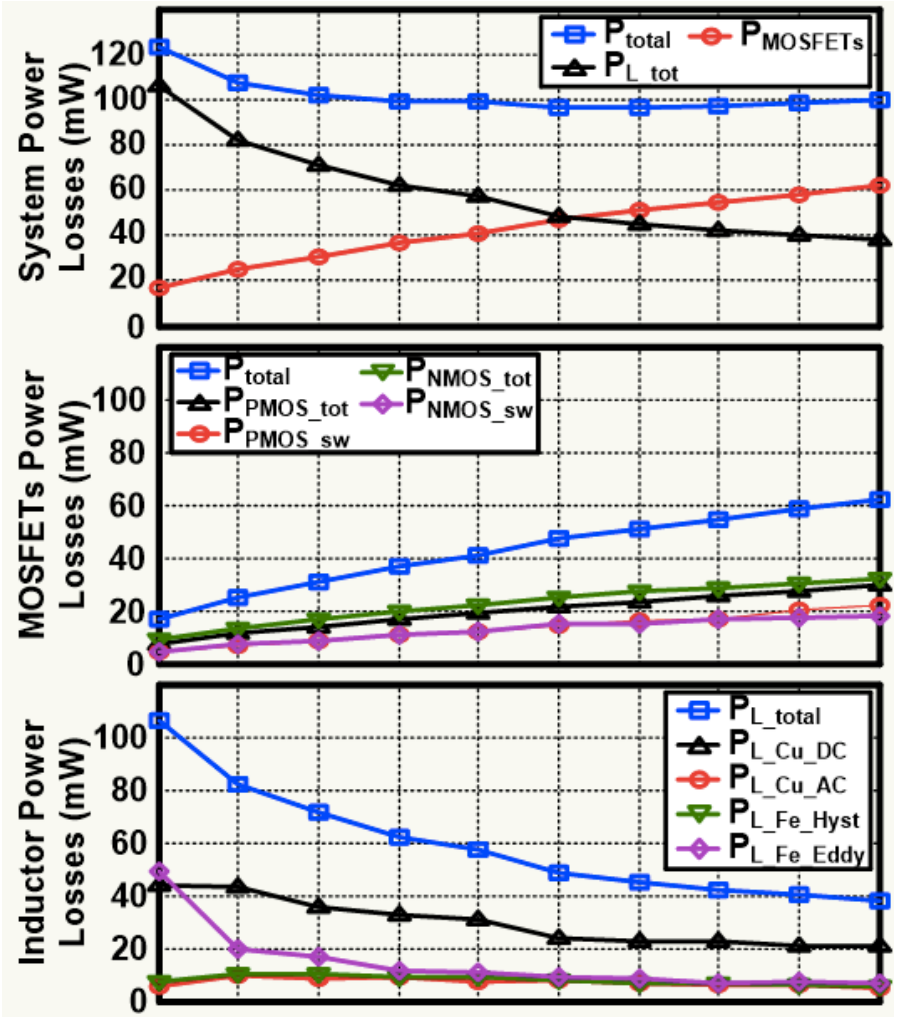


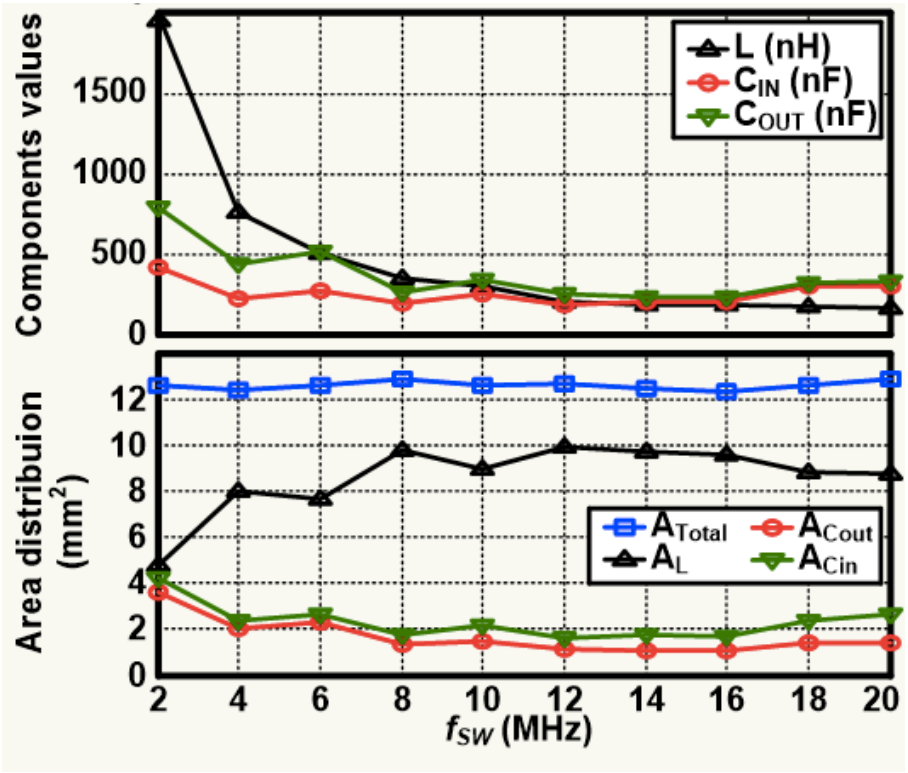
Real MOSFETs – Inductor with Cu losses



Results (& “what if” analysis)

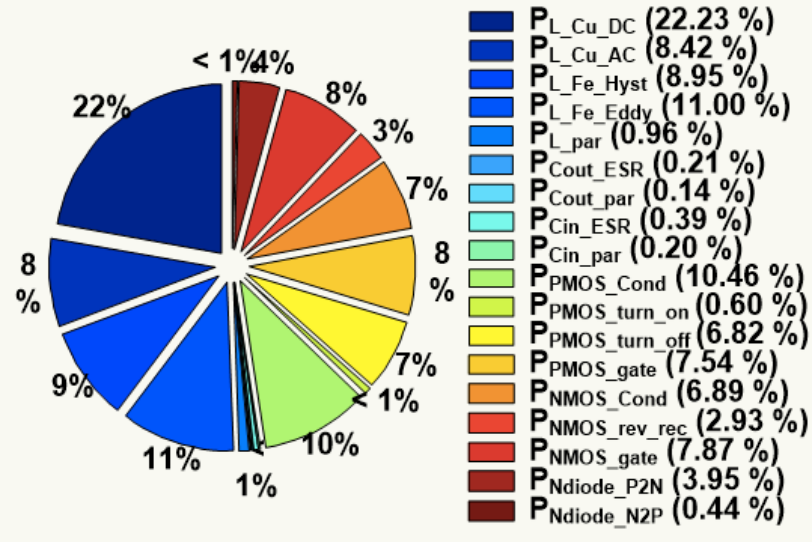
Real MOSFETs – Real Inductor



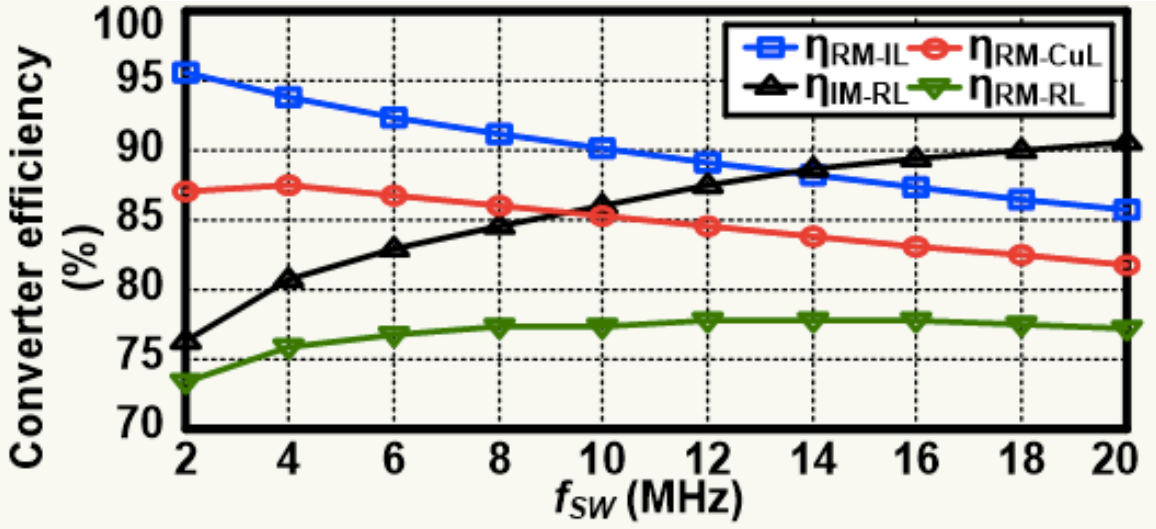


Results (& "what if" analysis)

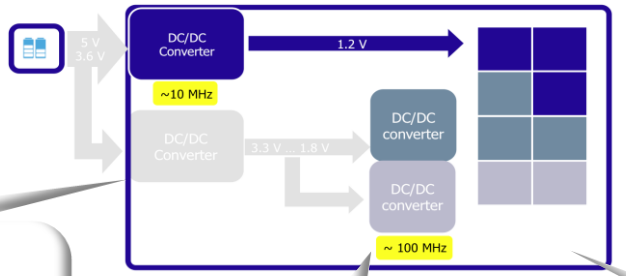
Optimal solution: Losses Breakdown



Converter efficiency comparison



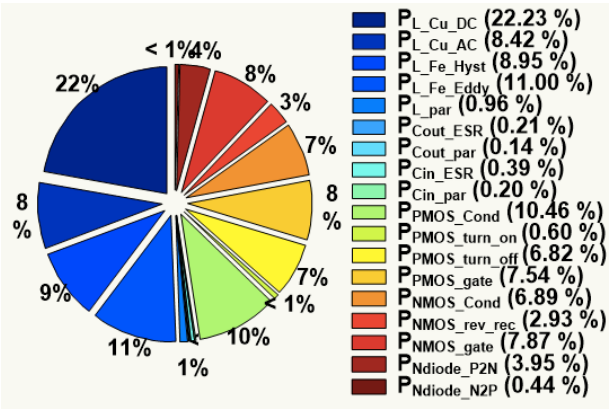
Summary



Technology impact:

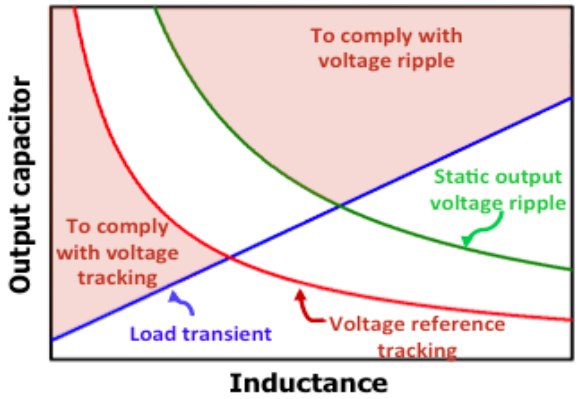
- CMOS improvement: optimum f_{sw} ↑
- Inductor technology improvement: : optimum f_{sw} ↓

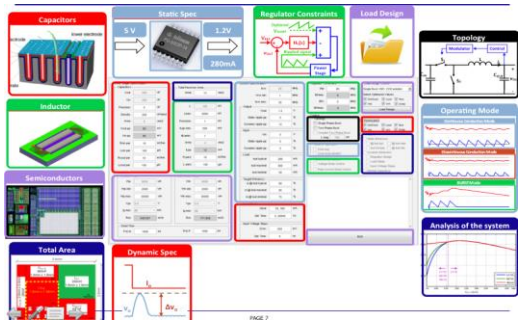
Models, algorithms and tools to **OPTIMIZE** your design



Calculate the **"Design space"** for your specs:

- Load steps
- Voltage or reference steps
- V_{out} ripple
- Multi-phase, modulation delays, …





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