Optimizing Power MOSFET Behavior for High Frequency Switching

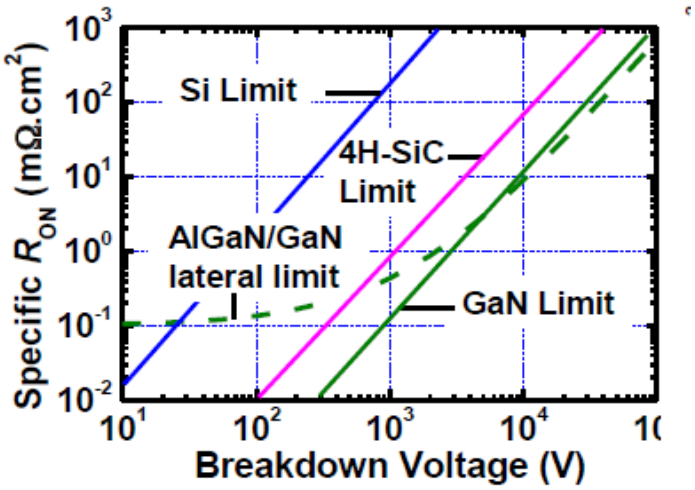
PwrSoC 2014

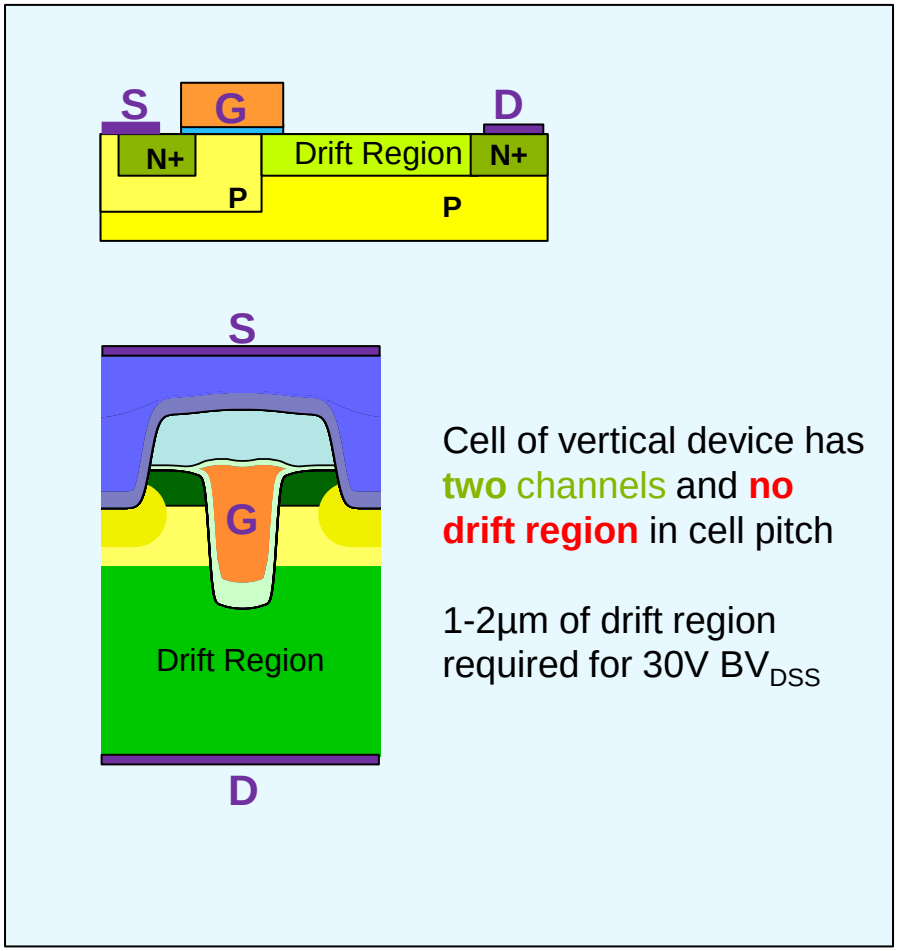
Outline

- Why Vertical Silicon MOSFETs?
- What Limits Switching Performance?
- Die Level Optimisations
  - Voltage Overshoots
  - Switching Uniformity
  - Packaging
- Conclusion

Why Vertical Silicon?

1. Power Density:
   - Superior $R_{DS(on)}/mm^2$
     - 30V Vertical silicon ≈5mΩmm²
     - 30V Lateral Si ≈15mΩmm²
     - 30V GaAs ≈14mΩmm²
     - 30V GaN ≈12mΩmm²





Cell of vertical device has **two** channels and **no drift region** in cell pitch

1-2µm of drift region required for 30V BV_{DSS}

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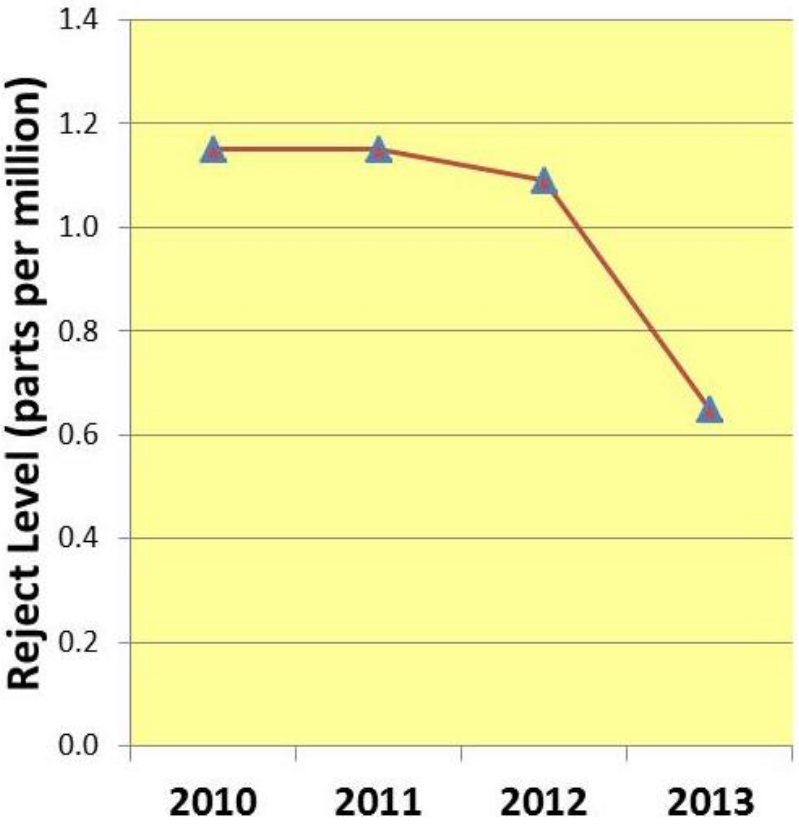
     - 30V Lateral Si ≈15mΩmm²
     - 30V GaAs ≈14mΩmm²
     - 30V GaN ≈12mΩmm²

2. Reliability
   - Proven sub ppm level
     - Effective defectivity screening
       - Low leakage (nAs; GaN 10s µAs)
       - Avalanche & Gate Stress tests



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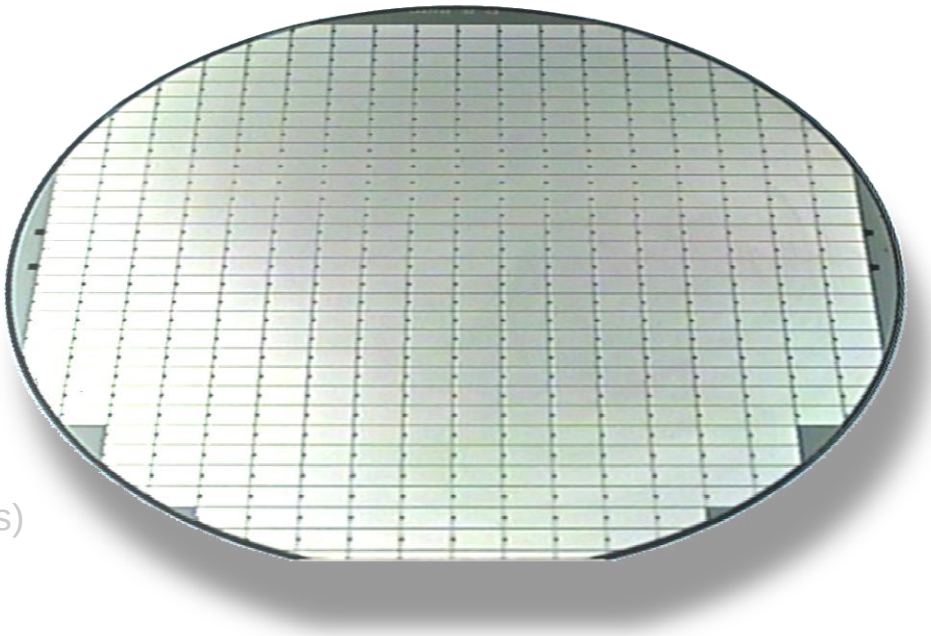
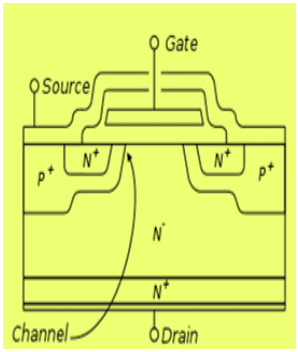
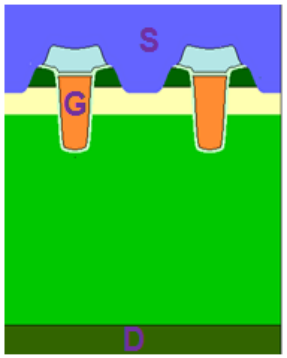


3. Wafer Cost
   - Silicon vertical ≈ Silicon lateral
   - GaN ≈ 25x ➔ 4x (?)

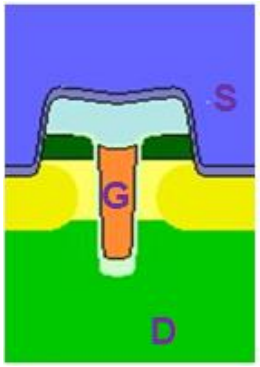
Power MOSFET Structure s



Vertical DMOS

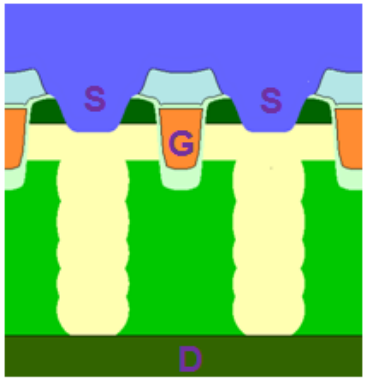


TrenchMOS

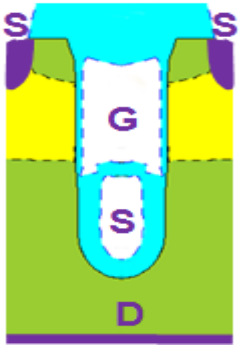


Thick Bottom Oxide TrenchMOS

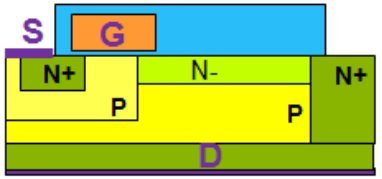
Superjunction Trench



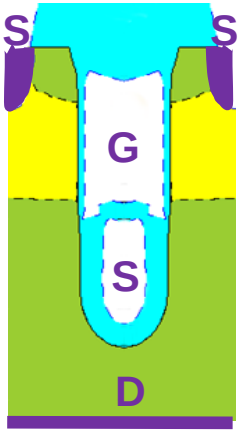
Charge Balance Trench

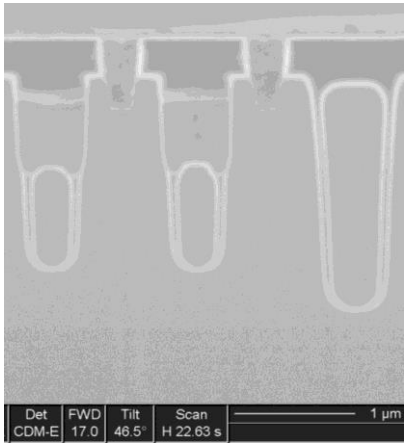


Pseudo Vertical LDMOS



Charge Balance TrenchMOS

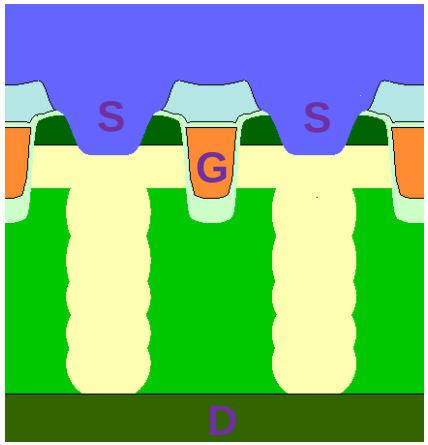


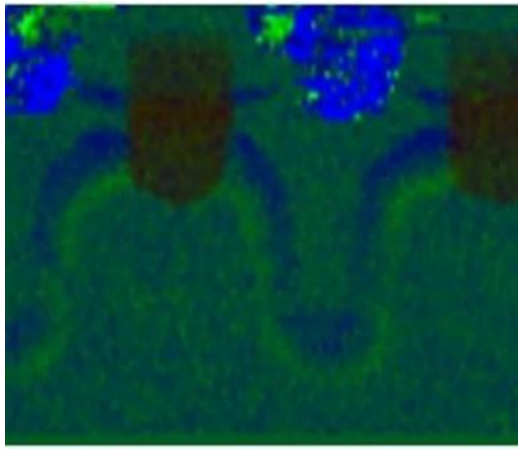


- Most common structure for LV Discrete ≈2008
  - Infineon, Fairchild, On Semi, Vishay, AOS…
- Source Electrode shields Gate from Drain
  - Increased Process Complexity
  - Effective in reducing Q_{GD} but at expense of increasing Q_{OSS}
  - Layout critical to prevent fast dV/dt effects

E.g.: “Split-gate Resurf Stepped Oxide (RSO) MOSFETs for 25V applications with record low gate-to-drain charge”; Goarin, P.; et. Al.; ISPSD 2007

LV Superjunction TrenchMOS



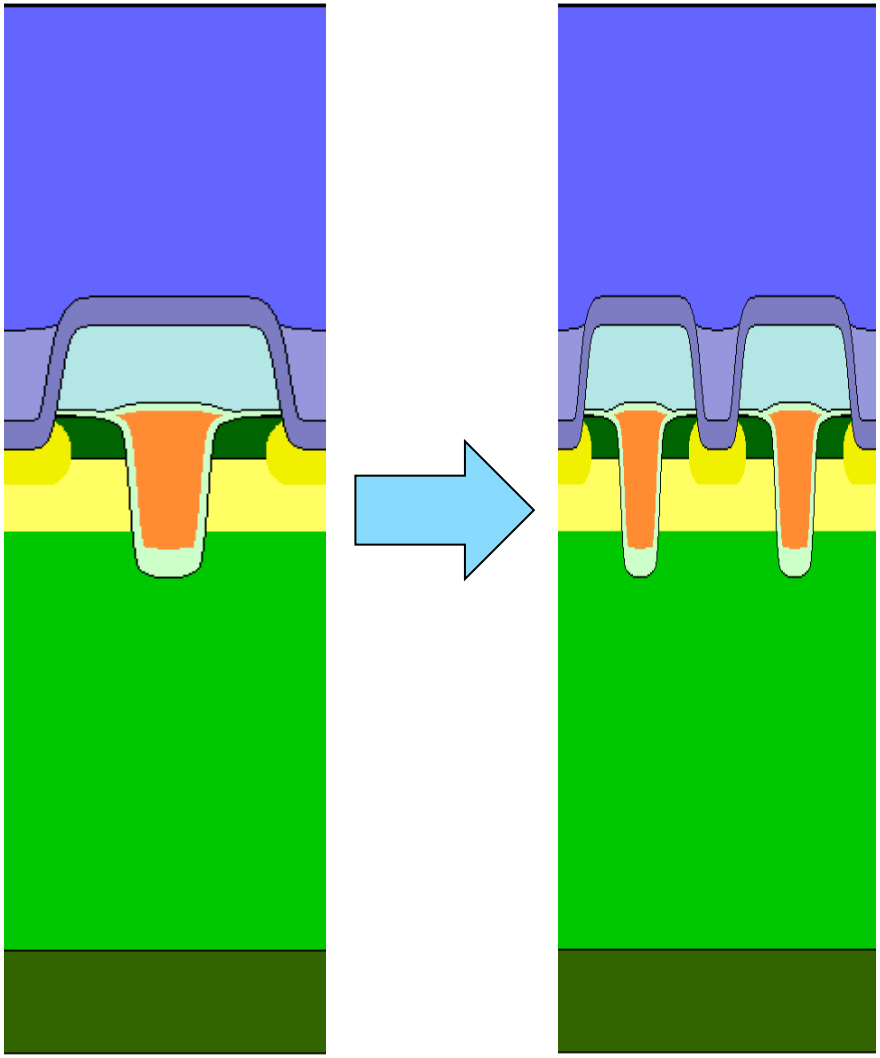


- First Used for Low Voltage ≈2010
  - Commonly used for 400V – 600V
  - NXP (NEC in literature, production?)
  - P-type pillars shield trench sidewall (JFET effect) for low Q_{GD} and gives low Q_{rr}
  - Relaxed cell pitch gives improved linear mode capability

E.g.: “Low voltage TrenchMOS combining low specific RDS(on) and QG FOM”; Rutter, P.; Peake, S.T .; ISPSD 2010

E.g.: “Low voltage superjunction power MOSFET: An application optimized technology”; Rutter, P.; Peake, S.T .; APEC 2011

The Problem with Cell Pitch Reduction?



$$Q_G \cdot R_{DS(on)} \approx Q_G\left(R_{Channel} + R_{Drift}\right)$$

$$Q_G \approx \frac{Area}{Cell\ Pitch}$$

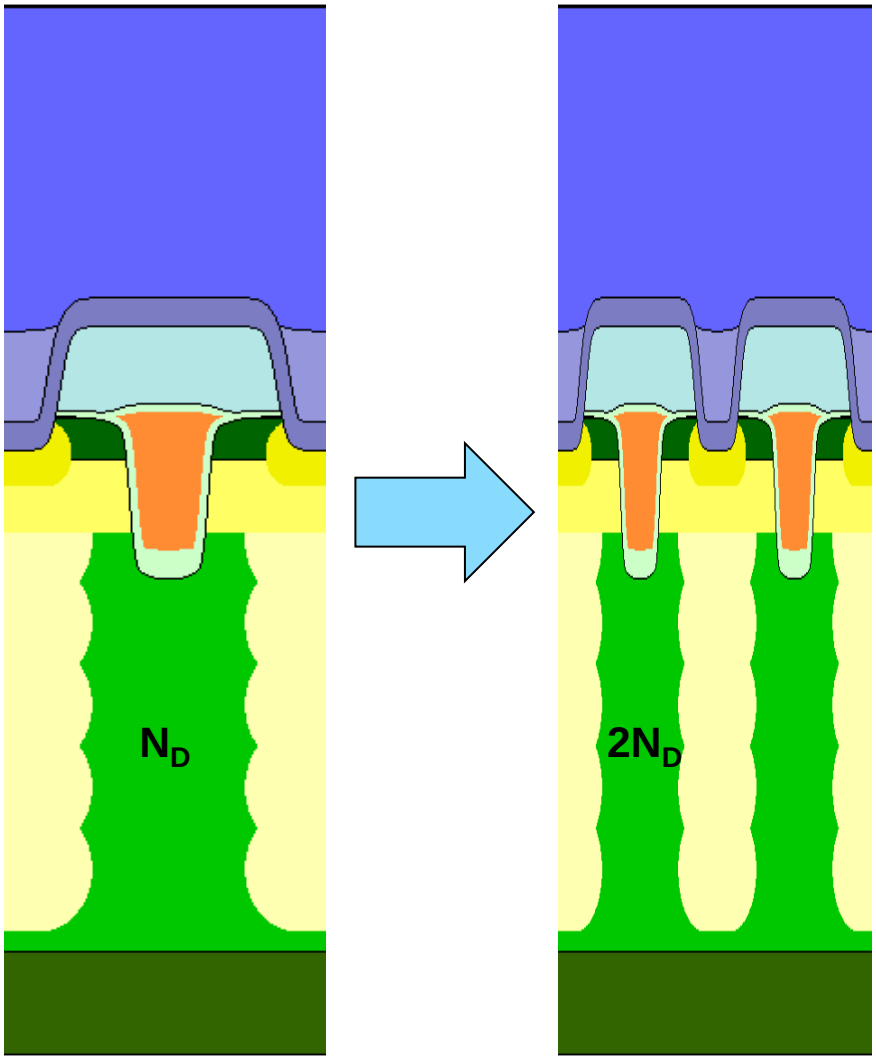
$$R_{Channel} \approx \frac{Cell\ Pitch}{Area}$$

$$R_{Drift} \approx \frac{1}{Area}$$

$$Q_G \cdot R_{DS(on)} \approx 1 + \frac{1}{Cell\ Pitch}$$

Low Sp.$R_{DS(on)}$ and low Q_G FOM are mutually exclusive!

RESURF & Cell Pitch Reduction



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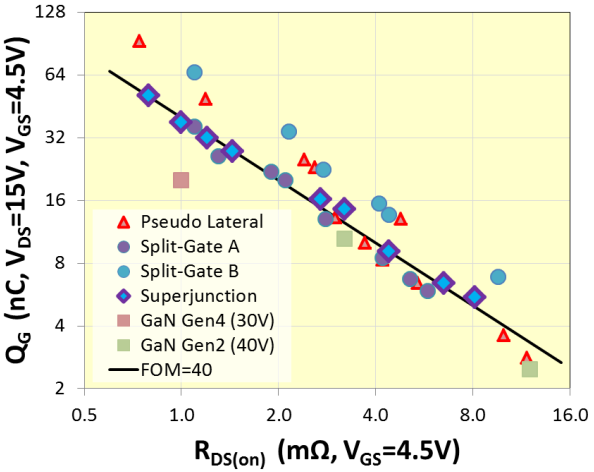
$$R_{Channel} \approx \frac{Cell\ Pitch}{Area}$$

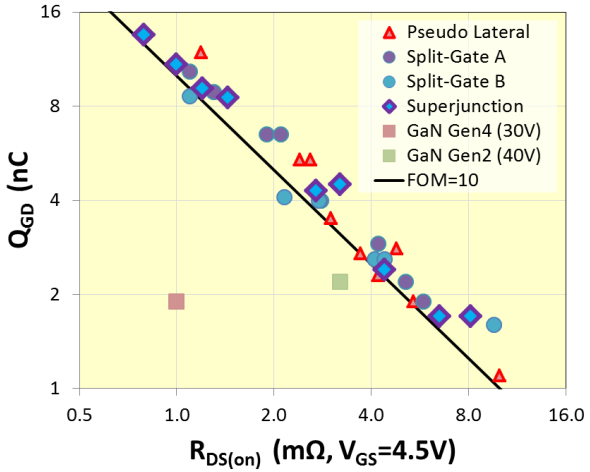
$$R_{Drift} \approx \frac{Cell\ Pitch}{Area}$$

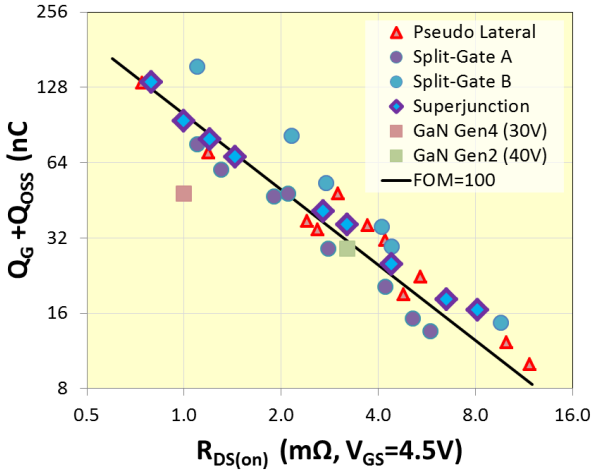
$$Q_G \cdot R_{DS(on)} \approx 2$$

Low Sp.$R_{DS(on)}$ & Low Q_G FOM are achievable

FOM Benchmarking





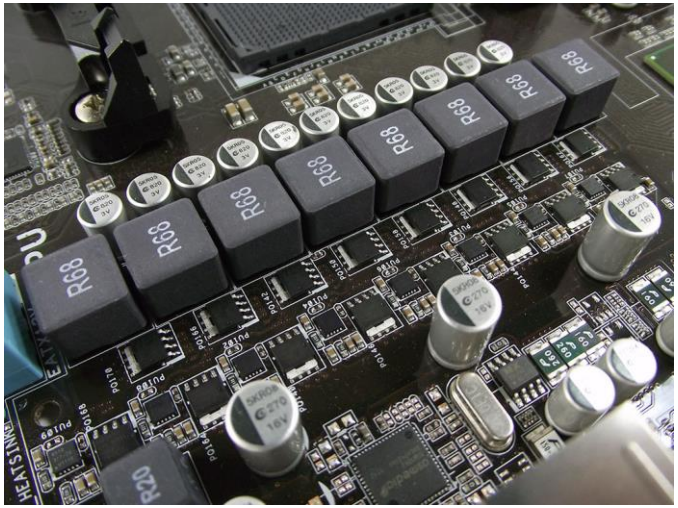


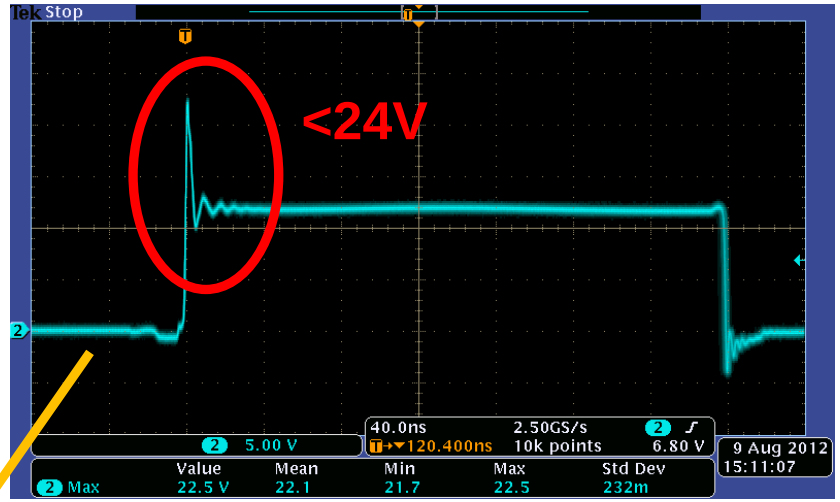
All silicon technologies have similar performance, recent 30V GaN devices demonstrate potential of this material

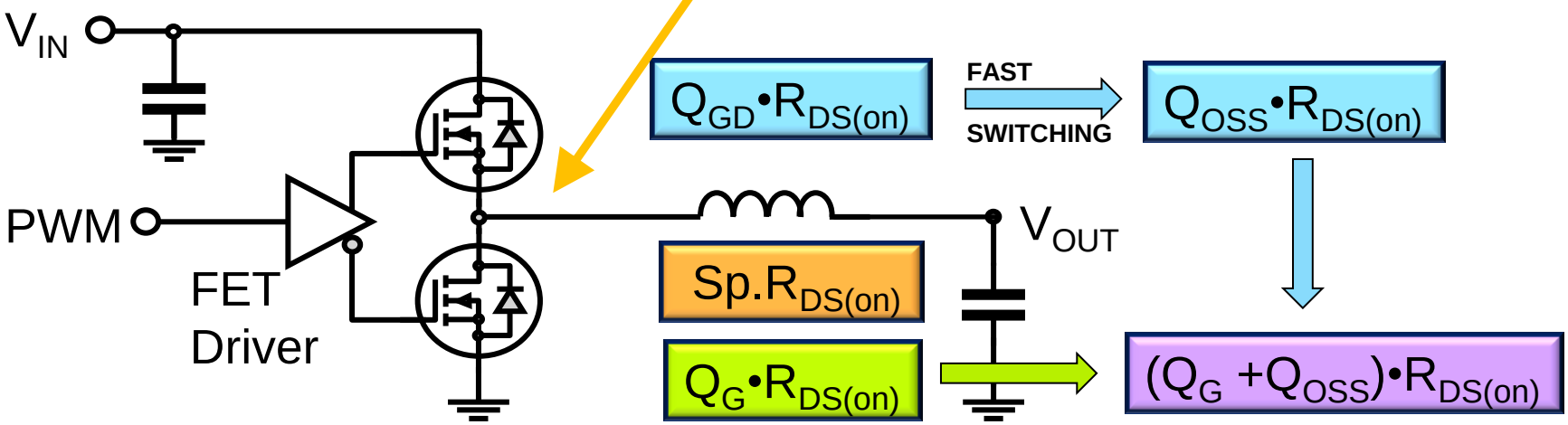
BUT performance FOMs are only part of the story; product design including packaging is critical to get the most out of a technology….

*** Datasheet values; includes package resistance**

DC-DC Buck Converter







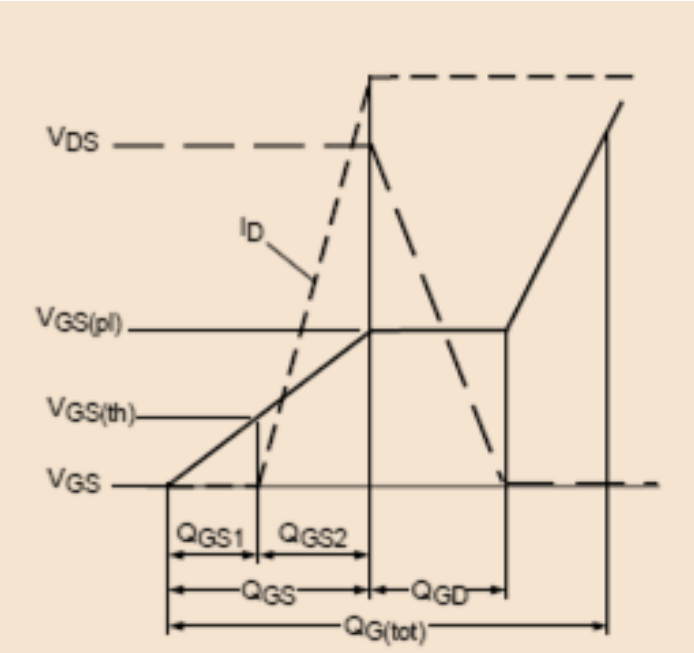
E.g.: Advanced Design for Fast Switching Power MOSFETs"; Goergens et al. .;Professional Education Seminar APEC 2011

What Limits Switching Speed?

Silicon?

$$\frac{dI_D}{dt} = \frac{I_D \cdot I_G}{Q_{GS2}} \approx 28\ A/ns$$

$$\frac{dV_{DS}}{dt} = \frac{V_{IN} \cdot I_G}{Q_{GD}} \approx 13\ V/ns$$



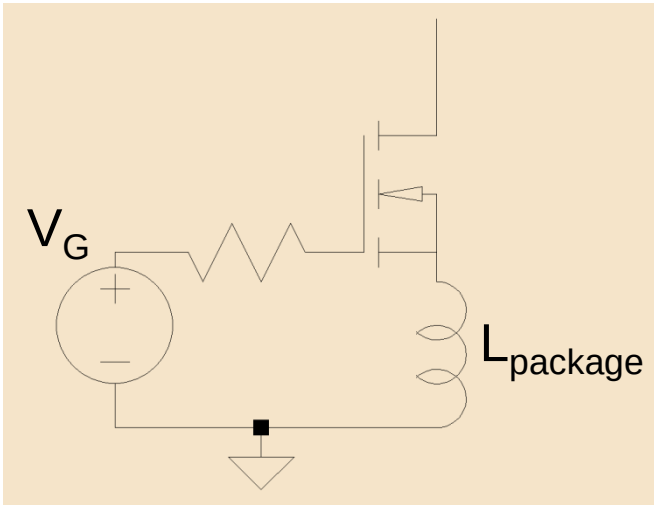
$R_{DS(on)}$	6.5mΩ
Q_{GS2}	0.8nC
Q_{GD}	1.4nC
$Q_{G(tot)}$	5.5nC
$V_{GS(th)}$	1.6V
$V_{GS(pl)}$	2.7V
V_{DS}, V_{IN}	12V
I_G	1.5A
I_D	15A
V_G	5V
$L_{package}$	0.6nH
L_{total}	2.4nH
f_{osc}	100MHz

What Limits Switching Speed?

Package?

$$\frac{dI_D}{dt} = \frac{V_G - V_{GS(pl)}}{L_{Package}} \approx 4\ A/ns$$

$$\frac{dV_{DS}}{dt} = \frac{V_{IN} \cdot I_G}{Q_{GD}} \approx 13\ V/ns$$



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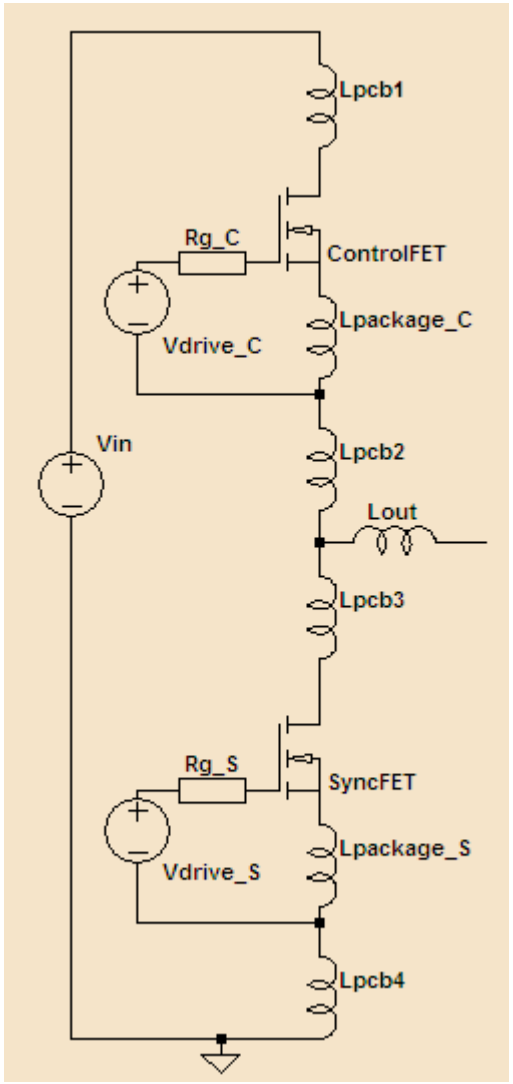
f_{osc}	100MHz

What Limits Switching Speed?

Circuit?

$$\frac{dI_D}{dt} = \frac{V_{IN}}{L_{total}} \approx 5\ A/ns$$

$$\frac{dV_{DS}}{dt} = 12 \cdot V_{IN} \cdot f_{osc} \approx 14\ V/ns$$



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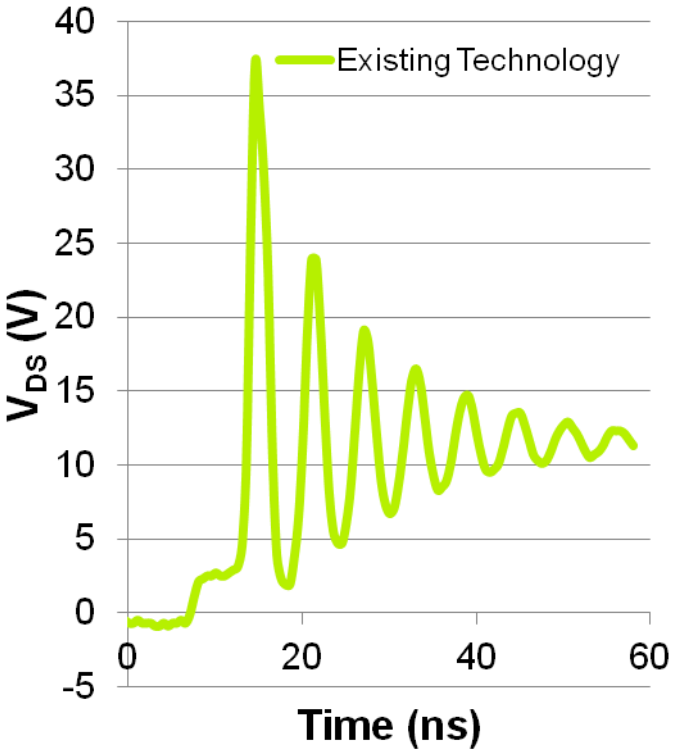
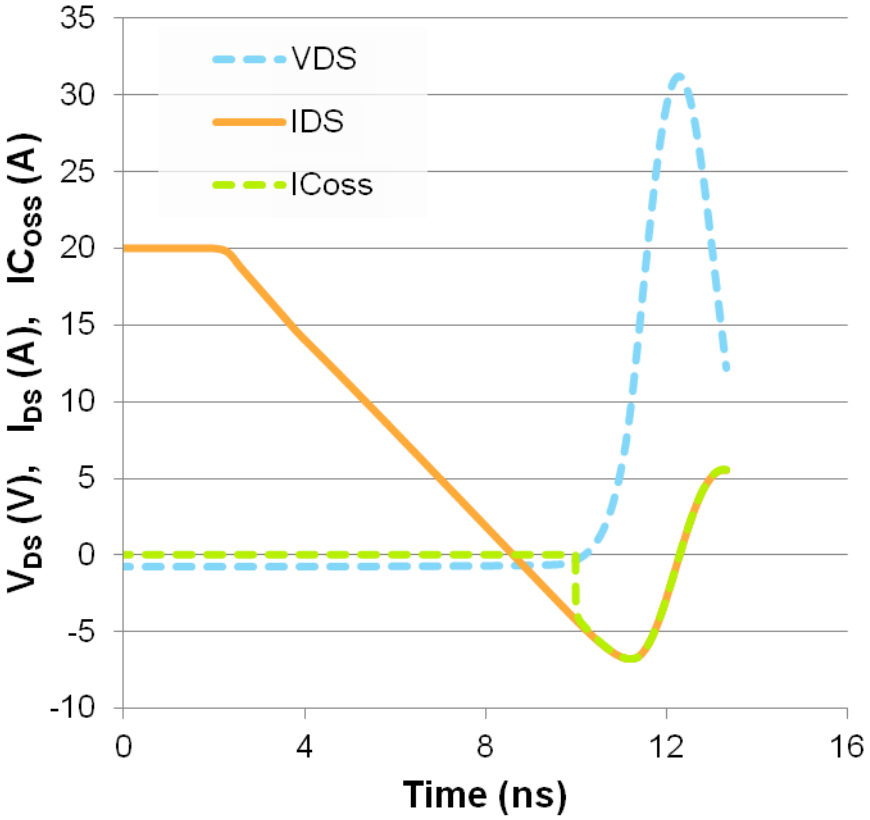
What Limits Switching Speed?

	Silicon	Package	Circuit
dI_D/dt	28 A/ns	4 A/nS	5 A/ns
dV_D/dt	13 V/ns	13 V/nS	14 V/ns

- Silicon is not the limiting factor!
- Approaching situation where circuit parasitics dictate switching speed
- Consequence is excessive voltage overshoots
- Lower Q_{GD} technologies like GaN need improved packaging to be effective

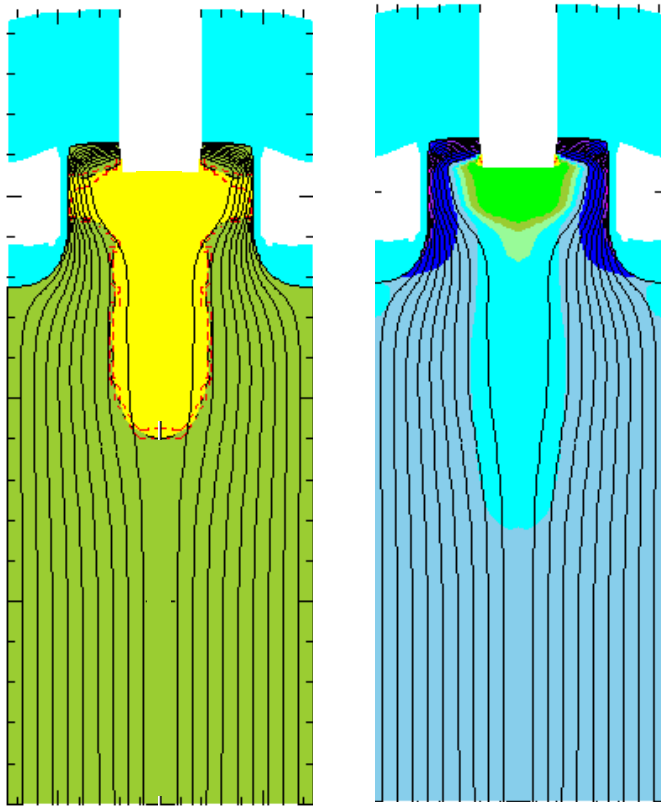


Simulated Reverse Recovery



Current Flow

Electron Concentration

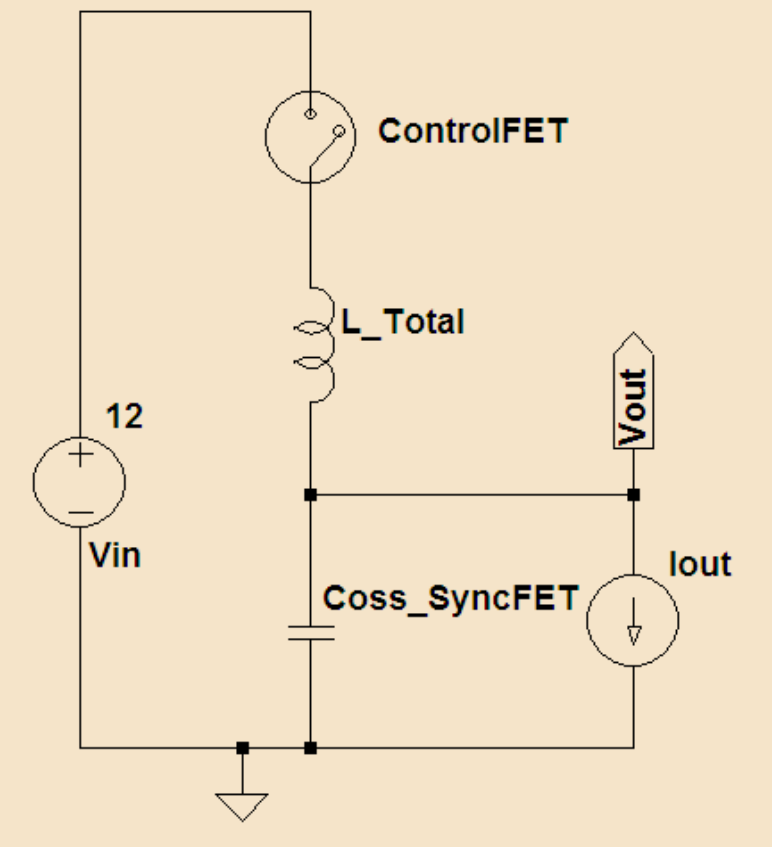


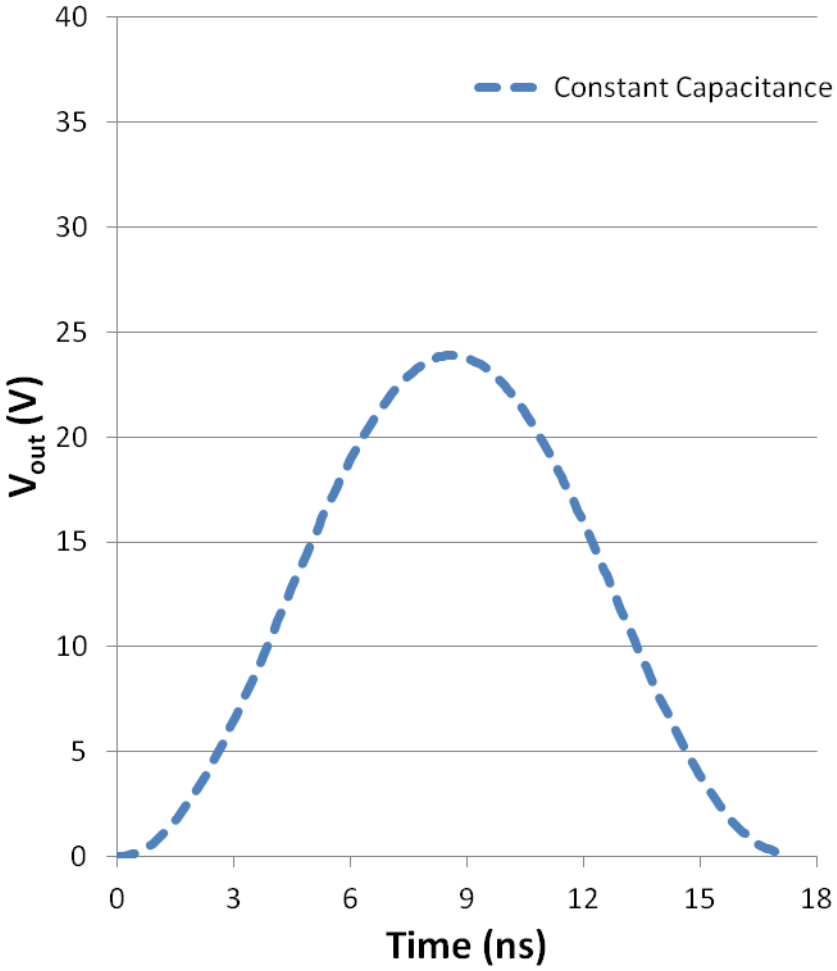
Qrr=14.7nC, 21% (3.1nC) is stored charge

Body diode stored charge **NOT** major cause of voltage overshoots!

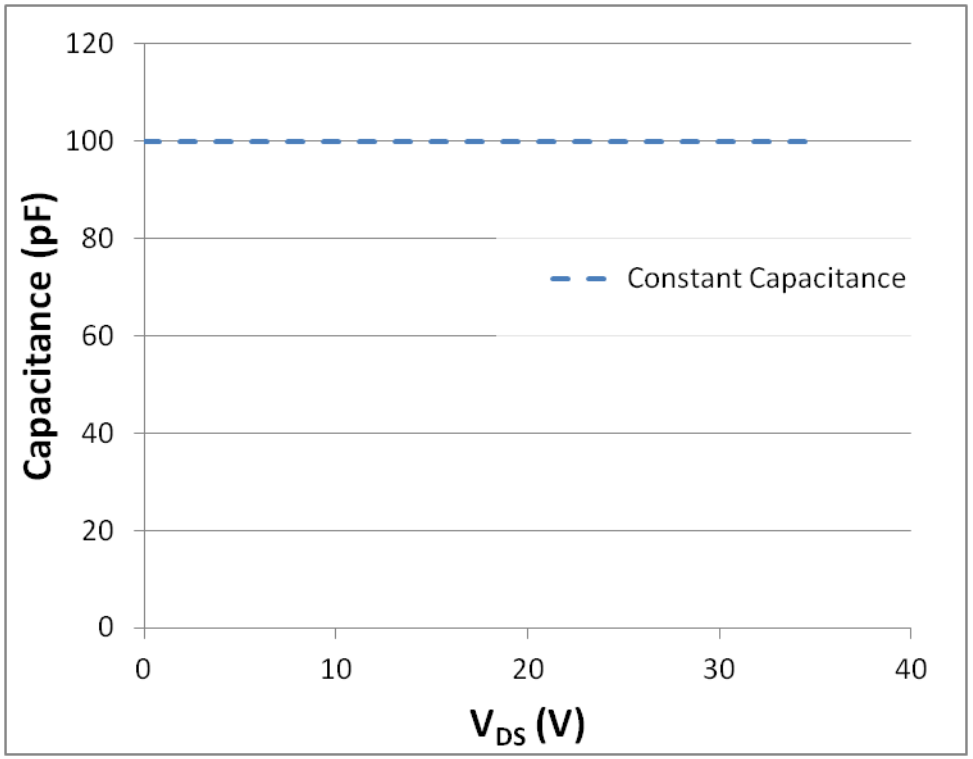
Voltage Transients – Ideal Case

- di/dt and dv/dt set by circuit
  - control FET closes instantaneously
  - Ideal capacitor (no V_{DS} dependency)

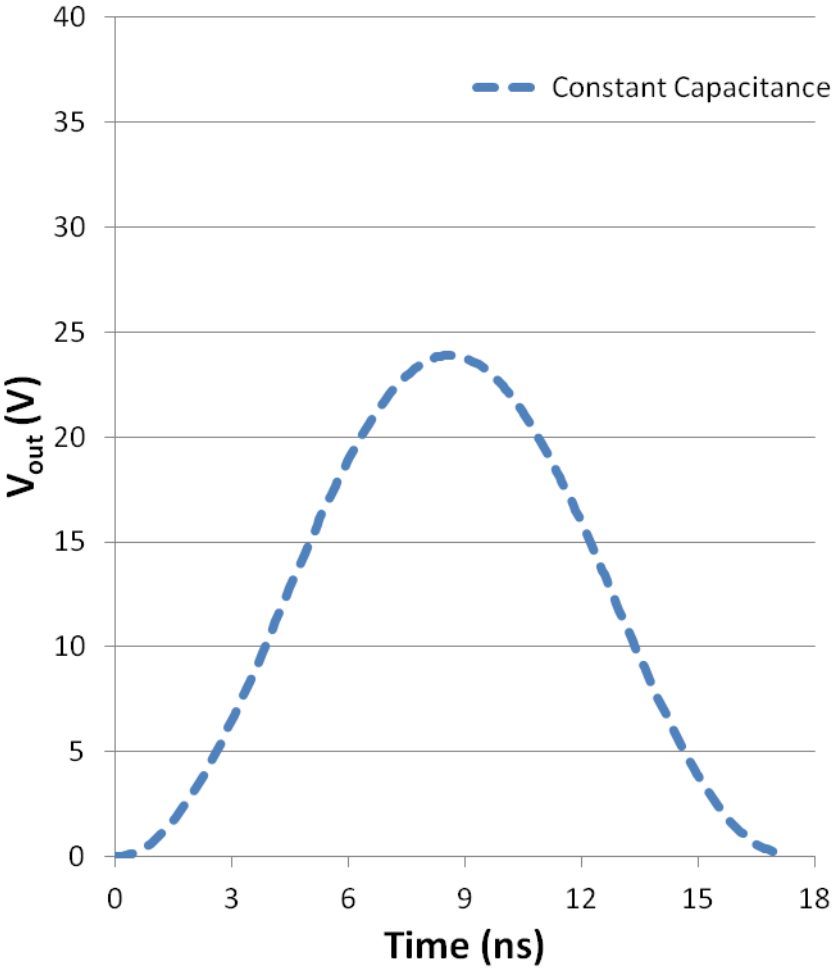




Effect of Coss ‘shape’ on Voltage Transients



$$C_{OSS}(V_{DS}) = C_{OSS}(V_{DS} = 0V)\sqrt[m]{\frac{v_j}{v_j + V_{DS}}}$$



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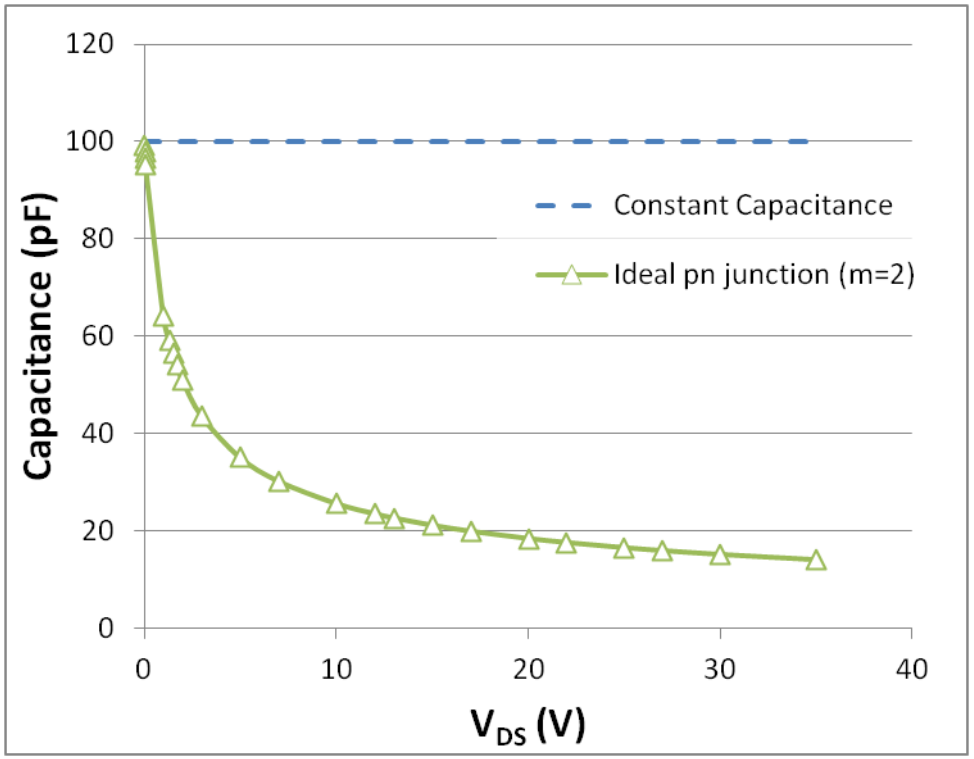

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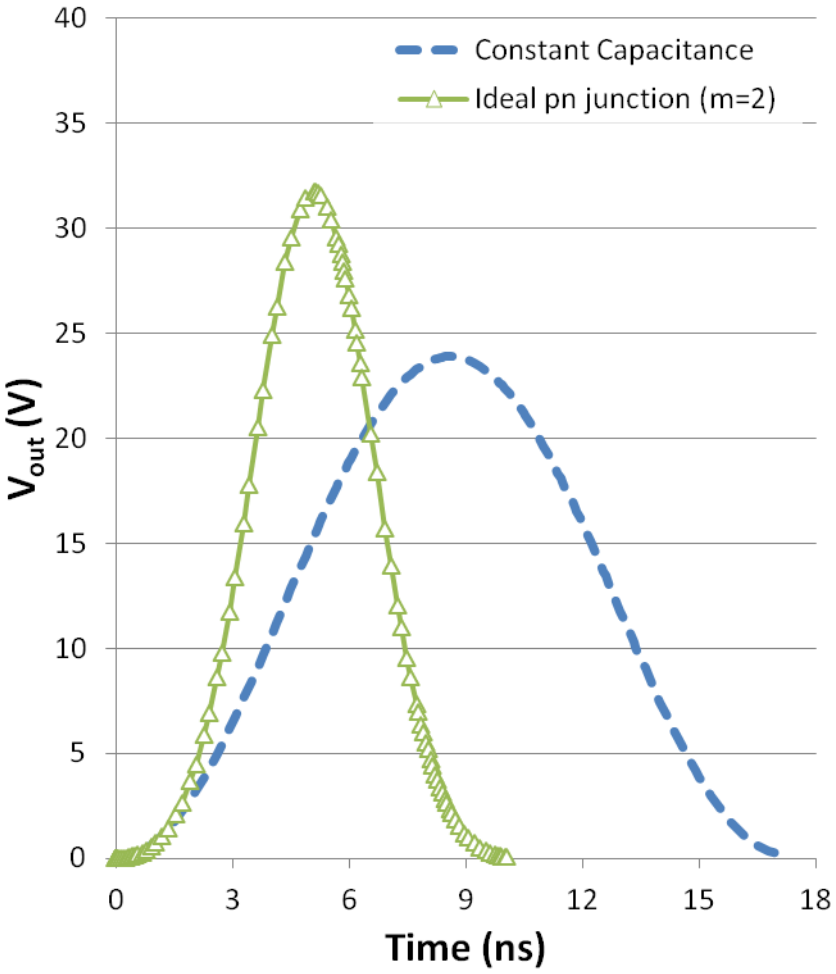

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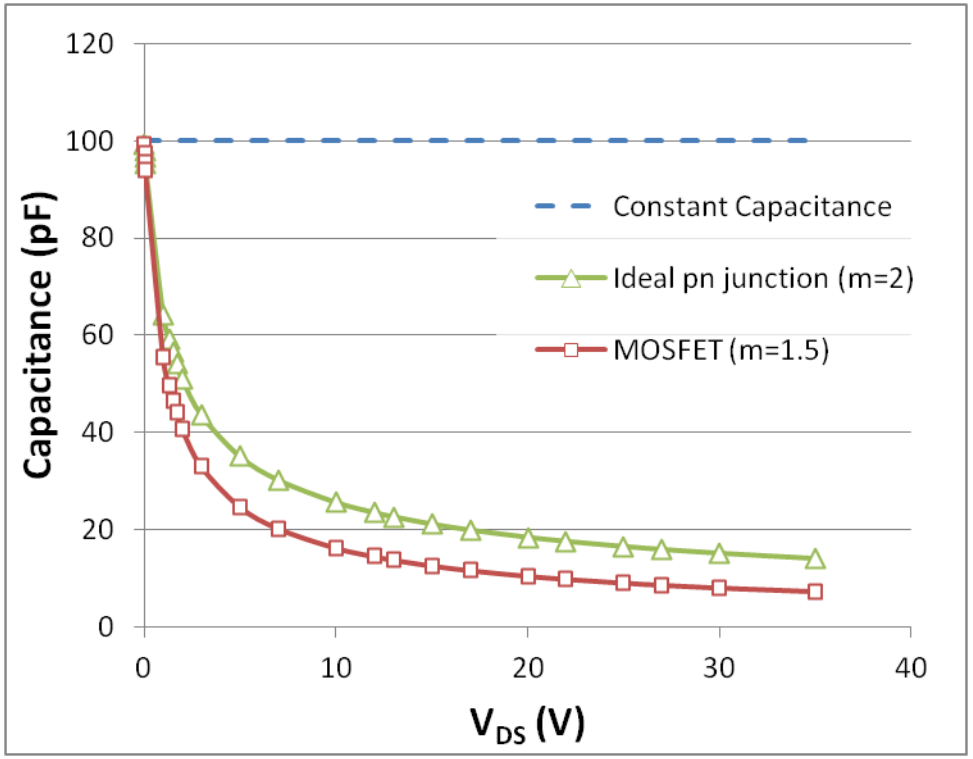

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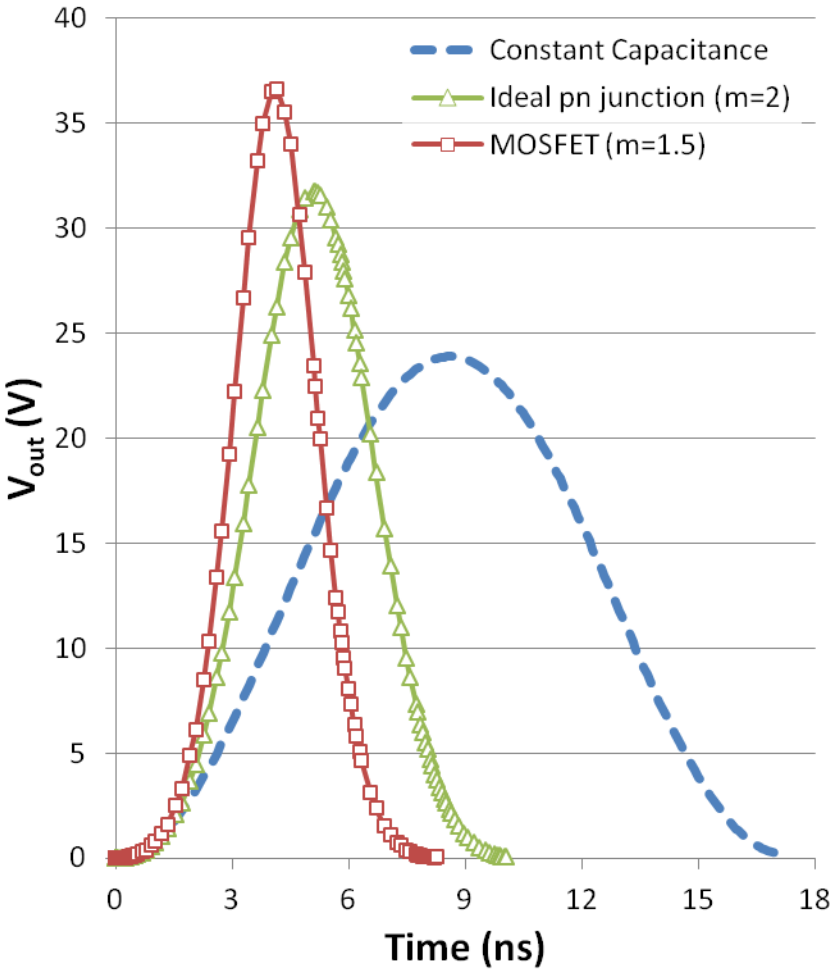

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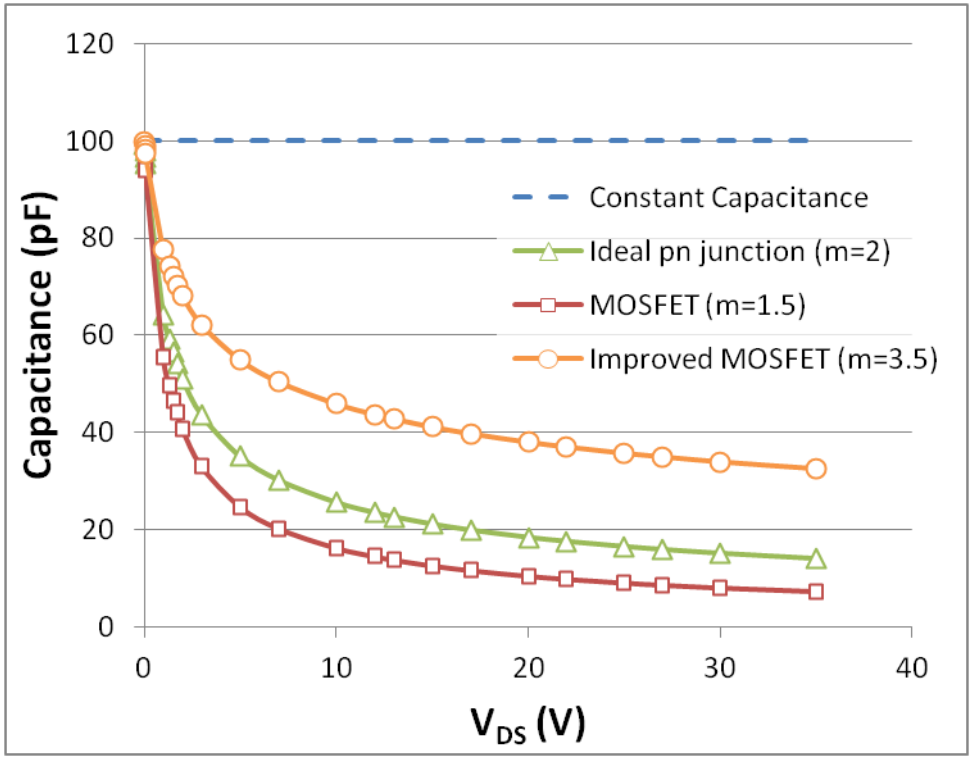

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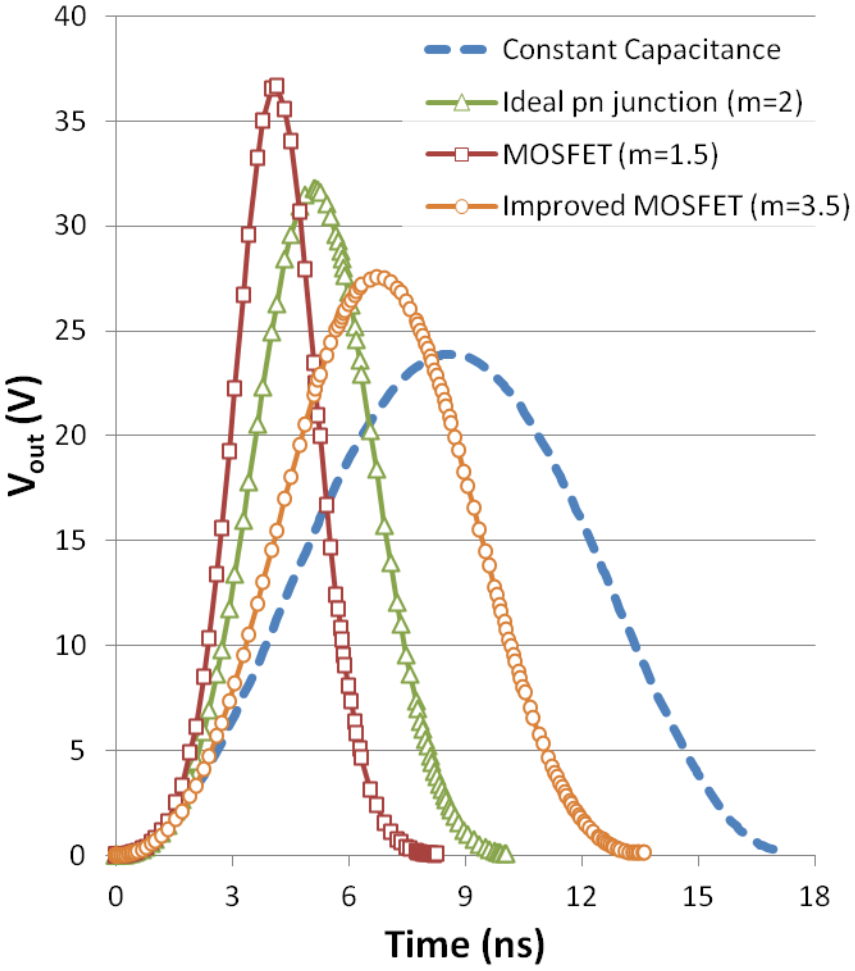
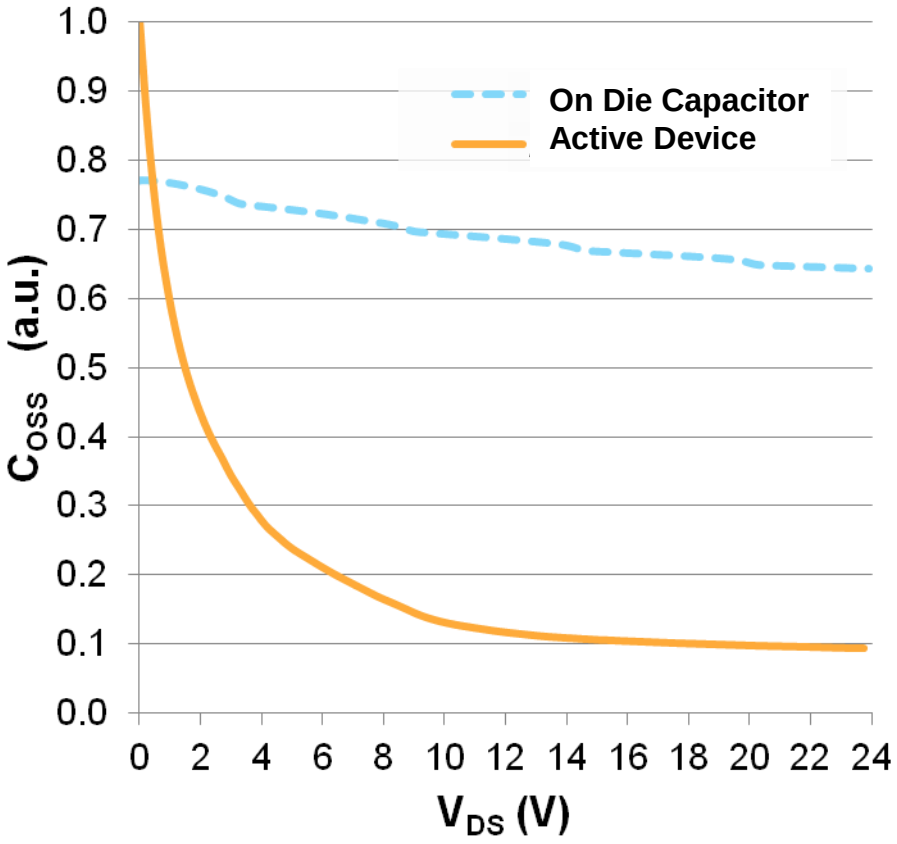


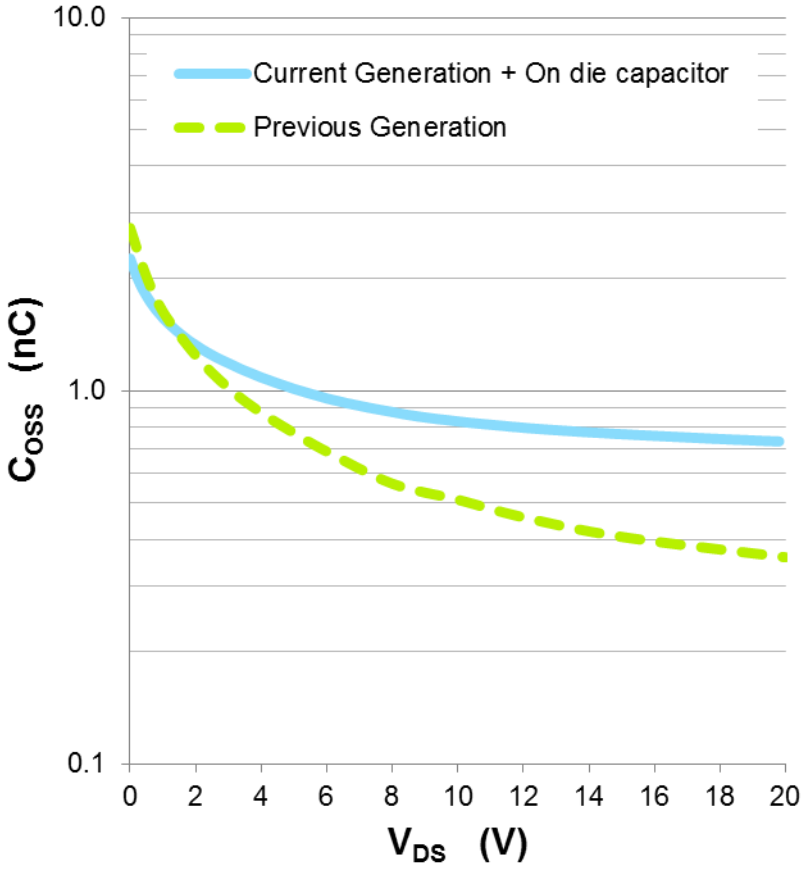
Modifying C_{OSS} 'shape'



Additional on die capacitors have an almost linear $C(V_{DS})$ behaviour and can be used to improve in nonlinear capacitive behaviour of a design

Impact on efficiency is much less than adding external snubber, or lowering switching speed to reduce voltage overshoots

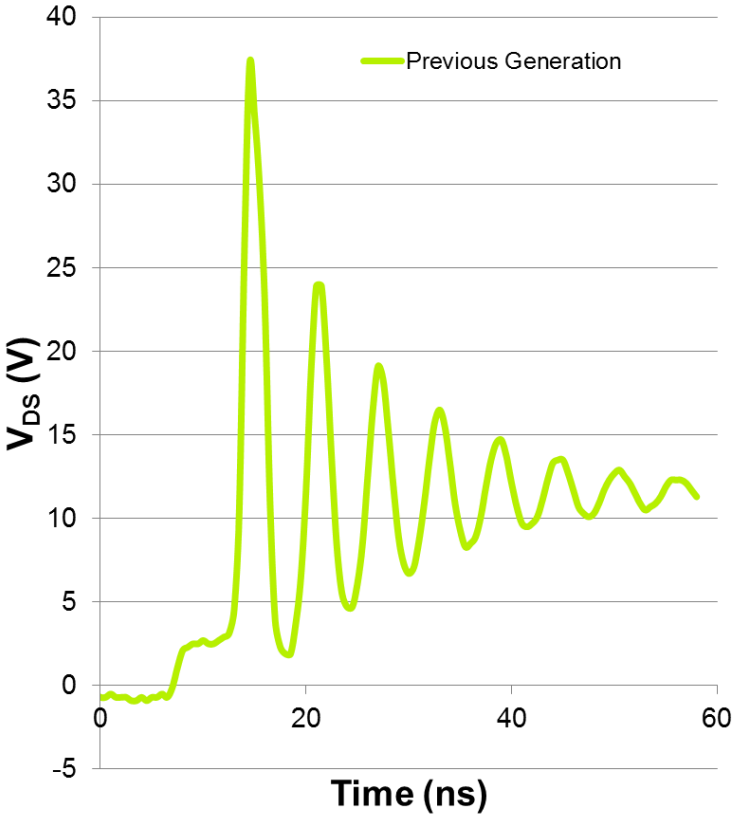
Results: Device Comparison

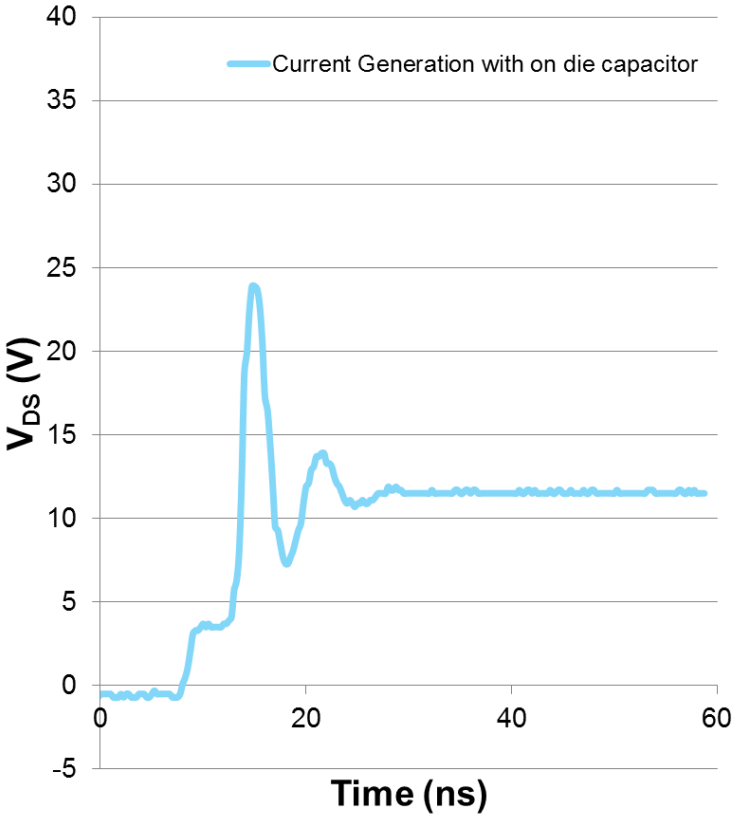


	Previous Generation	Current Generation
$R_{DS(on)}$ (V_{GS}=10V)	3.3mΩ	3.2mΩ
$R_{DS(on)}$ (V_{GS}=4.5V)	4.25 mΩ	4.2 mΩ
Q_G (V_{GS}=4.5V)	14nC	9.5nC
C_{OSS} (V_{DS}=15V)	**380pF**	**755pF**
Q_{OSS} (V_{DS}=15V)	10.2nC	16.7nC
$Q_G \cdot R_{DS(on)}$	60mΩnC	40mΩnC
$(Q_G+Q_{OSS}) \cdot R_{DS(on)}$	103mΩnC	110mΩnC

*FOMs include package resistance

Results: Applications Testing

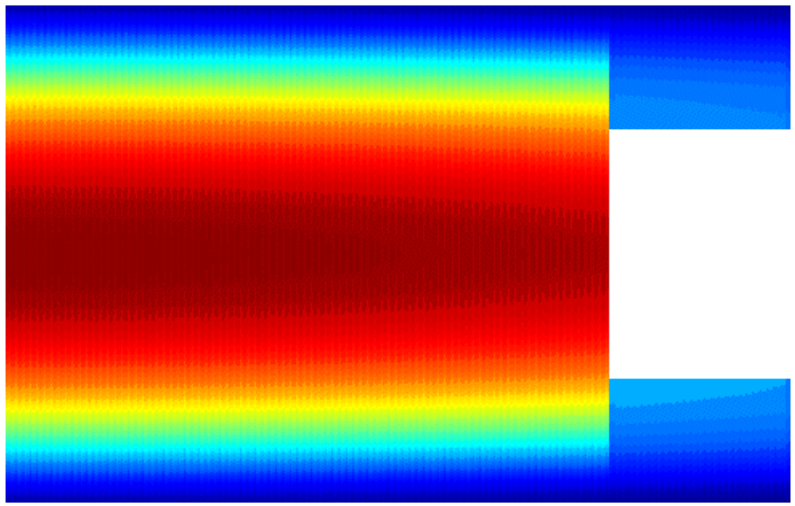


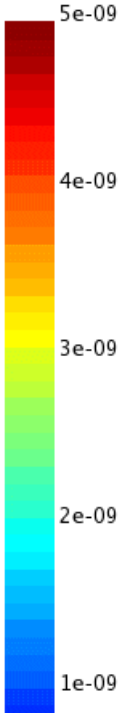


Significant improvement in voltage overshoots due to improved C_{OSS} shape

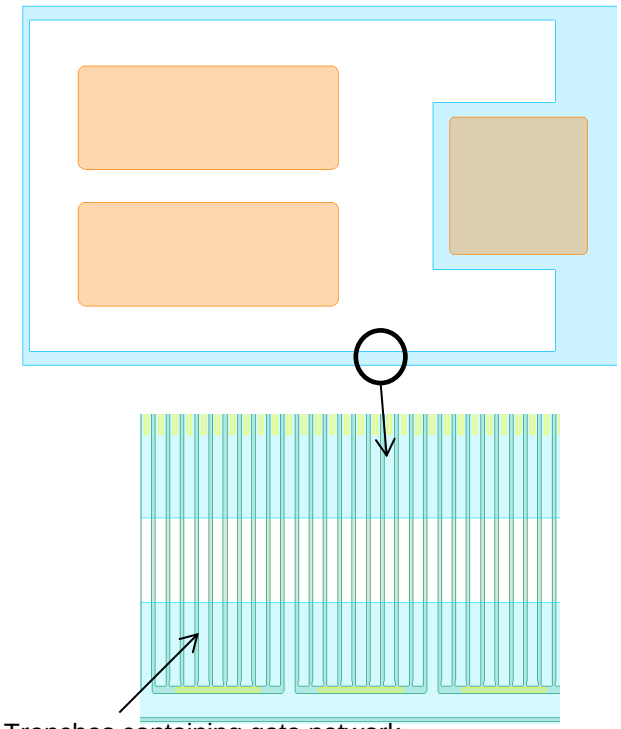
Internal Switching of MOSFET

- Simulation of internal gate structure shows large variation of switching times across a MOSFET
- MOSFETs will still have both low and high R_G parts of the die



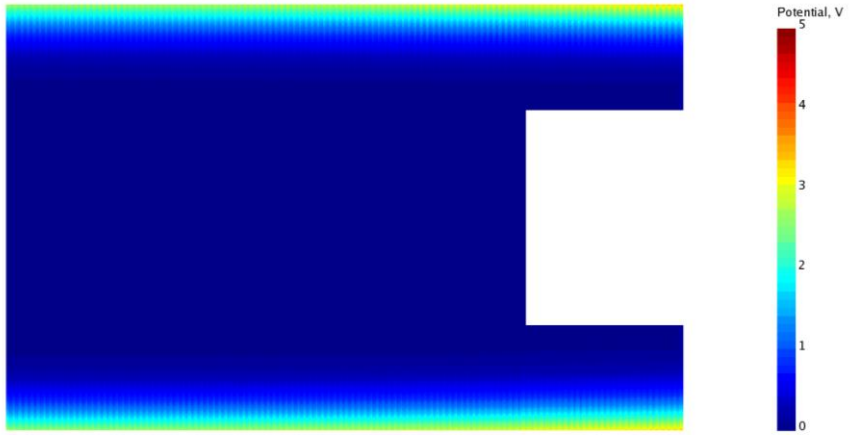


Time to reach 0.63 of applied voltage

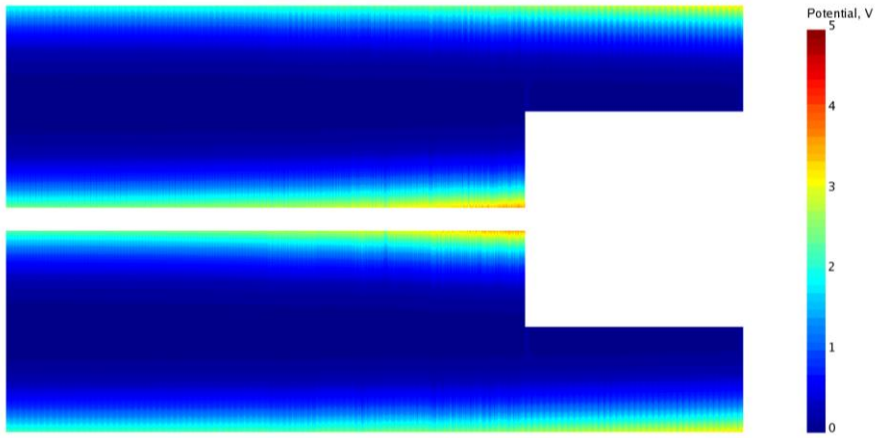


After 0.1ns of 5V V_{GS} applied

R_G =2.1Ω



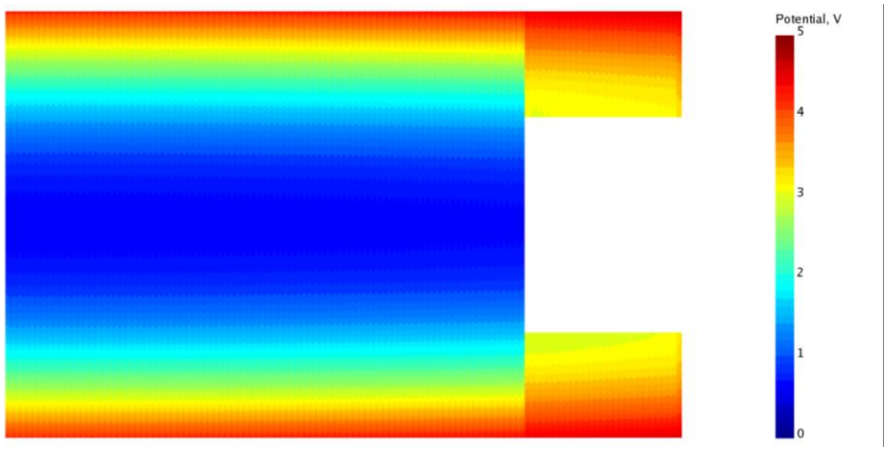
R_G =0.6Ω



- Comparison of two designs of equal active area
- One design has additional gate bus bar to distribute hate signal
- Switching improvement based on measured R_G should be x3.5 faster

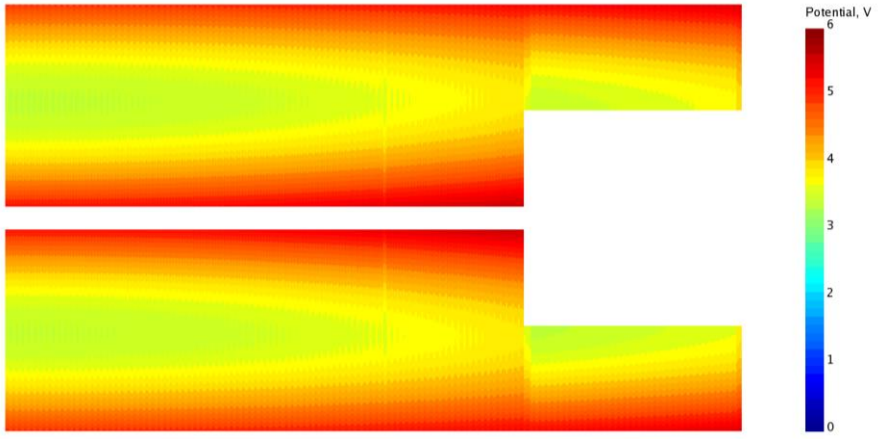
After 1.06ns of 5V V_{GS} applied

R_G =2.1Ω



- High RG part still turns on quickly due to low R_G portion of die

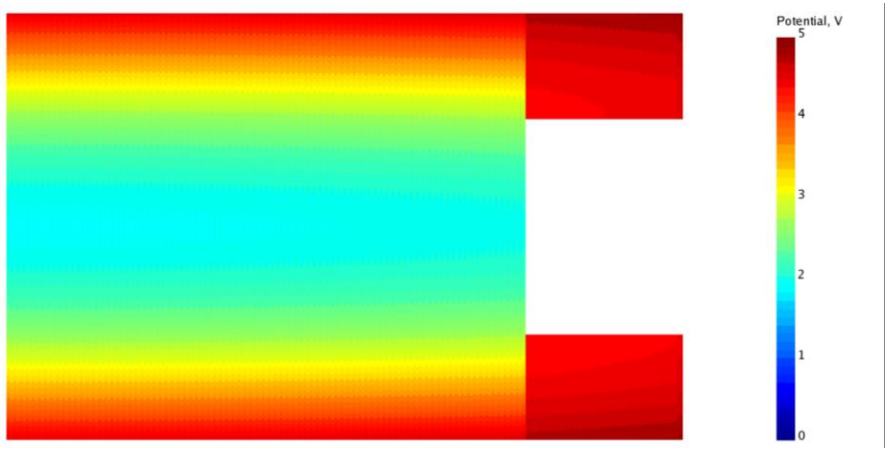
R_G =0.6Ω



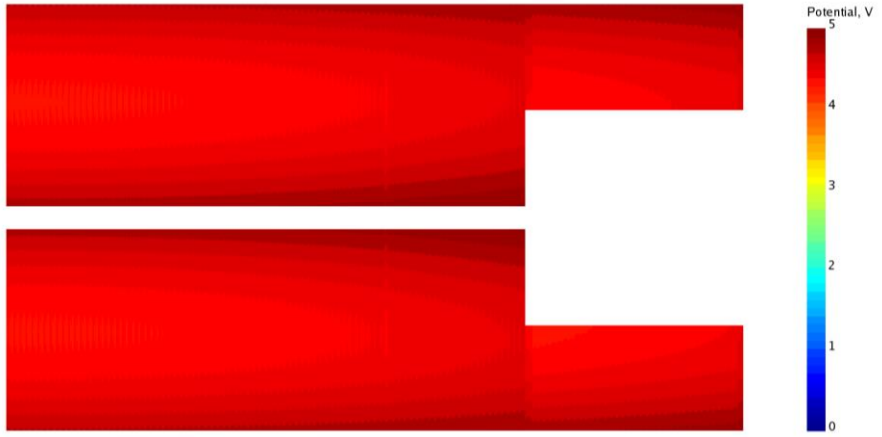
- Low R_G part turns on much more uniformly

After 2.25ns of 5V V_{GS} applied

R_G =2.1Ω



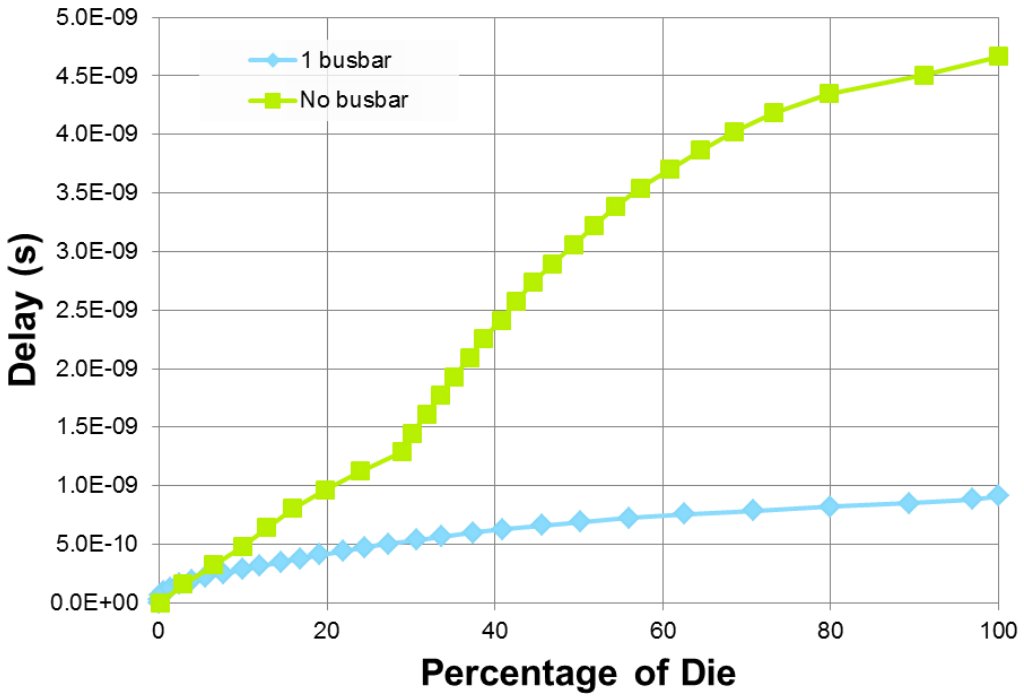
R_G =0.6Ω



- Can observe see almost 3V difference in V_{GS} across the high R_G die
- Major impact of poor switching uniformity is to give slow turn off, resulting in reduced efficiency

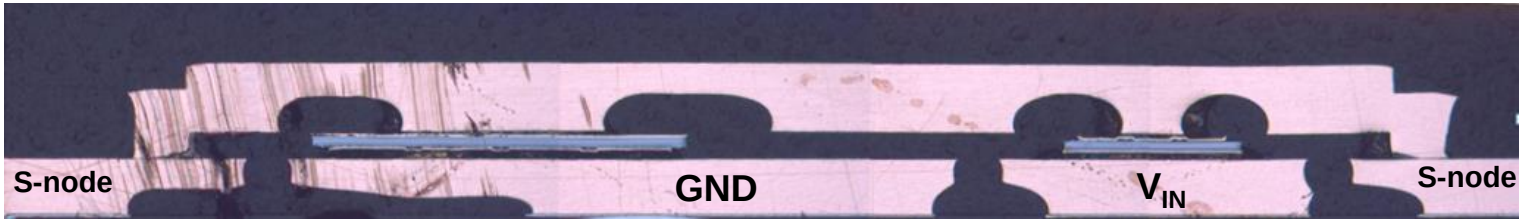
Delay Distributions

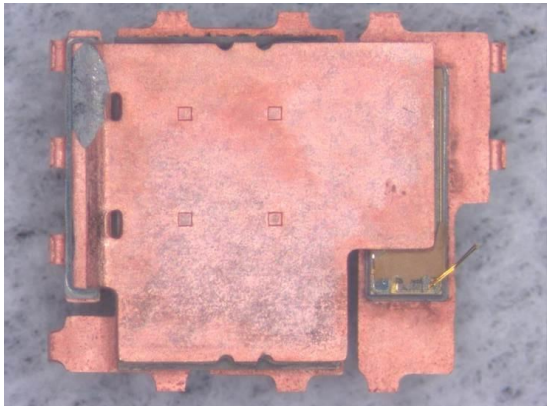
- At turn on both designs will quickly
- At turn off, switching is speed is related to the slowest part of the die
  - Lower R_G 5.1x faster than high R_G (R_G values suggested x3.5 difference)



Packaging Evolution

- Discrete Packages limited to <1MHz due to package & layout inductance rather than silicon performance
- Multi-die packaging or embedded die technology with inverted die & clips will enable >1MHz switching





Conclusions

- Vertical silicon offers the best overall solution for DC-DC conversion
  - reliability, cost, footprint, performance
- Switching performance of Power MOSFETs are approaching the natural switching speed of the circuit (i.e. its resonant frequency)
  - $(Q_G+Q_{OSS})\cdot R_{DS(on)}$ becomes most important FOM
  - Low inductance packaging and layout critical
- Fast switching results in high voltage overshoots
  - Non linear behaviour of the C_{oss} means these overshoots $\approx$3x V_{IN}
  - Voltage rating of the MOSFET can be exceeded
  - Creating a more linear $C_{oss}(V_{DS})$ can reduce voltage overshoots
- Fast turn off requires low internal R_G to all parts of the die