MagnaChip

Analog & Mixed Signal Company

High-Frequency Power Management Technologies

François Hébert, Michael Sun, Kwangil Kim, Taehoon Lee, Juho Kim,
Hanseob Cha, Kyungho Lee, Jung Lee, Yue Chen, Namkyu Park, Taejong Lee

Francois.Hebert@MagnaChip.com

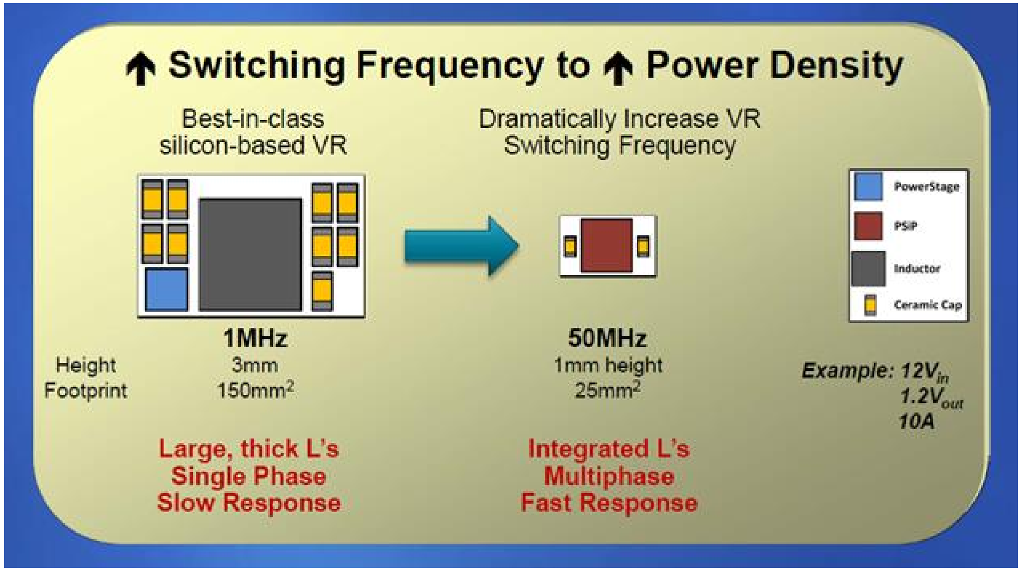
PowerSoC 2014 Workshop

Outline

- Why High-Frequency Power Management?
- What is High-Frequency?
- Silicon-based Power Technologies
- Compound Semiconductor Power Technologies
- Figures Of Merit & Device Performance Analysis
- Comparison of Technologies
- Future Trends
- Acknowledgements

Why High-Frequency Power Conversion?

- **Performance, Cost, Volume, Power Density, Weight, Temperature…**
  - **Smaller Power Inductor & Output Capacitors**
  - **Smaller Snubbers**
  - **Reduced heat sinking and cooling requirements**
- **Improved Overall System performance**
  - **High-frequency envelop tracking for RF systems**
  - **“LDO Killer” products: Switching regulator with integrated compact inductors**



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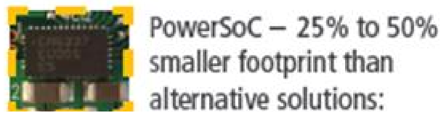
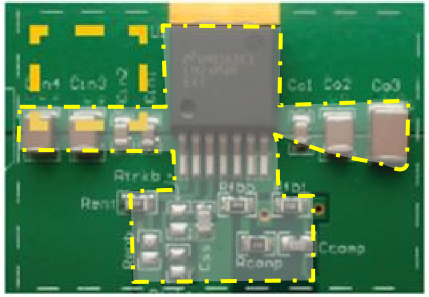
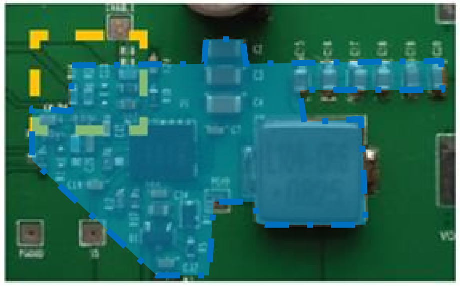


4MHz Integrated Inductor Regulator



400KHz-1MHz Regulator Module



100KHz-450KHz Discrete Regulator

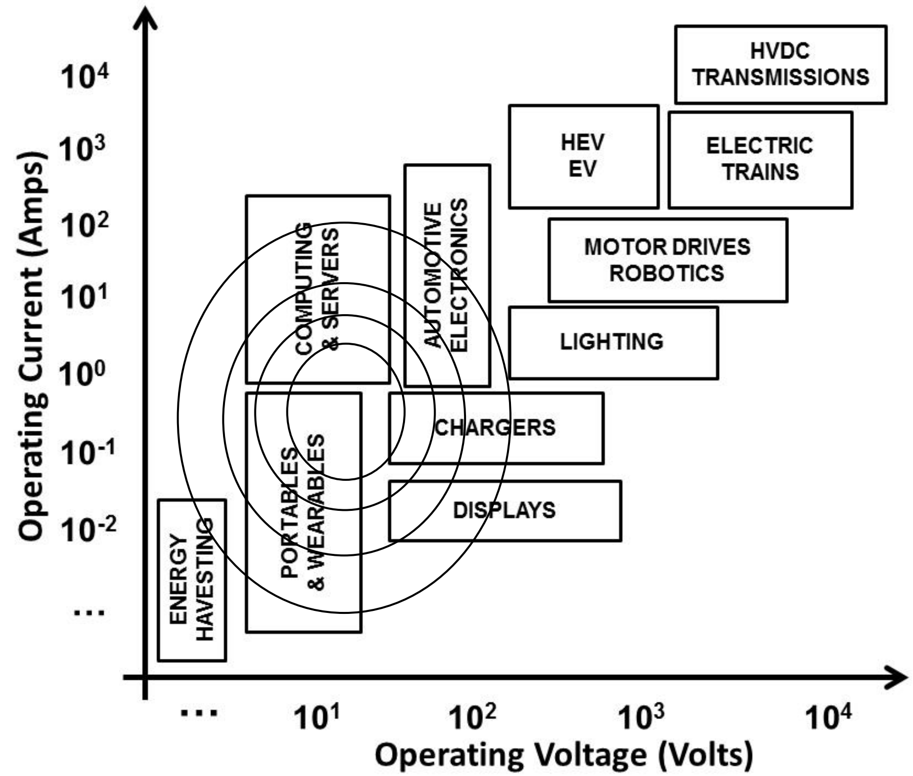
http://www.altera.com/literature/br/br-enpirion-brochure.pdf

What is High-Frequency Power Management

In this work, we focus on technologies which increase the operating frequency over the prior art, for Power Management applications which include:

- Energy Harvesting
- Wearables
- Mobile Devices (Smartphones)
- Internet Of Things
- Computing
- Servers
- Chargers (wired and wireless)

- **Frequency Ranges**
  - ~GHz: <3V, <0.1A
  - 10-100's MHz: <10V, <1A
  - 1-10 MHz: <30V, <40A
  - 100's KHz: <100V, <100A
  - 10's KHz: <1KV, <200A
  - ≤ 10KHz: >1KV, >200A



Silicon High-Frequency Power Management Technologies

- Si CMOS
- Si & SiGe Bipolars
- Si-SiGe Strained MOSFETs
- LIGBTs
- LDMOS

Review of Si-based Technology Options

In this section, Si-based technologies which capable of addressing the needs of high-frequency power management products and PowerSoCs, are considered

- CMOS
- Bipolar
- SiGe HBT
- Strained SiGe nLDMOS
- High-Frequency nLDMOS
- LIGBT

Performance analysis of the technologies and integrated devices, will be carried out in the following sections

- Qualitative review of the key technologies is included in this section

CMOS for High-Frequency Power

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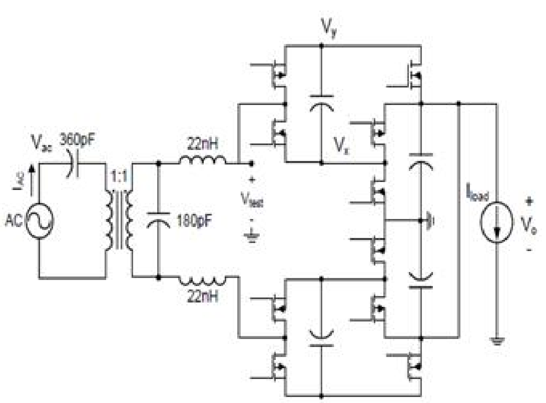
Sub-Micron CMOS and BCD are ideally suited for high-frequency Energy Harvesting SoCs. Key features:

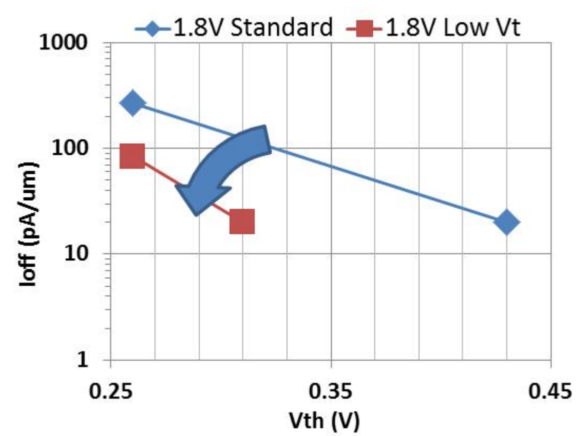
- **0.35, 0.18, 0.13, 0.11 µm, and below**
  - **to 5MHz, 15MHz, 30MHz, 50MHz and above, respectively [1]**
- **Low-Vth, Low Leakage Low-Voltage CMOS**
- **Medium-voltage CMOS for Analog and I/Os**
- **Low-leakage Bipolars and JFETs**
- **Low-Leakage Isolation (DTI, SOI, SOI+DTI)**
- **Fast Switching for GHz operation**

Switched-Capacitor Power Converters is another application of CMOS

[1] Wei Fu, Ayman Fayed, 2009 IEEE DCAS Workshop, Dallas TX



W.Li, D.J. Perrault, "Switched-Capacitor Step-Down Rectifier for Low-Voltage Power Conversion", APEC 2013



MagnaChip Energy Harvesting 0.18µm CMOS technology

0.18µm Energy Harvesting CMOS
(Example: MagnaChip HLG18)

LV
- 1.8V CMOS
- 1.8V Low Vth CMOS

MV
- 3.3V or V or 6V CMOS

Options
- DTI, SOI, DTI+SOI
- Thin-Film (TaN) Resistors
- High Value Poly Res
- Vertical NPN, Lateral PNP pJFET, nJFET
- MV MOS Cap, HV MOS Cap MIM Cap
- Poly Fuse, OTP, MTP
- Zener Diode, Isolated Diode Schottky Diode
- Thick Top Al, Thick Top Cu

Bipolar High-Frequency Power

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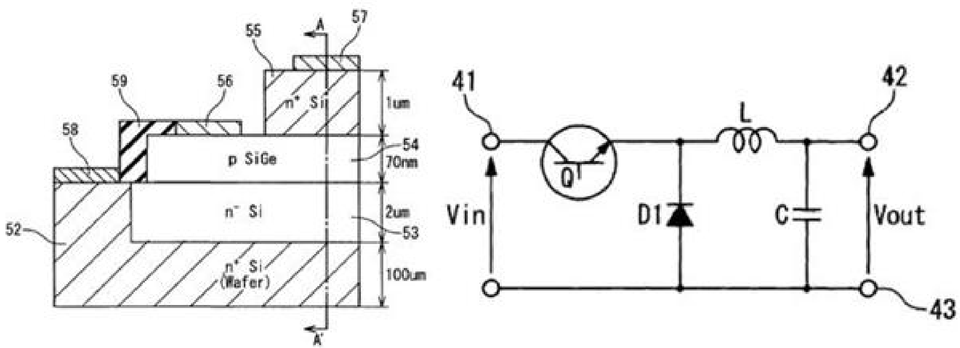
Silicon Bipolar-based technologies have been employed for more than 50 years for high-frequency power converters

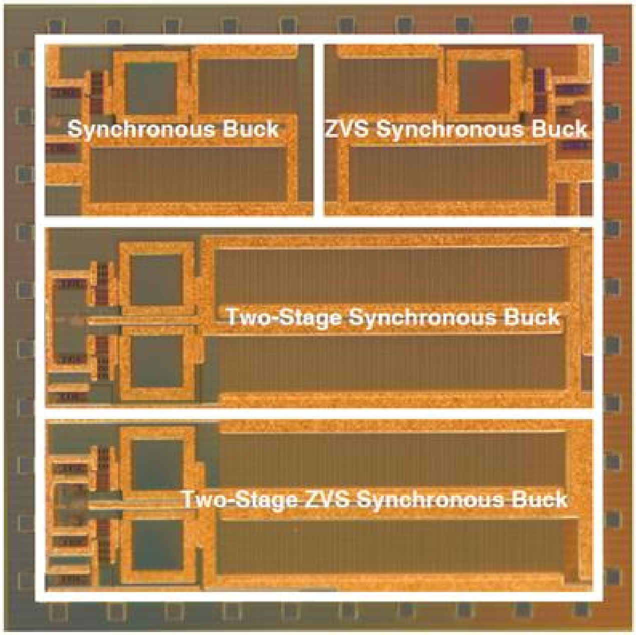
- Pure-Bipolar, CBip, BiCMOS, CBiCMOS, BCD
- V-NPN: high Ft, Fmax, BVceo, and low Rb, Vcesat
- Companies such as LTC, National/TI, Analog Devices, Motorola/Freescale, many others

- **Today's trend:**
  - Bipolar for Analog, and FETs for the Power
  - HBTs are keeping "Bipolar Power Alive and Well"



SiGe Power HBT: 20MHz Buck design with L and C only 5% of the values of conventional Bucks

US Patent 7042293, May 9, 2006



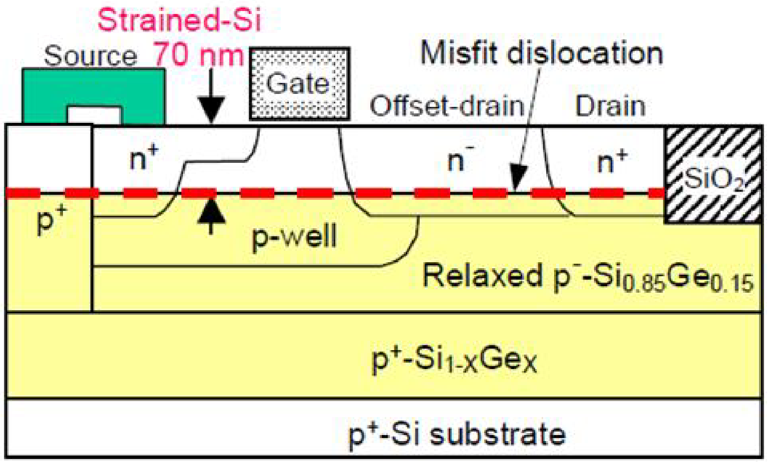
A Multi-Stage Interleaved 45MHz Synch Buck Converter with Integrated Output Filter in a 0.18μm SiGe Process

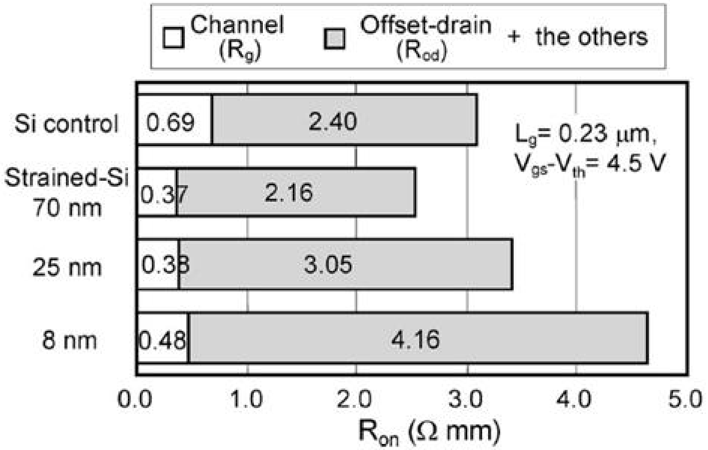
S. Abedinpour et.al.. Session 19.7, ISSCC Conference, February 2006

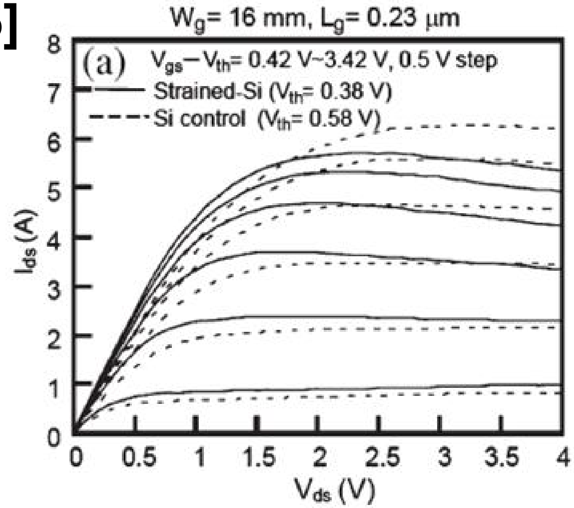
Strained Si-SiGe nLDMOS

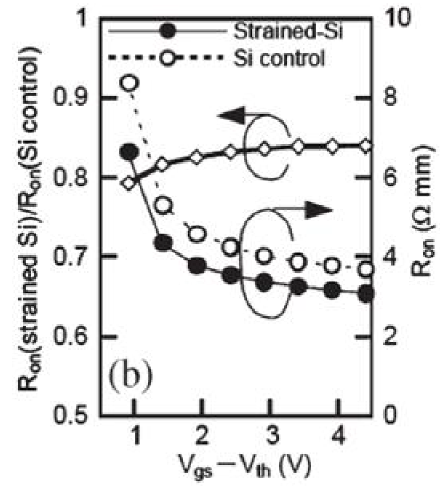
MOSFETs for lower voltage applications, can be improved by "strain engineering"

- **Strained Si-SiGe nLDMOS with improved performance over Si control devices, have been reported [1]**
- **This approach may be ideal for high-frequency PowerSoC based on deep-sub-micron CMOS with Strain-Layers.**
- **Intel reports integration of PowerSoC devices in ≤ 22 nm CMOS [2,3,4,5]**









[1] *M.Kondo et.al. IEEE Trans. Electron Dev, Dec 2006, pp 3136-3145*

[2] *http://www.eetimes.com/document.asp?doc_id=1263259*

[3] *http://www.pcper.com/reviews/Processors/Intel-Core-M-Processor-Broadwell-Architecture-and-14nm-Process-Reveal/Broadwell-M*

[4] *http://www.scribd.com/doc/236507605/Intel-14nm-presentation*

[5] *http://hothardware.com/News/Haswell-Takes-A-Major-Step-Forward-Integrates-Voltage-Regulator/*

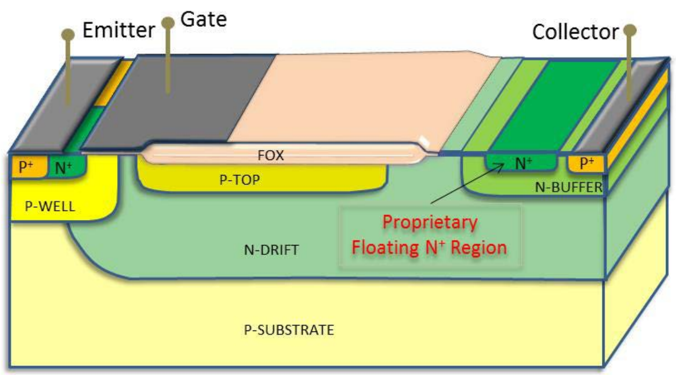
High-Frequency LIGBT

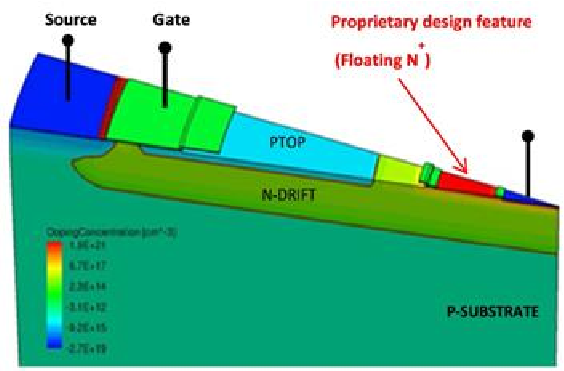
IGBTs are considered for High-Voltage and Dense solutions

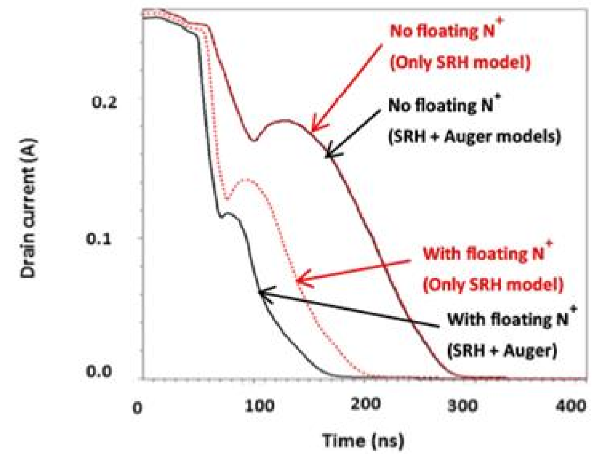
- LIGBT can be integrated with CMOS & BCD technologies

One challenge is the switching losses associated with bipolar IGBTs

- Innovative solutions are being developed
- Ex: Floating N+ region in collector (Cambridge Semi. and Camutronics (UK))
- 800V-rated LIGBT Drift regions based on Double-RESURF approach
- Can be driven by standard LV CMOS gate drivers (Vgs 3.3/5V)
- Width of Floating N+ region adjusted to trade-off between conduction (Rsp 23 to 90 mOhm*cm^2, switching time 100-300ns, BVdss 850V) to optimize the total losses for specific applications





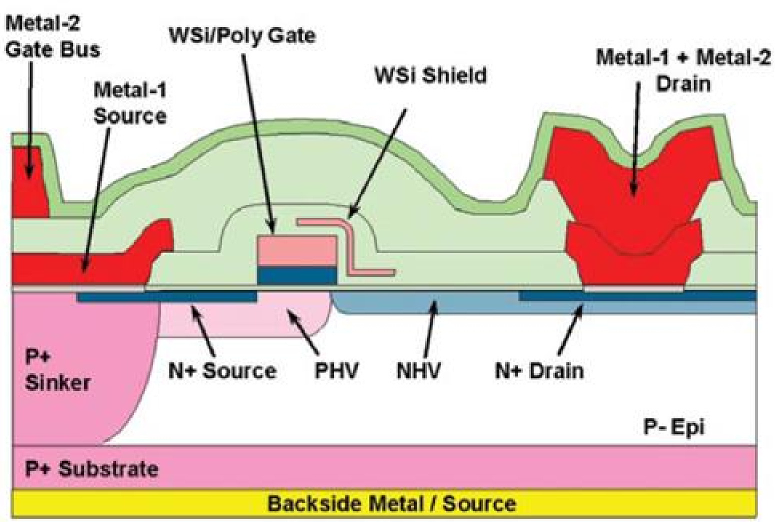


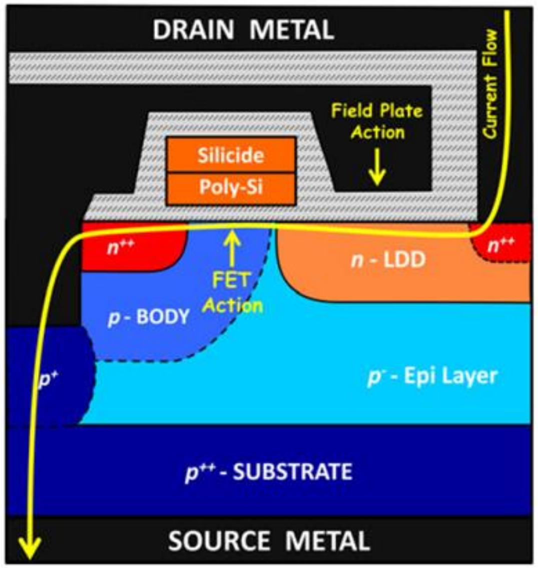
800V Lateral IGBT in Bulk Si for Low Power Compact SMPS Applications T. Trajkovic et.al., ISPSD 2013, Session 11.4

Discrete Low-Qg Power nLDMOS

High-Frequency Power LDMOS are typically referred to as RF-LDMOS or Bottom-Source LDMOS

- P+ Substrate connected to the source using sinkers or conductive trenches
- Planar structure with self-aligned body and drift-drain diffusions
- Low-resistance polycide or salicided gate electrode
- Well known examples include: Freescale (Motorola) since 1990's, TI (Ciclon)
- Drawback: not compatible with fully integrated PowerSoC BCD technologies





*Ron*Qg ~38*
BVdss>25V

http://www.eetimes.com/document.asp?doc_id=1229814

http://www.freescale.com/files/rf_if/doc/white_paper/50VRFLDMOSWP.pdf

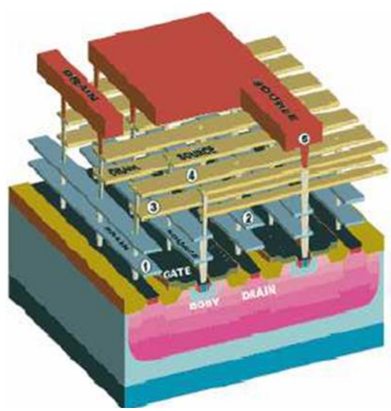
B. Yang et.al. "Advanced Low-Voltage Power MOSFET Technology for Power Sup ply in Package Applications", IEEE Trans. Power Electronics, Sept 2013, p 4202

Low-Qg nLDMOS compatible with BCD

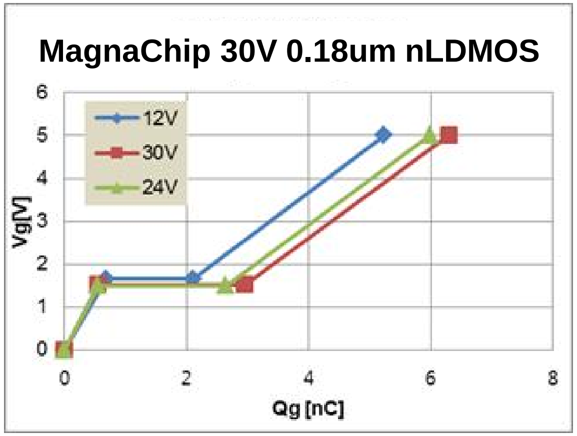
Bottom-Source nLDMOS cannot be integrated in standard High-Frequency BCD Power Management technologies.

Requirements of nLDMOS compatible with BCD, include:

- **Minimized additional processing steps (Cost)**
- **Fully Isolated Drain and Body (FISO)**
- **Optimized N-Drift for low Rsp (<10 mOhm*mm^2, BVdss>25V), Ron*Qg (<50mOhm*nC)**
- **Optimized Cell and Metal Layout**
- **Robust and capable of withstanding high avalanche current (UIS)**



http://www.siliconfrontline.com/files/Power_Device.pdf

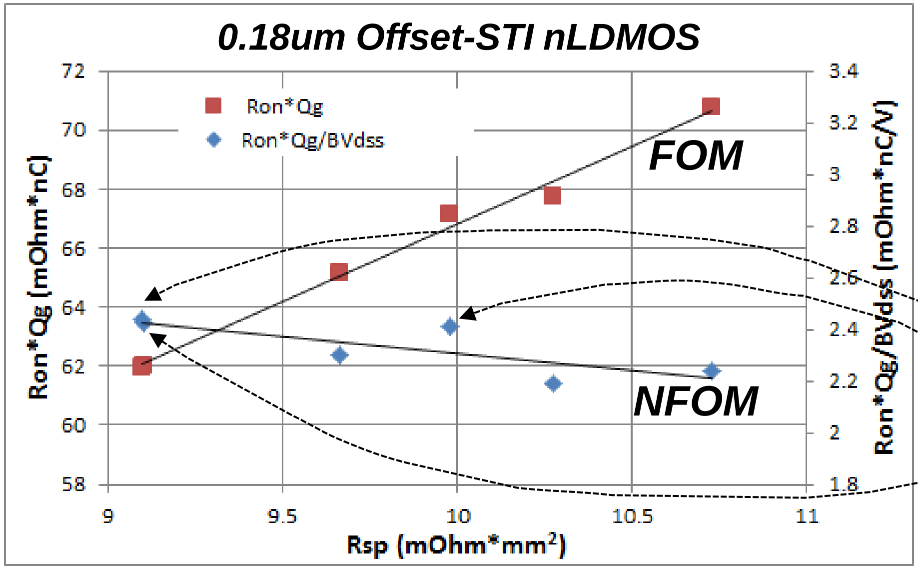


High-Frequency PowerSoC LDMOS Optimization

High-Frequency PowerSoC require nLDMOS switches which are compatible with highly integrated technologies (i.e. BCD) with performance equivalent to RF LDMOS

A new Figure of Merit is considered to facilitate device optimization

- **"Ron*Qg/BVdss", defined as NFOM (Normalized FOM)**
- **NFOM takes into account the strong correlation between BVdss & Rsp**
- **Excessive Trade-off can be identified and minimized**



Offset-STI 0.18um nLDMOS TCAD Simulation Results

Rsp	BVDSS	Ron*QQg	Ron*Qg/BVdss
10.73	31.62	70.75	2.24
10.27	30.94	67.78	2.19
9.67	28.29	65.18	2.30
9.10	25.60	62.03	2.42
9.98	27.88	67.16	2.41
9.10	25.40	61.94	2.44

Low-Qg BCD-Compatible nLDMOS Feasibility

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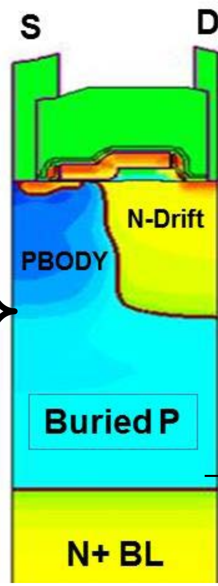
Fully-Isolated nLDMOS with performance equivalent to that of RF-nLDMOS are critical for high-frequency PowerSoCs

- Key Benchmark: 25V-rated nLDMOS Ron*Qg <40mOhm*nC (TI/Ciclon)
- "Offset" nLDMOS: Ron*Qg in the 40-55 mOhm*nC
- "Offset" nLDMOS Optimized Si Data: Ron*Qg 43mOhm*nC
- "Non-Offset" (ex: Planar) nLDMOS: Ron*Qg <40 mOhm*nC feasible

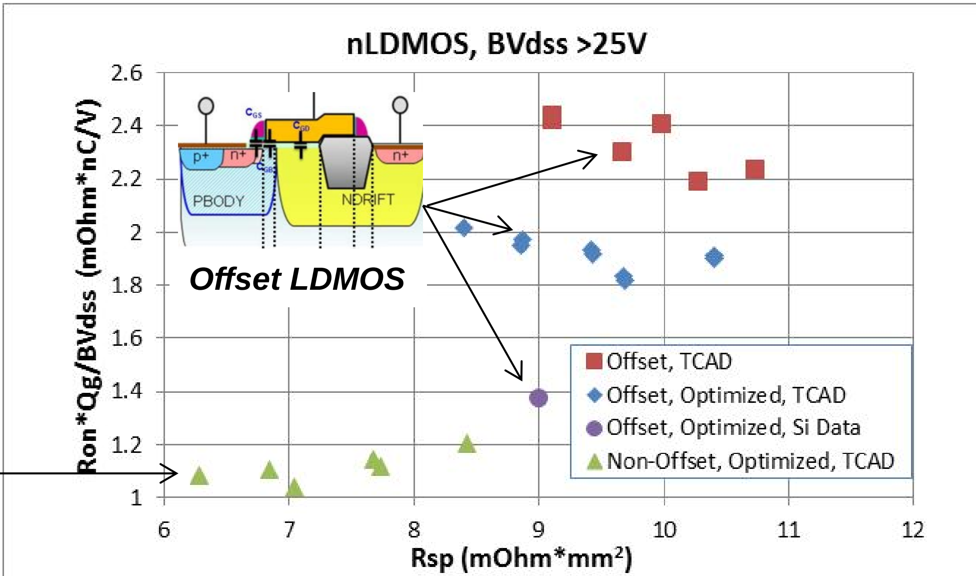
0.18um nLDMOS TCAD Simulation Results

Rsp	BVDSS	Ron*Qg	Ron*Qg/BVdss
7.04	29.38	30.61	1.04
6.84	30.12	33.30	1.11
8.42	32.67	39.33	1.20
7.68	31.78	36.41	1.15
6.28	27.36	29.68	1.08
7.74	31.23	34.88	1.12

nLDMOS with Ron*Qg~30, compatible with BCD feasible



Non-Offset nLDMOS

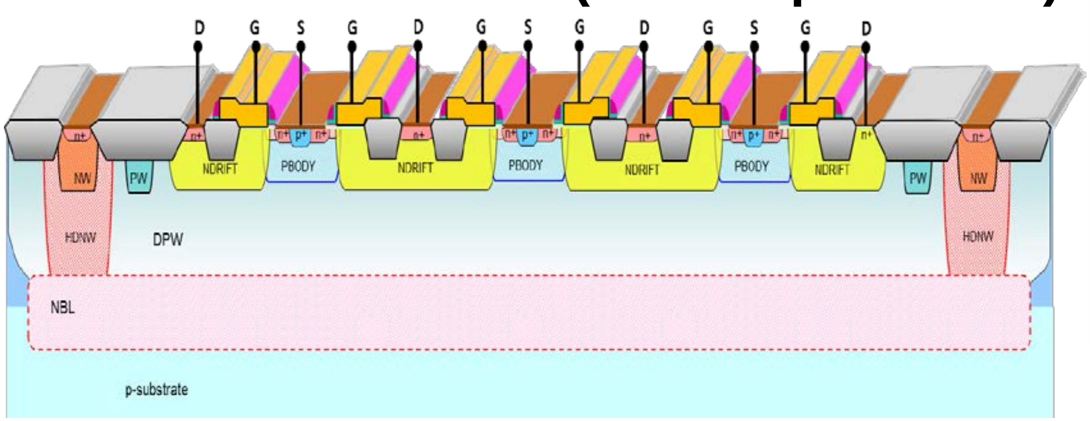


*Ron*Qg data for Vgs=4.5V, Vds=15V*

High-Frequency PowerSOC BCD

Full Function BCD for High-Frequency PowerSoC

- High-Current High-Frequency nLDMOS
  - *Ron*Qg ~40mOhm*nC (measured) today*
  - *Ron*Qg ~30mOhm*nC (TCAD) feasible!*
- Analog Extended drain n/pEDMOS
- CMOS (LV and MV)
- Bipolars (NPN, PNP)
- Passives (Res, Caps, Diodes)
- Power Interconnect (thick Top Al or Cu)



0.18µm High-Performance BCD
(Example: MagnaChip HP18E30)

HV
- 8V, 12V, 16V, 20V, 24V, 30V Fully Isolated (FISO) nLDMOS
- 12V, 20V, 24V, 30V High-Side n/p EDMOS

MV
- 5V or 6V CMOS

LV
- 1.8V CMOS

Options
- High Value Poly Res
- Vertical NPN BJT, Lateral & Substrate PNP BJT
- MV MOS Cap, HV MOS Cap, MIM Cap
- Poly Fuse, OTP, MTP
- Zener Diode, Isolated Diode, Schottky Diode
- Thick Top Al, Thick Top Cu

Compound Semiconductor High-Frequency Power Technologies

- GaAs: pHEMT, pHEMT + HBT
- GaN: HEMT, HEMT + CMOS

PowerSoC 2014 Workshop

Non-Si High-Frequency Power Management

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Material systems and device structures considered include

GaAs

- **PHEMT**
- **PHEMT + Bipolar**
- **Ron*Qg FOM reported to be <15 mOhm*nC for GaAs**

GaN

- **HEMT**
- **HEMT+ Si CMOS**
- **Ron*Qg FOM reported to be <25 mOhm*nC for GaN**

GaAs FET High-Frequency Converters

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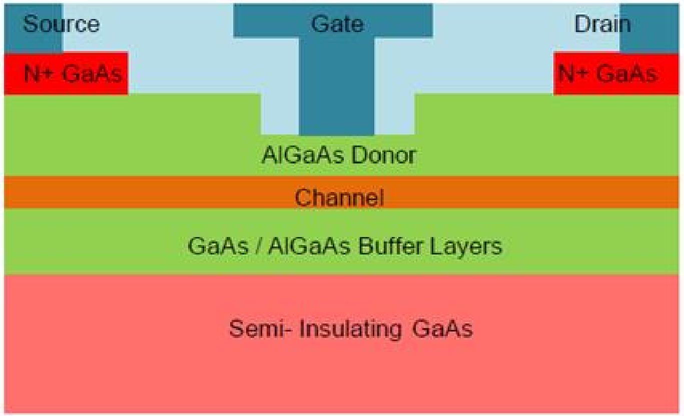
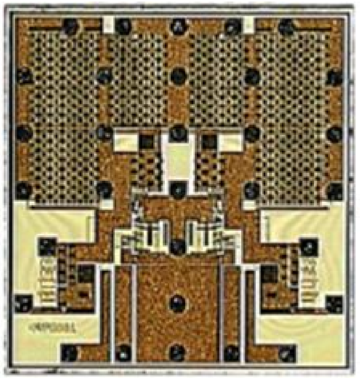
GaAs FET-based high-frequency DC converters considered since the late 90's

- 100MHz MESFET DC-DC (GaAs 2000)
- 150MHz pHEMT DC-DC (2010 RFIC Symp)
- 100MHz pHEMT DC-DC (2012 PowerSoC)

- **Technology features**
  - D-Mode MESFETs
  - D and E-Mode pHEMTs
  - D/E-Mode pHEMTs + HBT
  - Passive devices
  - Low Parasitic Interconnect



http://www.rpi.edu/cfes/AnnualConference/B6%20Mona%20Hella.pdf January 2013



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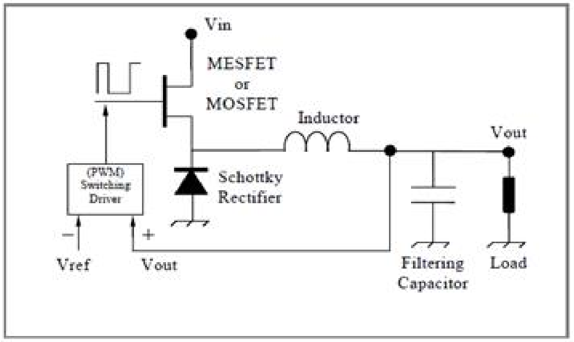
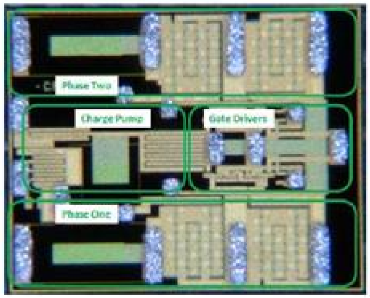
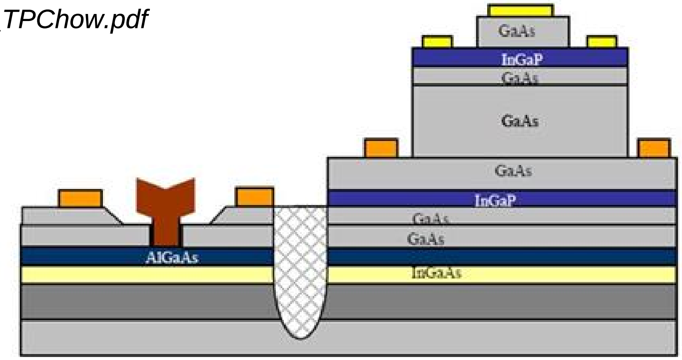


http://amsacta.unibo.it/226/1/GAAS11_4.pdf



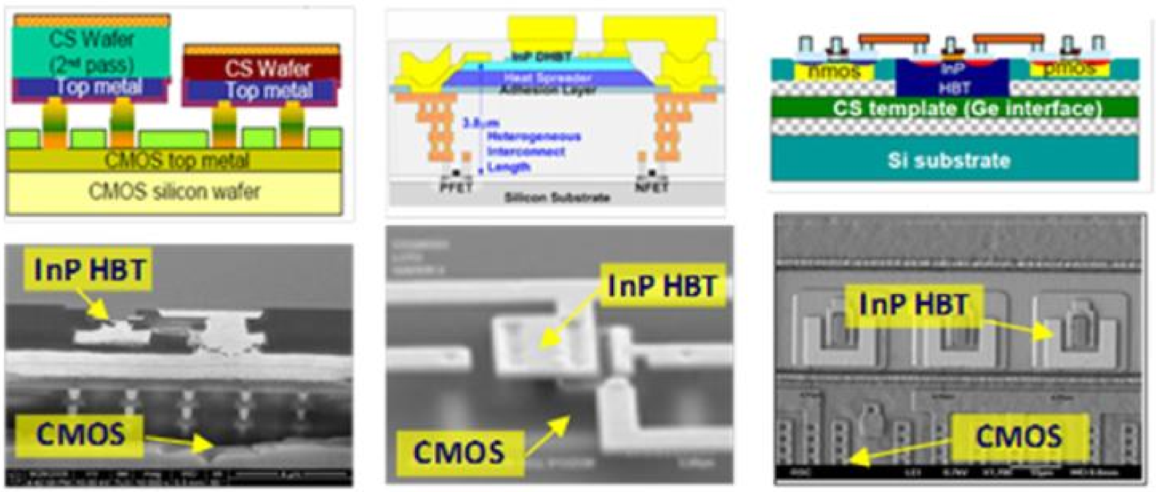
H. Peng et.al., IEEE RFIC Symposium, 2010, pp 259-262



http://gaasmantech.com/Digests/2007/2007%20Papers/13c.pdf

Heterogeneous Integration for PowerSoCs

Combination of InP HBTs with CMOS logic devices has been under development over the past decade



(a) (b) (c)

Figure 2: Heterogeneous integration processes being pursued in the COSMOS program, (a) micrometer scale assembly, (b) epitaxial layer printing, and (c) monolithic epitaxial growth using a multi-layered lattice-engineered substrate.

http://gaasmantech.com/Digests/2012/papers/3.1.010.pdf

GaN High-Frequency DC-DC (1)

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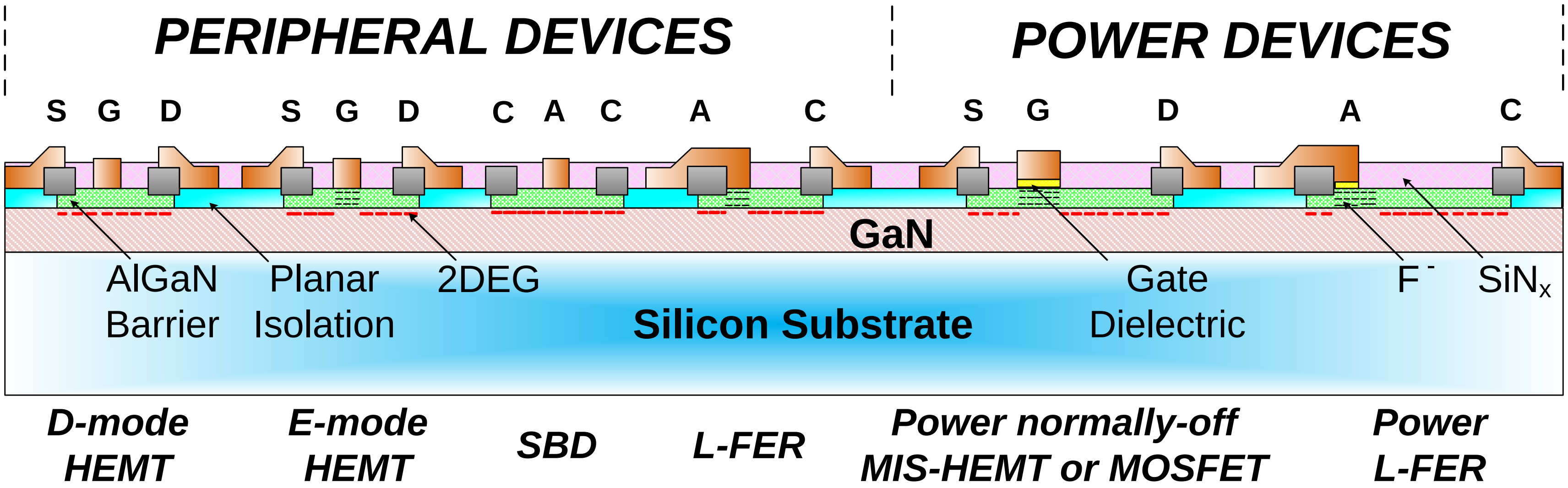
GaN Monolithic Power IC technology from HKUST:

- Complementary Devices
- E-Mode MIS-HEMT; E-Mode HEMT; D-Mode HEMT
- L-FER, SBD, Passive, Power Interconnect

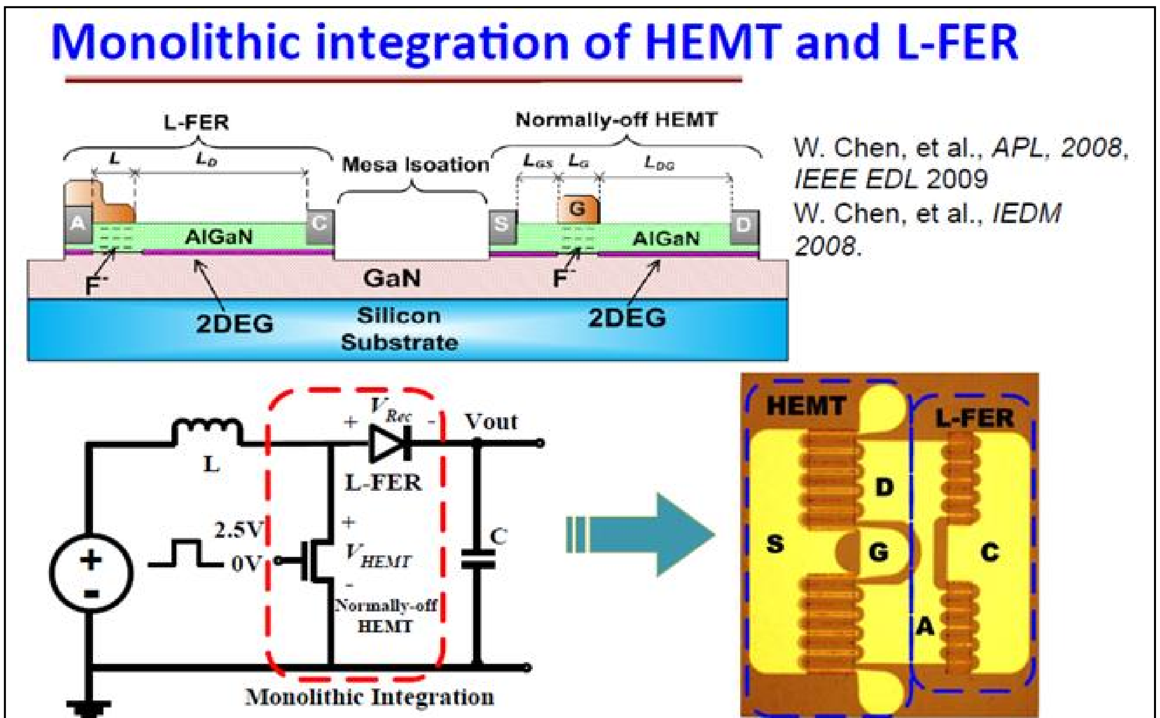


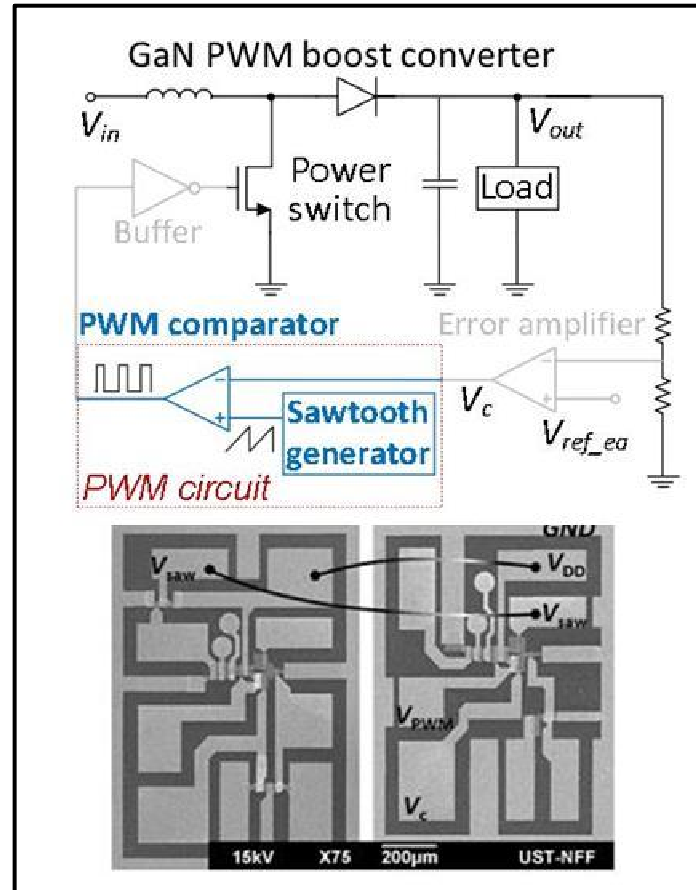
[1] K. –Y. Wong, W. Chen, and K. J. Chen, ISPSD, pp. 57-60, 2009.
[2] Y. Cai, et al, TED, vol. 53, pp. 2207-2215, 2006.
[3] W. Chen, et al, Appl. Phys. Lett., vol. 92, 208.

GaN High-Frequency DC-DC (2)

High-Frequency Power Circuits based on HKUST's monolithic Complementary GaN HEMT Technology :

- **PWM Converter and associated blocks**
- **Monolithic Boost Converter**





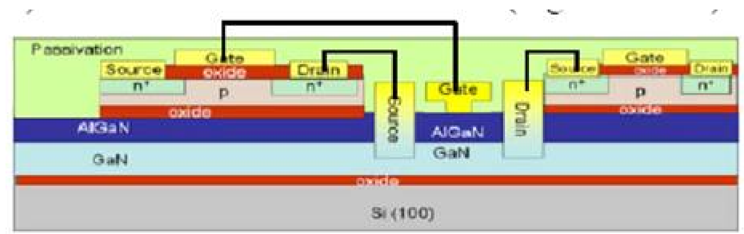
http://powersoc2012.org/session-2/2.3_KevinChen.pdf

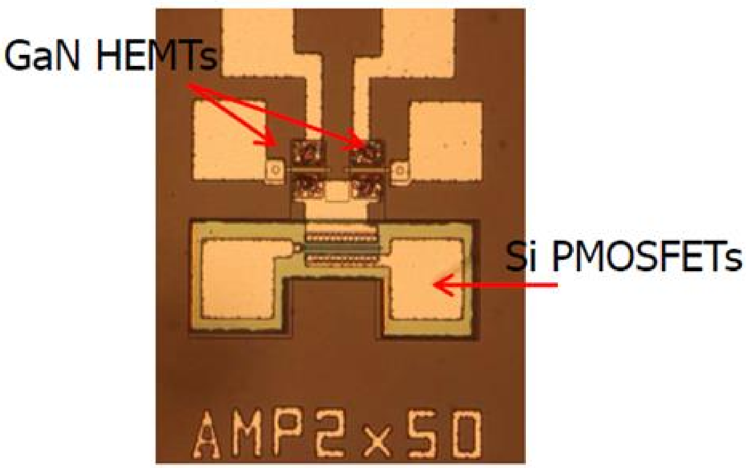
H. Wang, A. M. H. Kwan, Q. Jiang and K. J. Chen, ISPSD, pp.430-433, 2014.

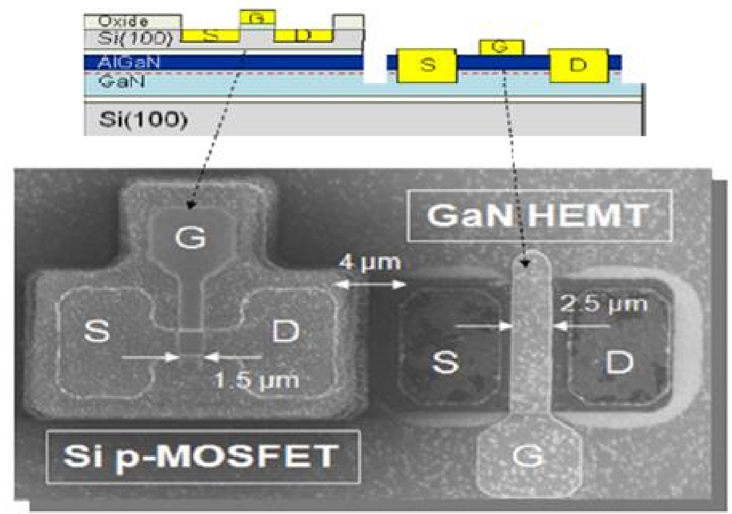
Monolithic Integration of GaN and Si

A critical requirement for PowerSoC applications is integration of dense Logic with the Analog & Power blocks

- **MIT & Raytheon, have successfully combined GaN HEMT devices with Si P-MOSFETs monolithically**
- **Functional circuits demonstrated**







T.E. Kazior et.al., CSICS, 2011, p 1-4

Chung, J. W. et al. "GaN-on-Si Technology, a New Approach for Advanced Devices in Energy and Communications." Proceedings of the European Solid-State Device Research Conference 2010 (ESSDERC). 52–56

GaN High-Frequency & High Voltage Converters

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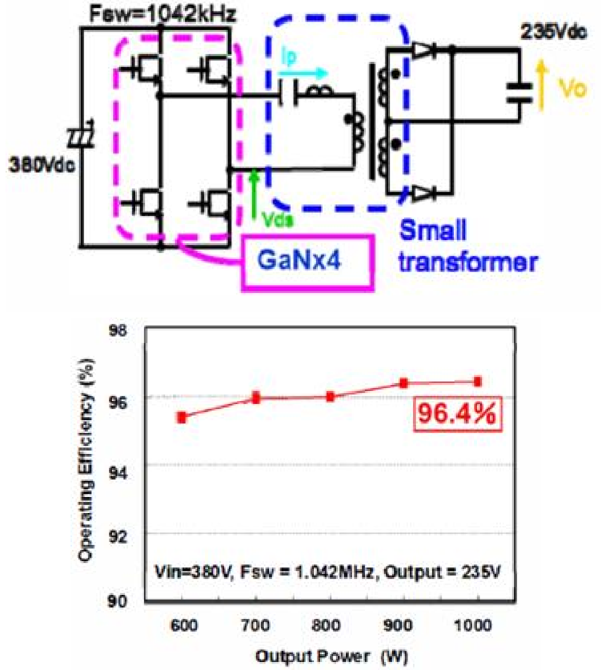
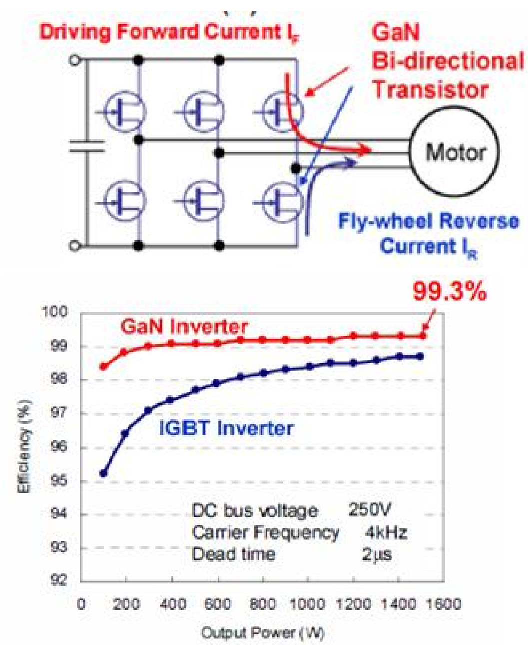
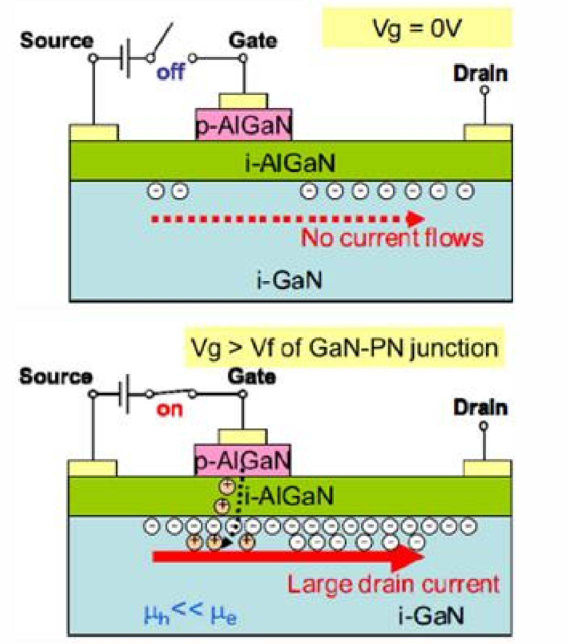
GaN e-mode HEMTS (P-doped Gate) Power Converters

- **Resonant LLC converter**
  - >350V, 1MHz operation, 96.4% efficiency
  - Equivalent Si-based converters operate at <1/2 frequency, efficiency <95%
- **Inverter**
  - >250V, 4KHz 99.3% efficiency, >1% higher than Si-based approach







T. Ueda, "Recent Advances and Future Prospects on GaN-Based Power Devices", IEEE 2014 International Power Electronics Conference, p. 2075

Figures of Merit

- Figures of Merit for Materials
- Figures of Merit for Devices
- Power Device Performance Comparison
- Comparison of High-Frequency Technologies

Figures Of Merit - Materials

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Multiple Figures of Merit have been developed to compare the performance of semiconductor materials and devices

Diamond is the best material!

- **But no Power Devices yet!**

GaN and SiC are fairly similar

- **SiC best for >600V Power (vertical devices, operation similar to Si devices, best thermals)**
- **GaN best for high-frequency and high-voltage (to ~600V) (lateral devices, compatible with Si fabs)**

GaAs is best for <30V RF Power applications

- **Being considered more and more for Power**

Table II: Main figures of merit for wide-bandgap semiconductors compared with Si [2].

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5304459
BPFM	1.0	0.9	57.3	35.4	10.7	594
BTFM	1.0	1.4	748.9	458.1	560.5	1426711

JFM : Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.

BFM : Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET

FSFM : FET switching speed figure of merit

BSFM : Bipolar switching speed figure of merit

FPFM : FET power handling capacity figure of merit

FTFM : FET power switching product

BPFM : Bipolar power handling capacity figure of merit

BTFM : Bipolar power switching product

http://power.eecs.utk.edu/pubs/epe2003_wide_bandgap.pdf?origin=publication_detail

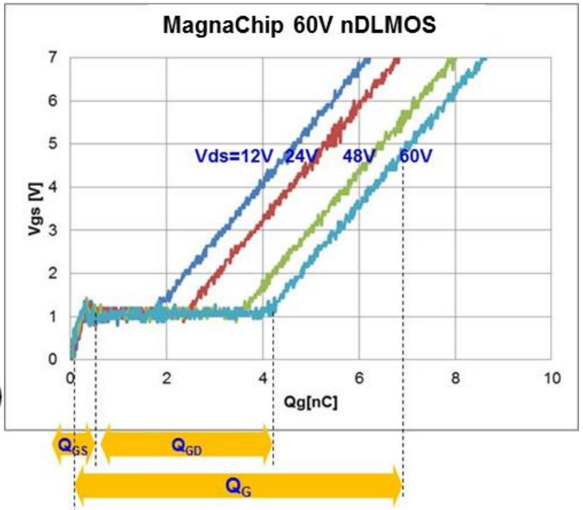
Figures Of Merit – Device Specific

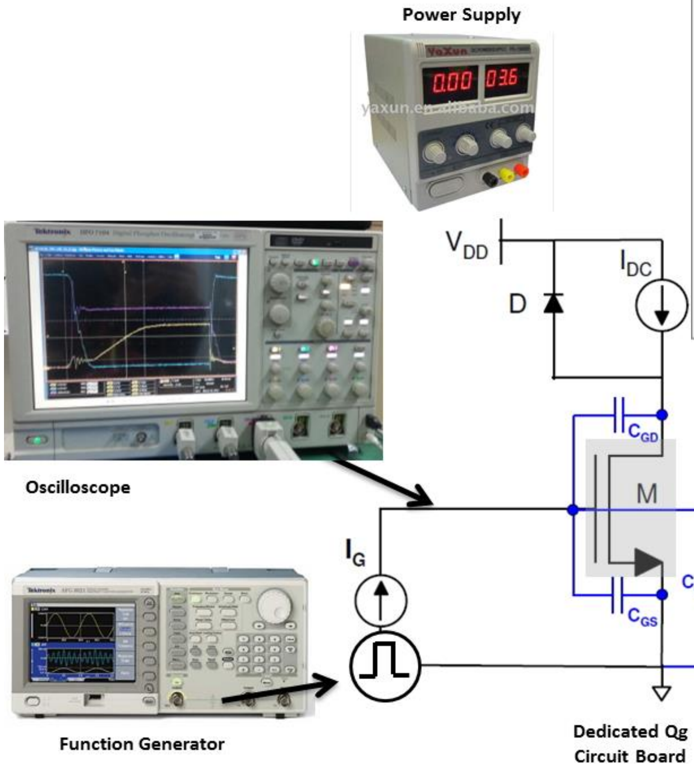
For high-frequency power management, Ron*Qg is the preferred FOM for selecting the best switching power devices

- **Minimize Qg to minimize switching losses**
- **Minimize Ron and Rsp (Rdson*Area) to minimize conduction losses and cost**

Wafer level measurements of low Ron and low Qg power devices established

On-wafer results are within a few percent of packaged device data





Power Device Performance Comparison

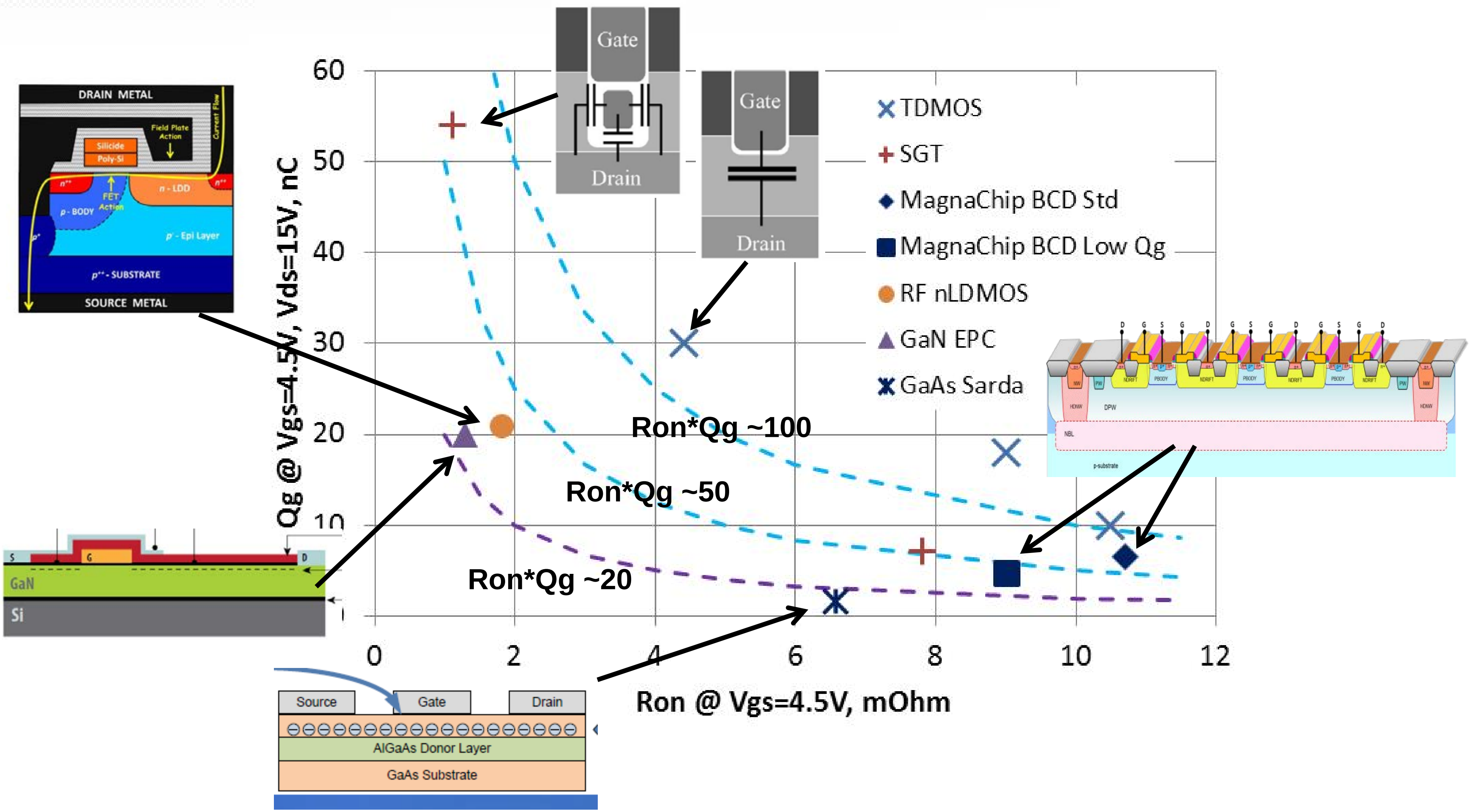
High-Current Power Device Performance Measured Data

- **Si, GaN and GaAs devices are compared**
- **There is limited BCD-nLDMOS data in the literature!**

Device Type	Device	Ron @ Vgs=4.5V	Qg @ Vgs=4.5V @Vds=15V	Ron * Qg mOhm*nC	BVdss Min (V)
TDMOS	Vishay SI7390	10.5	10	105.0	30
TDMOS	IR IRF7811W	9	18	162.0	30
TDMOS	IRF6612	4.4	30	132.0	30
SGT	AOS AON6918	7.8	7.2	56.2	25
SGT	Infineon BSN011NE2LS	1.1	54	59.4	25
RF LDMOS	TI CSD16401Q5	1.8	21	37.8	25
BCD 0.18	MagnaChip BCD Std	10.7	6.55	70.1	30
BCD 0.18	MagnaChip BCD LowQg	9	4.82	43.4	30
GaN P-gate	EPC EPC2023	1.3	20	26.0	30
GaAs PHEMT	Sarda	6.6	1.6	10.6	20

Data from published datasheets and references listed in this report. Measured Data.

FOM – High-Current Power Devices



Comparison of High-Frequency Technologies

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Si BCD with nLDMOS is the best option for mainstream high-frequency power management PowerSoCs applications

Requirements for High-Frequency PowerSOC	Si BCD + nLDMOS	GaAs pHEMT	GaN HEMT	GaN HEMT + CMOS
Source of Device Data	MagnaChip 0.18 BCD	Sarda PowerSOC 2012	EPC EPC2023	Raytheon+MIT 2011
Logic Density: Low, Med, High	High	Medium	Low	High
Memory, Trimming	Yes	No	No	Yes
Cost: Low, Med, High, Very High	Medium	High	High	Very High
Production Readiness	Mature	Mature	Product R&D	Early R&D
Robustness of Power Devices	High	Medium	Low	Low
Ron or Rsp (Vgs=4.5V) mOhm or mOhm*mm^2	9 $mOhm*mm^2$	6.6 mOhm	1.3 mOhm	n/a
Ron*Qg (Vgs=4.5V, Vds=15V) mOhm*nC	43	10.6	26	n/a
Min BVdss of device considered	>30V	>20V	>30V	n/a

Data from published datasheets and references listed in this report. Measured Data

Future Trends

Si BCD technologies are expected to continue to dominate Power Management applications over the next 5+ years

- High-Frequency nLDMOS, with Ron*Qg FOM less than 40 mOhm*nC will be leveraged in order to increase switching frequencies at high-power, to >1MHz
- Strain-Engineering is expected to be considered more broadly to improve the performance of Silicon-Based technologies

Integration of Power Management Circuits with other Circuit IP blocks will accelerate over the next 3 to 5 years, with a potential for volume production in 5+ years

- GaAs and GaN: High-Frequency envelope tracking DC-DC with RF Circuit blocks
- GaN: High frequency High-Voltage drivers and other DC-DC and AC-DC building blocks, integrated with Si CMOS Controllers

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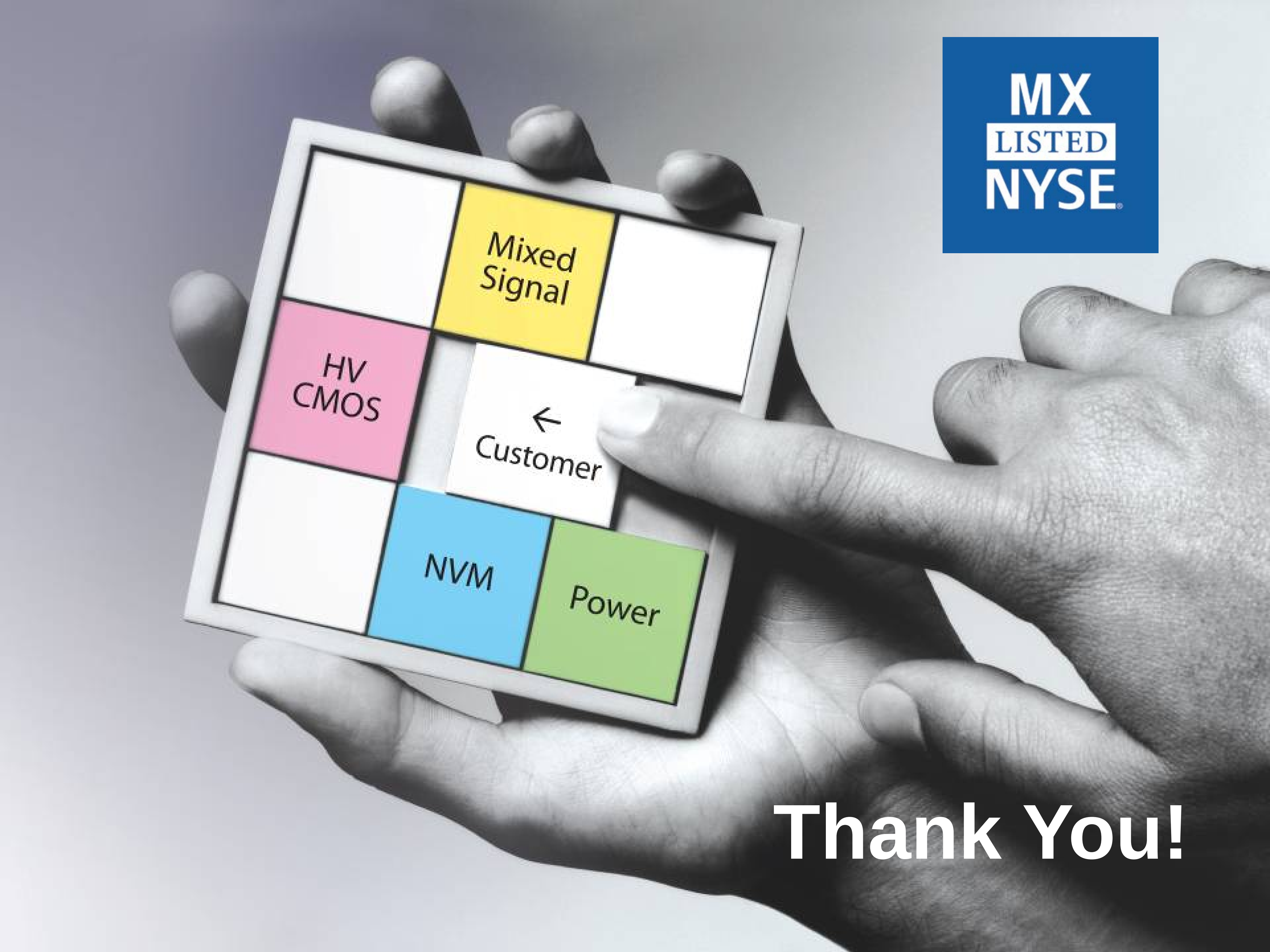
- **Excellent prior PowerSoC Workshop presentations**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Thank You!