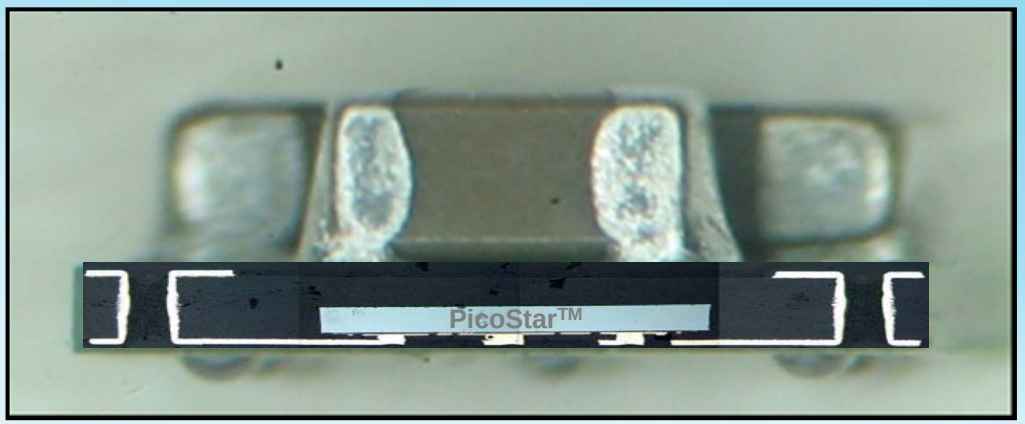
MicroSiP™ DC/DC Converters
Fully Integrated Power Solutions



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Thies Puchert, Udo Ottl,
Frank Stepniak, Florian Feckl

Outline

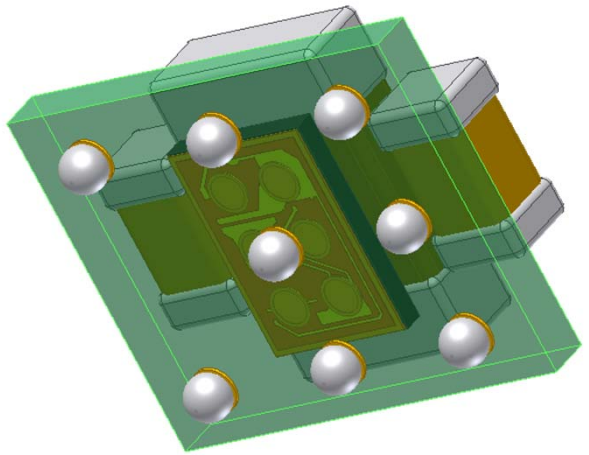
Illustrate TI's recent developments in the MicroSiP™ packaging technology

- **Overview**
- **Evolutions in the Subminiature SMPS Space**
- **MicroSiP™ Package Fabrication Flow**
- **Electrical Performance Aspect**
- **Conclusion**

MicroSiP™: Overview

✓ Tiniest Solution Size

- Passives integration (C_{IN}, C_{OUT}, L)
- Substrate featuring embedded silicon
- Small substrate layout

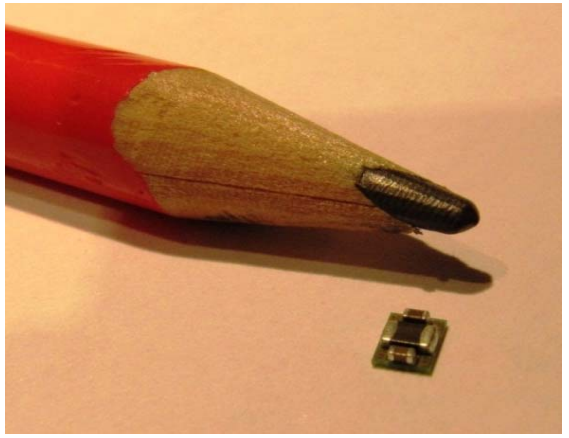


✓ Ease of Use

- Real pick-and-place solution
- No external passive components required
- One-Stop-Shop, reduces HW design and layout efforts

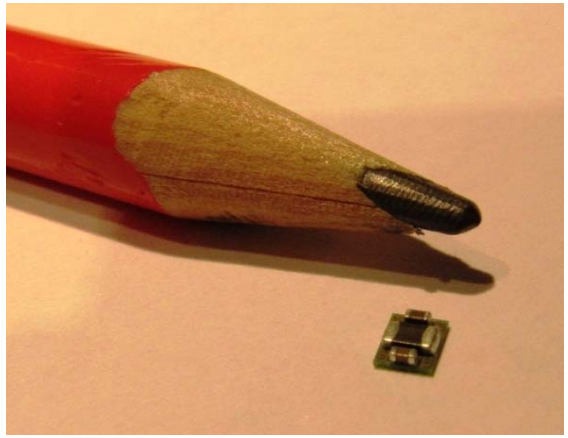
✓ Performance

- Passive components to match converter
- Performance optimized layout



2.5W Fully Integrated Power Converter
2.5V to 5.5V_{IN}

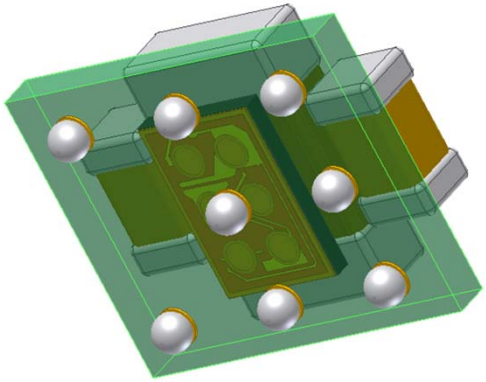
MicroSiP™: When Solution Size Matters



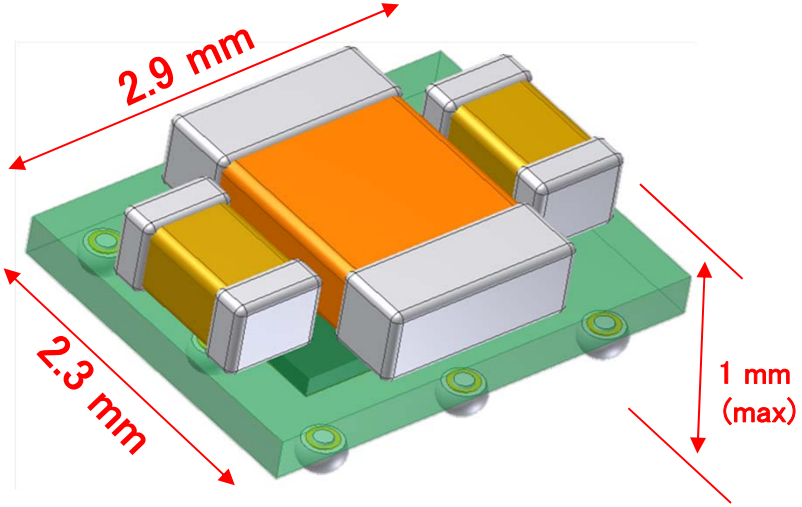
Solution size: >45% smaller vs. discrete solution

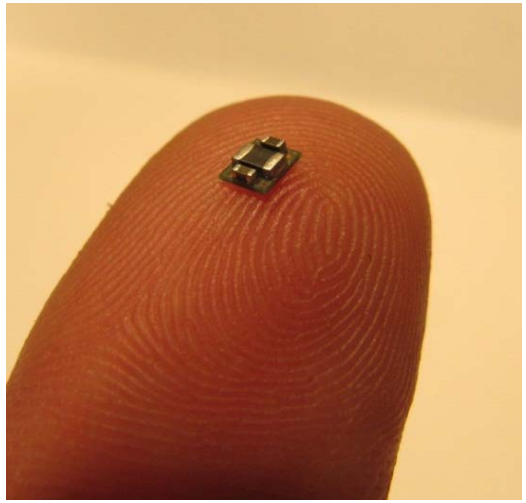
Profile: <1mm height

Power density: ca. 6500W/inch^3



OSP Plated LGA
80µm Solder Bumps

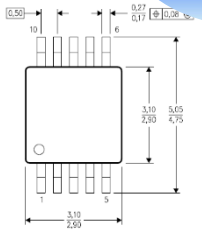


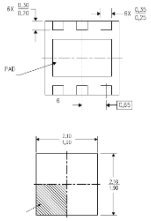


Miniature Power Solutions Evolution

L = 10µH
f_{SW} = 750kHz
MSOP

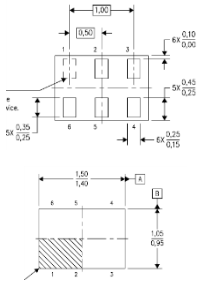
TPS6200x
170mm²
4mA/mm²





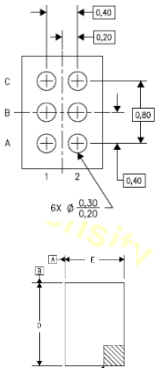
TPS6226x
21.5mm²
28mA/mm²

L = 2.2µH
f_{SW} = 2.2MHz
2x2 SON



TPS6223x
12mm²
42mA/mm²

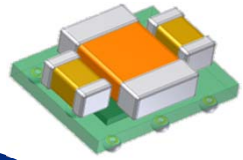
L = 1.0 to 2.2µH
f_{SW} = 3MHz
1x1.5 SON



TPS6262x
12mm²
50mA/mm²

L = 0.47µH
f_{SW} = 6MHz
1.3x0.95 WCSP

2700W/inch³



TPS8267x
6.7mm²
90mA/mm²

L = 1µH (gradual sat.)
f_{SW} = 5.5MHz
2.3x2.9 SIP

6500W/inch³

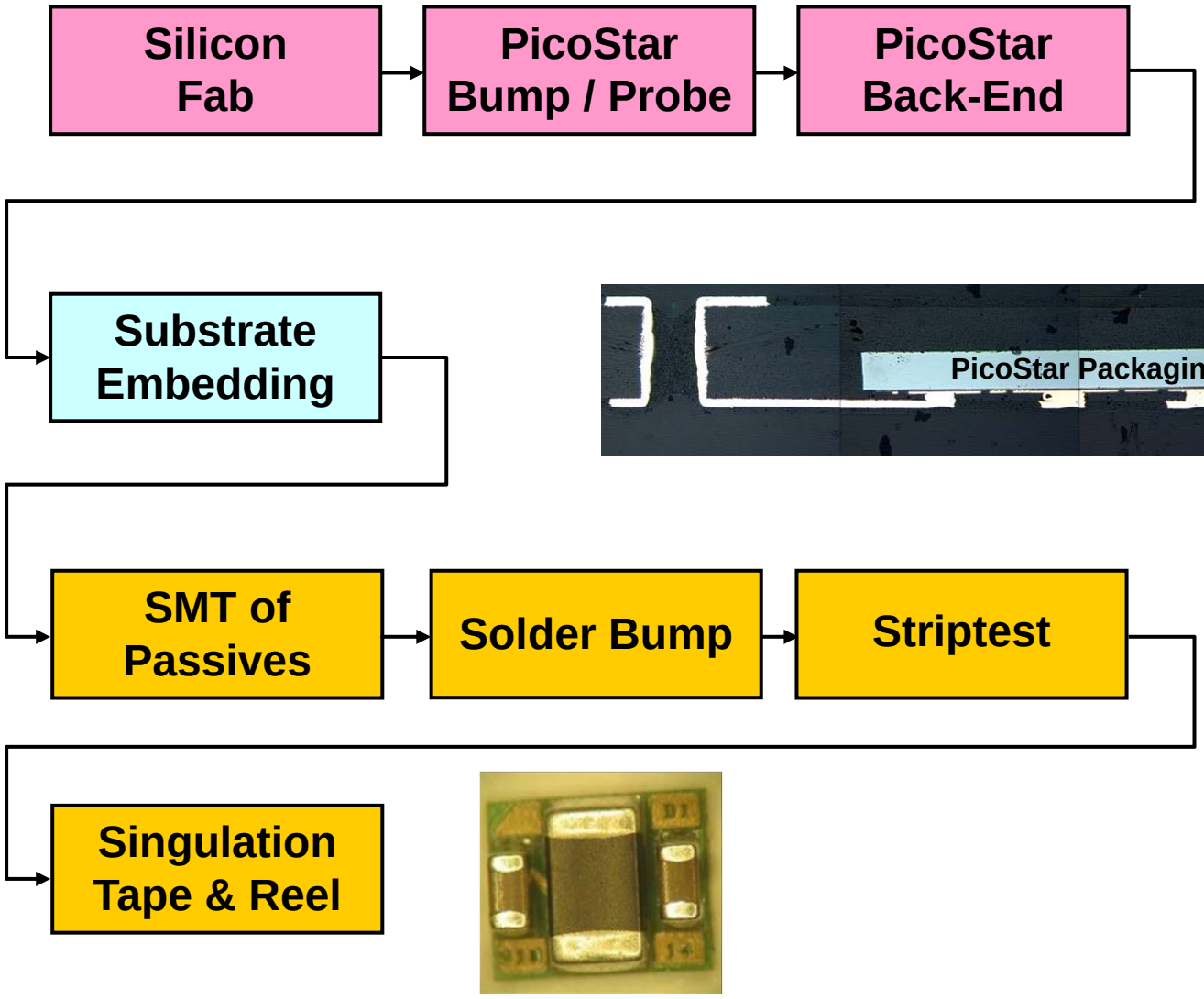
TPS8268x
6.7mm²
230mA/mm²

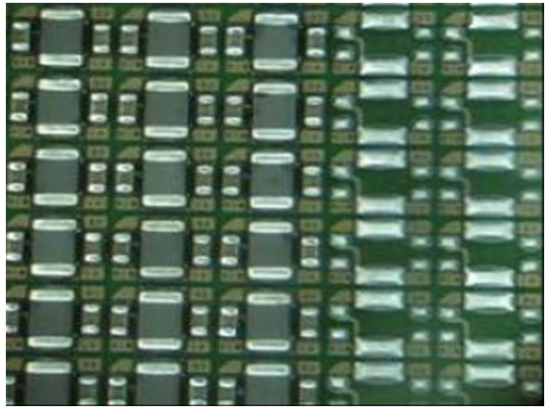
L = 0.47µH
f_{SW} = 5.5MHz
2.3x2.9 SIP

Note: Output power level in the range of 1 to 2W

2000 ——— **2014**

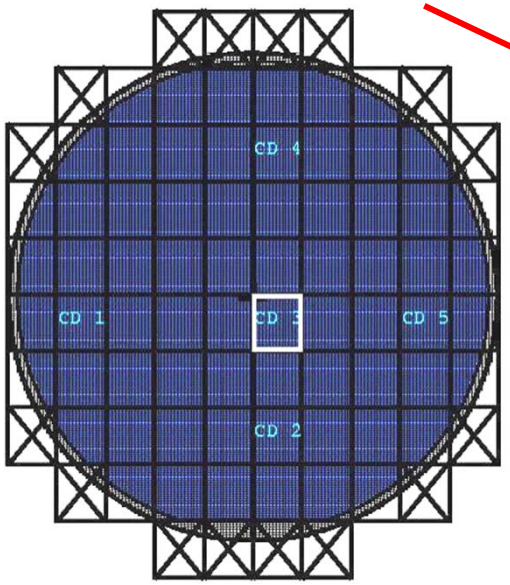
MicroSiP™: Production Flow



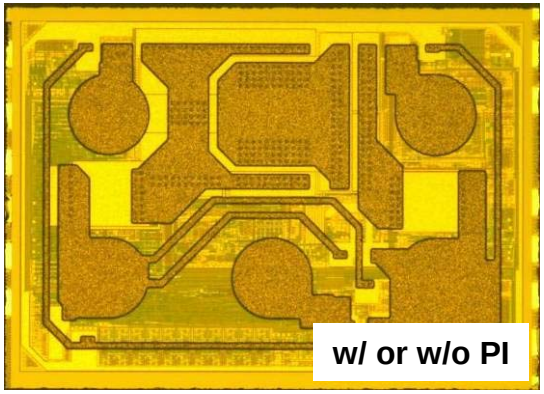


MicroSiP™: Assembly Flow

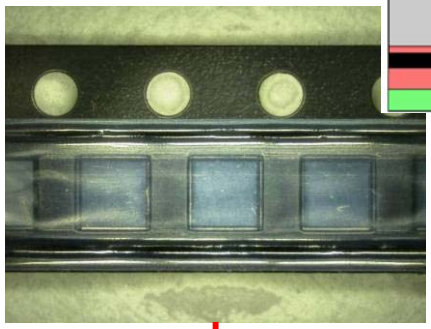
Wafer Fab

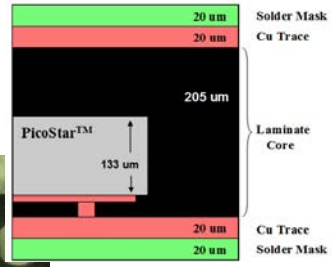


Thick Cu Process

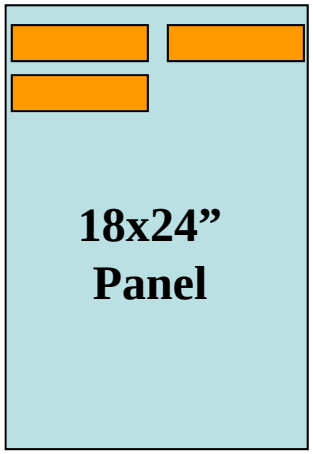


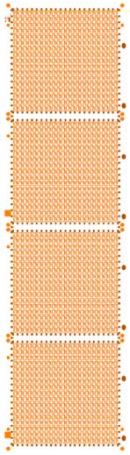
Grind/Saw/T&R



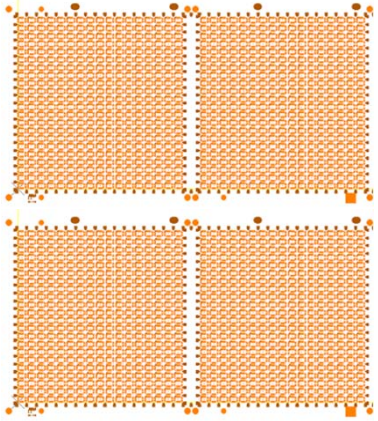


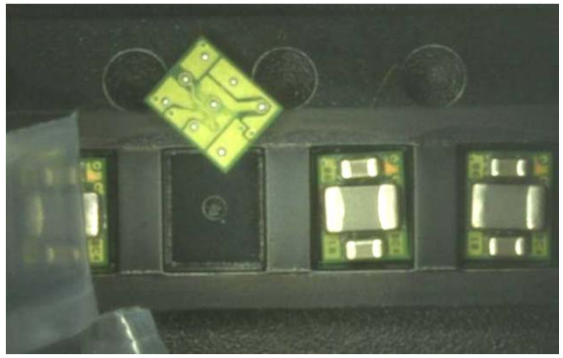
Substrate Embedding





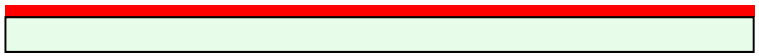
Subarray SMT/Singulate/Test/T&R



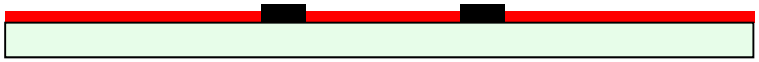


MicroSiP™: Embedding Process

Thin Copper film
adhered to carrier layer

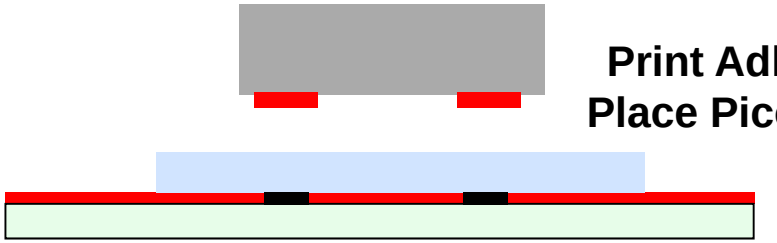


Pattern Cu film

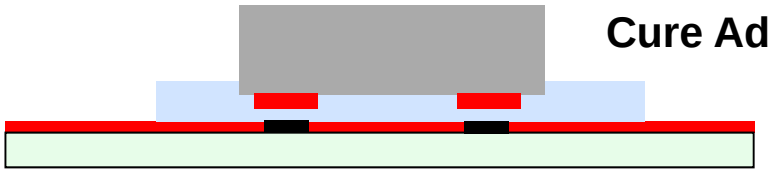


PicoStar™ Attach

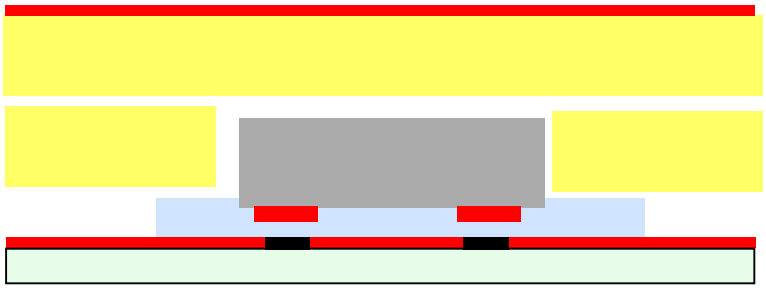
Print Adhesive
Place PicoStar™



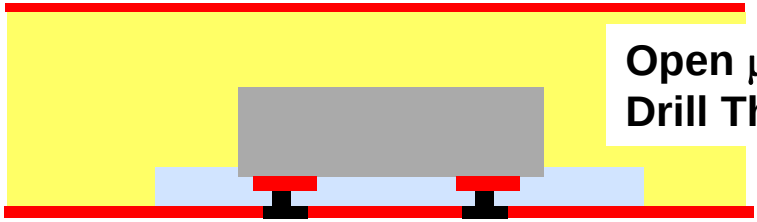
Cure Adhesive



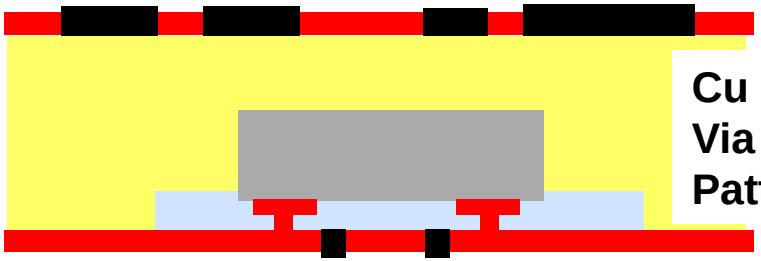
Pattern Core Pre-preg, Apply Pre-Preg
Laminate Top Metal Layer, Press/Cure



Open μvias (laser)
Drill Thru-Holes

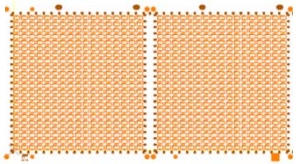


Cu Plating
Via Fill
Pattern/Etching



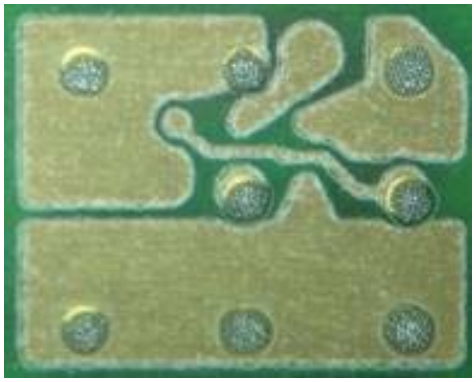
MicroSiP™: SMT Assembly

Sub array

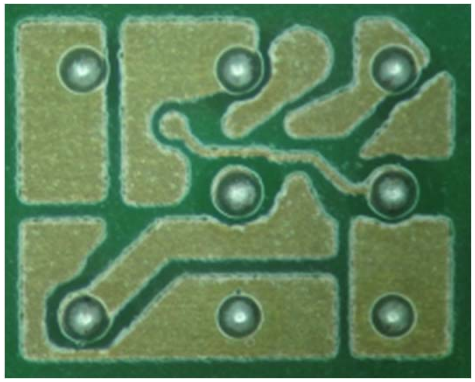


Backside

Solder Print



Reflow

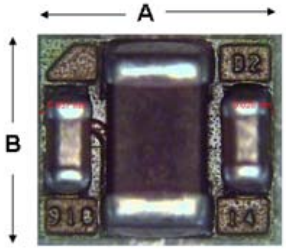


Frontside

Solder Print

Pick ‘n Place

Reflow



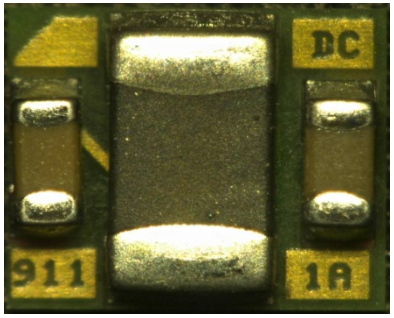
	A	B	H	H1
Average	2.89	2.29	0.91	0.077
Min	2.87	2.27	0.88	0.063
Max	2.90	2.30	2.90	2.30

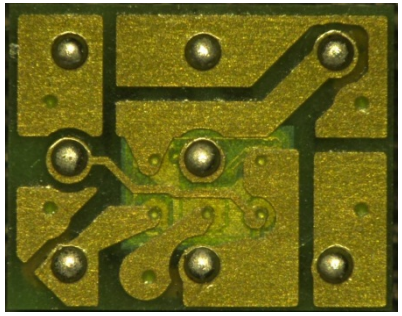
TPS8267x

5.5MHz, 600mA Fully Integrated Step-Down DC/DC

Features

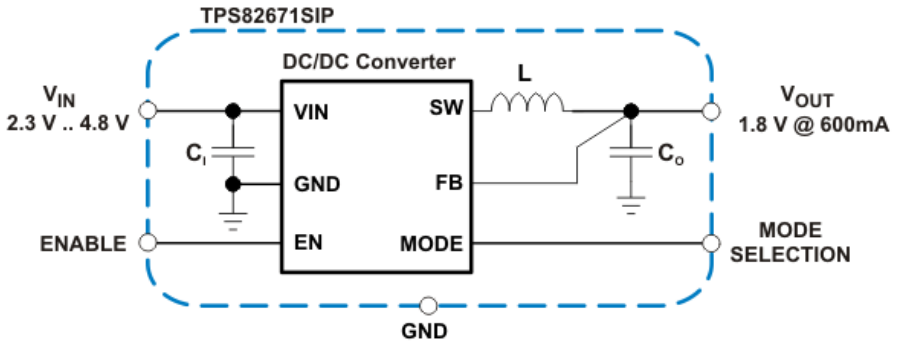
- **Input voltage:** 2.3V to 4.8V
- **Output current:** 600mA
- **Total solution size:** <7 mm^2
- **Fixed output voltage:** 1.0V to 1.9V
  - +/-2% DC accuracy in PWM
- **Over 90% efficiency at 5.5MHz Operation**
- **PWM switching frequency dithering**
- **Quiescent current:** 17 µA
- **Power Save Mode:**
  - Auto PFM/PWM transition
  - PIN selectable: Auto mode / Forced PWM
- **LGA package (2.3x2.9mm, 1mm height)**





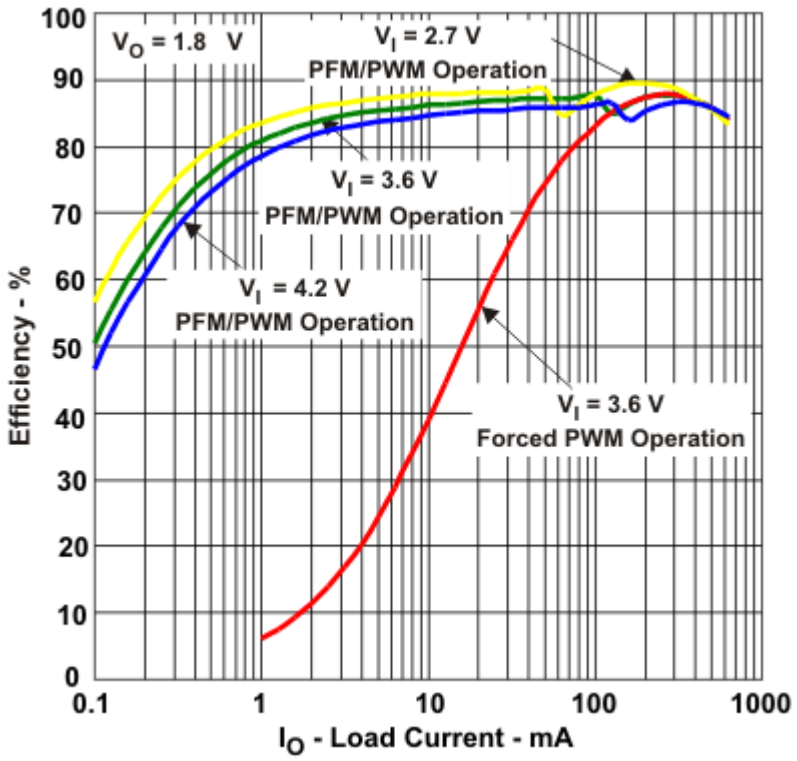
Benefits

- **High switching frequency enables active and passive components integration (PMIC optimum fit).**
- **PMIC embedded substrate (3D assembly):**
  < 7mm^2 total solution size, sub 1mm solution height
- **PWM frequency dithering for improved RF spurious performance. Radiated noise reduction.**
- **Mode pin for** highest efficiency or regulated frequency selection.
- **Easy system level integration:**
  reduces HW design workload, no more questionable layout.



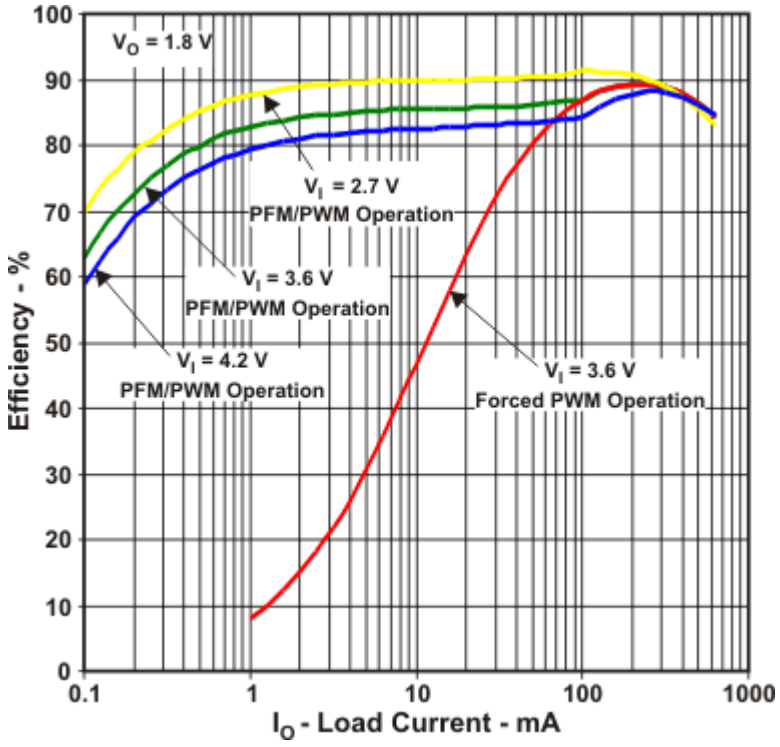
Fully Integrated Step-Down DC/DC
Benchmarking Integrated vs. Discrete Solution

DISCRETE SOLUTION



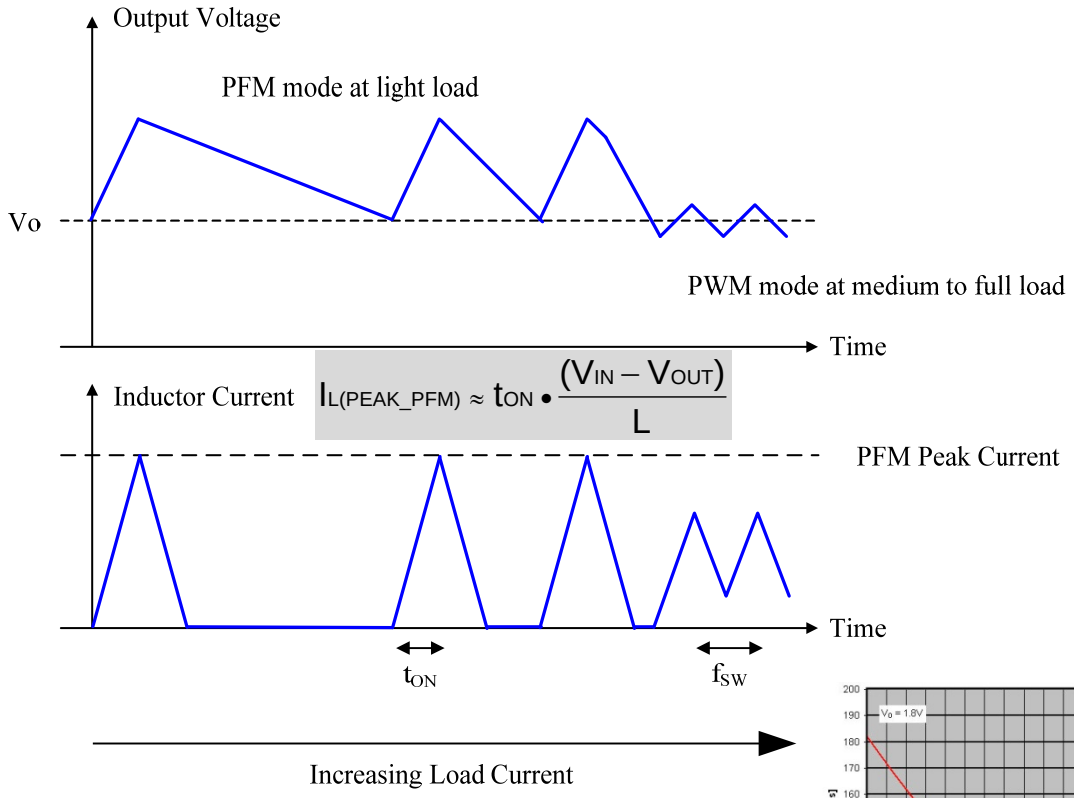
TPS62621

µDC/DC Solution

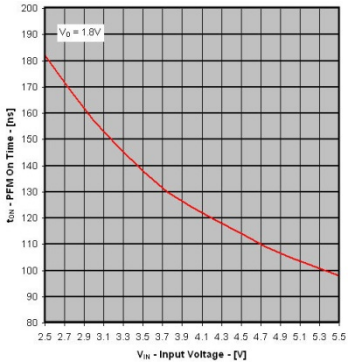


TPS82671SIP µDC/DC Converter

Efficiency Optimization
Time Controlled PFM Mode Architecture

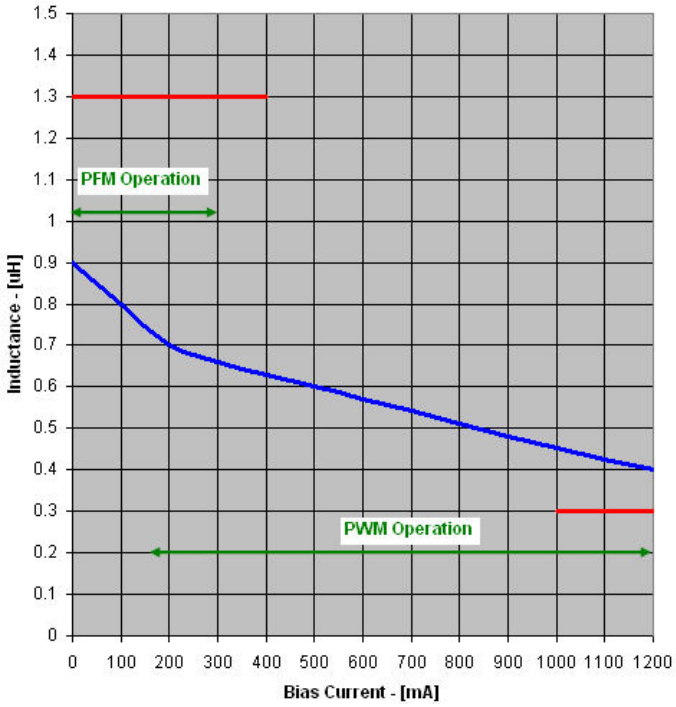


On-Time Controlled PFM Scheme

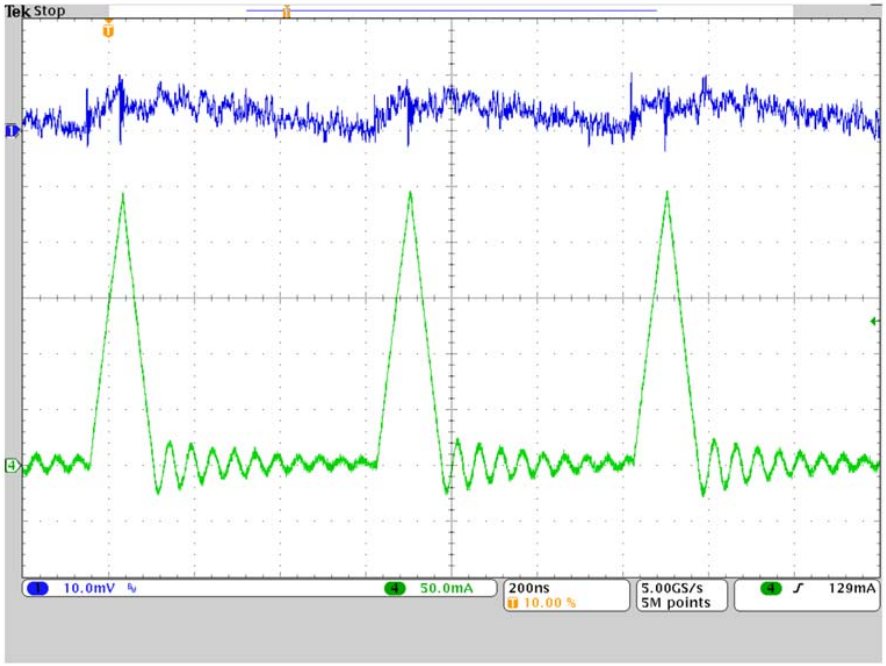


State-of-the art multilayer technology offers structures to realize non-linear inductances.

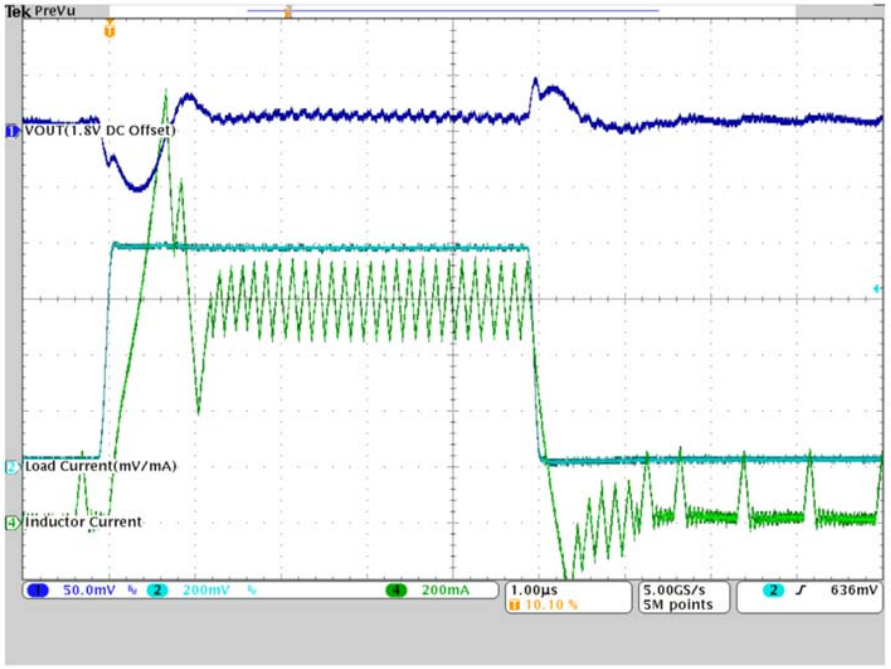
Gradual saturation inductor can help to maximize efficiency. Better tradeoff between Power FETs geometry and converter's transient response.



Fully Integrated Step-Down DC/DC
AC Regulation Performance



V_{IN} = 3.6V, V_{OUT} = 1.8V
PFM Mode Operation, I_{OUT} = 300mA



V_{IN} = 3.6V, V_{OUT} = 1.8V
Load Transient 20mA to 800mA
t_{rise}, f_{fall} ~ 100ns

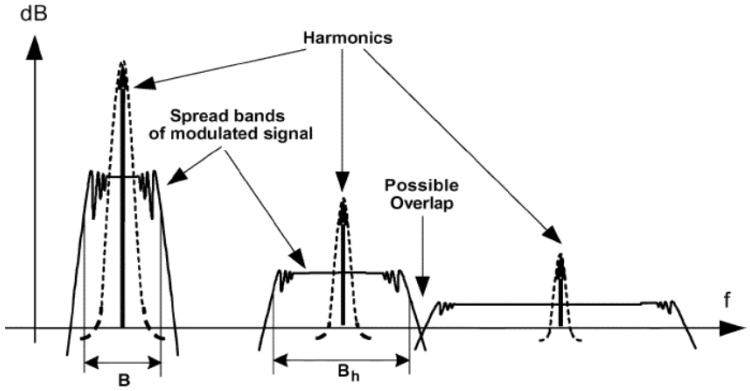
High Frequency DC/DC Conversion
Spread Spectrum Frequency Modulation (SSFM)

The spread spectrum architecture randomly varies the switching frequency by +/-5% to +/-20% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies.

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude.

- ☞ Easier to comply with EMI standards.
- ☞ Less filtering effort in RF apps, smaller solution size.

Spread bands of harmonics in modulated square signals



$$B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m)$$

$$B_h = 2 \cdot f_m \cdot (1 + m_f.h)$$

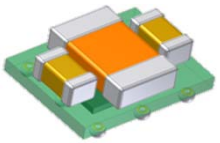
Modulation index is defined as: $m_f = \dfrac{\delta \cdot f_c}{f_m}$

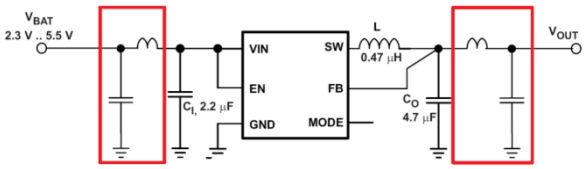
- f_c is the carrier frequency
- f_m the modulating frequency

- δ is the modulation ratio, $\delta = \dfrac{\Delta f_c}{f_c}$

TPS8267xSIP

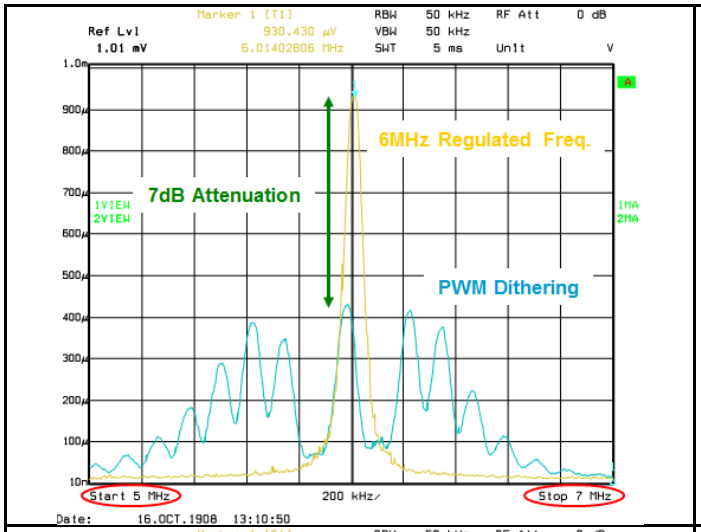
PWM Operation – Conducted Output Noise Measurement

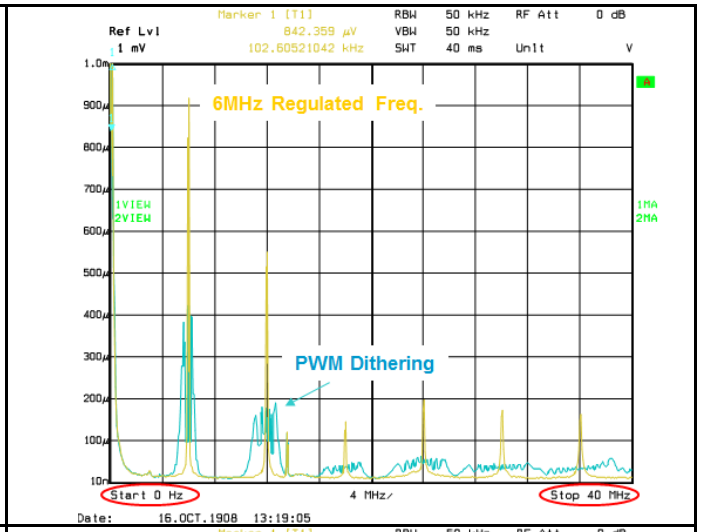


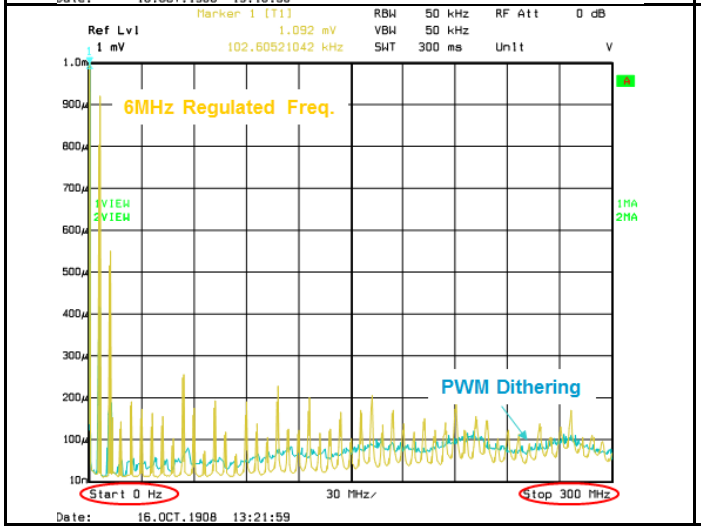


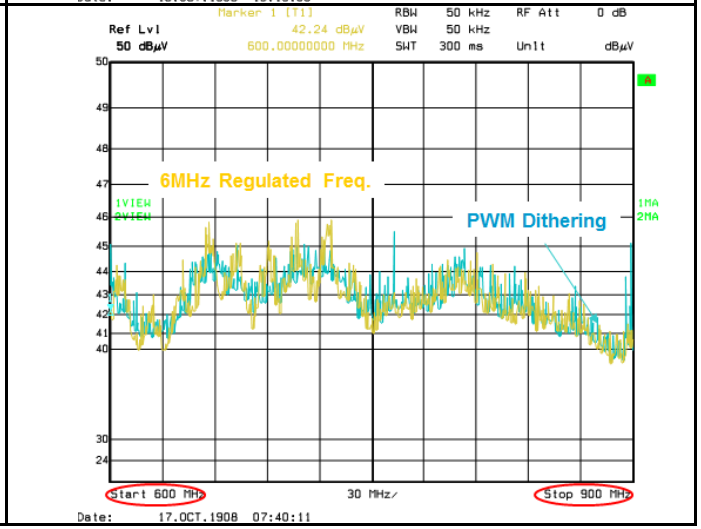
$3.6V_{IN}$, $1.2V_{OUT}$ @ I_{OUT} = 100mA

No EMI filters





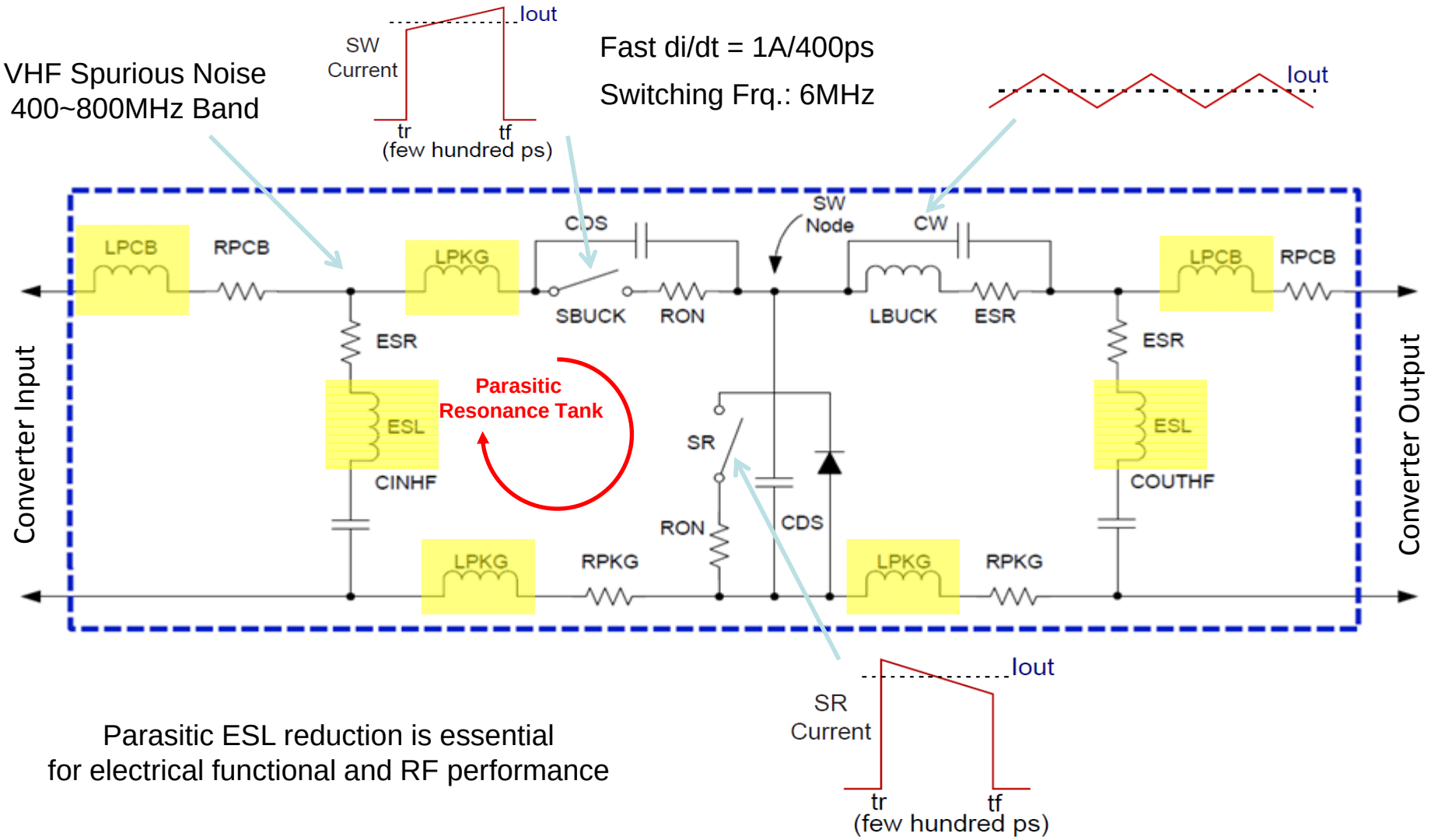




FREQUENCY DITHERING PARAMETERS

1- Δfc = c.a. 500kHz, fc = 6MHz, δ = 8.5%
2- f_m = 120kHz, m_f = 4.2
3- Triangular modulation

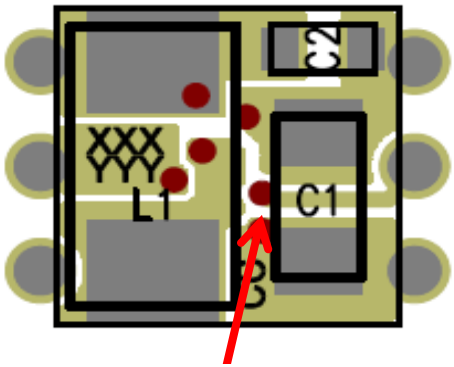
MicroSiP™: Better Co-Design Options to Reduce Parasitic



Parasitic ESL reduction is essential
for electrical functional and RF performance

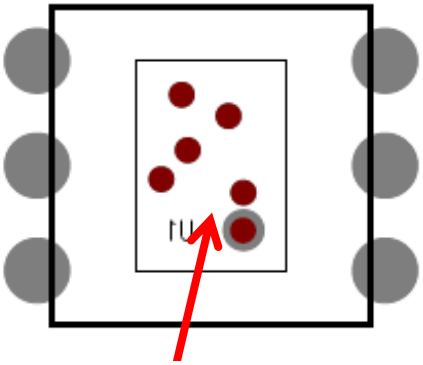
MicroSiP™: Improving Electrical, Thermal Performance

Top
2 x 2mm



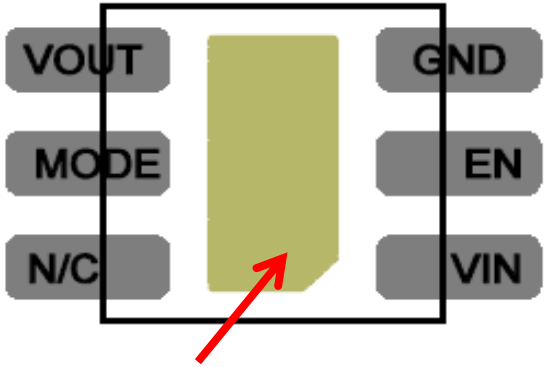
Min. Distance C_i-to-IC

Embedded



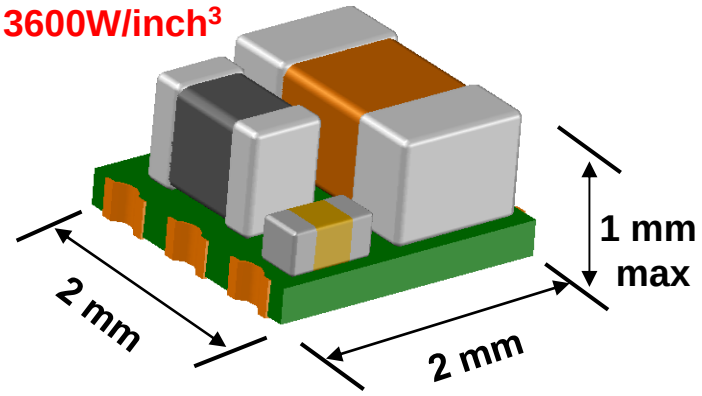
PicoStar Face-Up

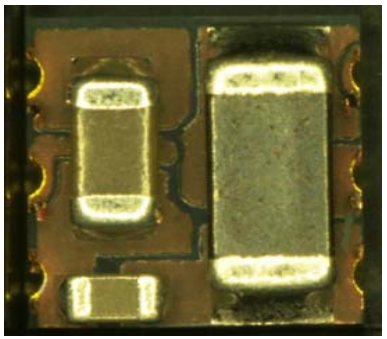
Bottom

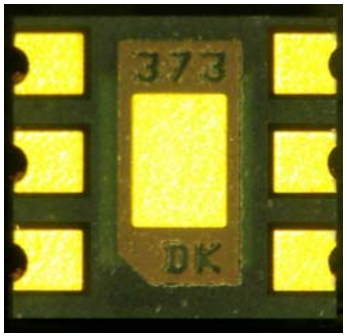


SON-like Thermal Pad
Enhanced θ_{JB}

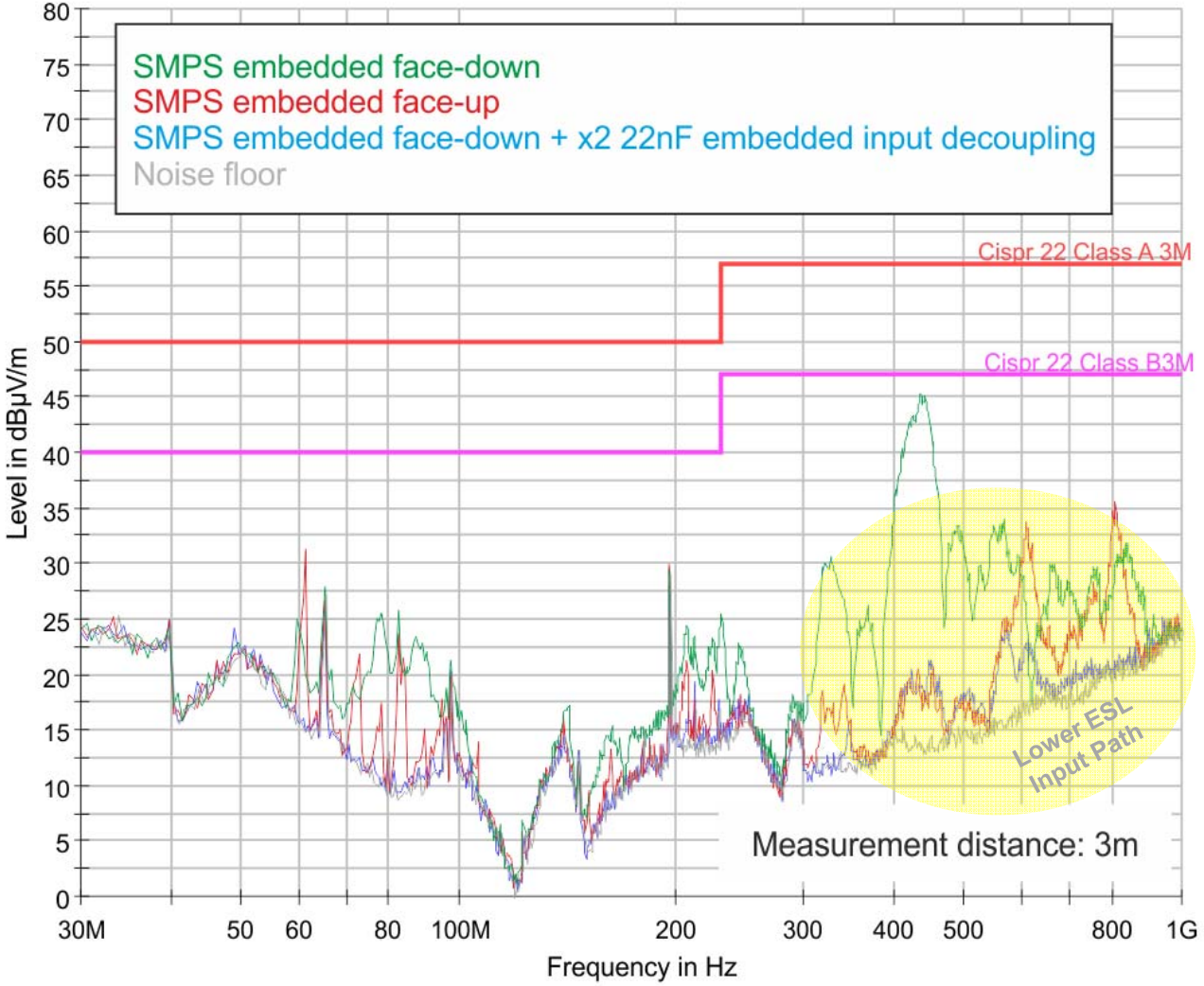
3600W/inch³

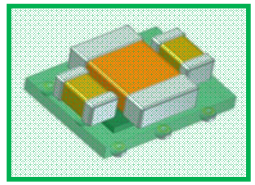


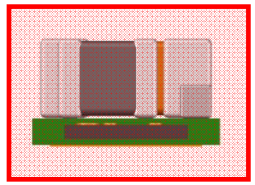


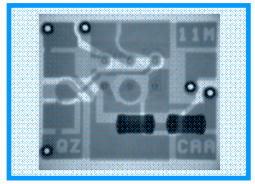


MicroSiP™: Radiated EMI Spectrum









$3.6V_{IN}$
$1.8V_{OUT}$ @ I_{OUT} = 550mA

No EMI filters
SSFM enabled

MicroSiP™ DC/DC Converters

1. Smallest solution size: Innovative 3D integration
2. Every SiP is a custom design: Certain rationales need to be met
3. Early-phase co-design from the inside out (IC, passives, substrate)
4. Optimize electrical performance: Comparable efficiency, lower EMI
5. What helps electrically tends to benefit the SiP thermal management