High Frequency Switching Regulators for High Current Slew Rate Applications

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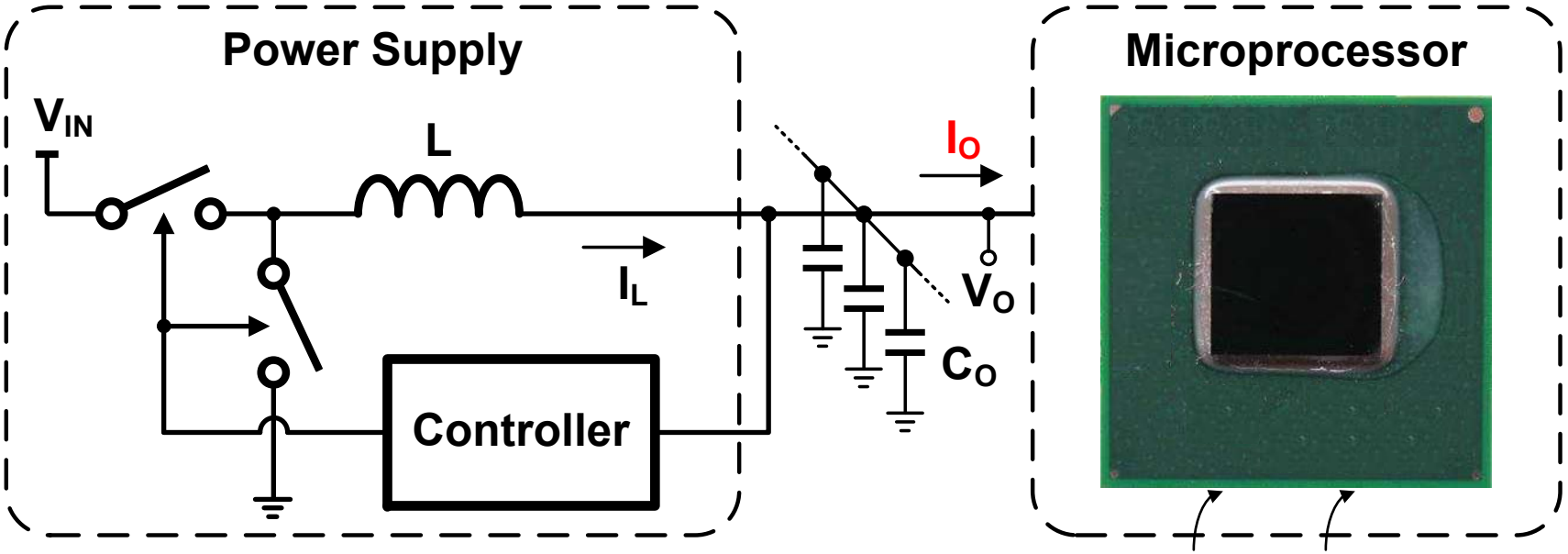
Outline

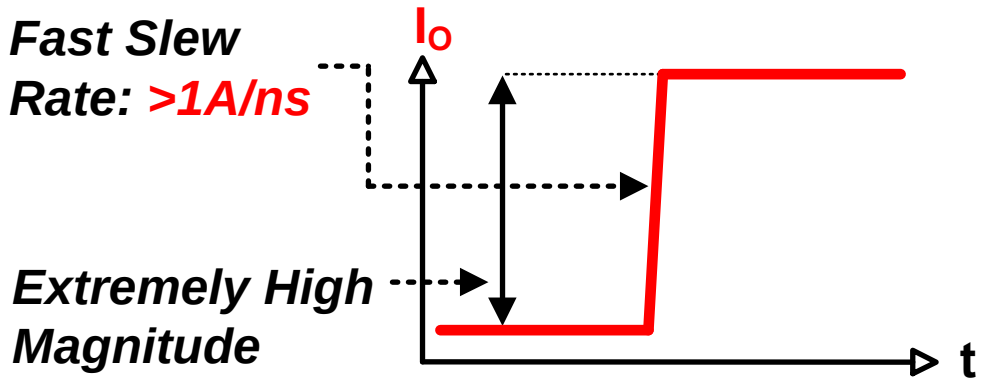
- Background and Challenges
- Integrated Design Solution
  - Near Zero Delay Response
  - f_{SW} Synchronization
  - Adaptive Voltage Tracking
  - High-Speed Current Sensing
- Design Examples
- Conclusions

Microprocessor Power Supply Trends

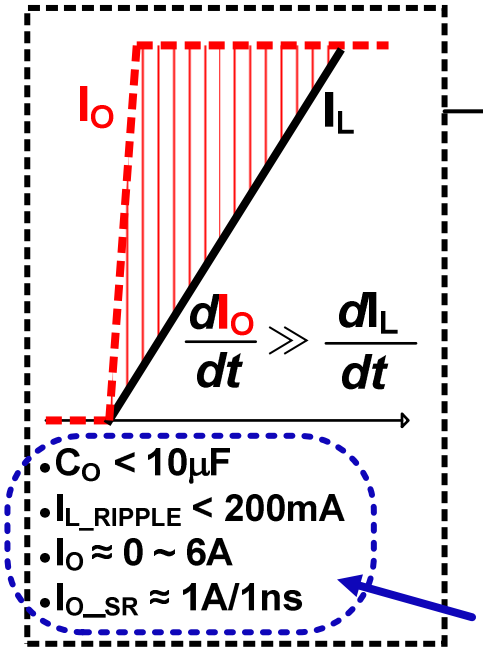


Recent Trends:

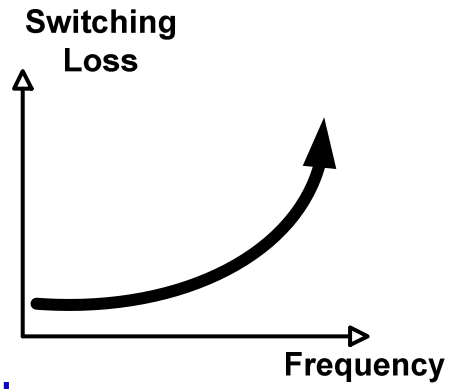
- Increasing clock frequency.
- Greater number of cores.
- Increasing power dissipation.

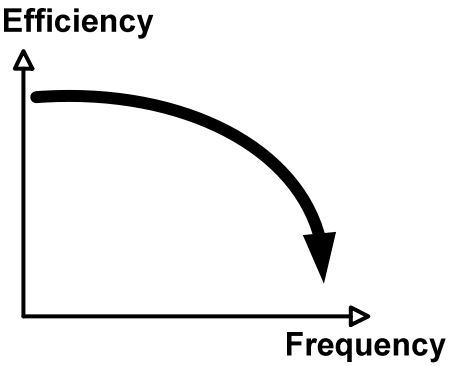


Key Design Consideration: f_{SW}



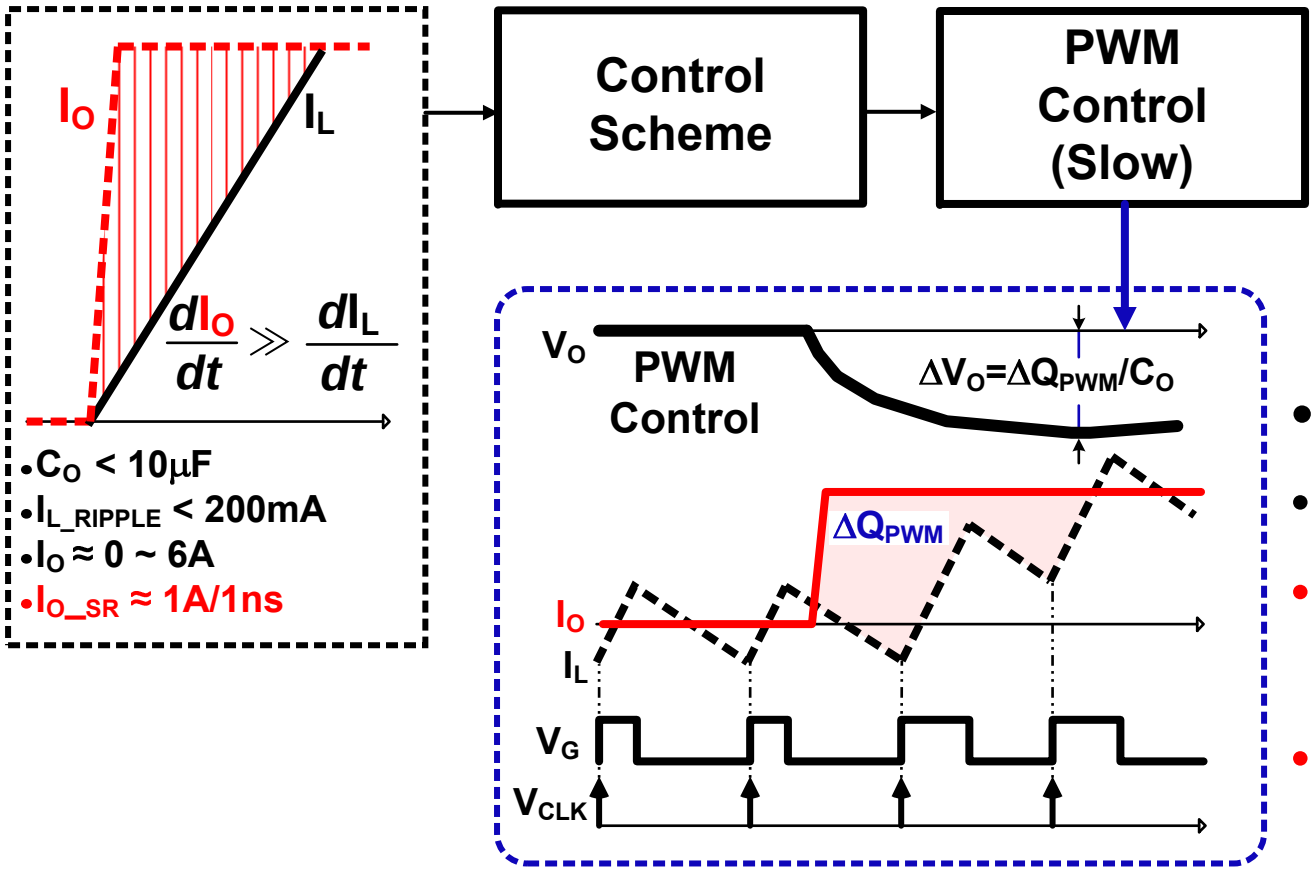
Trends of Advanced μProcessors in Mobile Applications





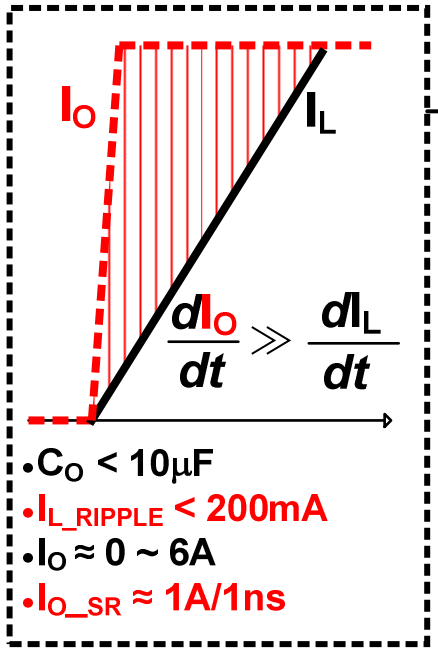
- f_{SW} Increase
  - To satisfy the Trends: f_{SW} ≈ 0.5~1GHz*
  - Dramatic switching power loss increase.
  - Significant efficiency drop.

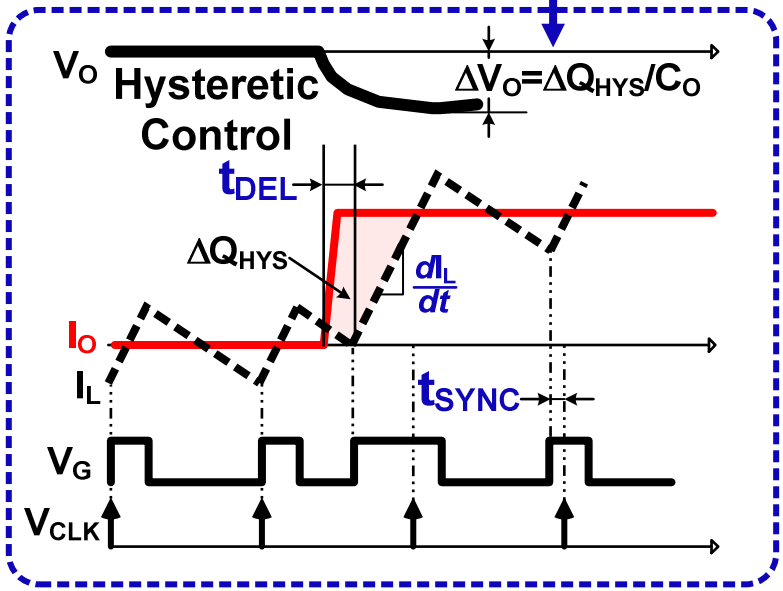
Key Design Consideration: Control Scheme



- **PWM Control**
- **Fixed f_{SW}.**
- **Slow feedback loop –ΔQ_{PWM}**
- **Larger V_O droop.**

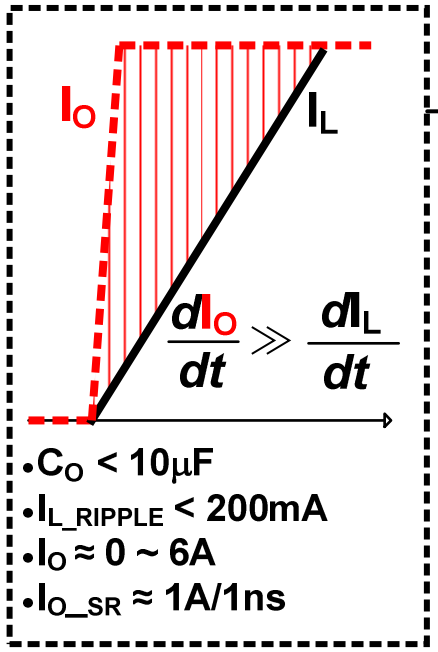
Key Design Consideration: Control Scheme

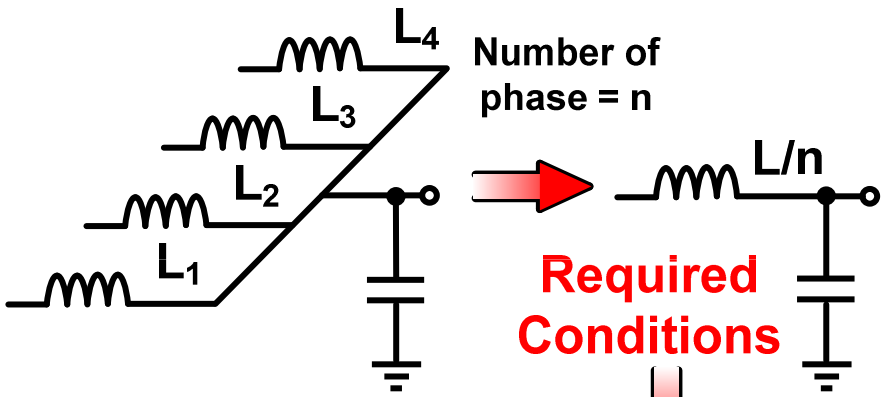


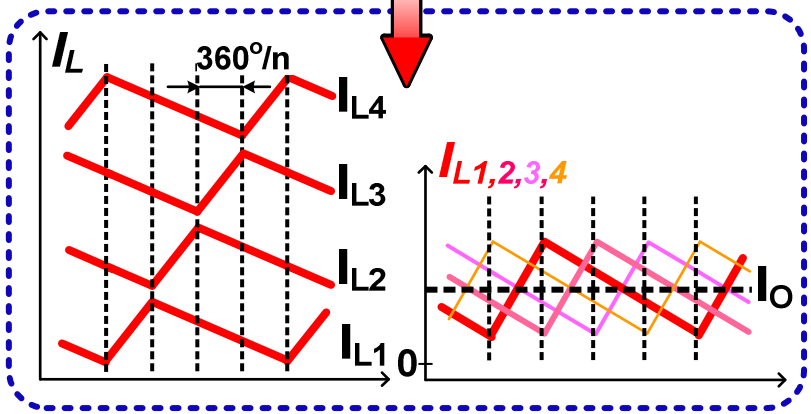


- **Hysteretic Control**
- **Fast response.**
- **Still, hysteresis delay. – t_{DEL}**
- **Varying f_{SW}. – t_{SYNC}**
- **Physical inductor current slew rate limitation. – dI_L/dt**

Key Design Consideration: Circuit Architecture



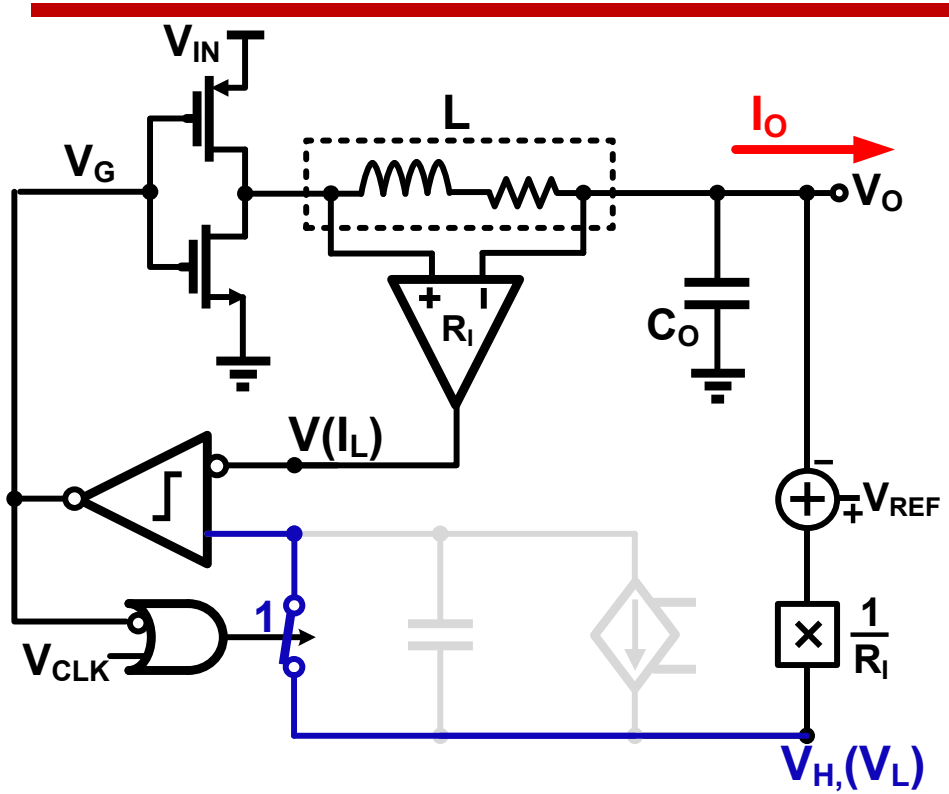


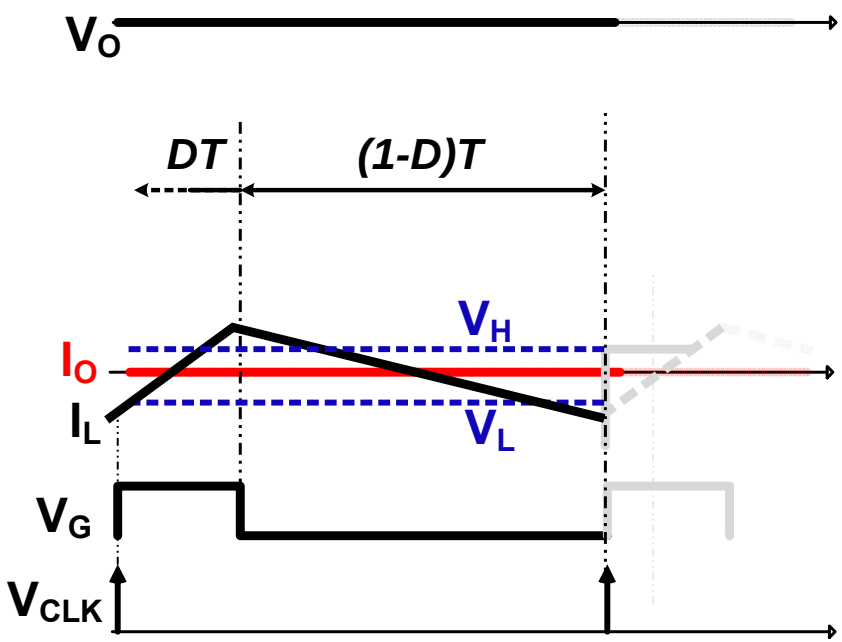


- **Challenges**
- **Synchronization, current-sharing* along with *fast hysteretic control.***
- **Circuit implementation of current sensing at VHF levels.**

* P. Li et al., "A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters," IEEE *Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3131-3145, Nov. 2009.

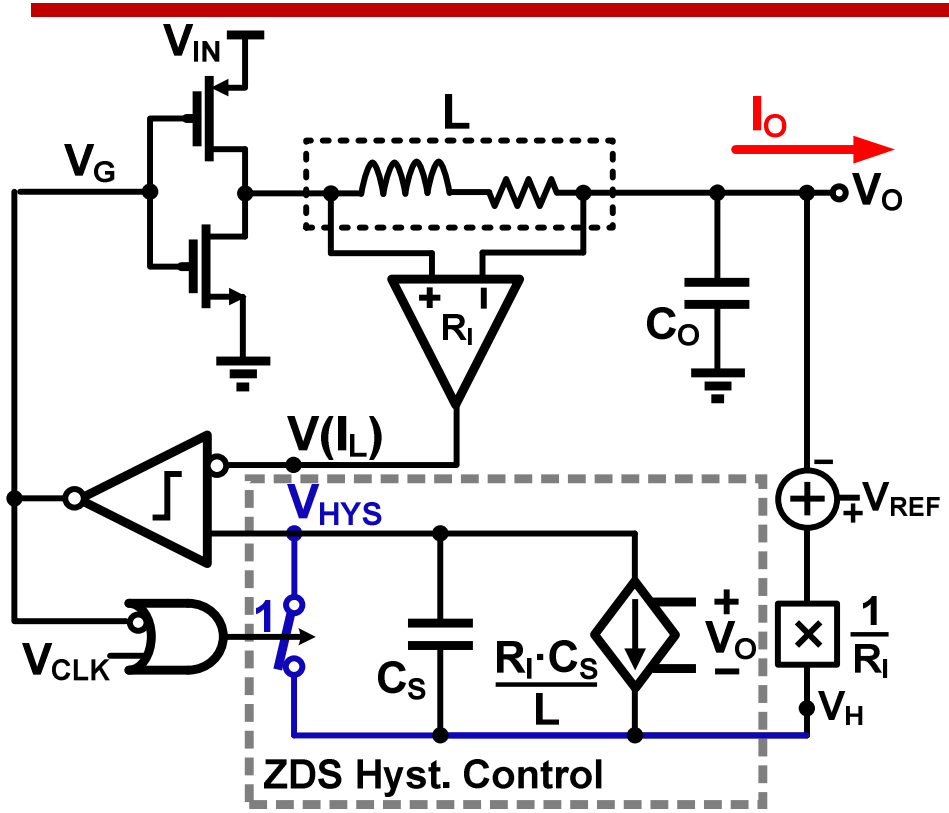
Conventional Hysteretic Control

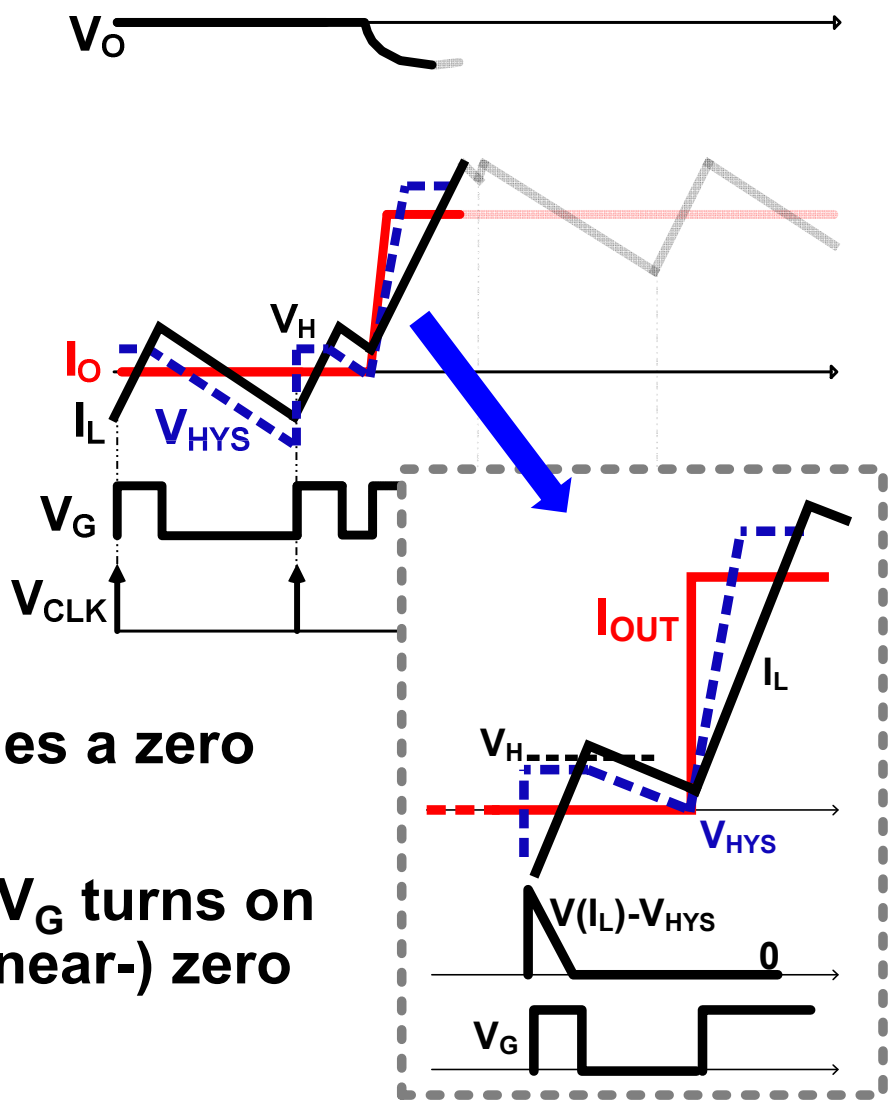




- **Fixed Hysteresis Window**
  - **Finite hysteresis window size of V_H-V_L.**
  - **Hysteresis delay $\propto$ V_H-V_L.**

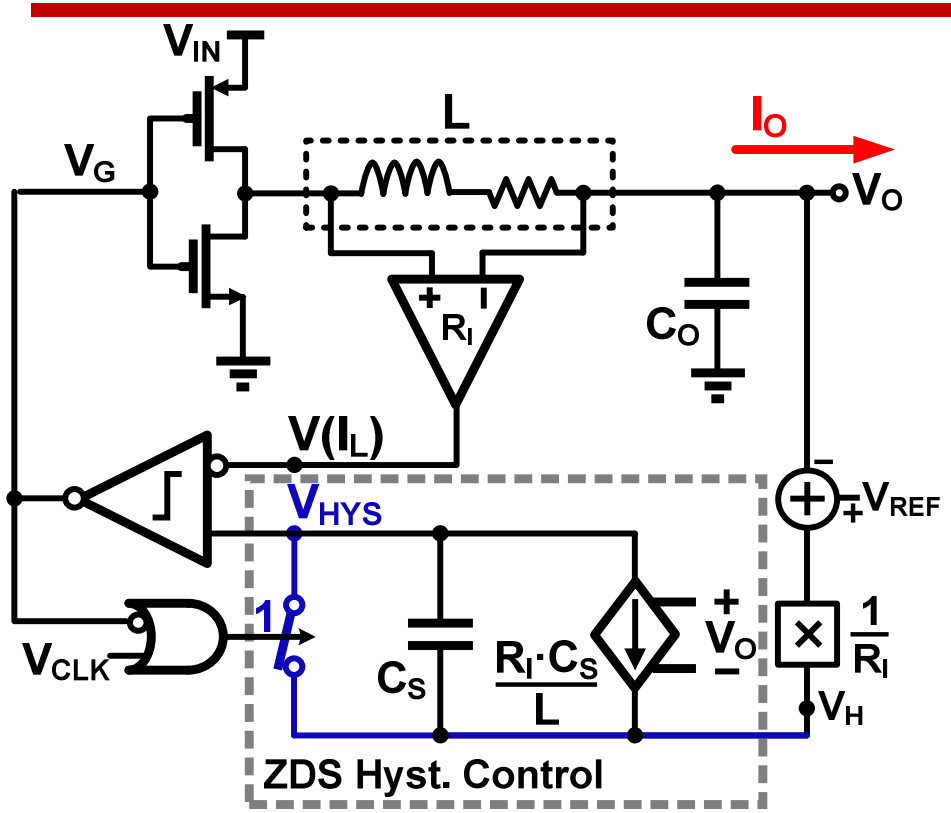
Zero Delay Response at I_O Step-Up

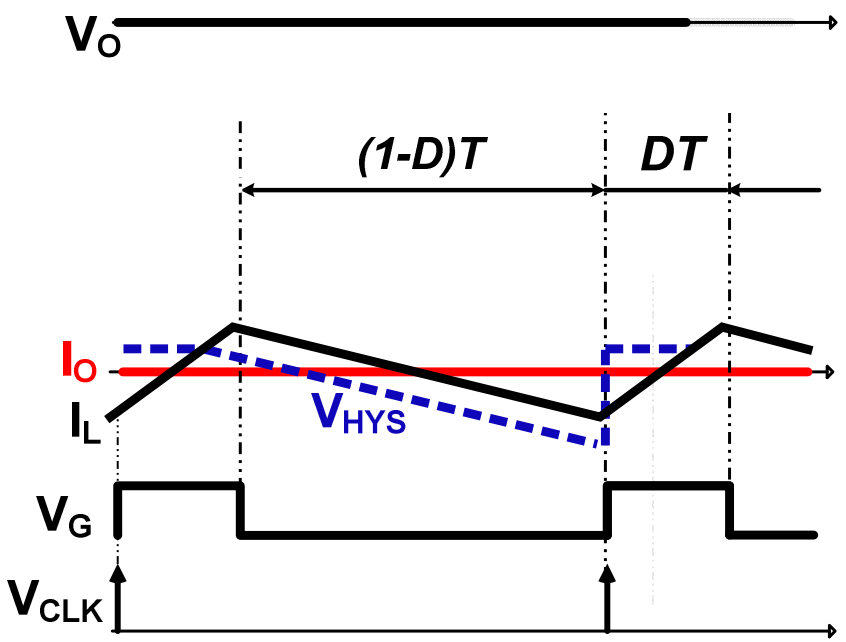




- During (1-D)T, the control provides a zero hysteresis window, $V(I_L)$-V_{HYS}=0.
- When I_O steps up during (1-D)T, V_G turns on without delay since I_L exits the (near-) zero hysteresis window instantly.

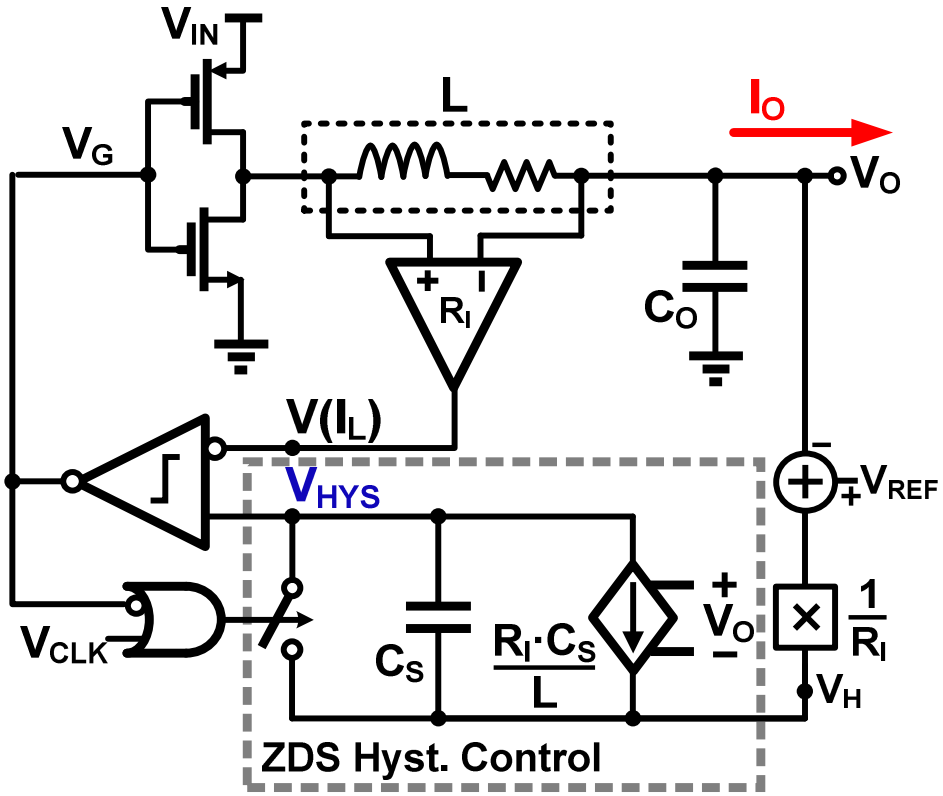
f_{SW} Synchronization

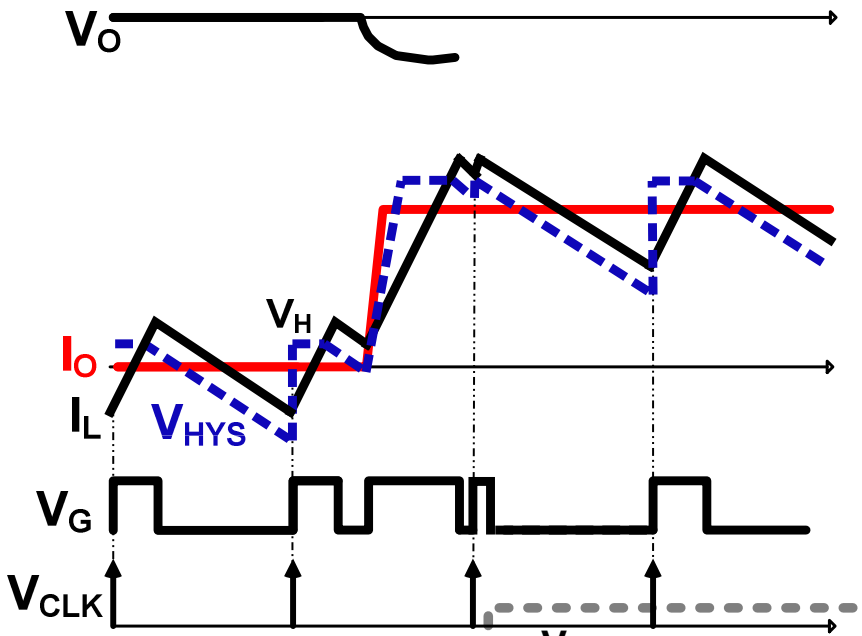


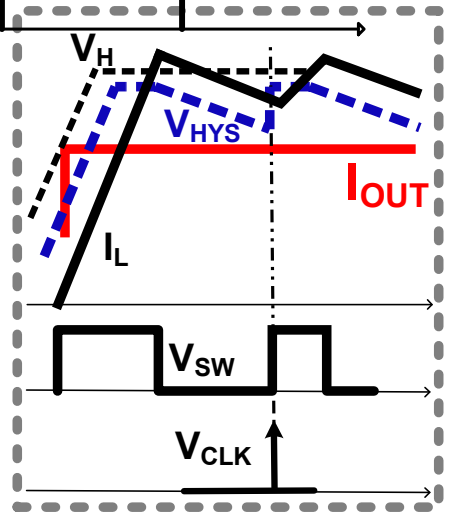


- At V_{CLK} pulse, V_{HYS} is reset to V_H.
- V_G turns on instantly when V_{HYS} hits I_L
- V_G remains on until I_L reaches to V_{HYS}.
- The leading edge of DT is synchronized to V_{CLK}.

f_{SW} Synchronization Recovery

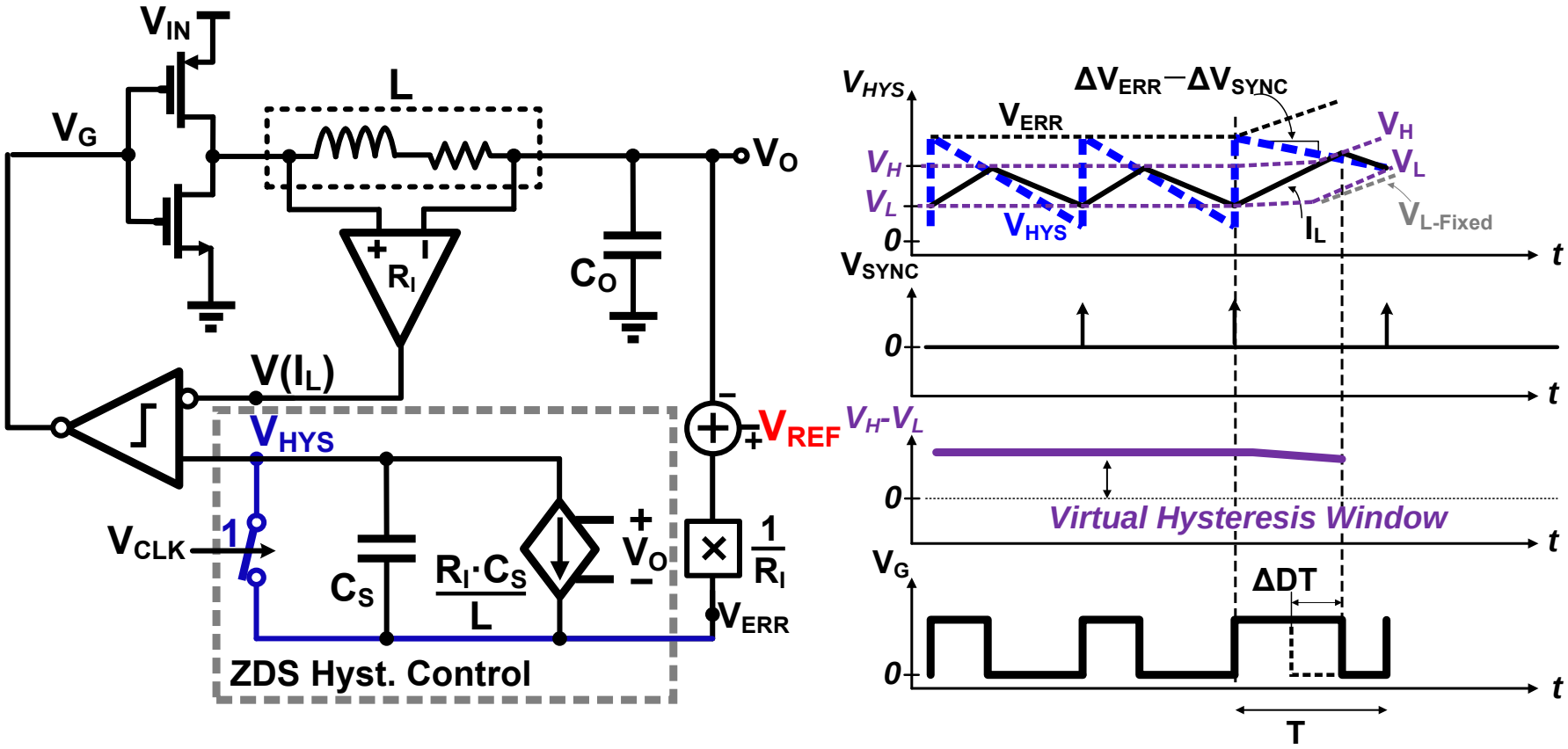






- **Synchronization Recovery Scenario**
  - **At the next V_{CLK} pulse, V_{HYS} is reset to V_H, triggering V_G on.**
  - **Leading edge of V_G is synchronized to V_{CLK}.**
  - **I_L is stabilized within a few cycles.**

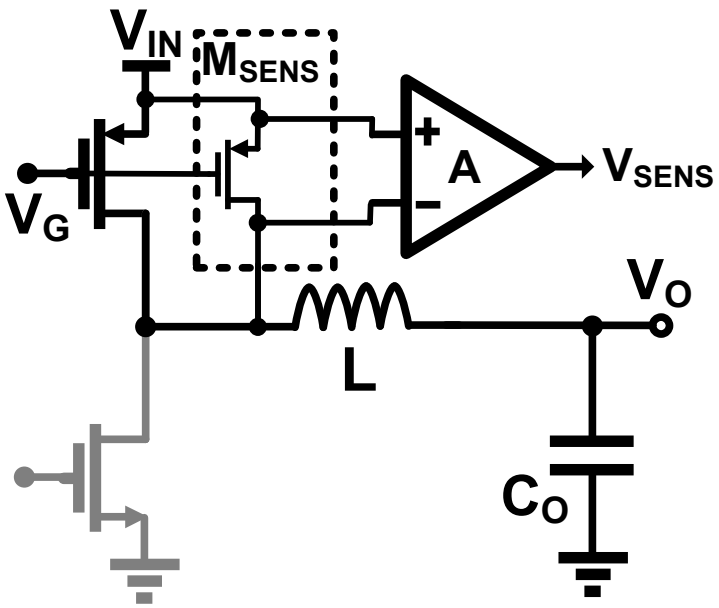
Adaptive Voltage Tracking



- As V_{REF} increases, V_{ERR} increases, causing the slope of V_{HYS} to become shallower.
- Sensed I_L takes longer to intersect V_{HYS}, causing an instantaneous duty ratio time change, ΔDT.

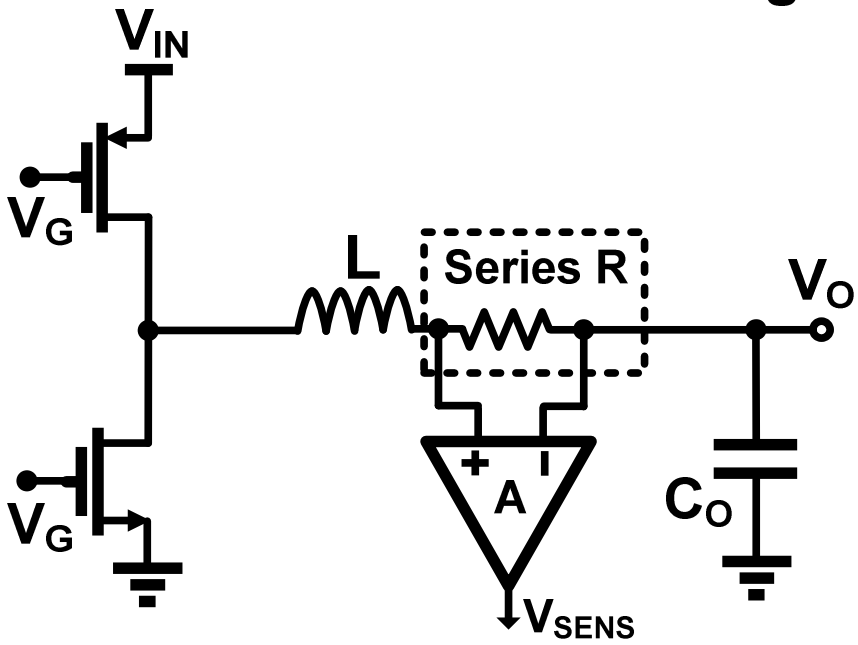
I_L-Sensing Limitations on VHF Operation

Transistor R_{DS} Sensing



- L_X-spiking.
- Discontinuous.
- Wide-bandwidth amplifier required.

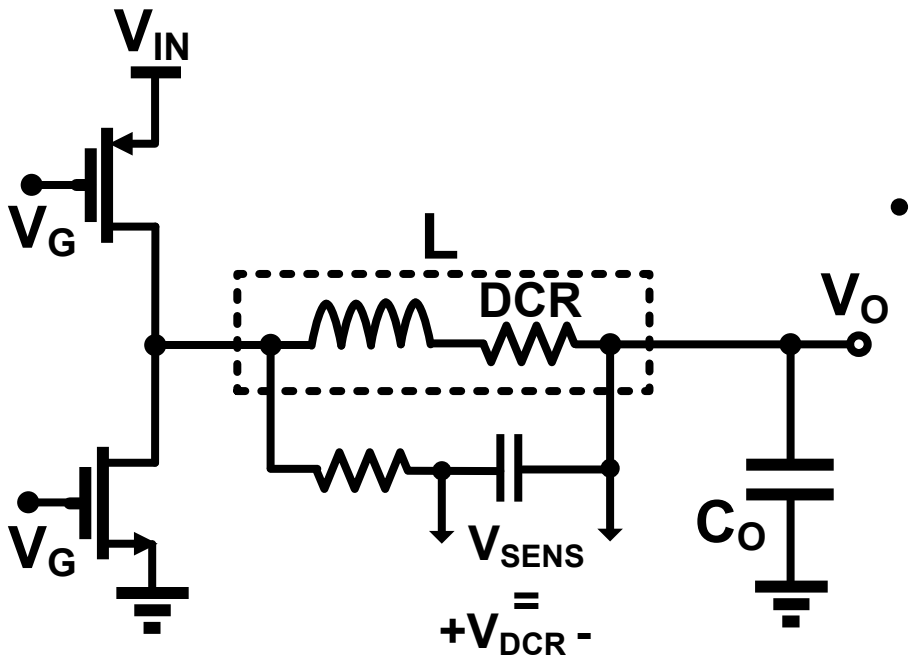
Series R_{SENS} Sensing



- Continuous.
- Power loss.
- Wide-bandwidth amplifier required.

I_L-Sensing Limitations on VHF Operation

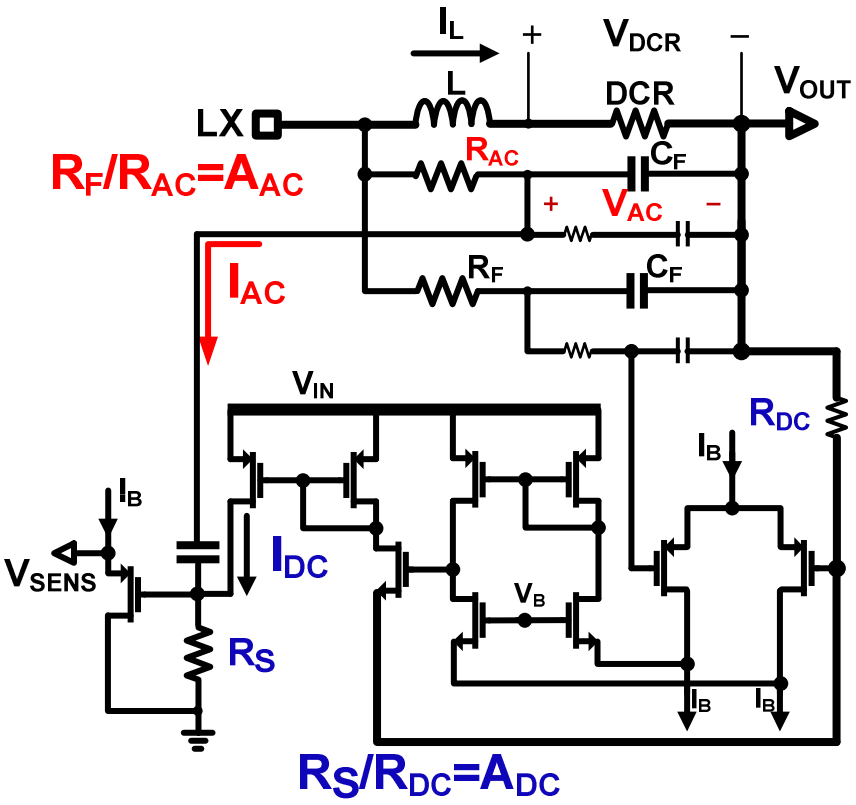
Inductor DCR Sensing

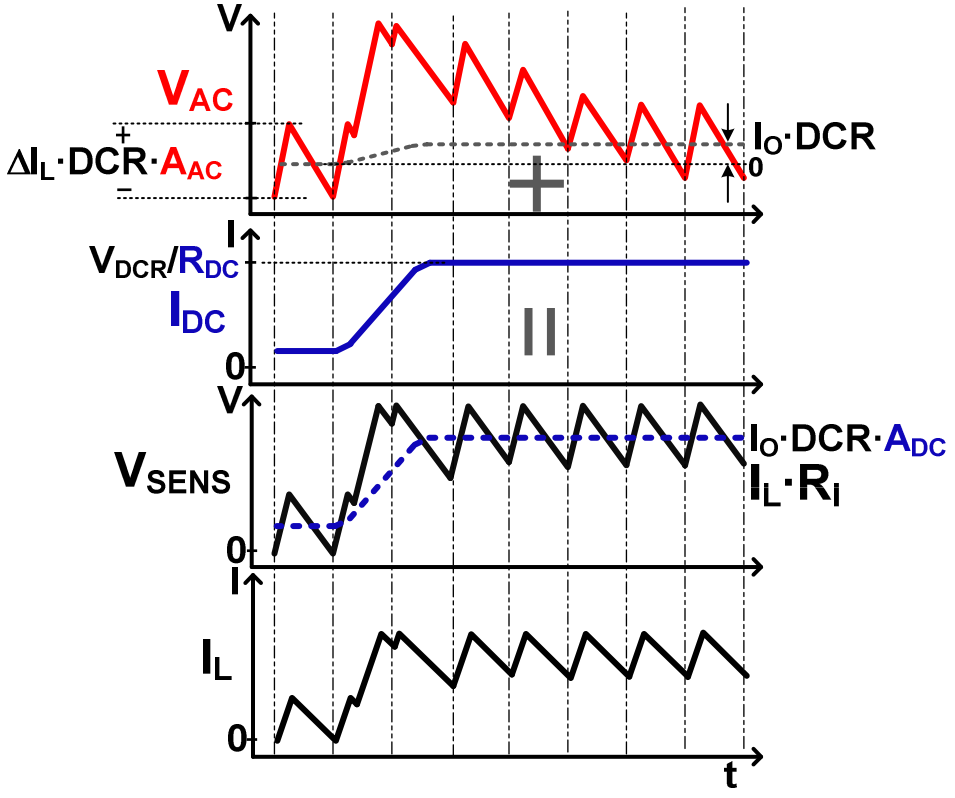


- **Pros:**
  - Continuous I_L sensing.
  - No additional power loss from series R.
- **Cons:**
  - Small DCR.
  - Insufficient current sense gain requires additional wide-bandwidth amplifier.

More power consumption as f_{SW} increases!

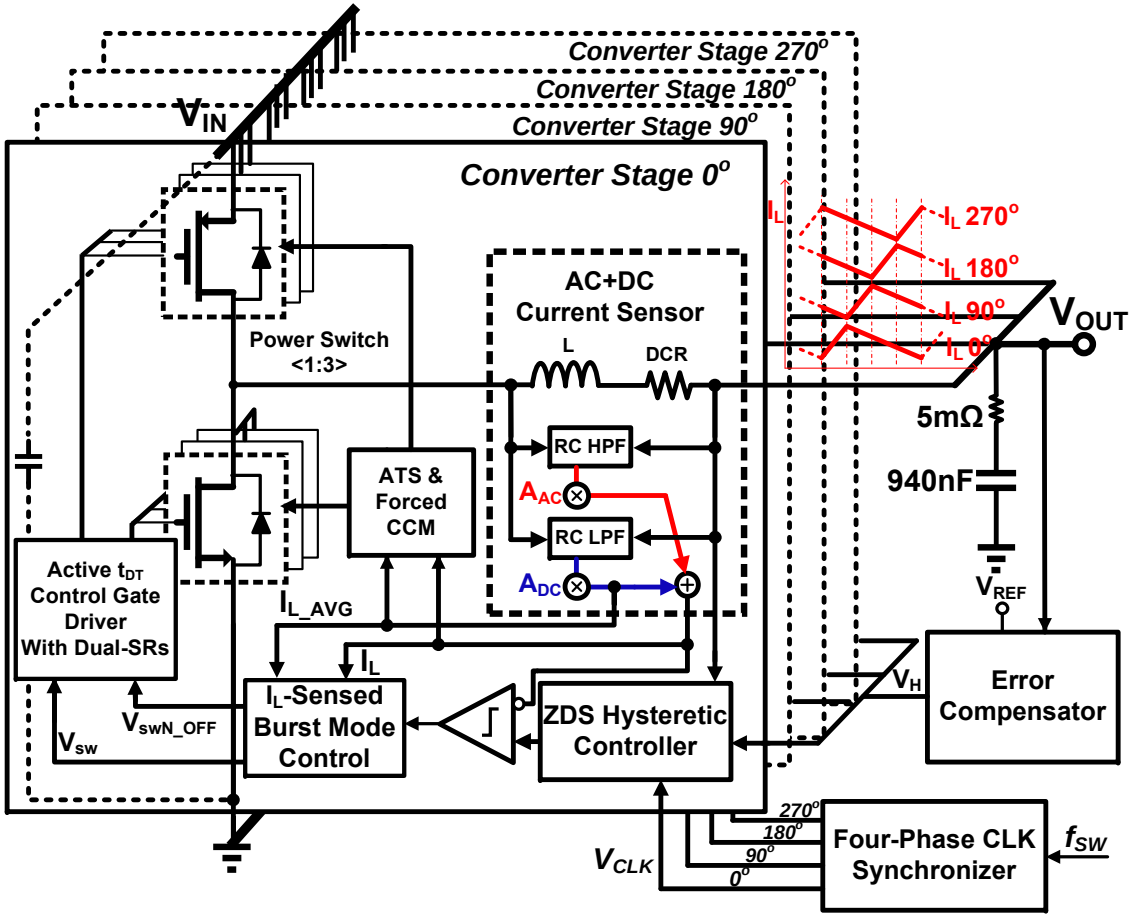
Emulated AC+DC Current Sensor

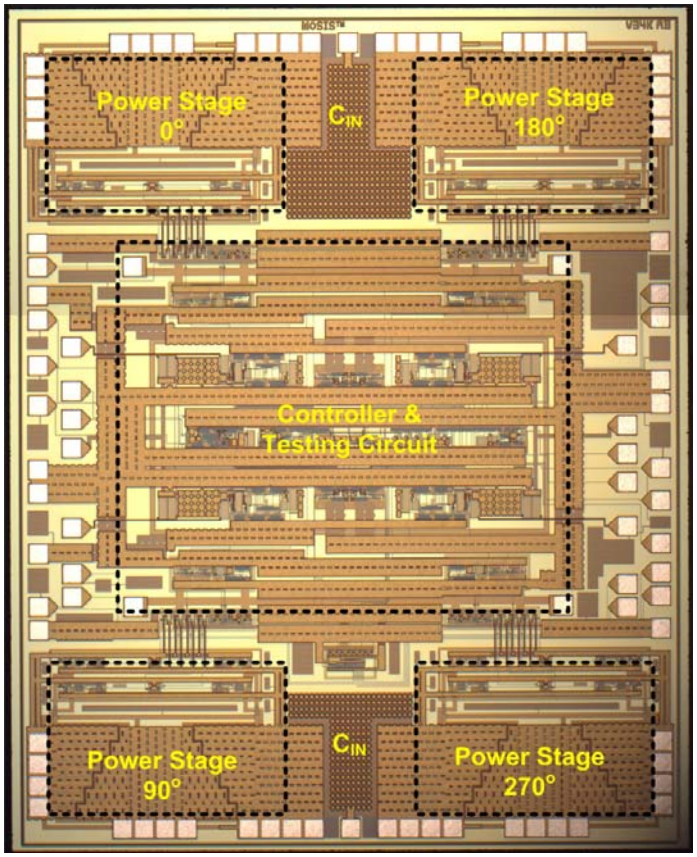




- Split the AC (fast) and DC (slow) portion of I_L, amplify them separately, and combine them together.
- It eliminates the need for a power hungry wide-bandwidth amplifier in order to amplify the V_{DCRs}.

Example 1*: PMIC for High I_O Slew Rate APs



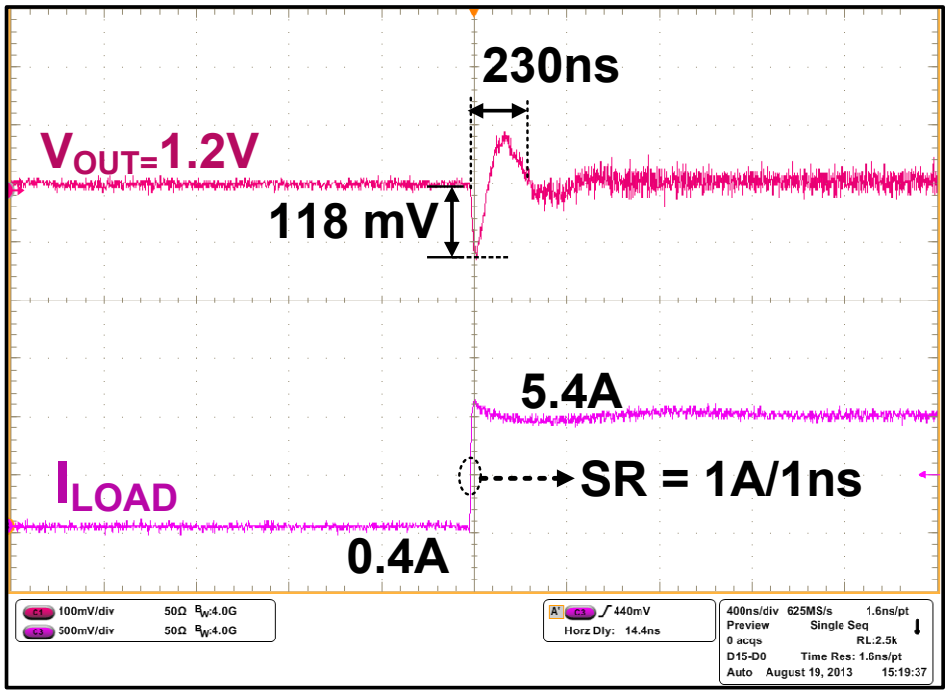


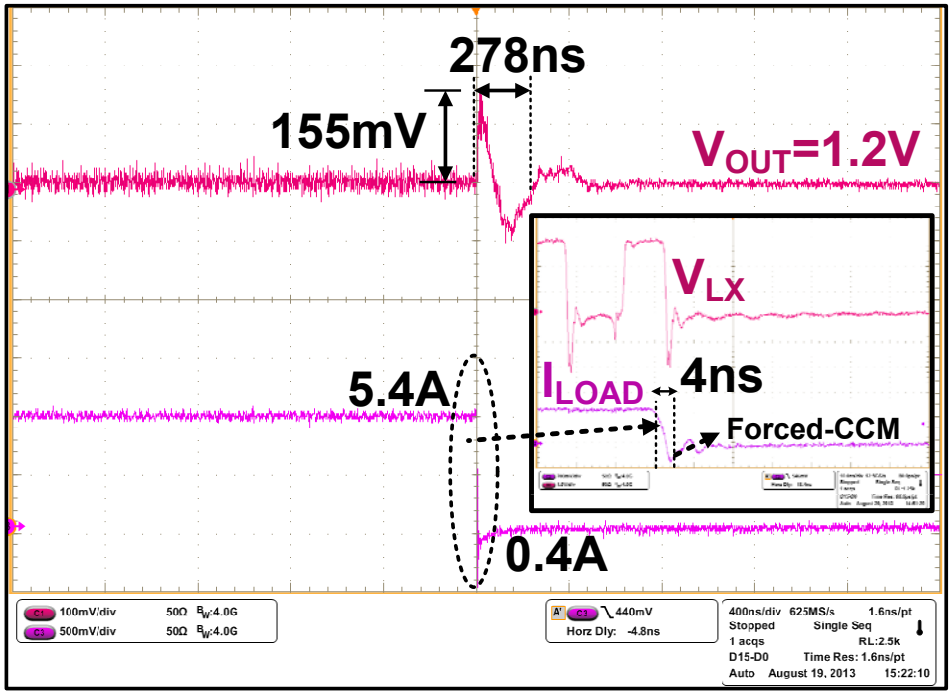
- ZDS Hysteretic Control
- 4-phase synchronization

- Cycle-by-cycle current sharing.
- Adaptive transistor sizing with forced-CCM and I_L-sensed burst mode control

*M. Song, J. Sankman, D. Ma, "A 6-A, 40-MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient," IEEE *ISSCC*, pp. 80-81, Feb. 2014.

Results: Transient Response



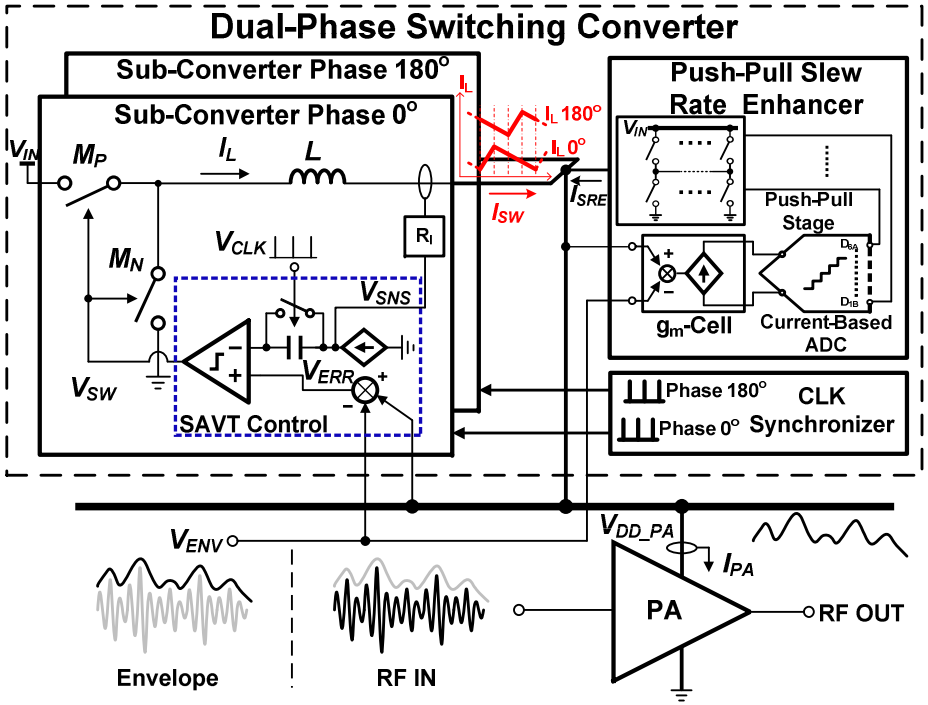


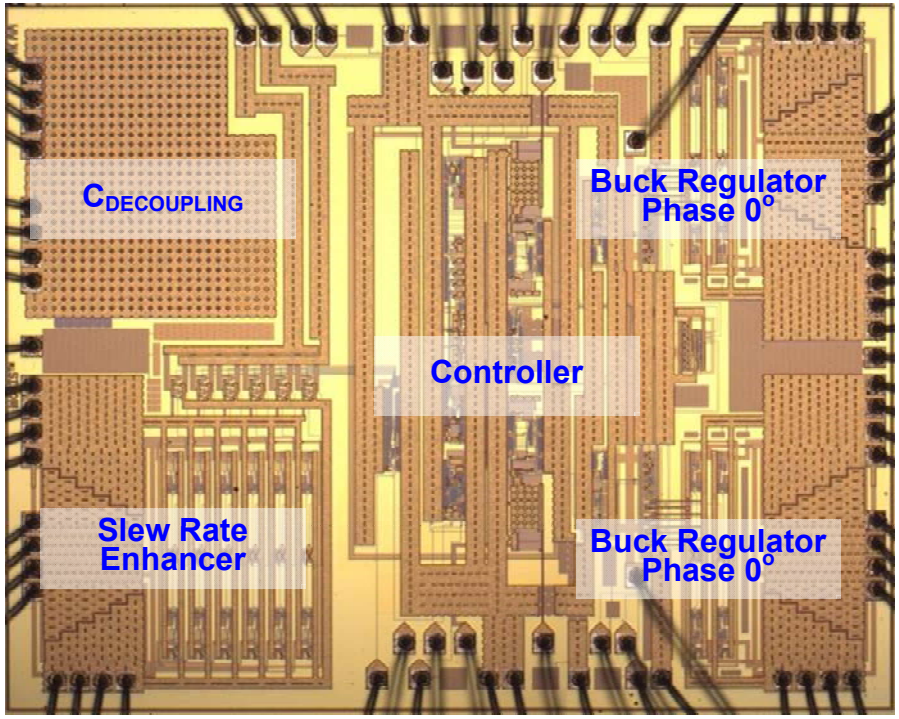
- 5A load step with >1A/1ns slew rate is tested with 2×470nF(10mΩ ESR) filtering output capacitor.
- Forced-CCM operation is temporarily active during the I_O step down.

Performance Comparison

	ISSCC '13 [1]	JSSC '05 [2]	JSSC '09 [3]	This Work
Control	PWM	Hysteretic	Hysteretic	ZDS Hysteretic
Current Sharing	Master-Slave	Cycle-by-Cycle	None	Cycle-by-Cycle
$V_{IN\ (MAX)}$ (V)	1.2	1.2	4.9	3.3
V_{OUT} (V)	0.6-1.05	0.9	0.86-3.93	0.7-2.5
f_{SW} (MHz) (phases)	100 (×4)	233 (×4)	32-35 (×4)	40 (×4)
L (nH)	8	6.8	110	78
C_{OUT} (μF)	0.00187	0.0025	0.2	0.94
I_{MAX} (A)	1.2	0.3	1	6
Load Step (mA/ns)	180 / 800	150 / 0.1	300 / 30	5000 / 5
1% t_{settle} (ns)	~2000	~30	~350	230
V_{OUT} Droop (%)	6.7% (V_{OUT}=0.9V)	10% (V_{OUT}=0.9V)	10% (V_{OUT}=1.8V)	9.8% (V_{OUT}=1.2V)
Peak Efficiency (%)	82.4	83.2	80	86.1

Example 2*: Envelope Modulator for LTE PAs

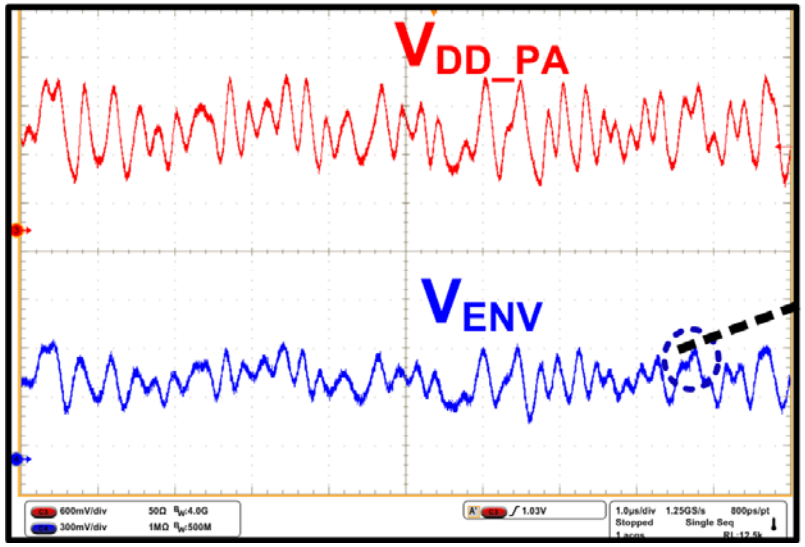


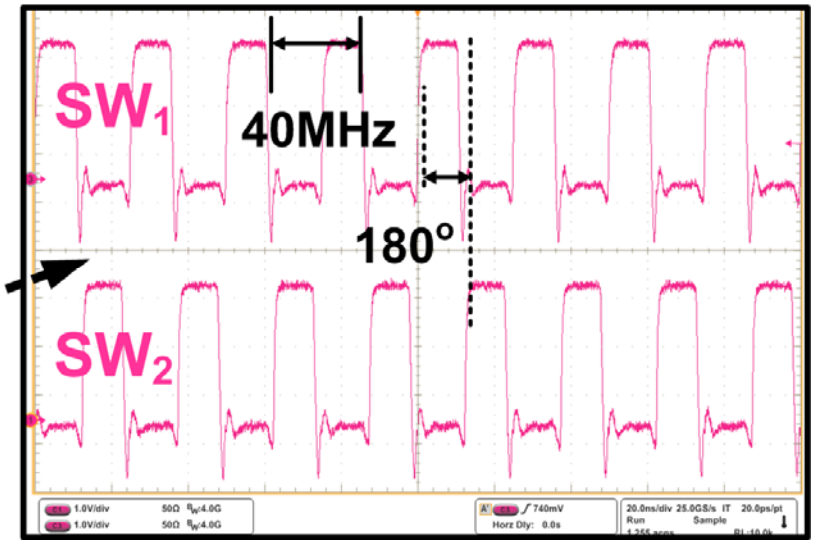


- **Dual-phase *switching converter-only* topology.**
- **Adaptive Voltage Tracking (AVT) control.**
  - **Fast hysteretic response.**
  - **Clock sync. for predictable noise**

*J. Sankman, M. Song, D. Ma, "A 40-MHz 85.8%-Peak-Efficiency Switching-Converter-Only Dual-Phase Envelope Modulator for 2-W 10-MHz LTE Power Amplifier"," IEEE *VLSI Symp.*, pp. 214-215, June 2014.

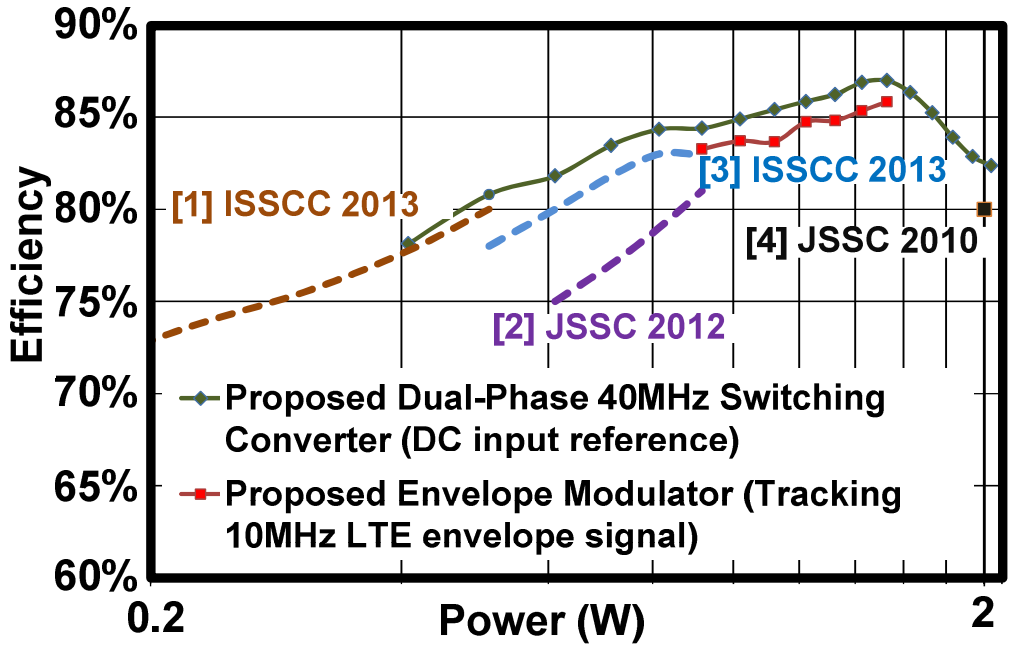
Key Results





Specs:

- 2-W PA
- V_{IN} = 3.3 V
- 10-MHz LTE
- The dual-phase converter
- synchronized at 40MHz with 180° phase shift.



Conclusion

- Current SoCs face speed bottleneck imposed by slow and bulky power management solutions.
- Strong demands for “smart” power and performance control push the power management to be achieved on-chip.
- As high density, high frequency and high speed become necessary, they create unprecedented design challenges.
- Cross-layer design efforts are needed in order to achieve desired performance breakthroughs.

Acknowledgements

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