Efficient on-chip power conversion for energy harvesting and low-power mobile applications

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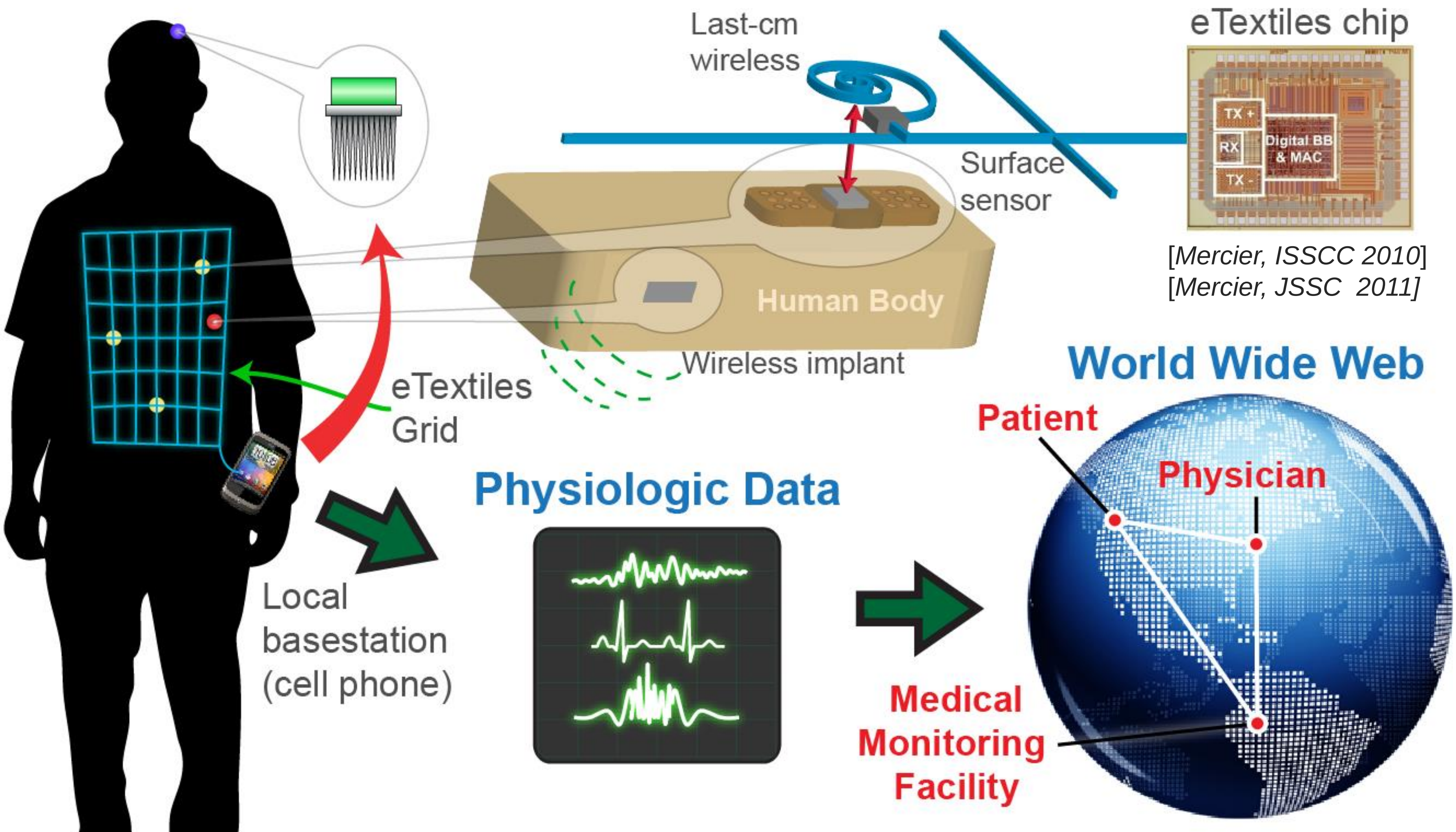
Application example 1: wearable devices



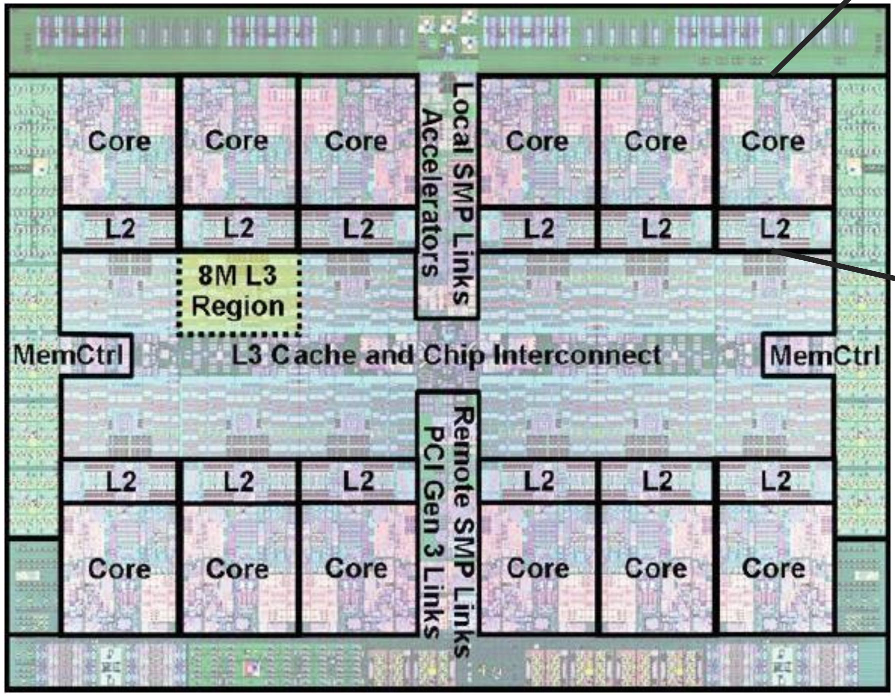
Battery life limits usability; require high efficiency energy processing and/or energy harvesting for long operational time

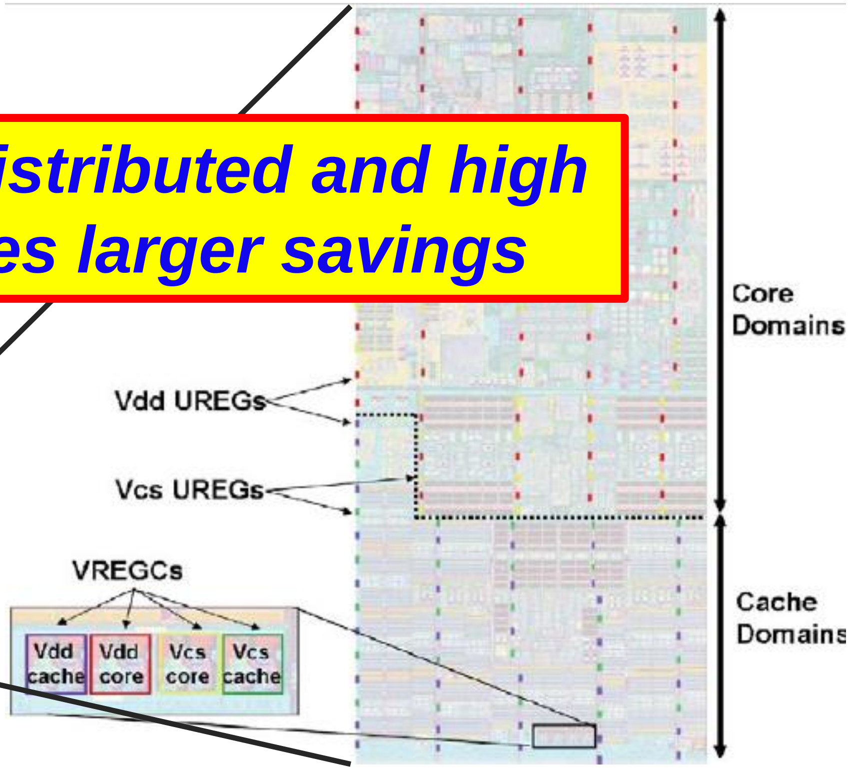
Application example 2: fine-grain power management

- *POWER8*, IBM

A fully-integrated distributed and high η regulator enables larger savings

ISSCC'14





- ***48 DVFS domains, each with ~64 μRegulators***
- ***~1.5x power savings even with LDOs (η >61%)***

The key challenge…

…in both applications is achieving

high power conversion efficiency

in **very small sizes**

Talk outline

- Energy harvesting from the human body
- Switched-capacitor converters: principal challenges
- New switched capacitor topologies that achieve high efficiency over large voltage ranges:
  - Recursive binary
  - Recursive ternary
- Conclusions

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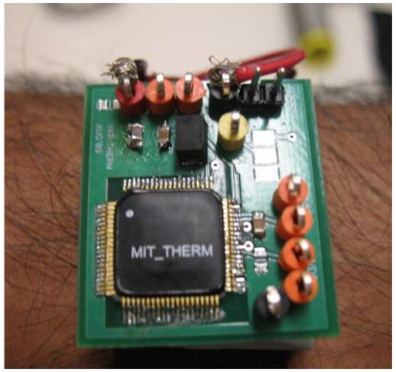
Harvesting energy from the human body

Leg motion (~10W)
(Bionic Power)

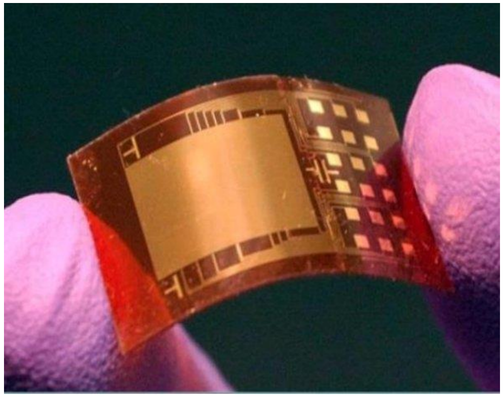
Heel strike (~1W)
(MIT)



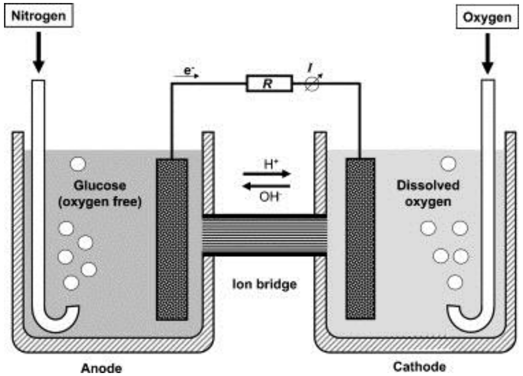
Thermoelectric (~100μW)
(MIT)

↑ **External**

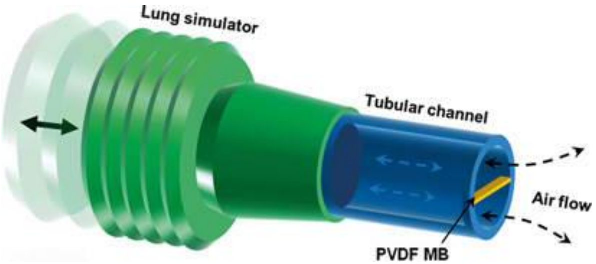
↓ **Implantable**



Nanogenerator (~1mW)
(Georgia Tech)

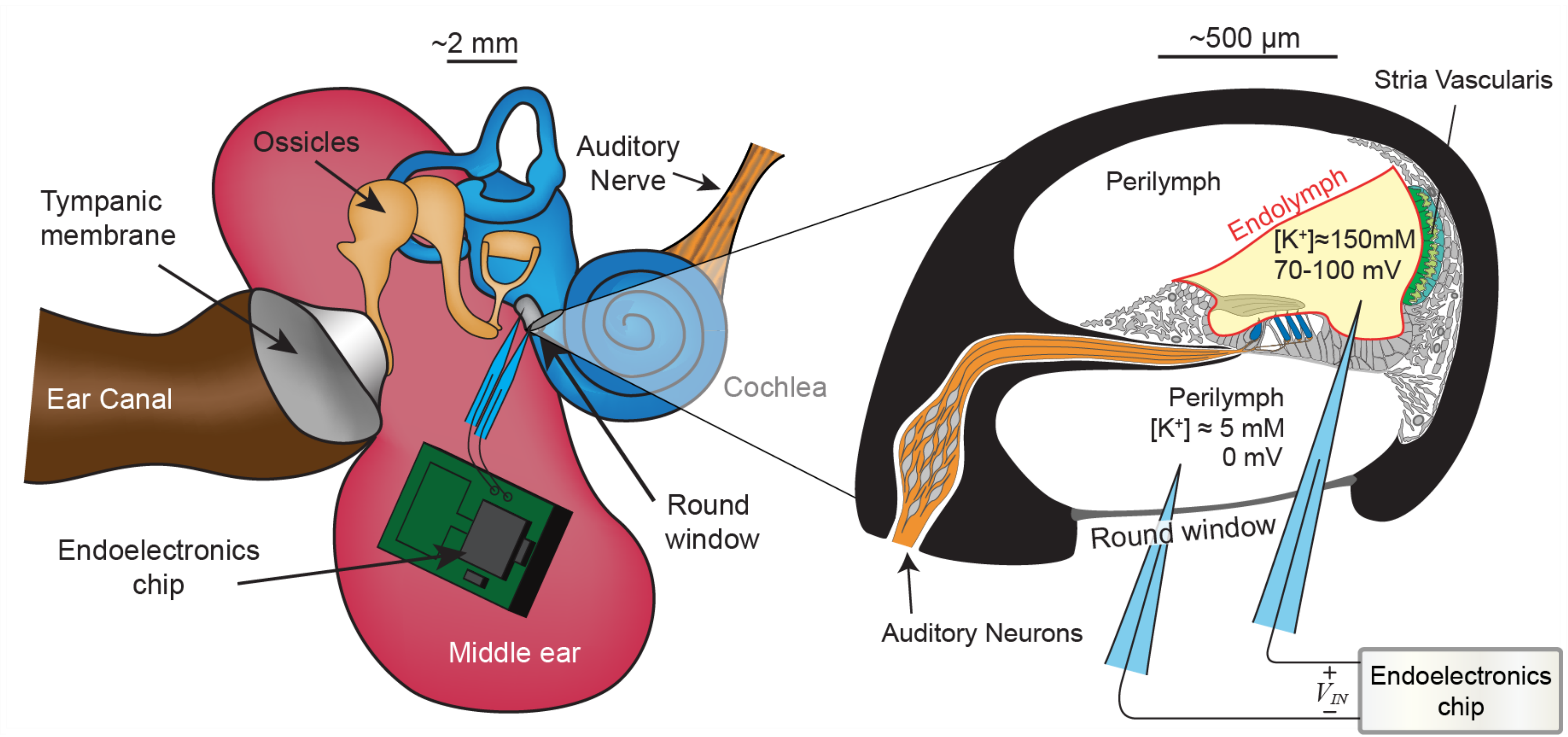


Glucose fuel cell (~10μW)
(U. Freiburg)



Respiration (~100nW)
(U. Wisconsin-Madison)

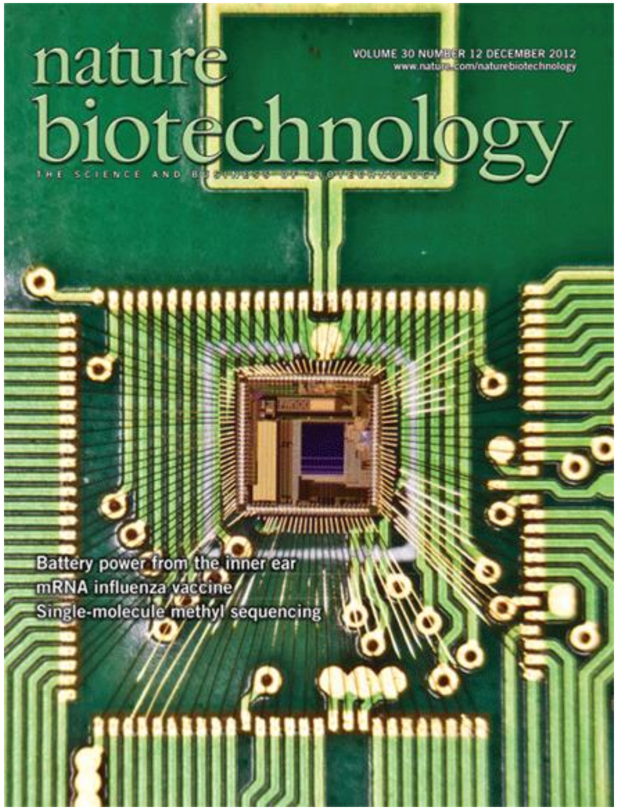
A (new) energy harvesting source: the endocochlear potential

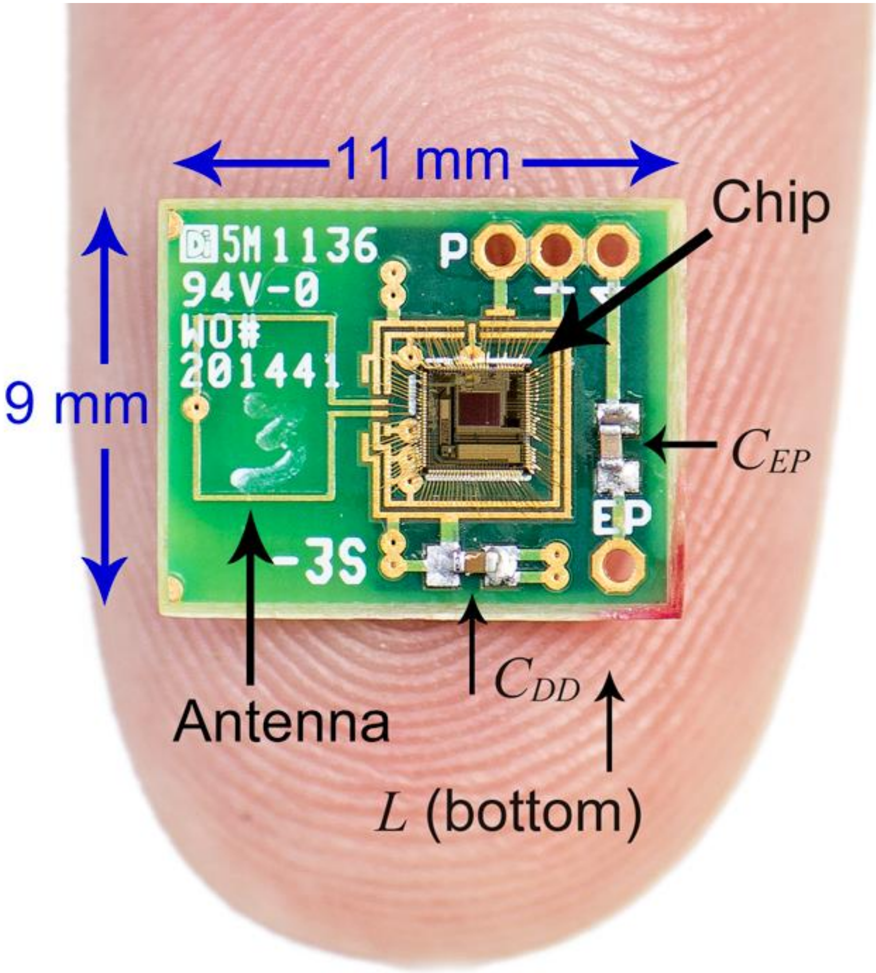


Challenge: anatomically-miniaturized electrodes limit extractable power to ~2nW

Yes we can!

Chip implementation details:



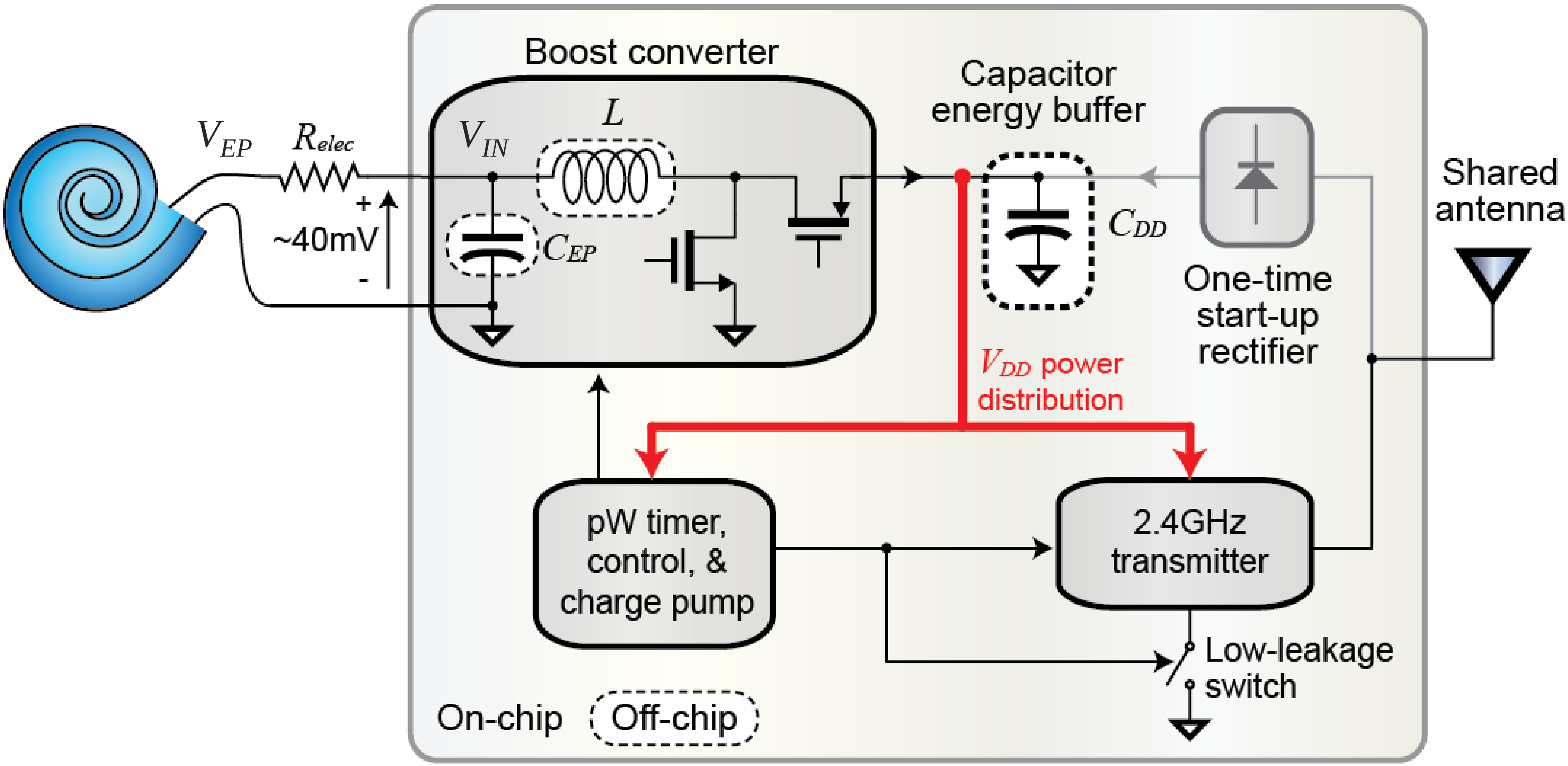


Technology	0.18 µm CMOS
Supply	0.8 - 1.1 V
Charge-pump	1.4 - 2.2 V
Radio data rate	0.1 - 10 Mbps

Chip-on board small enough to fit in the human mastoid cavity

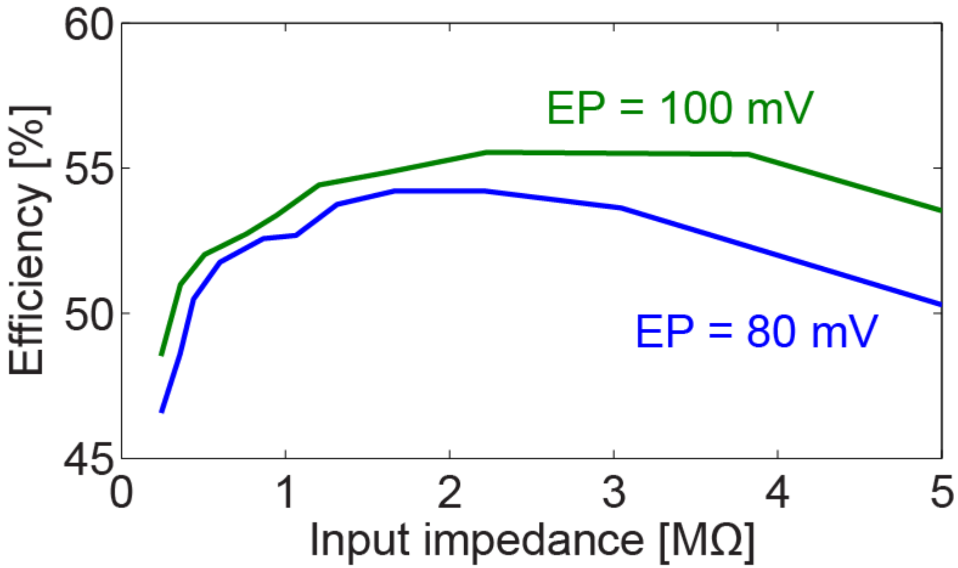
[Mercier *et al.*, *Nature Biotechnology*, Dec. 2012]

Endoelectronics chip: EP harvester architecture



Acknowledgements: Saurav Bandyopadhyay, Anantha Chandrakasan, Konstantina Stankovic, Andrew Lysaght

We can extract net positive power!



Efficiency of power train (@ R_{elec} = 1 MΩ)

×

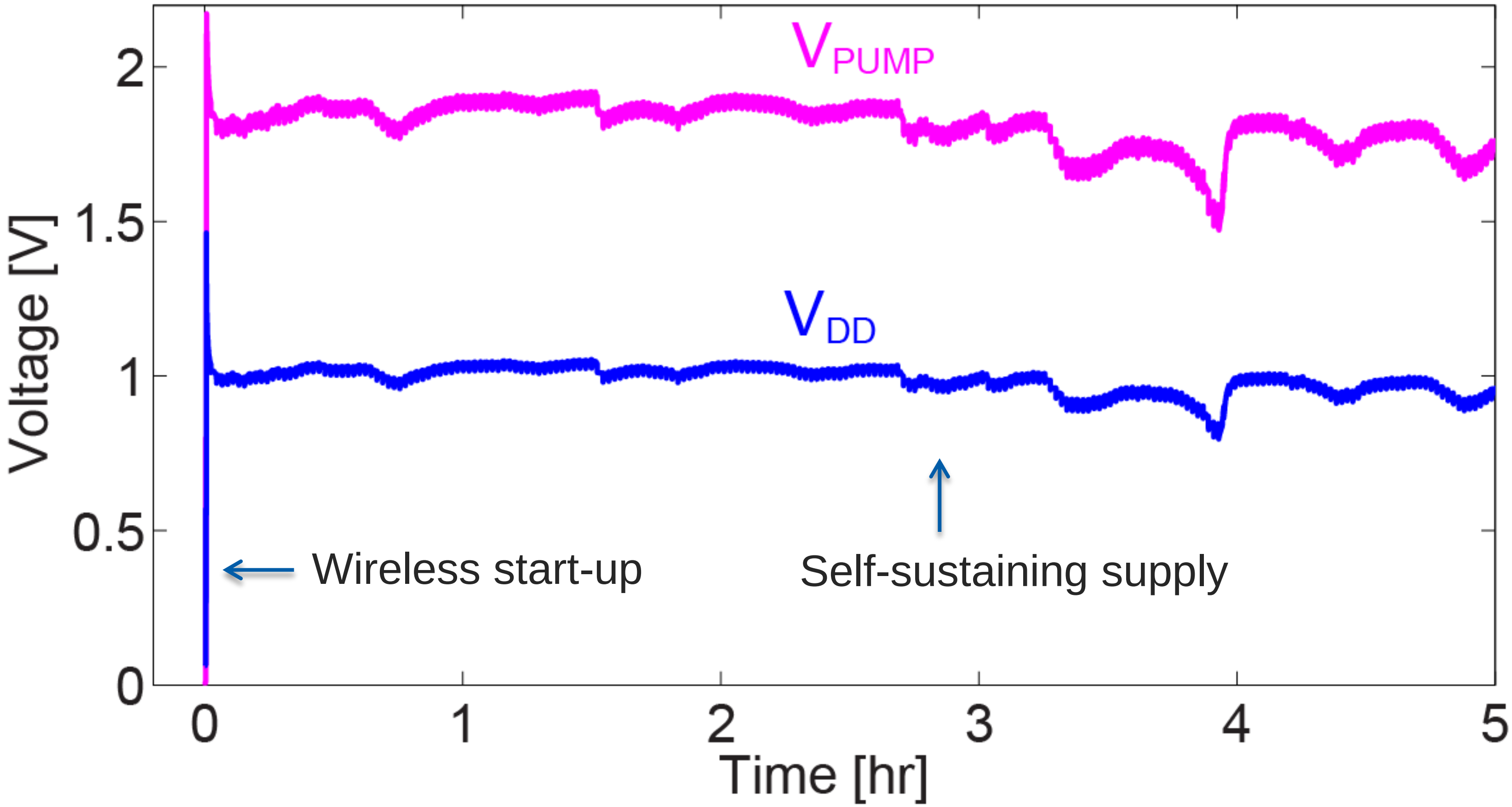
Available input power (1.6 – 2.5 nW)

−

Block power consumption	
12.5 Hz timer	350 pW
Control + drivers	100 pW
Charge-pump	70 pW
Total:	**520 pW**

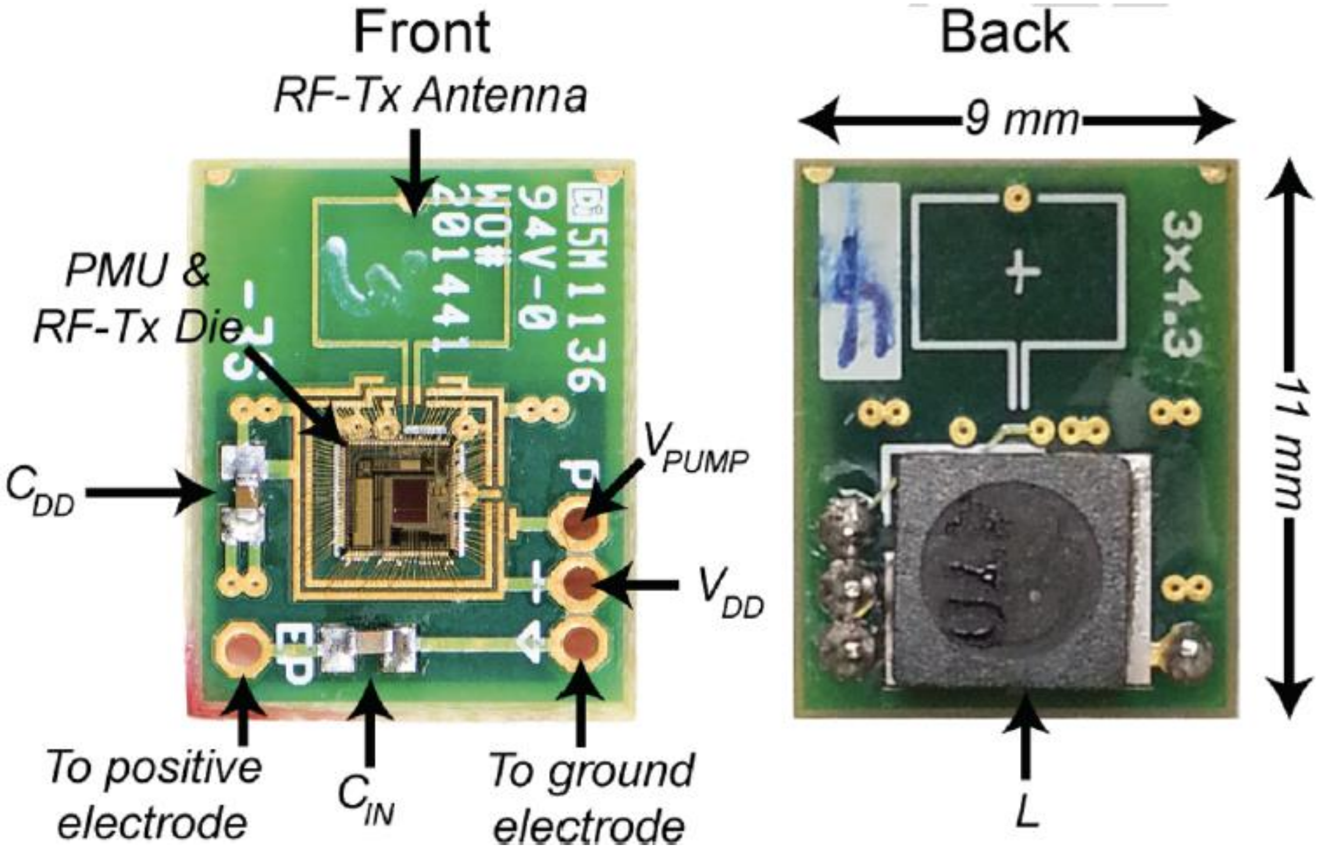
First boost converter at this power level

Clinical guinea pig experiments - results



First demonstration of an electronic system sustaining itself from a mammalian electrochemical potential!

Size constraints



- The inductor is larger than the chip, and we are dealing with nanowatts!
  - Ultimately limits implant size
- Difficult to integrate in multi-output applications

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Switched-capacitor DC-DC converter: inherent size advantage

Power inductor:

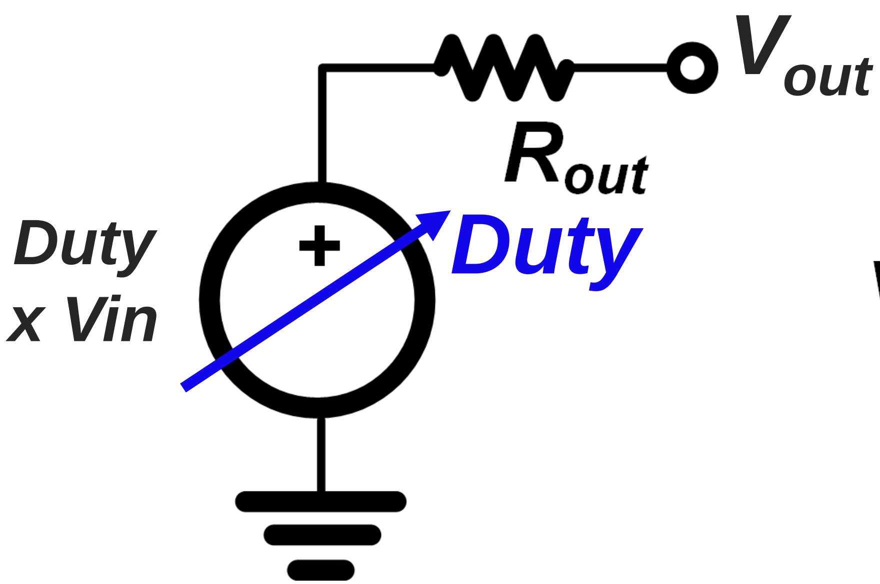
- 7x higher BOM cost
- 8x larger footprint
- Difficult to integrate on-chip

Capacitor:

- Higher inherent power and energy density
- Easily integrated on-chip (e.g., MIM, MOSCAP, deep-trench)

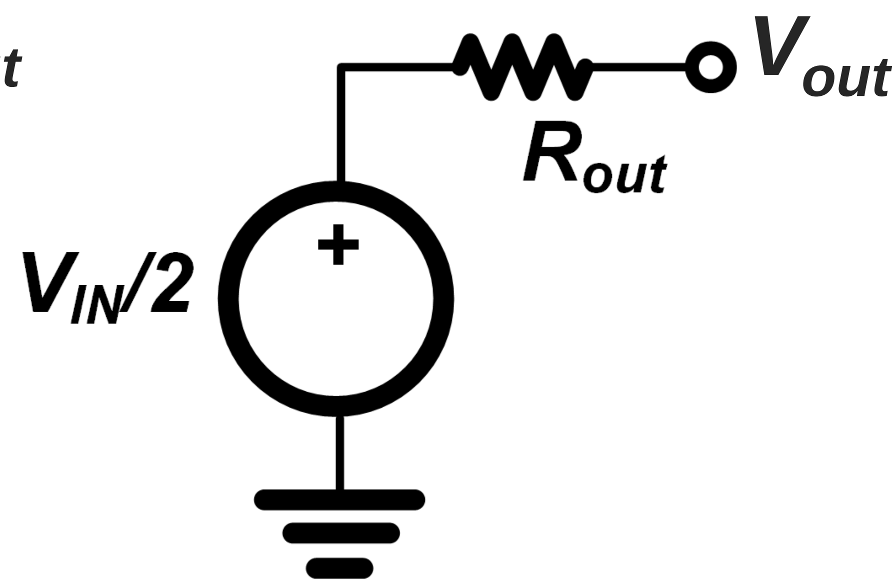
SC problem in DC-DC conversion

Continuous DC conversion ratio



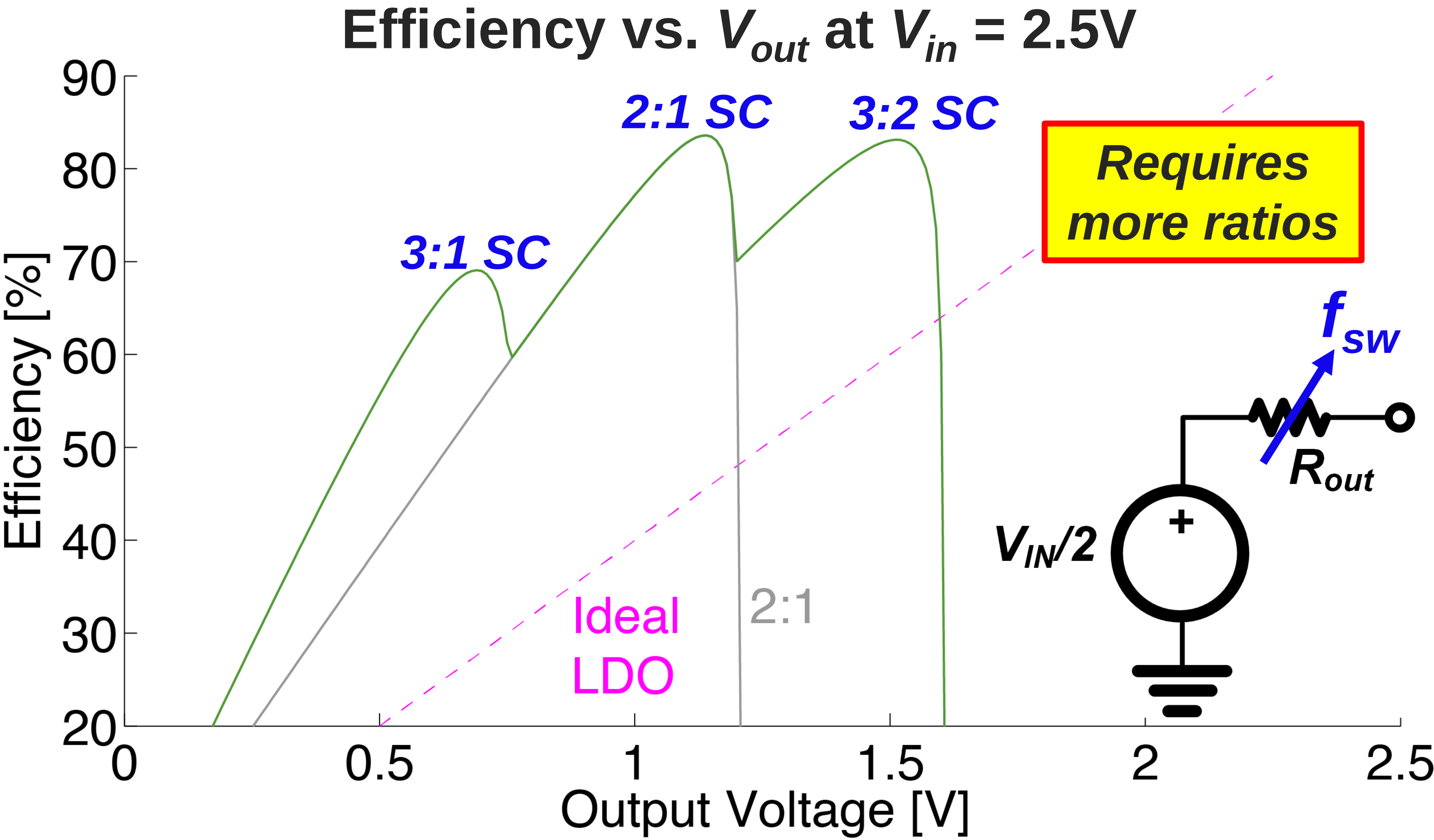
Switched Inductor

Fixed DC conversion ratio



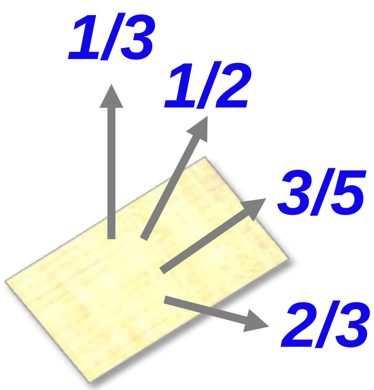
Switched Capacitor

SC Efficiency



Higher Number of Ratios Challenge with Conventional SC Topologies

GOAL: **would like to re-use available capacitance for all ratios *to limit size***



PROBLEM:

- ***No. Of caps and switches increases exponentially***
- ***Each ratio requires a unique arrangement, which is difficult to re-use among other ratios***

More ratios requires a Modular topology

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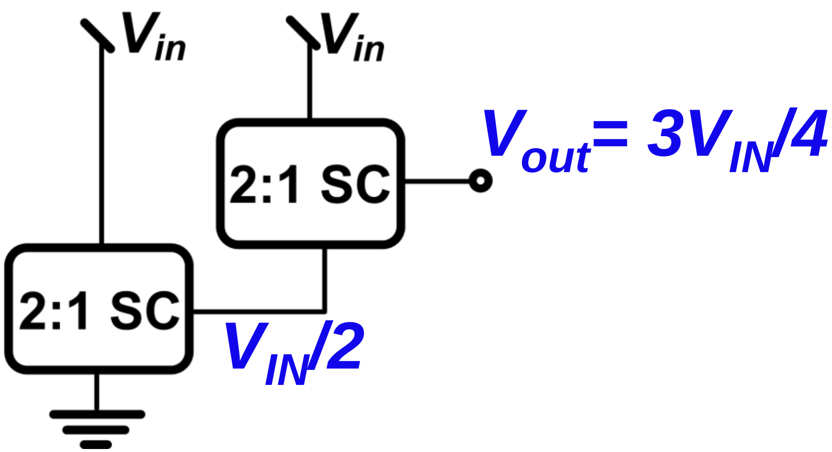
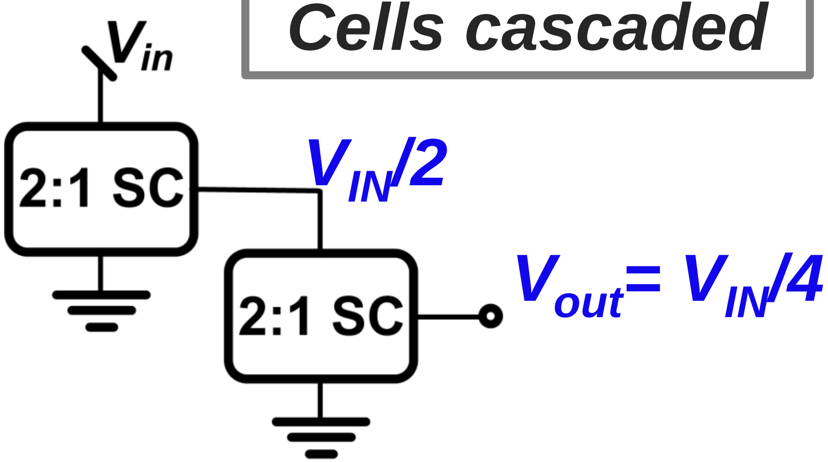
Solution part 1: modular reconfiguration

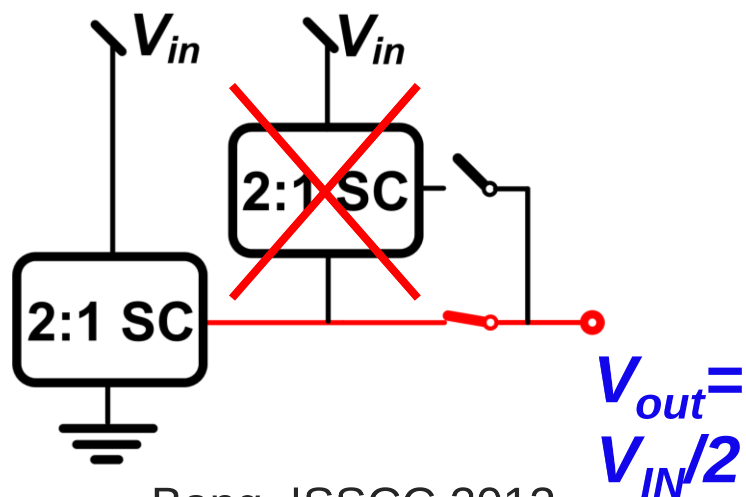
Cells Stacked



Cells cascaded



Route V_{out} from 1st cell for 1/2

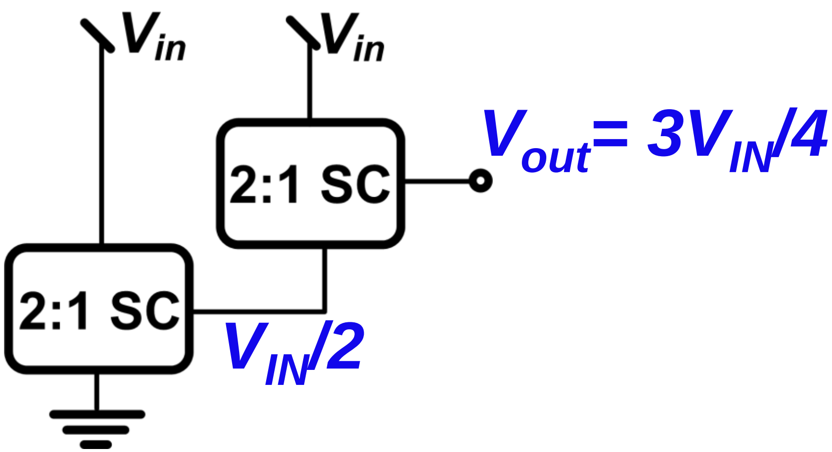


Bang, ISSCC 2013

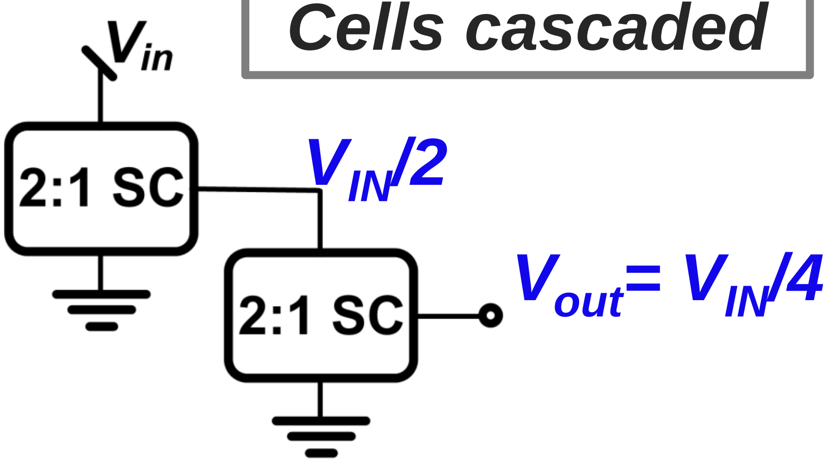
***PROBLEM*: Wastes the capacitance of the 2nd cell → lower η**

Solution part 2: recursive reconfiguration

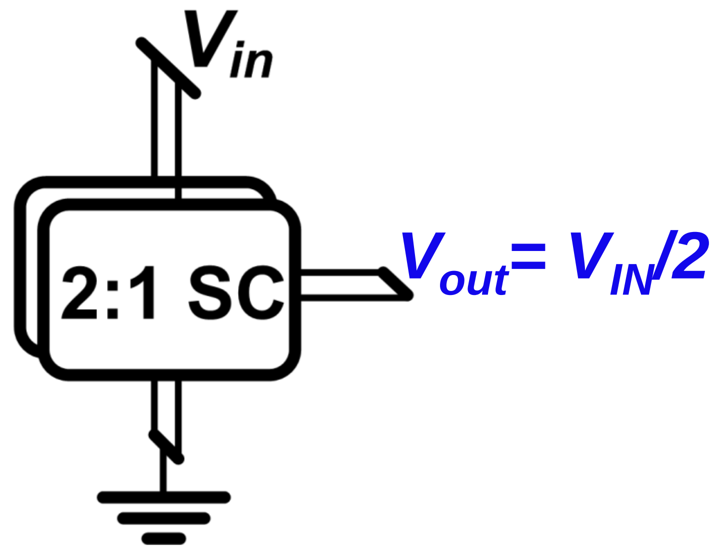
Cells Stacked



Cells cascaded



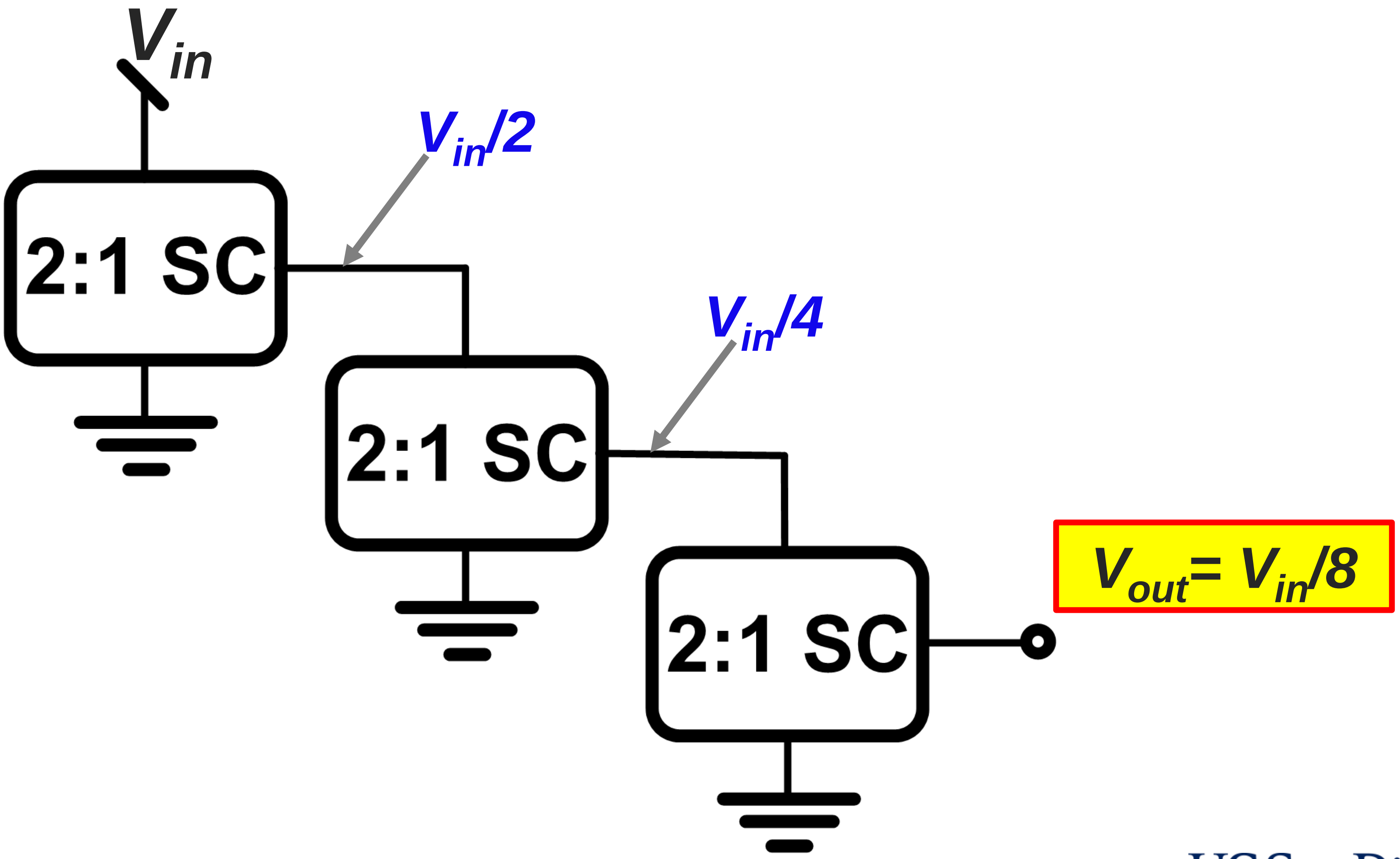
Cells in parallel for 1/2



Recursive Inter-cell Connection**: 100% of caps used amongst all ratios**

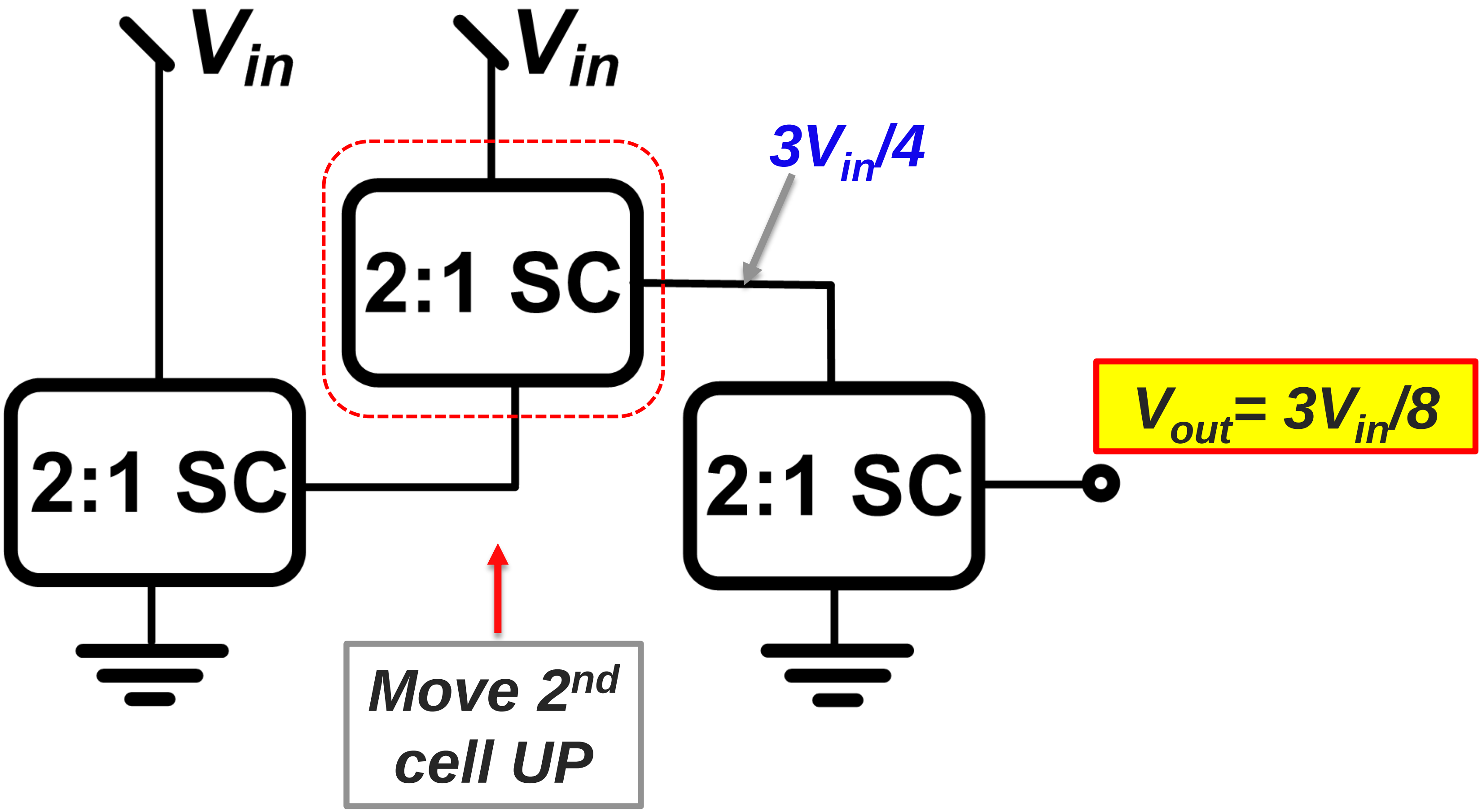
Recursive 3-bit SC

- Adding a third 2:1 SC cell: resolution = $V_{in}/2^3$



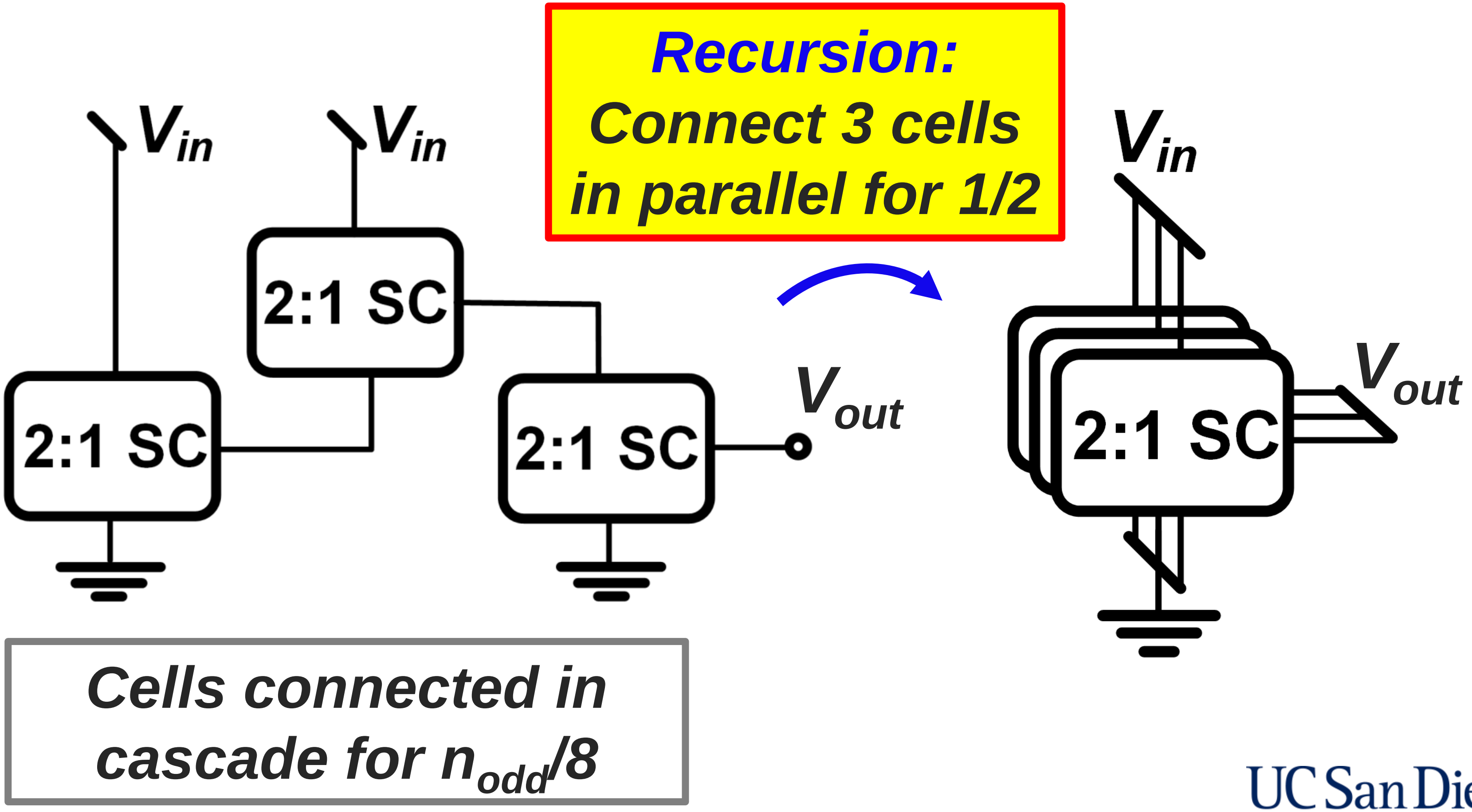
Recursive 3-bit SC

- Realizing 3/8 ratio



Recursive 3-bit SC: 1/2 Realization

- Now 1/8, 3/8, 5/8, 7/8 are realized, how to achieve 1/2 using 3 cells?



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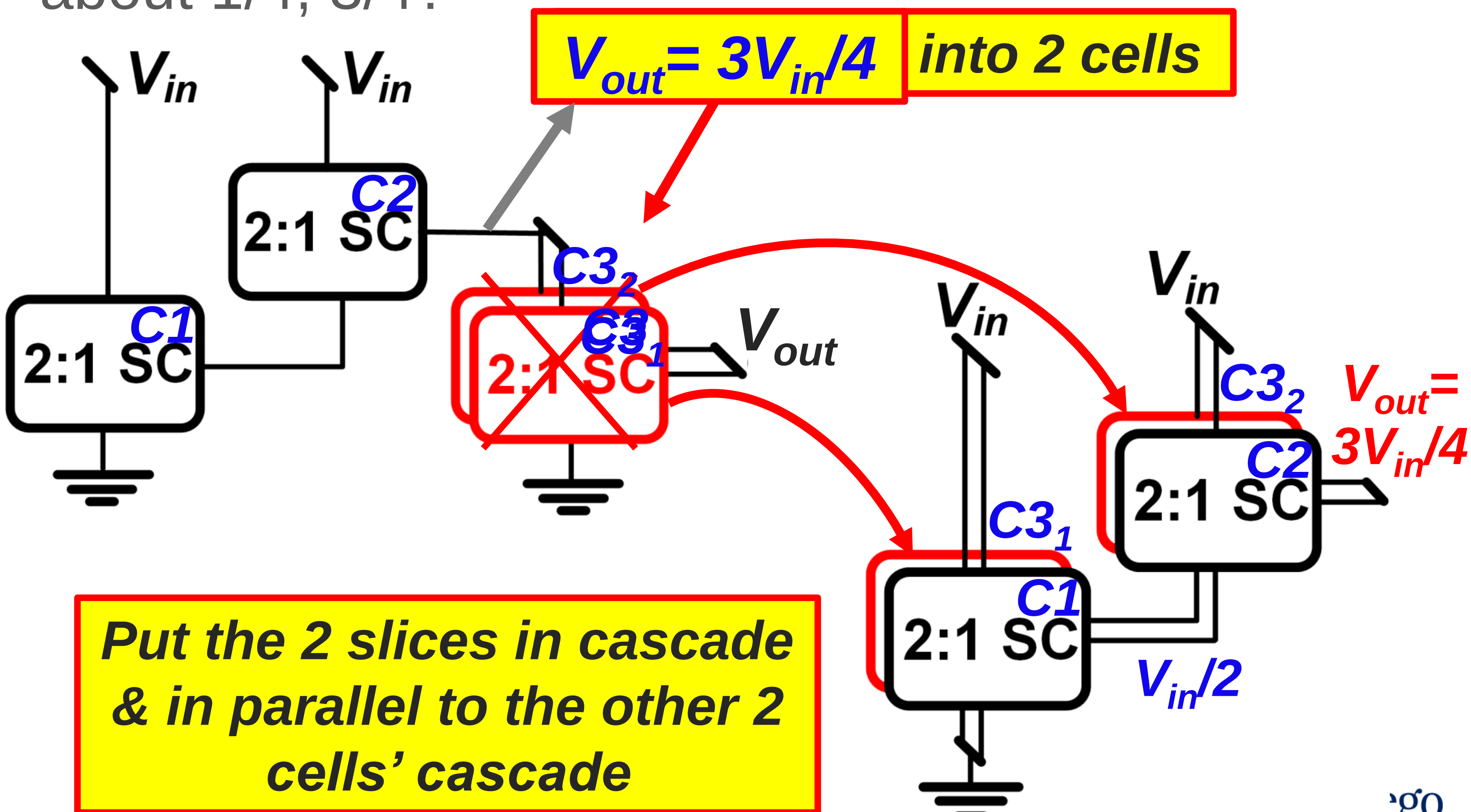
Recursive 3-bit SC: 1/4, 3/4 Realization

- Now 1/8, 3/8, 5/8, 7/8, and 1/2 are realized, what about 1/4, 3/4?



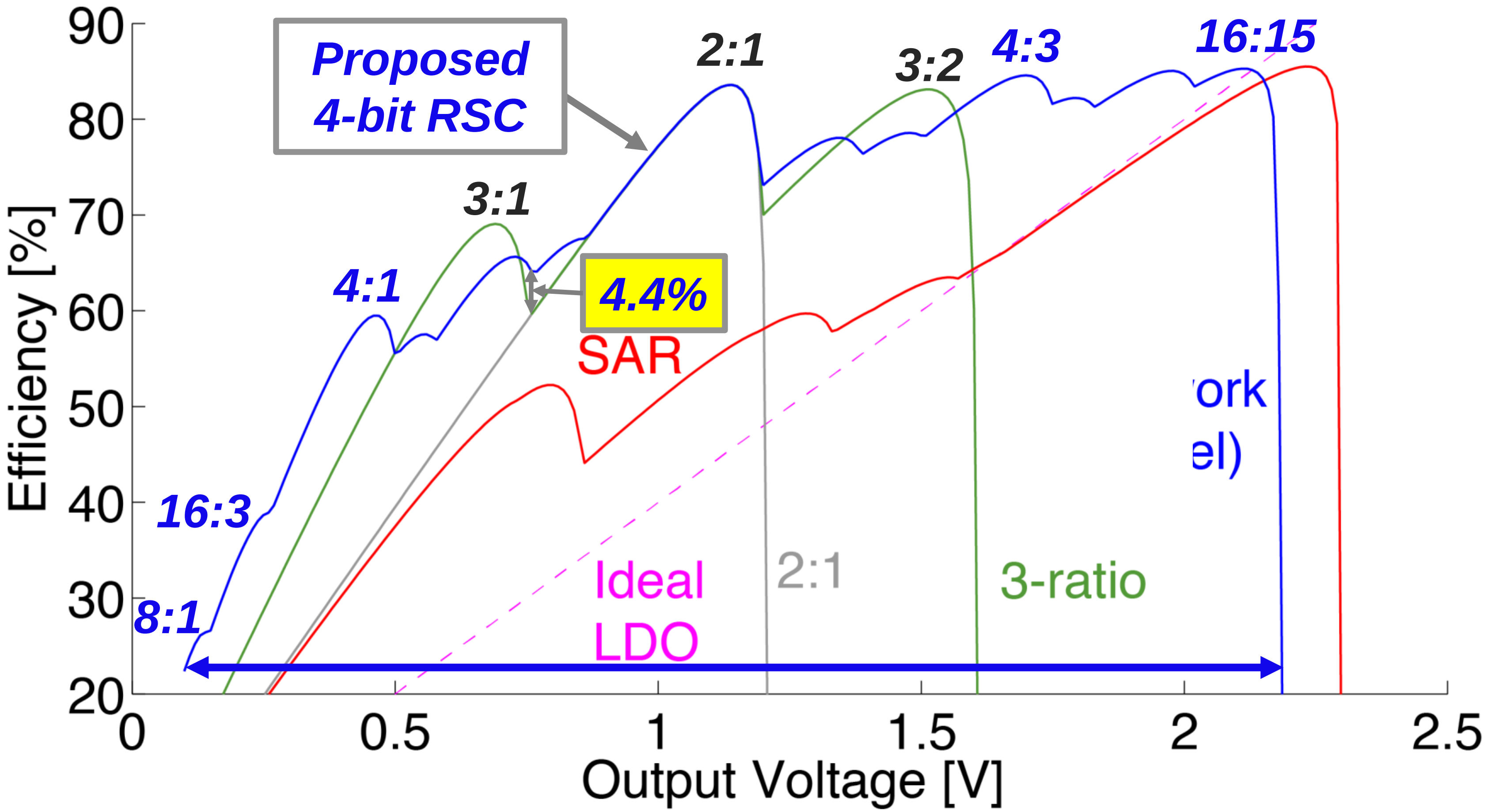
Recursive 4-bit SC

- A 4-bit Recursive SC topology is implemented
  - *Balance between complexity and flat η*

Realizing 15-ratio, of high η by:

- ***Recursive inter-cell connection for 100% cap utilization***
- ***Maximizing V_{in} & GND connections***
- ***Binary relative sizing***

4-bit Recursive SC Efficiency vs. V_{out}



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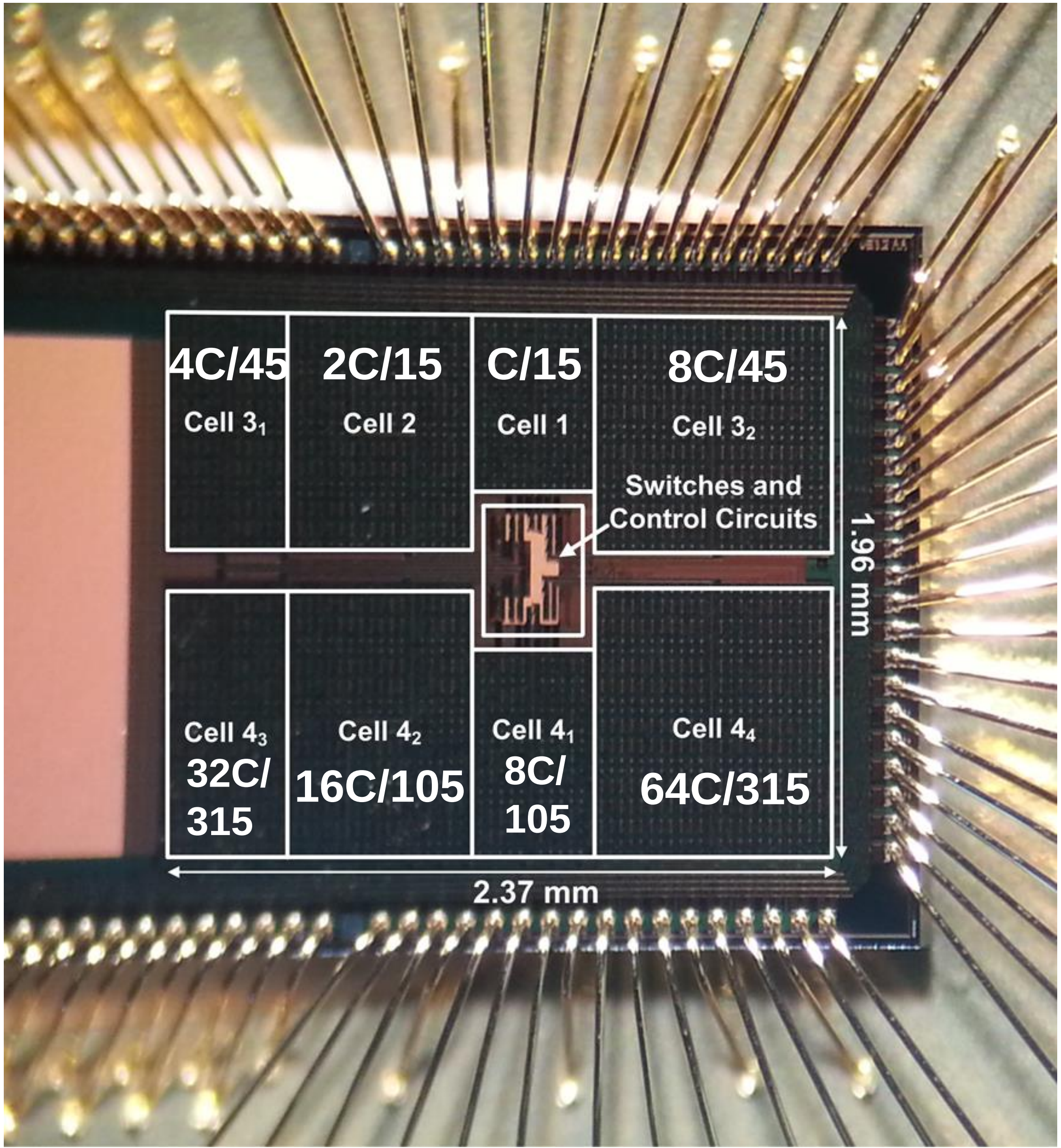
Fully Integrated Recursive 4-bit SC Prototype



0.25um 2.5V
bulk CMOS
MIM ~ 0.9 fF/um²

- **8 2:1 cells are used to enable recursion**
- **Cells are binary weighted for optimal relative sizing**

[Salem & Mercier, ISSCC 2014]

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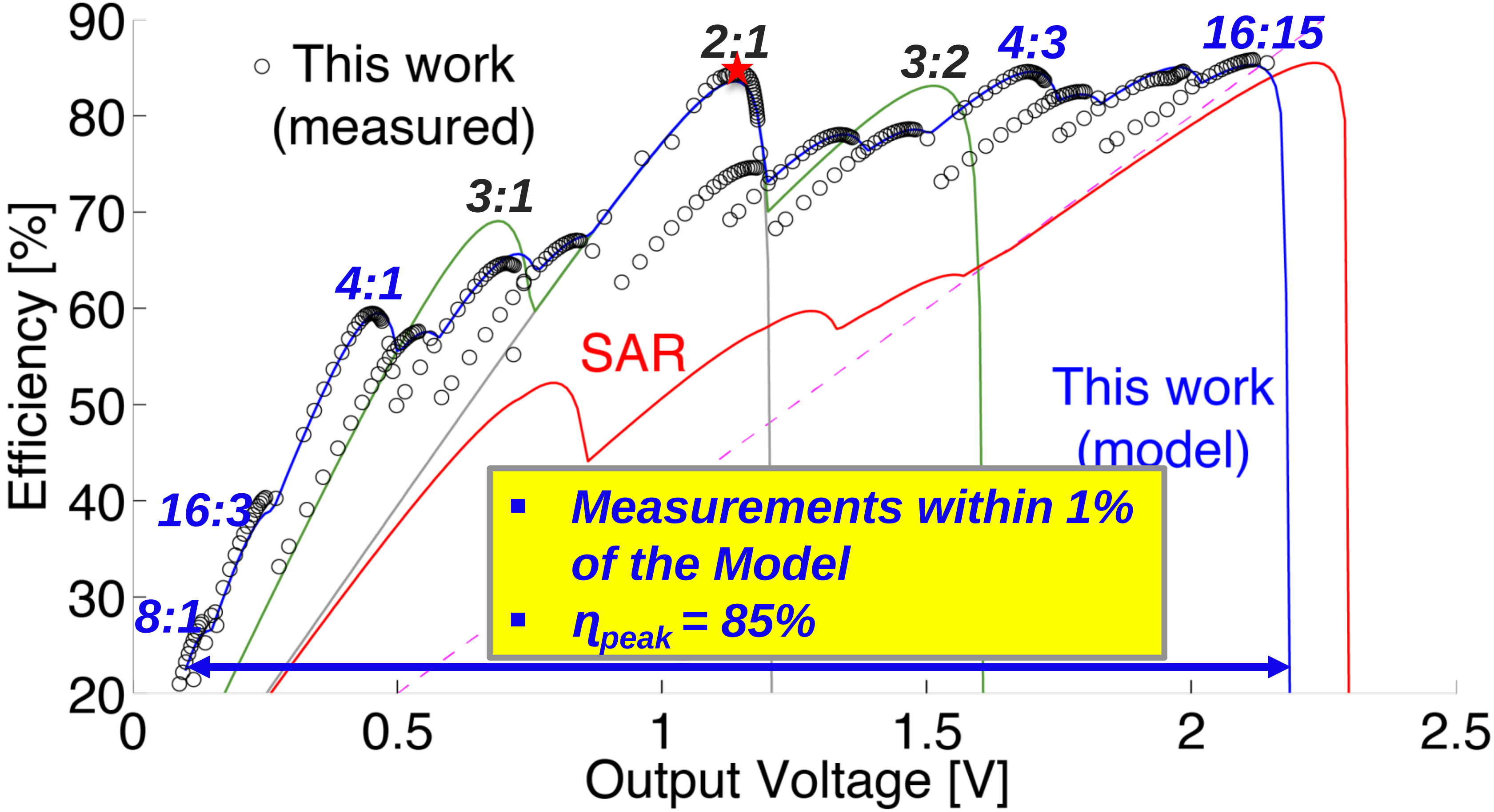
Measured Efficiency vs. V_{out}



For same silicon area: widest operating range, highest average efficiency

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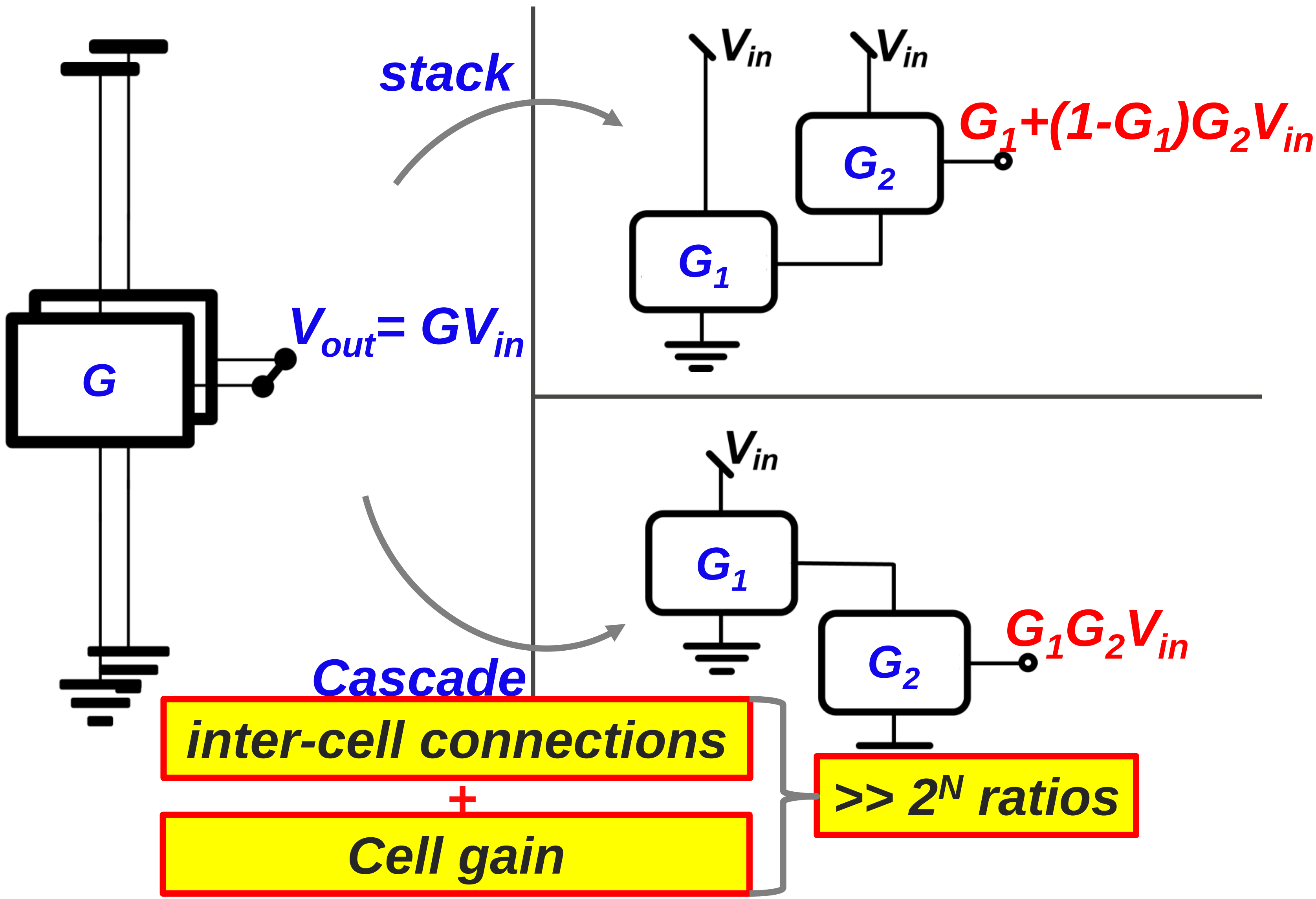
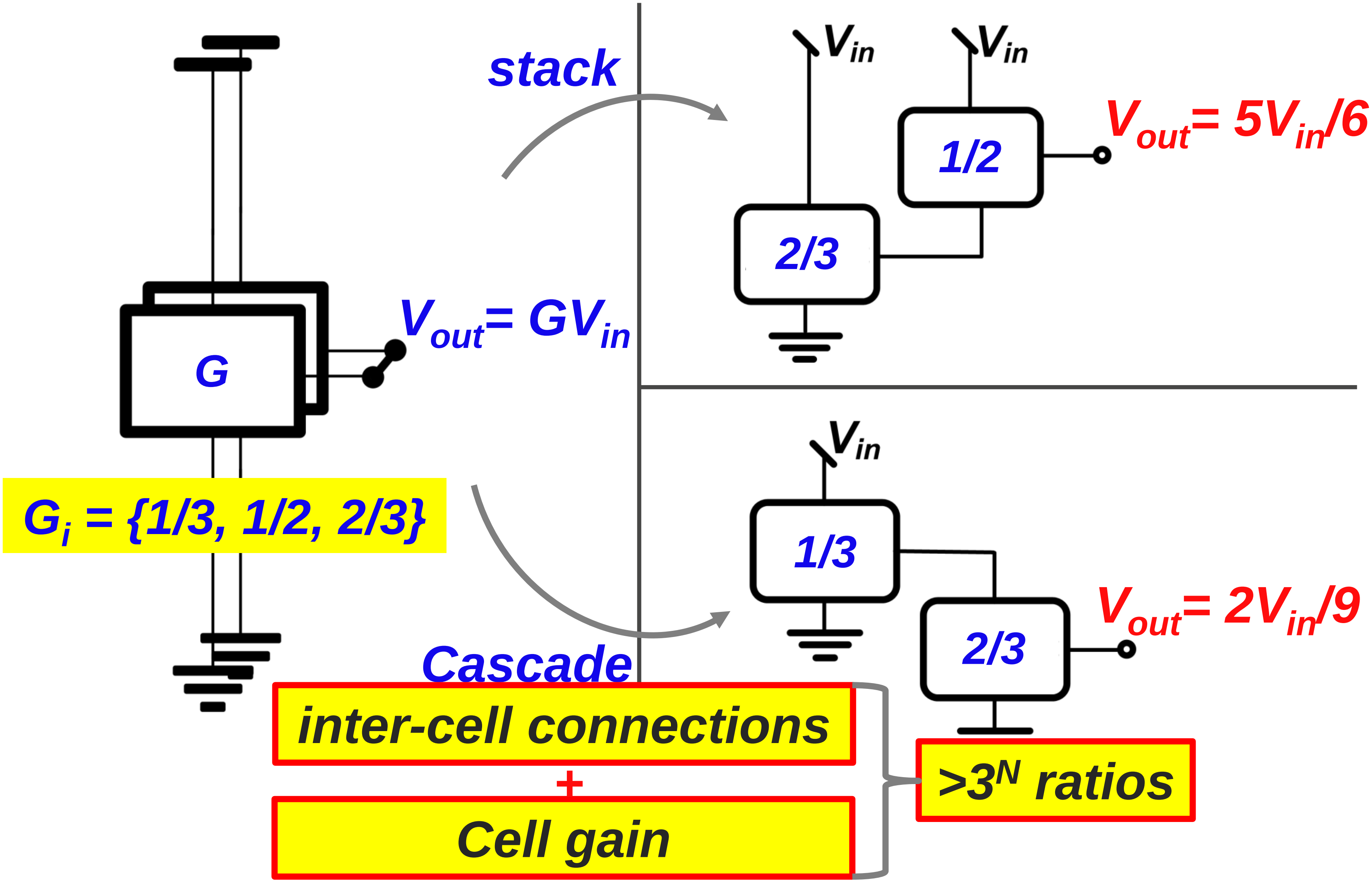
A new topology: Recursive Ternary SC

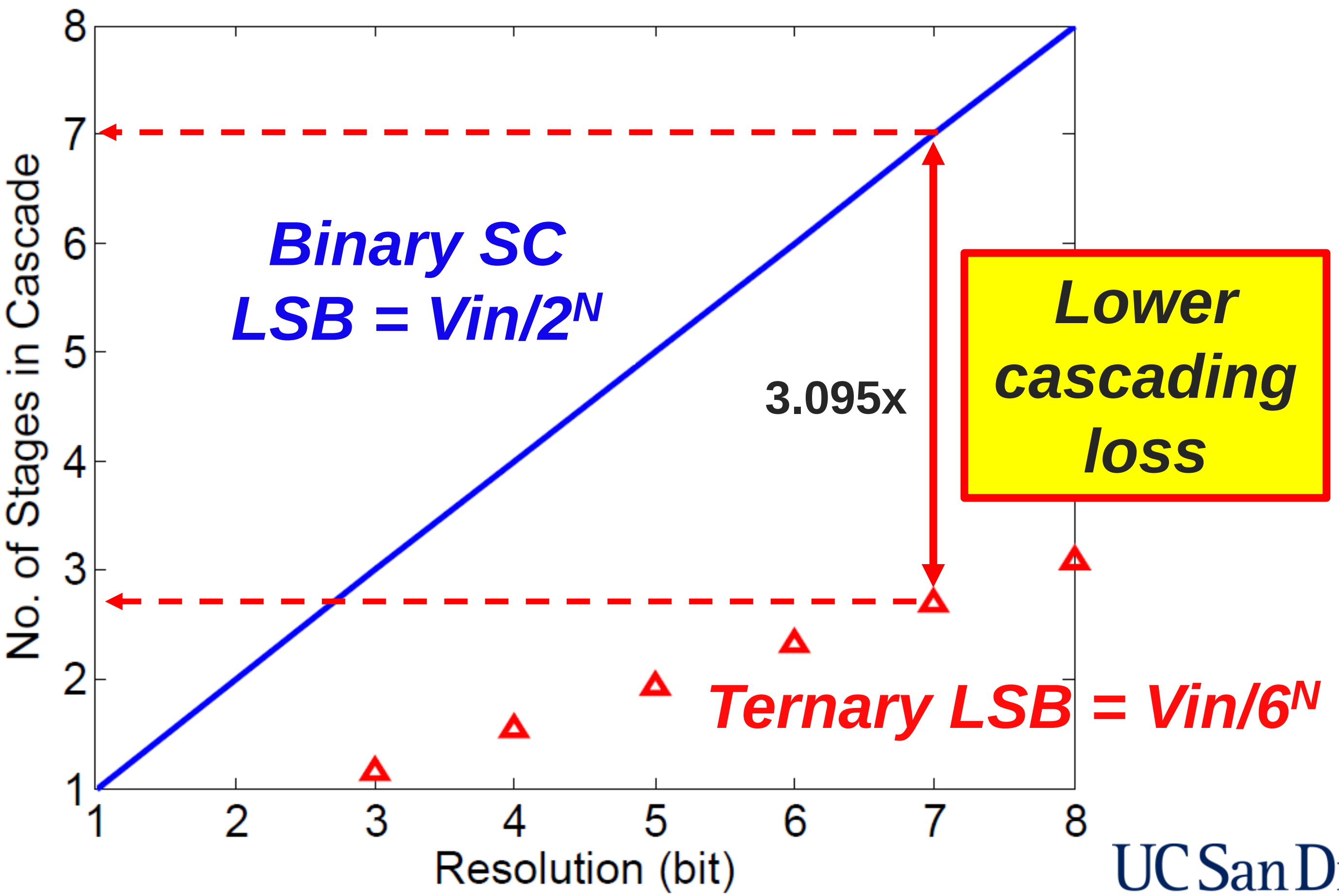


Proposed Recursive Ternary SC



Ternary SC: Minimum LSB

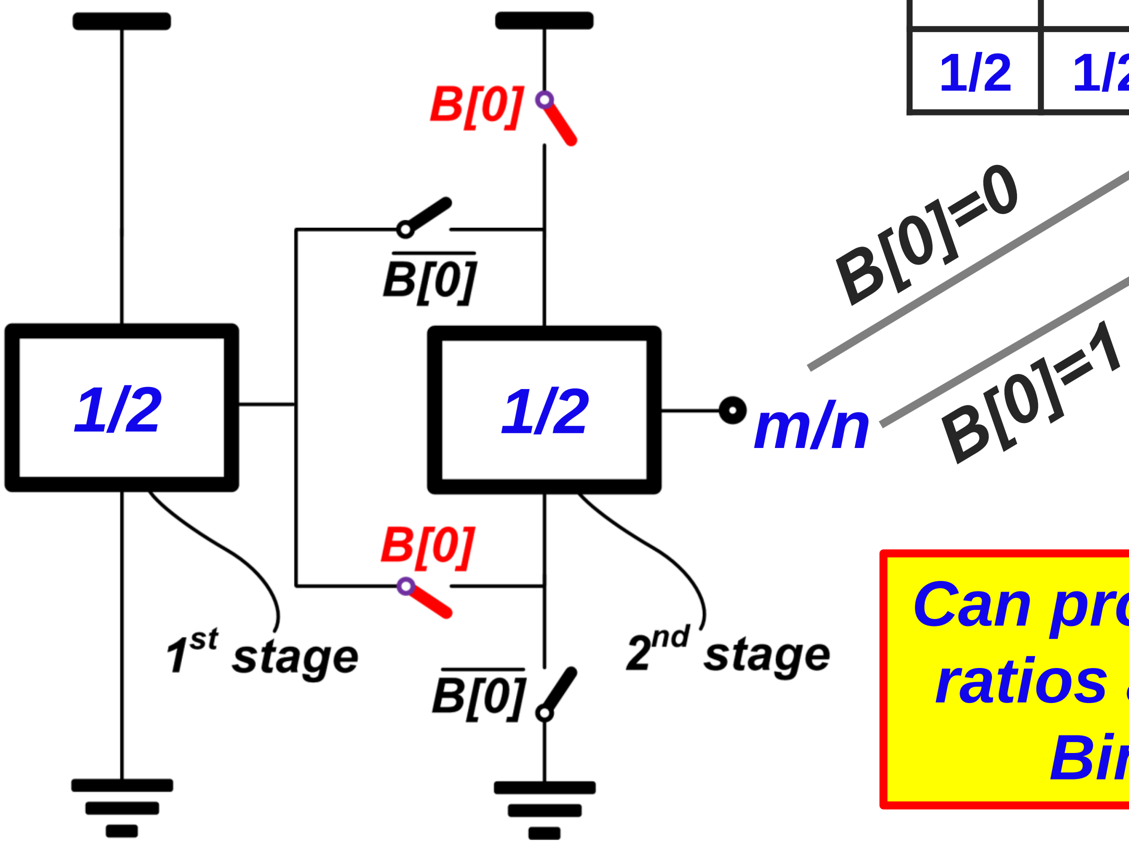
- Binary SC LSB ~ *Vin*/2^N
- Ternary SC LSB ~ *Vin*/6^N



Ternary SC: What Ratios Result

- Binary conversion modes

G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4



Can produce the same ratios as a Recursive Binary odd/2^2

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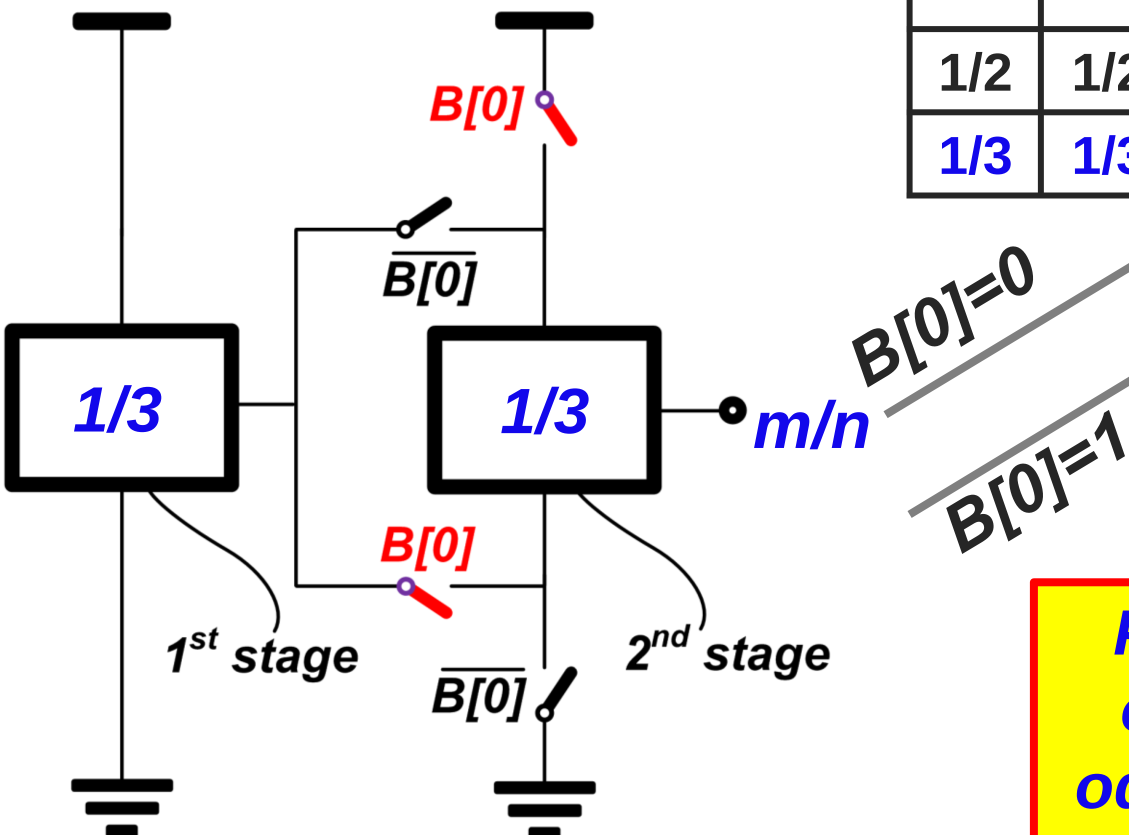
Ternary SC: What Ratios Result

- Ternary conversion modes

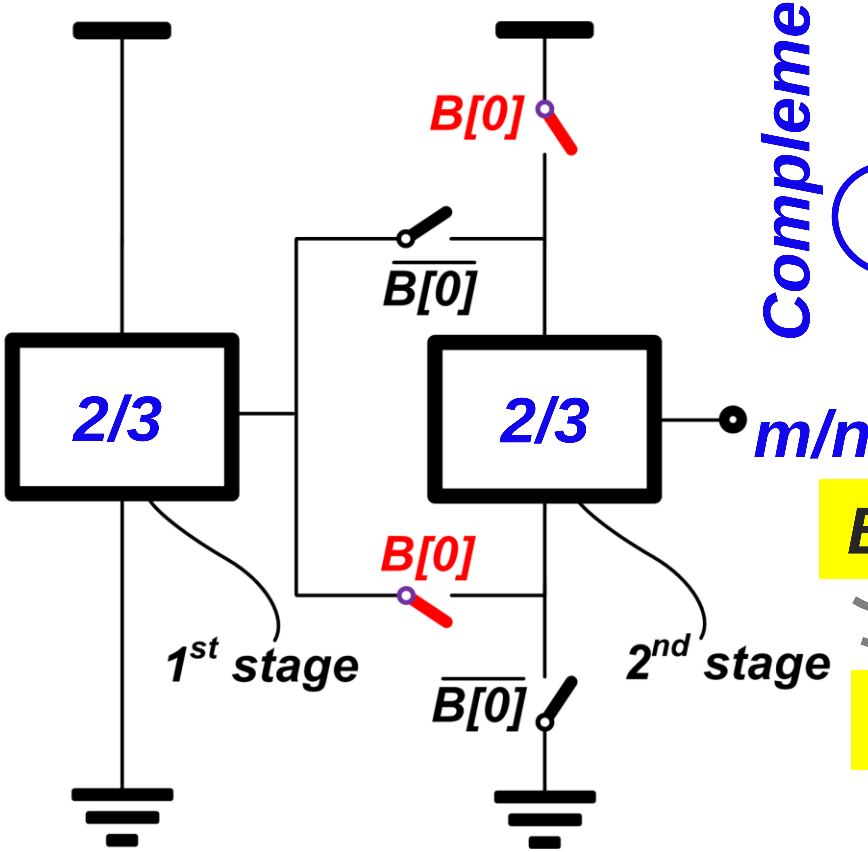
G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
1/3	1/3	1/9 5/9



Produces odd/3^2 as odd/2^2 for ½ cell gain

Ternary SC: What Ratios Result

- Ternary conversion modes



Complements

G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
1/3	1/3	1/9 5/9 (odd)
2/3	2/3	4/9 8/9

B[0]=0

B[0

- ➢Produces even/3^2
- ➢Produces the even complements

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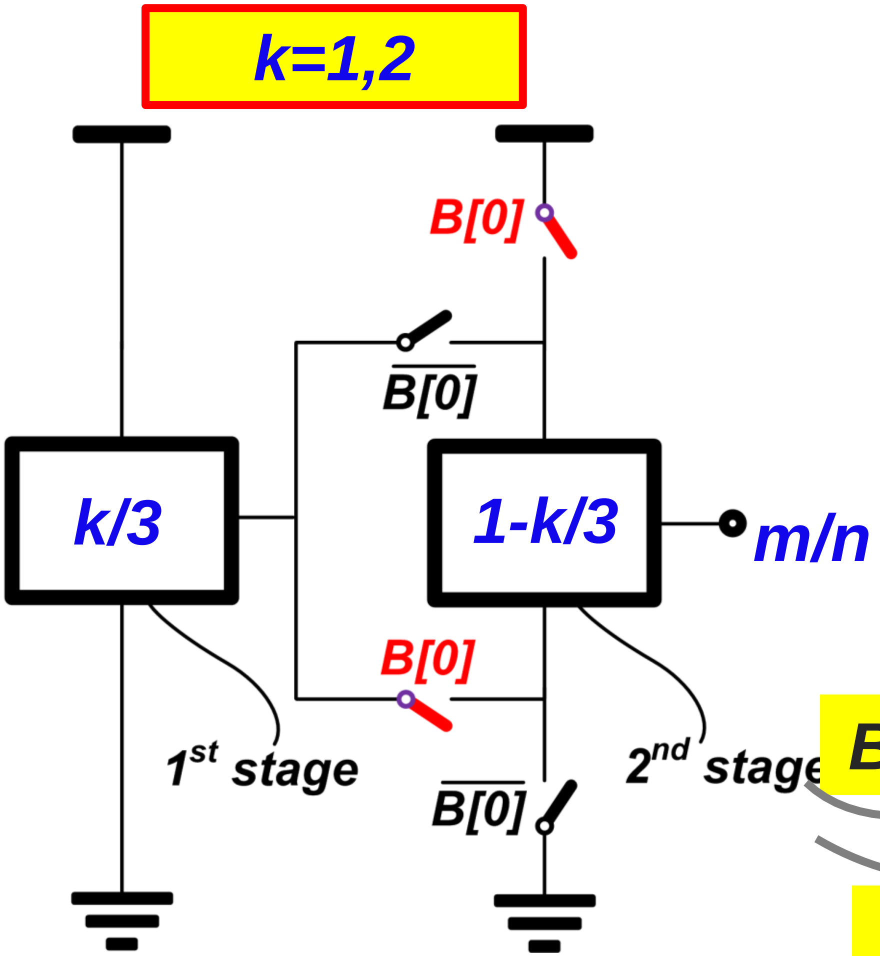
Ternary SC: What Ratios Result

- Ternary conversion modes



G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
1/3	1/3	1/9 5/9 (odd)
2/3	2/3	4/9 8/9 (even)
1/3	2/3	2/9 7/9
2/3	1/3	2/9 7/9

B[0]=0

B[0]=1

Produces complementary ratios

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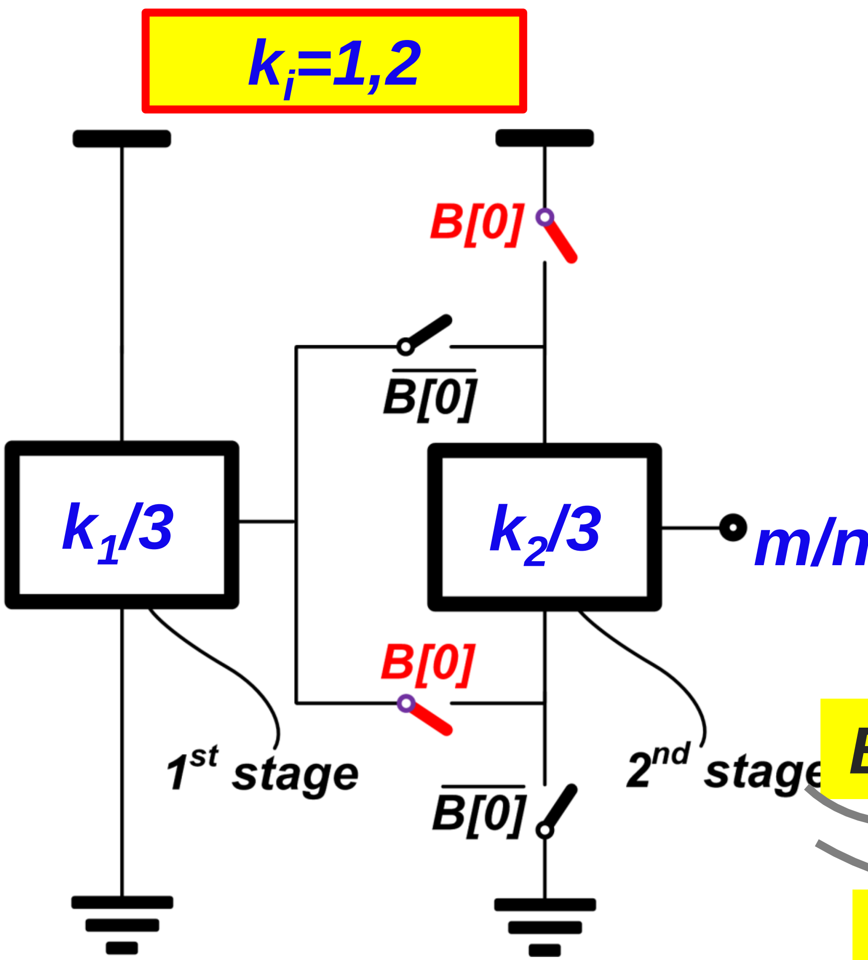
Ternary SC: What Ratios Result

- Ternary conversion modes



G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
1/3	1/3	1/9 5/9 (odd)
2/3	2/3	4/9 8/9 (even)
1/3	2/3	2/9 7/9 (complements)
2/3	1/3	2/9 7/9

B[0]=0

B[0]=1

Produces all $m/3^2$ ratios except 3/9, 6/9 (i.e. 1/3, 2/3)

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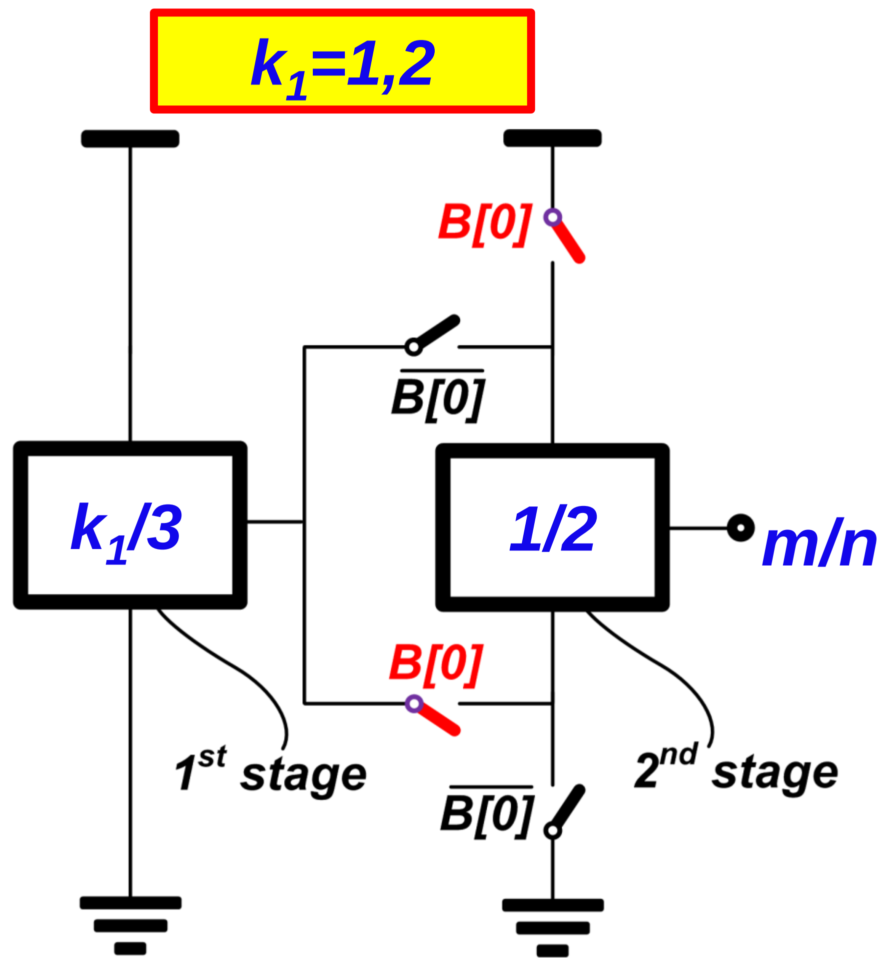
Ternary SC: What Ratios Result

- Mixing conversion modes



G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
1/3	1/3	1/9 5/9
2/3	2/3	4/9 8/9
1/3	2/3	2/9 7/9
2/3	1/3	2/9 7/9
1/3	1/2	1/6 6/9
2/3	1/2	3/9 5/6

B[0]=0

B[0]=1

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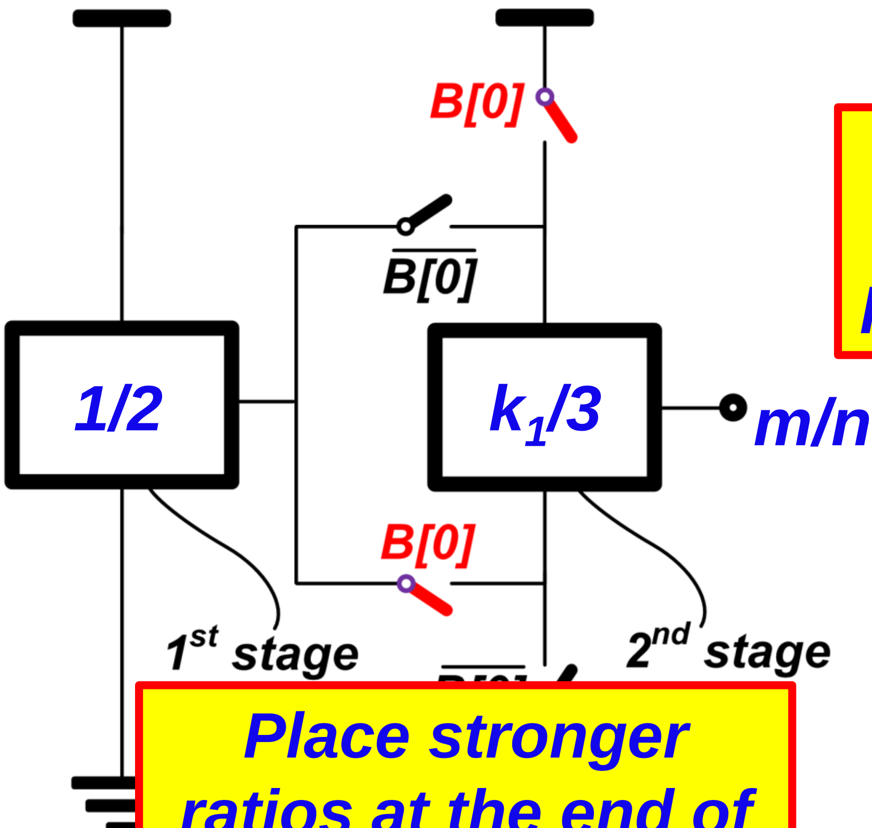
Ternary SC: What Ratios Result

- Mixing conversion modes



G1	G2	Converter Ratio m/n
1/2	1/2	1/4 3/4
[illegible]	[illegible]	[illegible]/9 5/9
[illegible]	[illegible]	[illegible]/9 8/9
[illegible]	[illegible]	[illegible]/9 7/9
2/3	1/3	[illegible]
1/3	1/2	1/6 6/9
2/3	1/2	3/9 5/6
1/2	1/3	1/6 6/9
1/2	2/3	3/9 5/6

Weak ratios, 1/3 handles larger currents

Higher loss

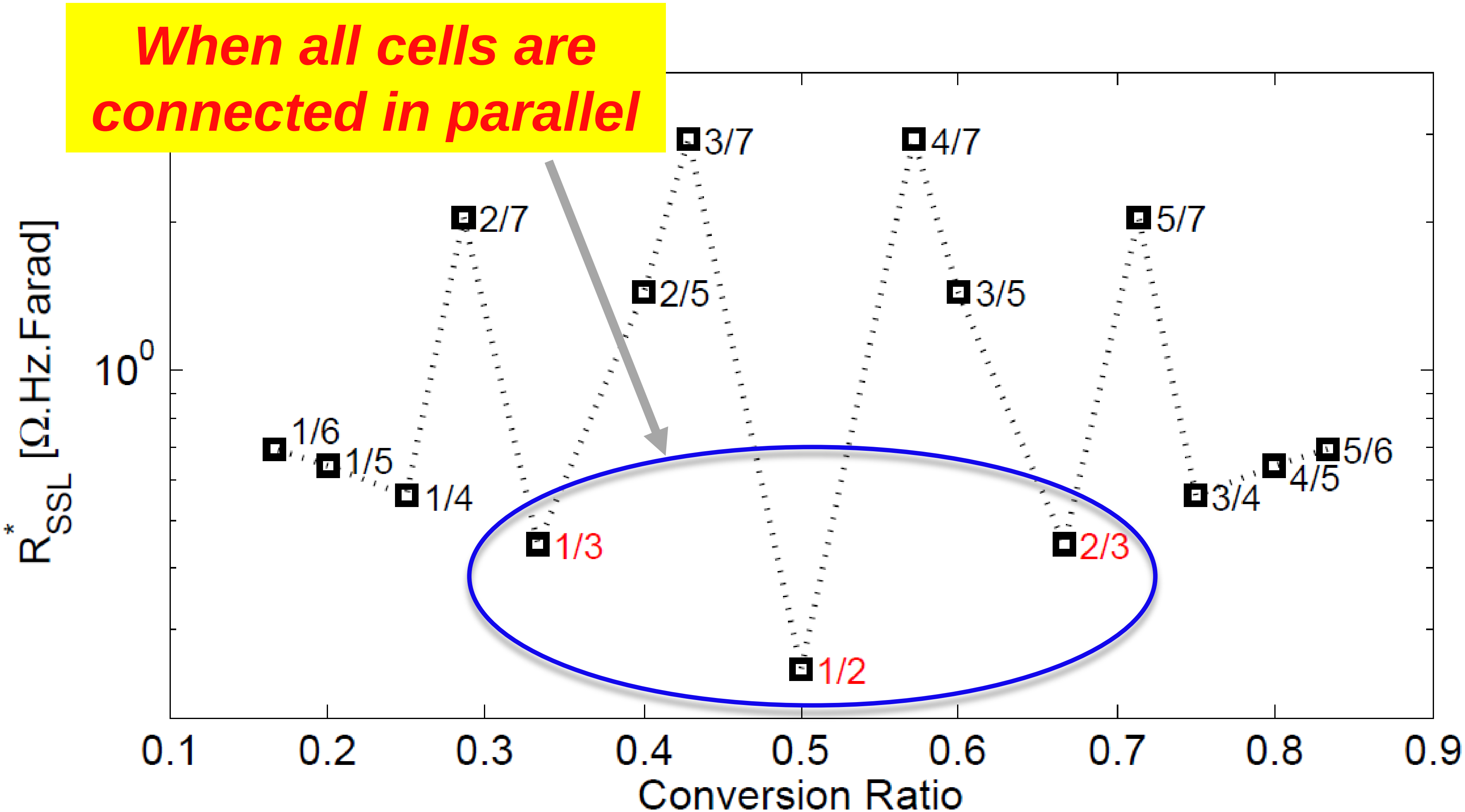
Place stronger ratios at the end of the cascade

B[0]=0

B[0]=1

Proposed Recursive Ternary SC

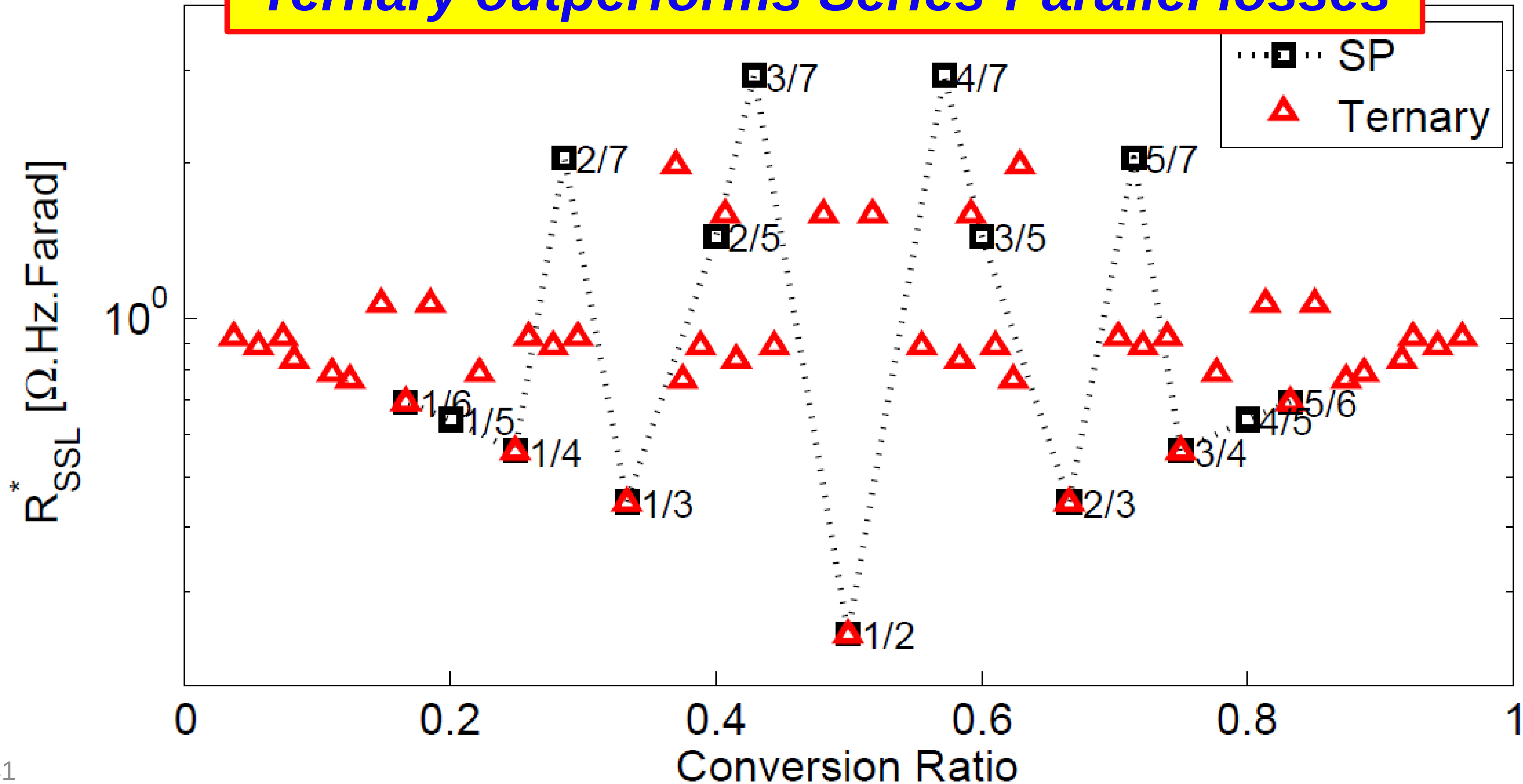
- Recursive Ternary incorporates the 3-Ratio Series-Parallel minimal charge sharing loss.



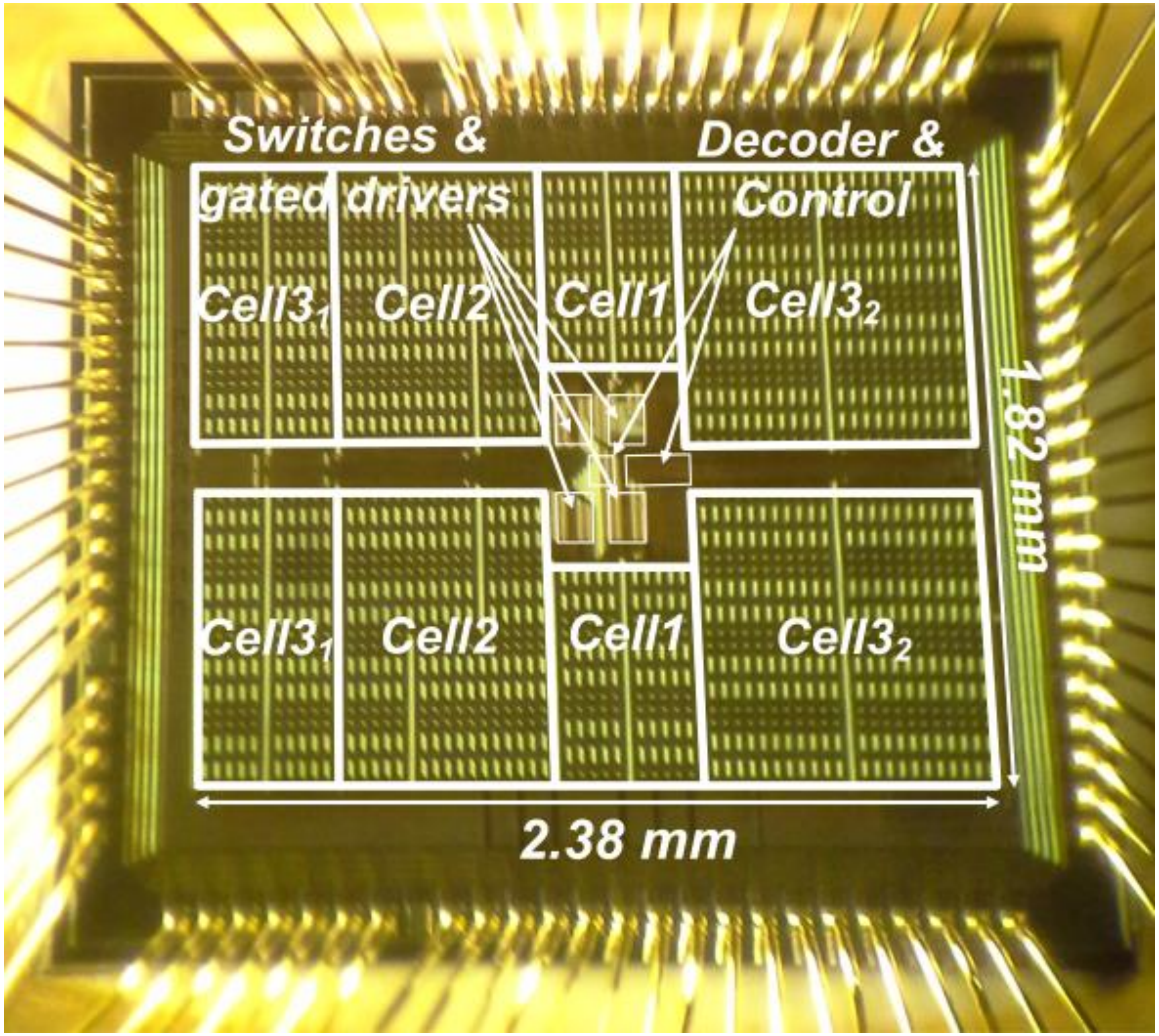
Proposed Recursive Ternary SC

- Recursive Ternary *inherits* the superior performance of the 3-Ratio Series-Parallel topology

Ternary outperforms Series-Parallel losses



Recursive Ternary SC Prototype

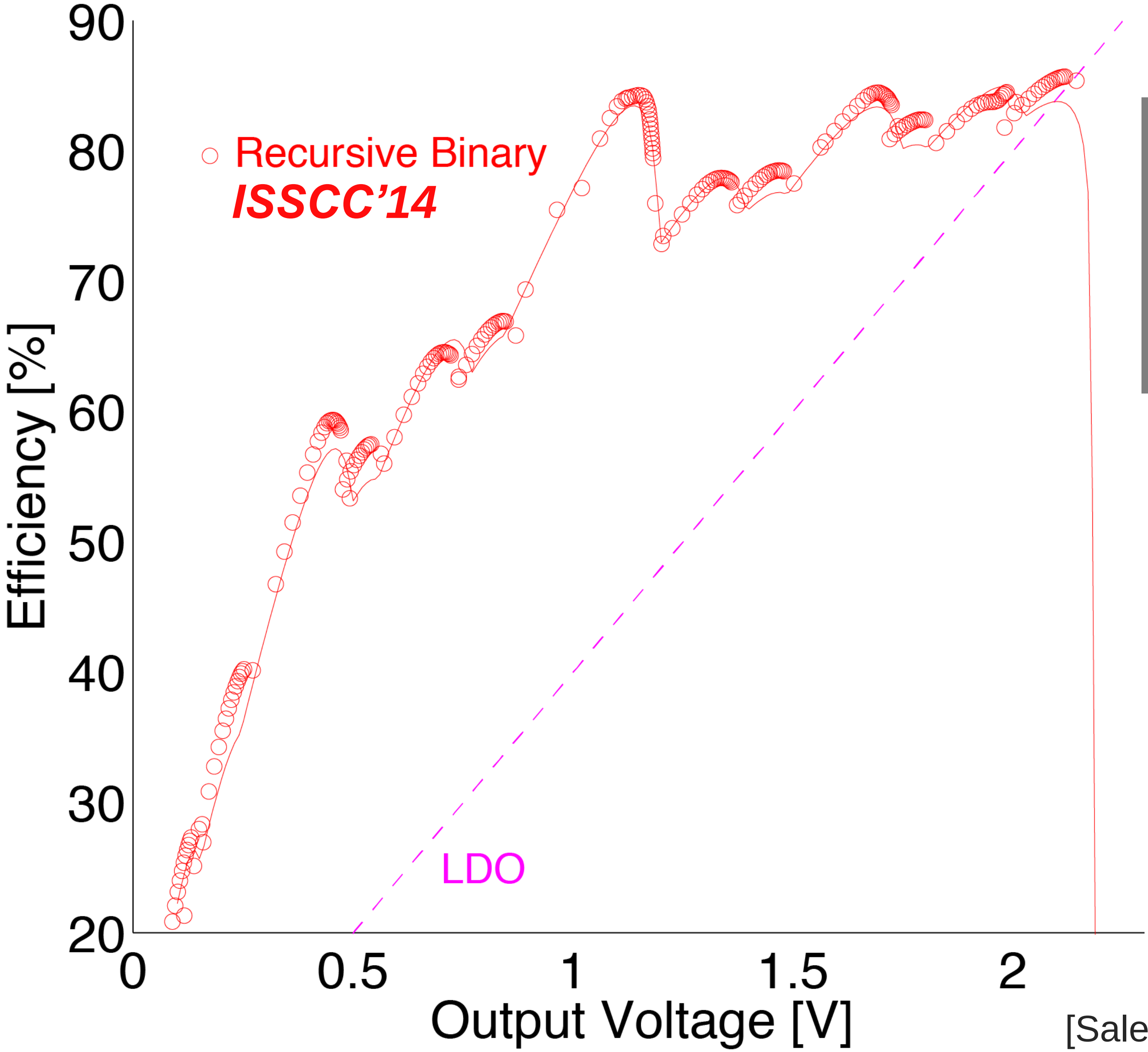


Tech.	0.25μm
Topology	3-stage RT
# of Ratios	45
Area	$4.3mm^2$
Cap.	2.8nF

- ***Cells are binary sized***
- ***Bottom row is 0^o phase***
- ***Top is 180^o***

[Salem & Mercier, CICC 2014]

Measured Efficiency vs. V_{out}



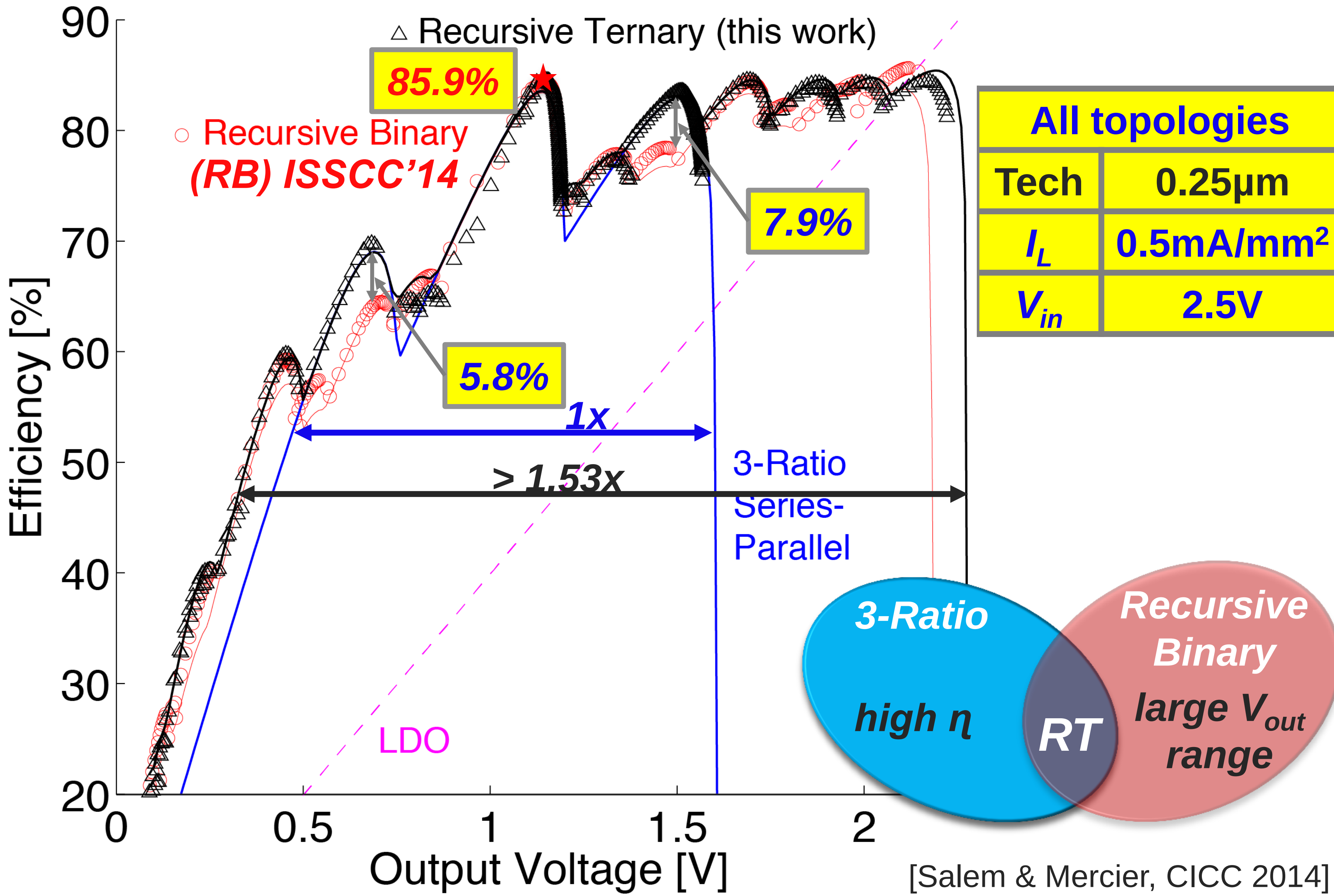
All topologies	
Tech	0.25µm
I_L	0.5mA/mm²
V_{in}	2.5V

Recursive Binary

large V_{out} range

[Salem & Mercier, CICC 2014]

Measured Efficiency vs. V_{out}



All topologies	
Tech	0.25µm
I_L	0.5mA/mm²
V_{in}	2.5V

[Salem & Mercier, CICC 2014]

Conclusions

- Miniaturized & efficient power converters are required for next-generation mobile and energy harvesting applications
- Switched-capacitors offer a route towards miniaturized efficiency
- New modular topologies are presented that achieve a large # of conversion ratios while maintaining the performance benefits of simpler topologies
  - Recursive binary implementation: 15-ratios, 85% peak efficiency, 0.2-2.2V range
  - Recursive ternary implementation: 45-ratios, 86% peak efficiency, 0.2-2.2V range
    - Combines the benefit of RB and 3-ratio SP for best-in-class efficiency

Acknowledgments:

- *Energy harvesting*: Saurav Bandyopadhyay, Anantha Chandrakasan, Konstantina Stankovic, Andrew Lysaght (MIT/Harvard/MGH/MEEI), SRC IFC/C2S2
- *Switched capacitor DC-DC converters*: Loai Salem (UCSD)