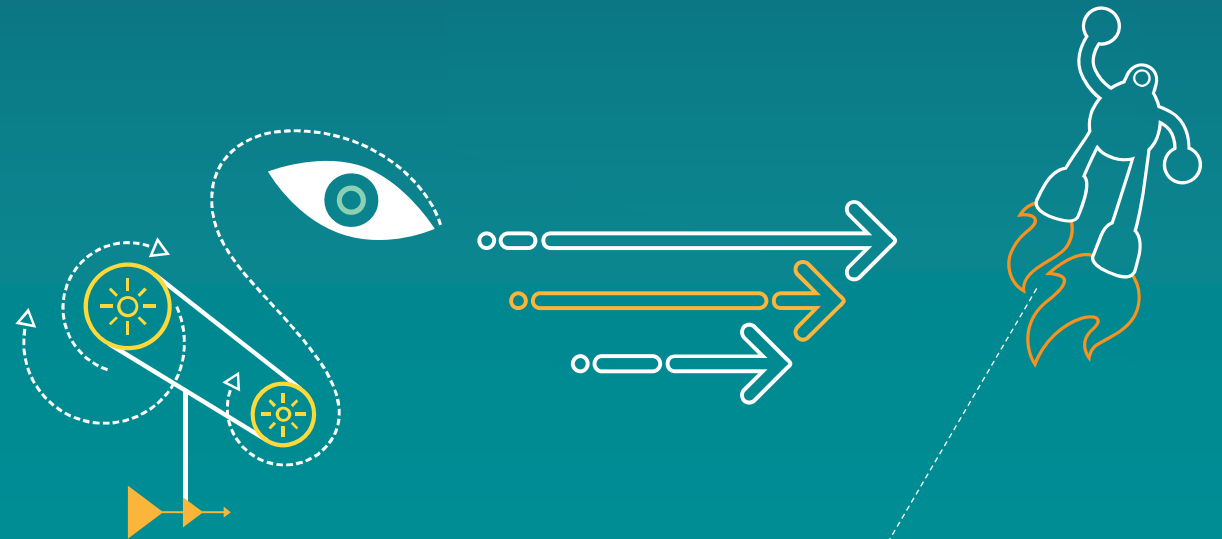


Francesco Carobolante
Vice President Engineering
Qualcomm Technologies, Inc.

Power Supply on Chip: from R&D to commercial products



PwrSoC 2014
Plenary Session



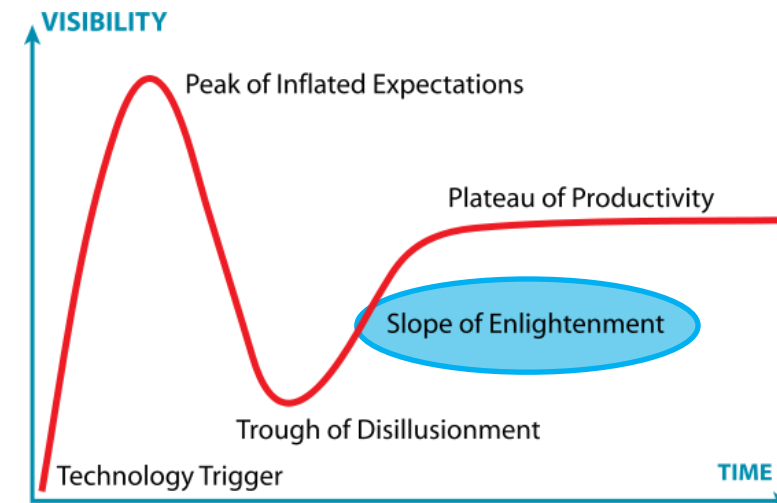
Agenda

Where are we in the technology cycle?

- Applications driving Power Integration
- Why Power Supply on Chip is inevitable
- System constraints and Technology trajectory
- Challenges and opportunities

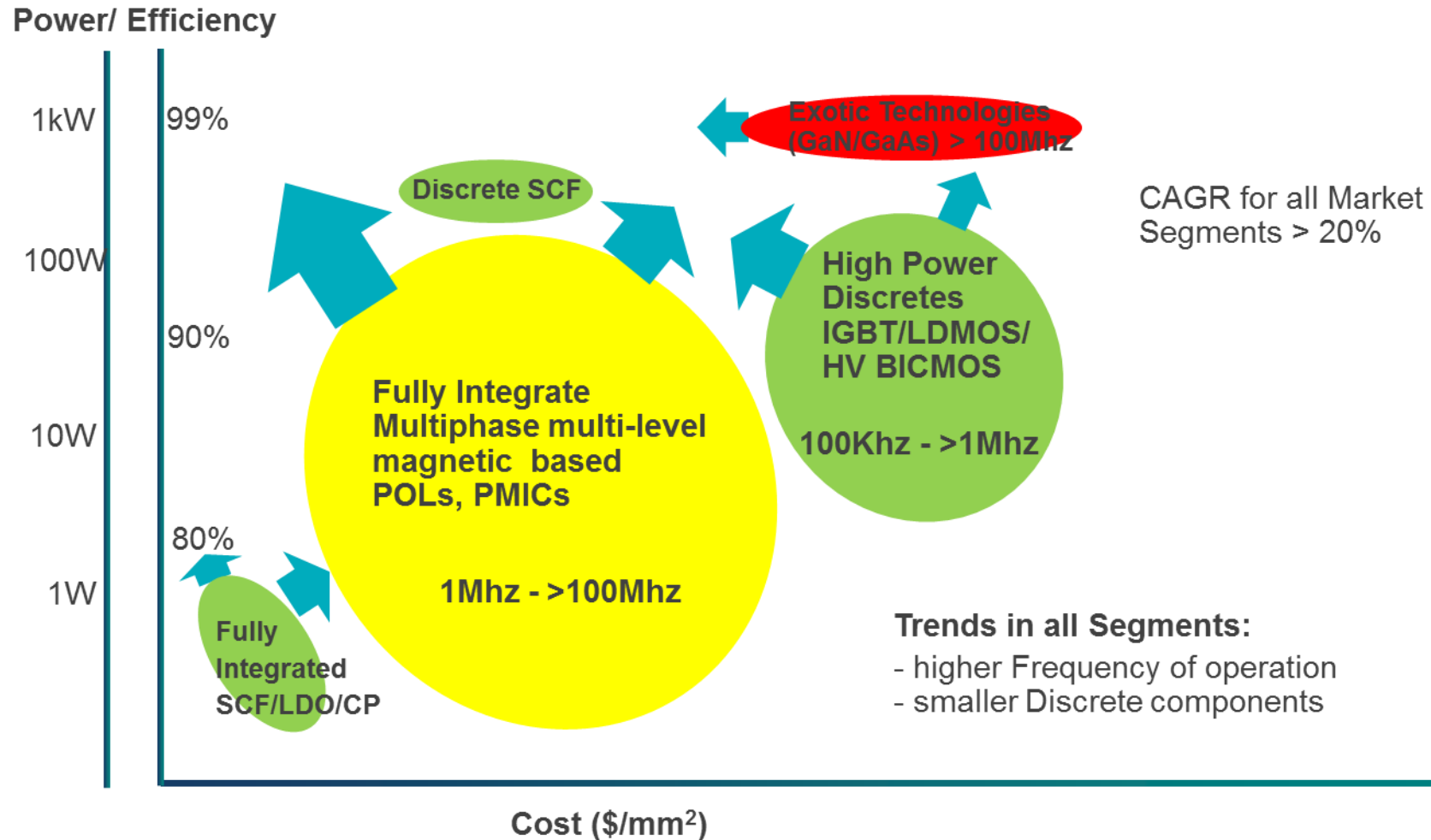
- Contributors:

- J. Doyle
- M. Erturk
- J. Duncan



VR Technology Landscape

Size ~ TAM, Arrows indicate trends (their size represents effort and investment)



Power Supply on Chip is already a high volume product!

So, what is next?

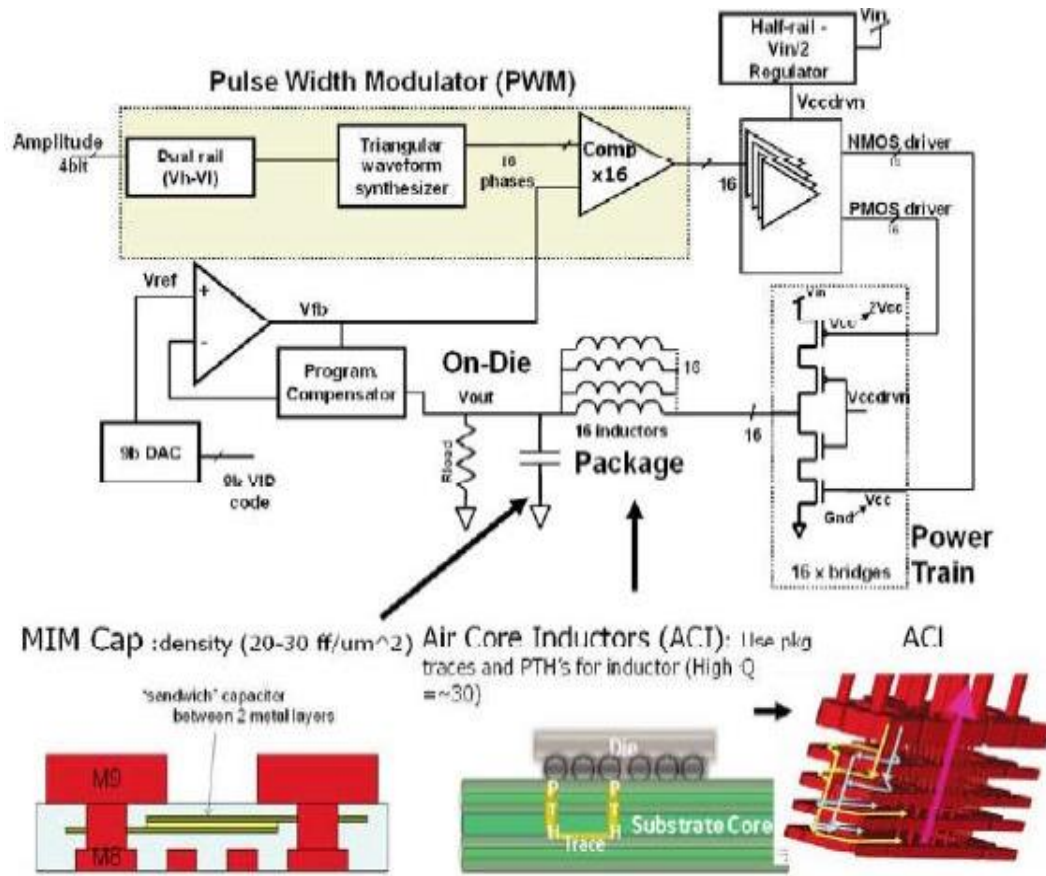


Figure 5.9.3: FIVR controller architecture.

ISSCC 2014 / SESSION 5 / PROCESSORS / 5.9

5.9 Haswell: A Family of IA 22nm Processors

Nasser Kurd, Muntaquim Chowdhury, Edward Burton, Thomas P. Thomas, Christopher Mozak, Brent Boswell, Manoj Lal, Anant Deval, Jonathan Douglas, Mahmoud Elassal, Ankireddy Nalamalpu, Timothy M. Wilson, Matthew Merten, Srinivas Chennupaty, Wilfred Gomes, Rajesh Kumar

Intel, Hillsboro, OR

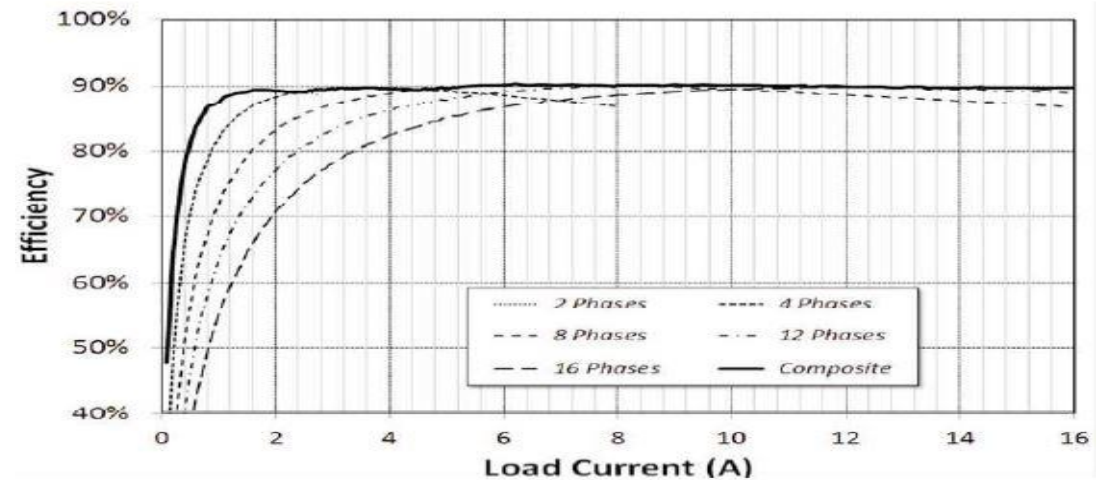


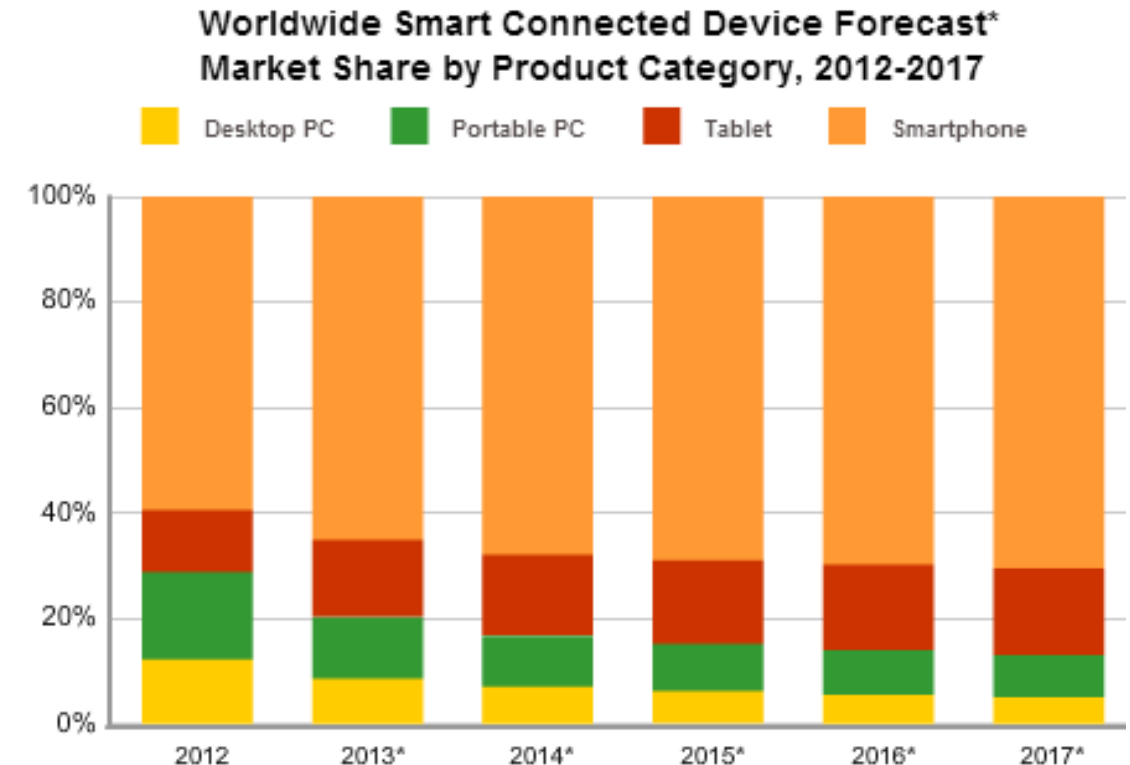
Figure 5.9.4: Measured efficiency for two, four, and eight phases active on a core voltage domain ($V_{CCIN} = 1.7V$, $V_{out} = 1.05V$).

Applications driving Power Integration

- Energy harvesting and Internet of Things (IoT)
 - Compact, low power, heterogeneous integration
- High Performance Computing
 - Performance and efficiency constraints
- Mobile devices
 - Limited space, highest performance, efficiency

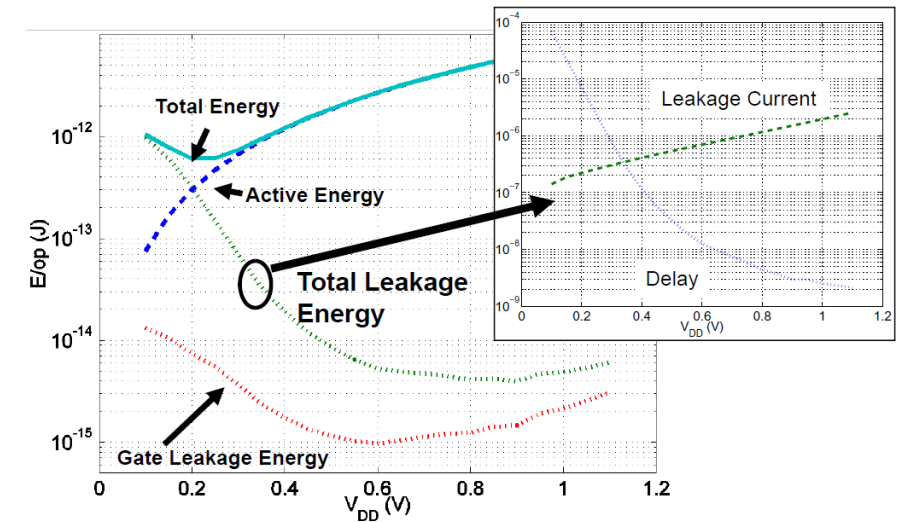


**87% Of Connected Devices
Sales By 2017 Will Be Tablets
And Smartphones**



Motivations

- Thinner, smaller, more “stuff” in the same volume... yet area occupied by power management is NOT a key driver (although it is the most “visible” benefit)
- Efficiency is job #1, due to battery limitations (total energy available) as well as thermal budget (max dissipation).
- From power management to energy management: tens to hundreds of power domains, each optimized. The key F.O.M. is $\sum_{i=0}^N \int V_i I_i dt$



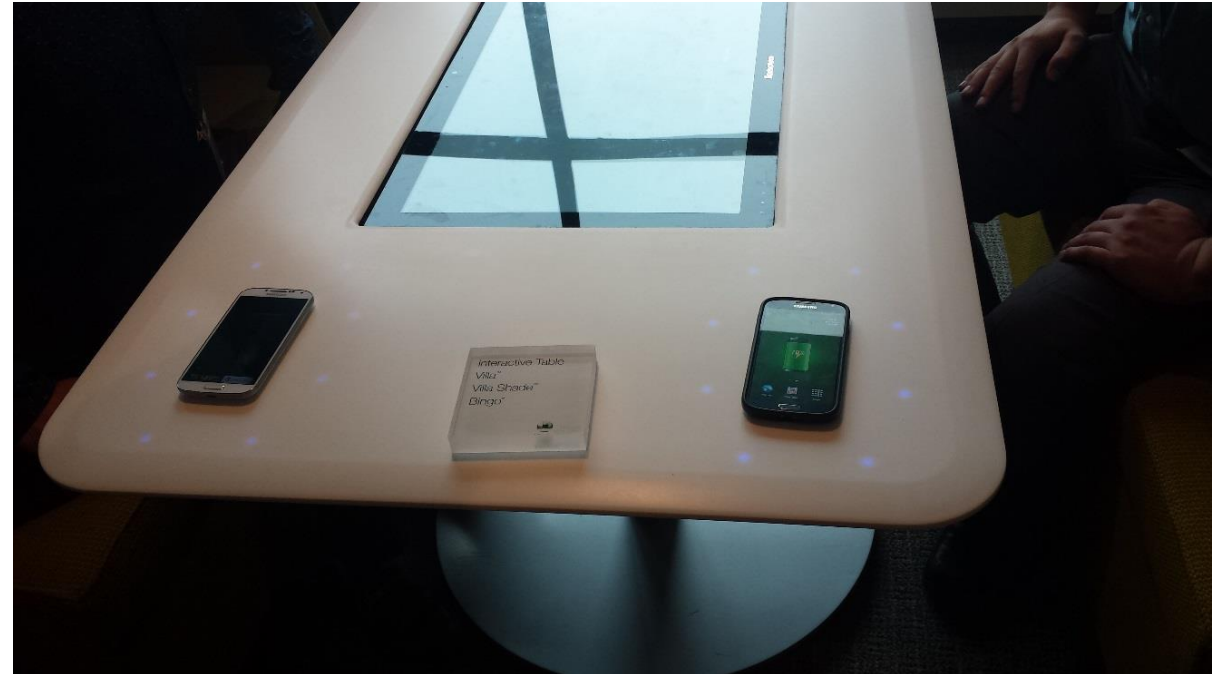
A. Chandrakasan, MIT

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

Your mobile device is... your PC

And it has to service your every need – all day long

- Thermal envelope is the limiting factor to processors' performance, especially in the upcoming “wireless docking” use case.



Your mobile device is... your Digital Persona – and a lot more!

Integration of every possible sensor, radio link, DSP...

- Your digital assistant
- Your health advisor – 24/7
- Your data: in the cloud or in your personal cloud?



QUALCOMM
TRICORDER X PRIZE

...it will only get worse!

Wearables are an even bigger challenge

- Size matters!
 - A conductor parasitic elements (L, R) are proportional to length and increase as cross-section is reduced
 - Their impact is dramatically affected by operating frequency (skin effect, proximity effects, Eddy currents and EMI mitigations become dominant)

Why did I say it was inevitable?



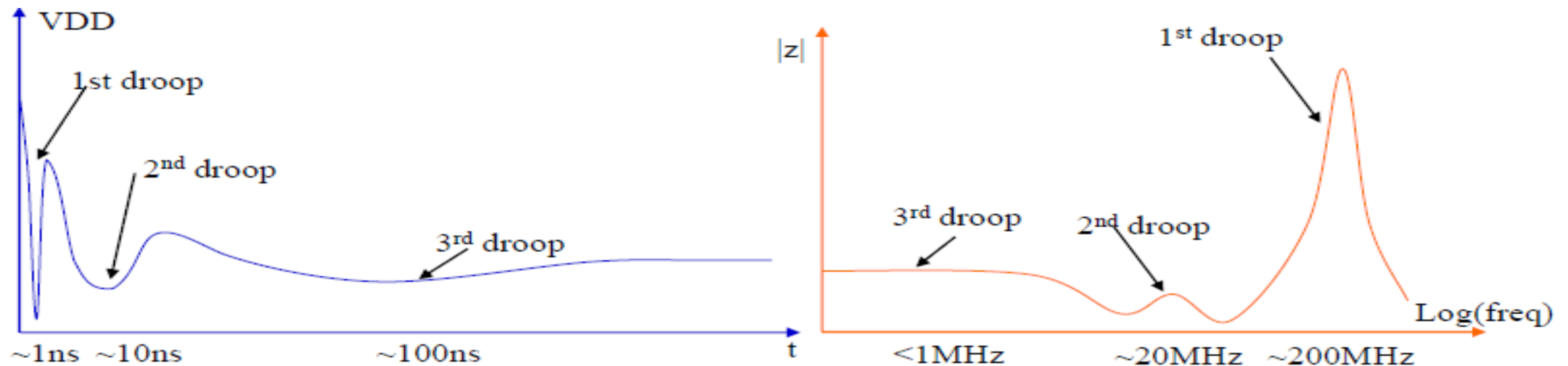
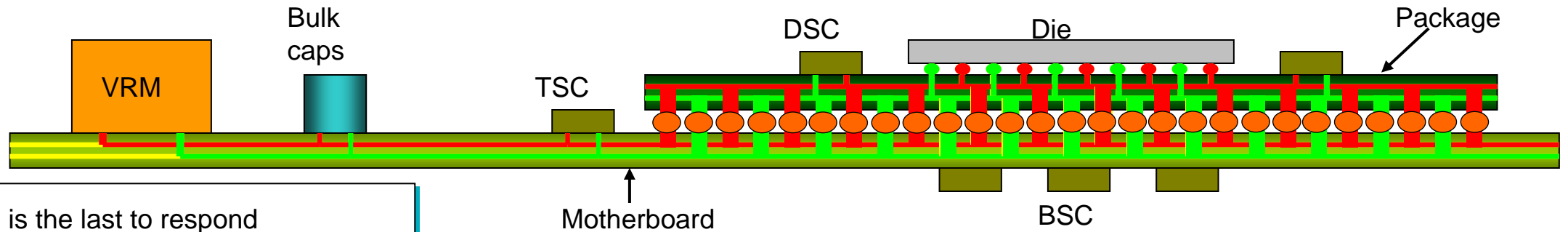
Power Delivery Network (PDN)

Bulk caps come third

Package caps are the first to respond

The VRM is the last to respond

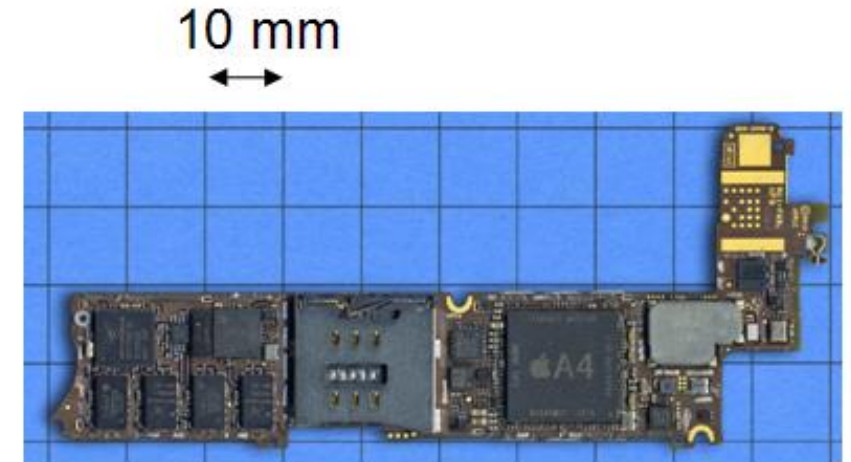
MB caps are the second to respond



Power Delivery Network (PDN) requirements

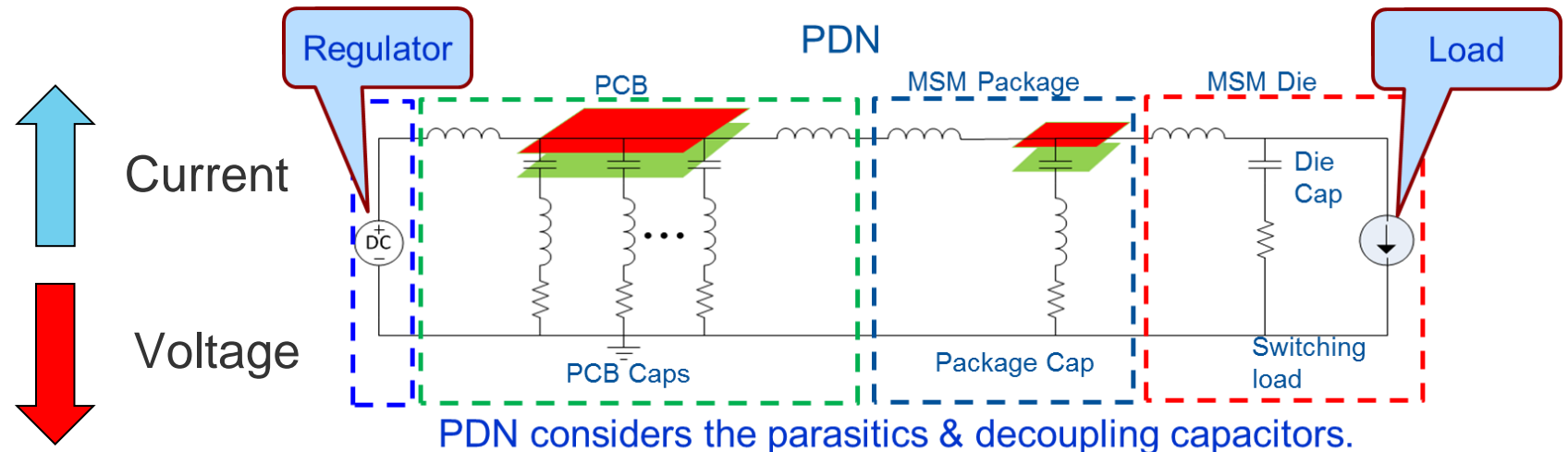
If all that happened were “half the voltage and twice the current”...

- PC Boards are often skinny and long, making it difficult to optimize routing
- As performance of processors continue to increase, current increases and voltage decreases. The impedance of the PDN must decrease in order to keep the same performance



...we would need to make the impedance $\frac{1}{4}$!

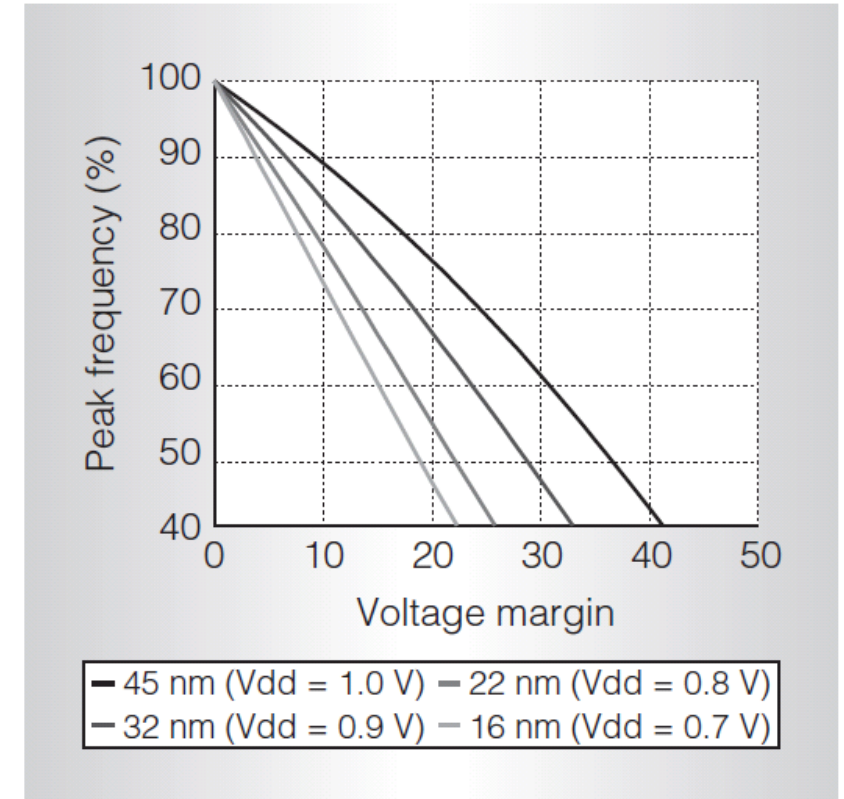
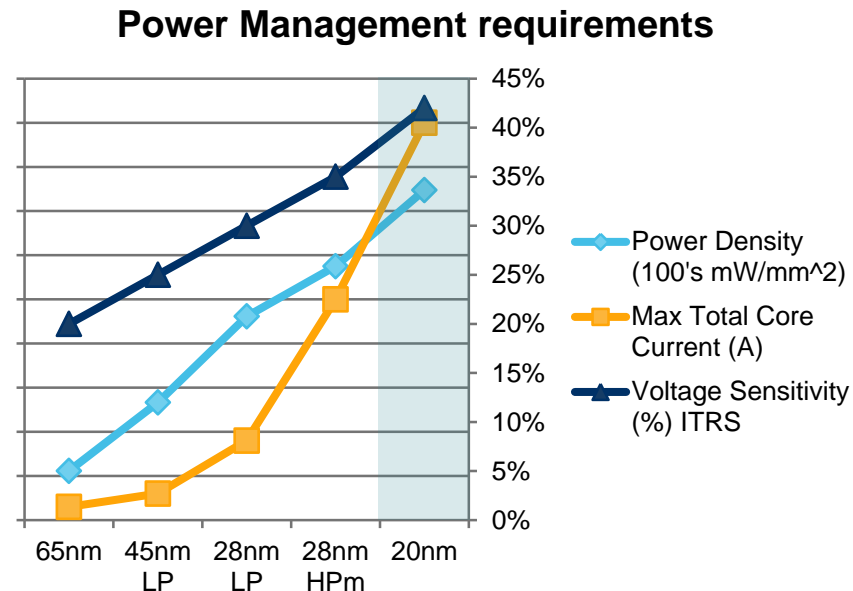
But...



It gets worse:

Voltage sensitivity of the silicon process increases

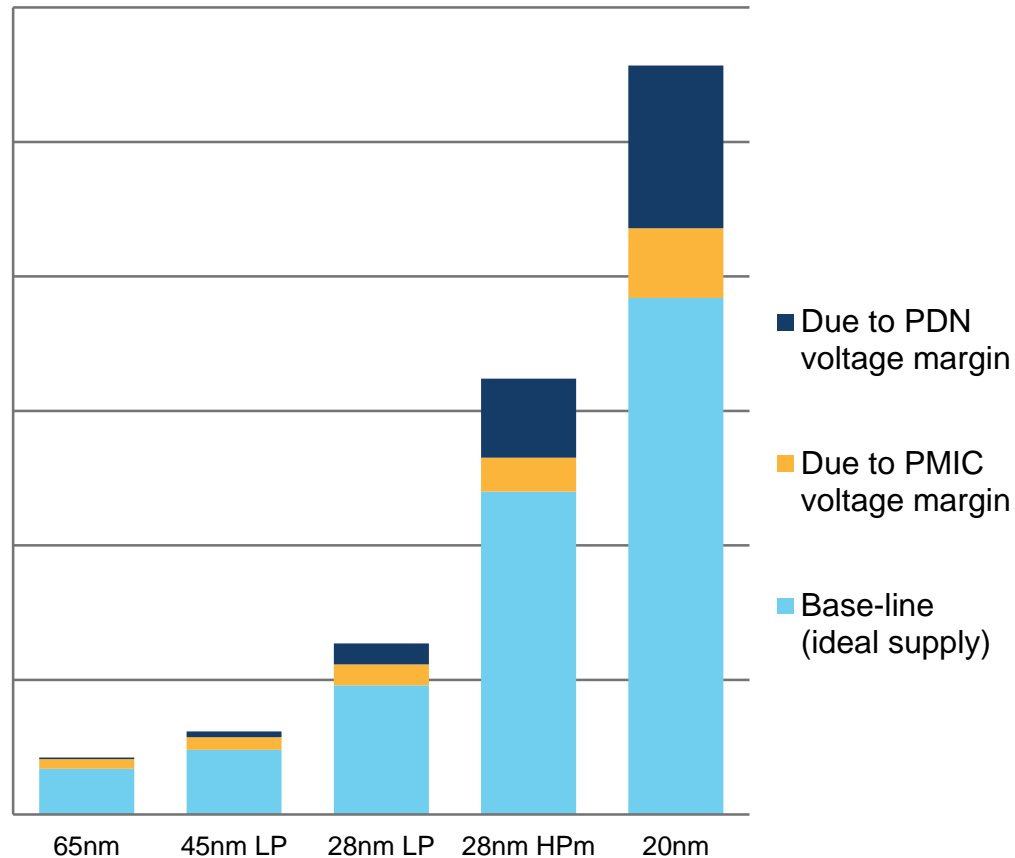
- V_t is not scaling with supply voltage reductions. As a result, while at 45nm a 10% supply margin caused approx. 10% reduction in peak operating frequency (vs. an ideal supply), the same voltage margin may cause about 20% reduction in peak operating frequency at 28nm and 32% at 22nm
- Furthermore, due to the size shrinkage of transistors, power density increases with any new process generation.



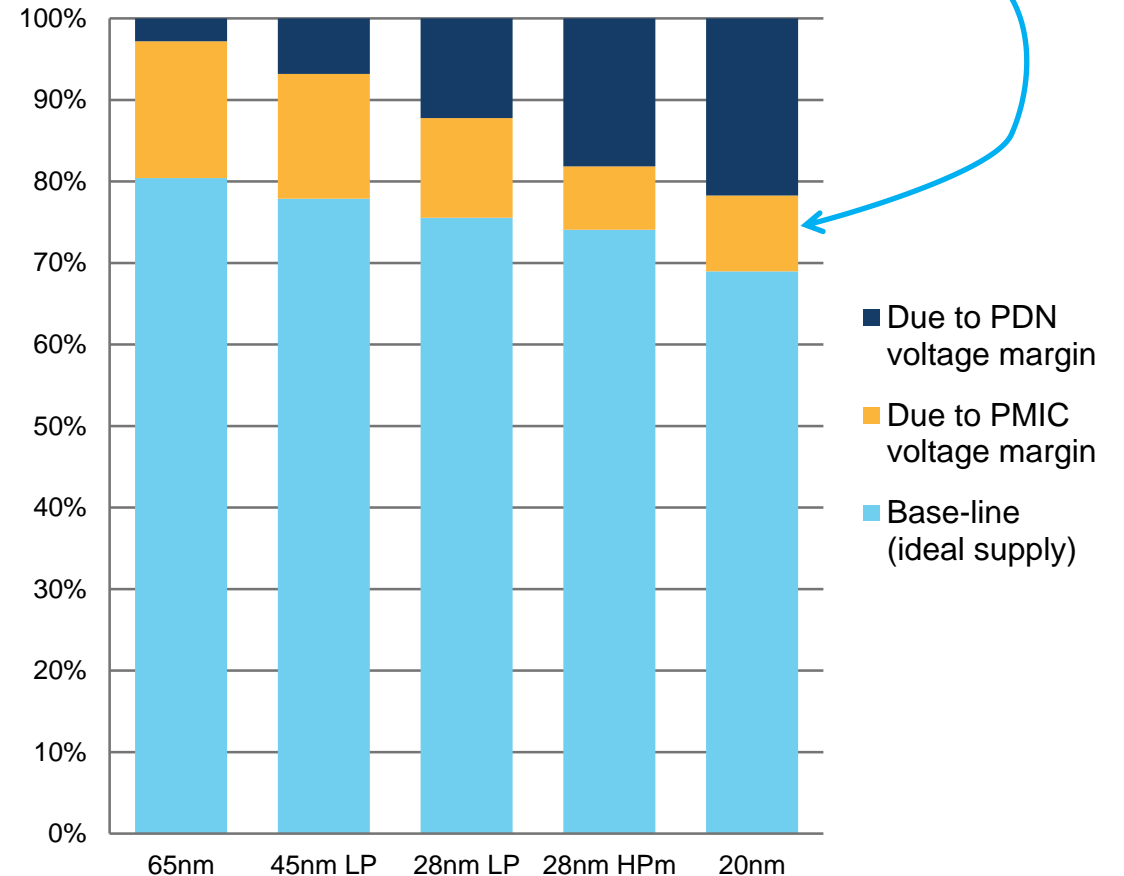
Inefficiency grows due to lower load impedance and fast transients

Gains achievable from Power Management “outside” the package are limited

Power dissipation in processors (W)



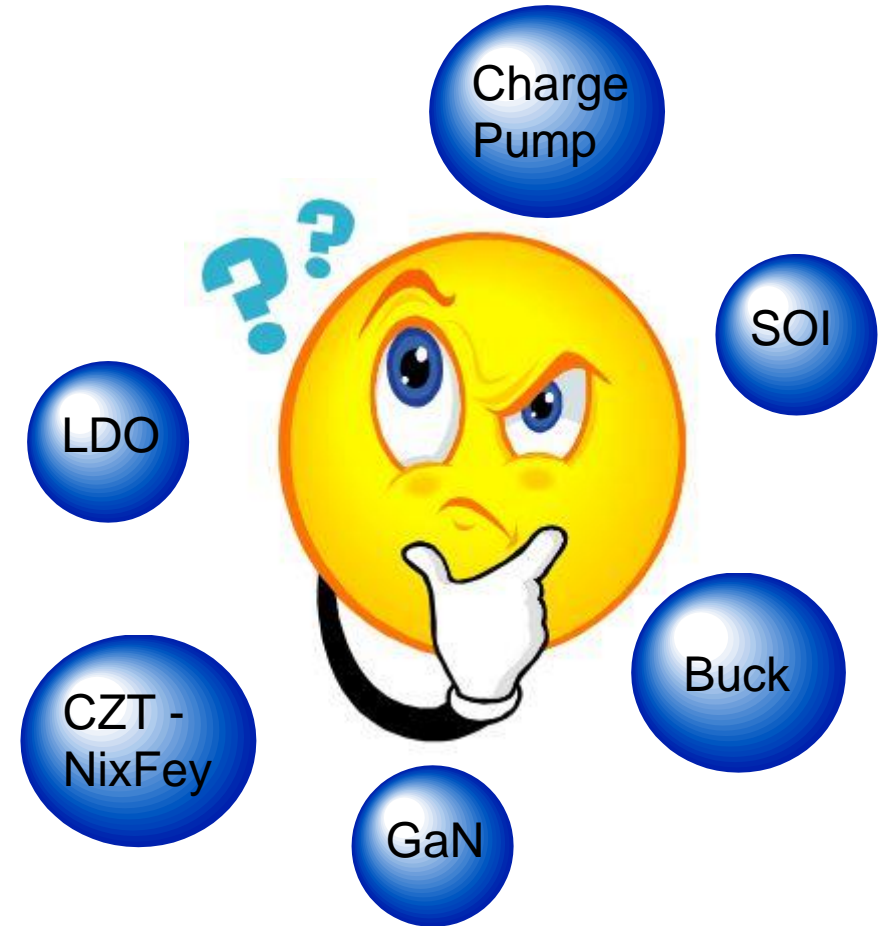
Processors Power dissipation



Key technologies

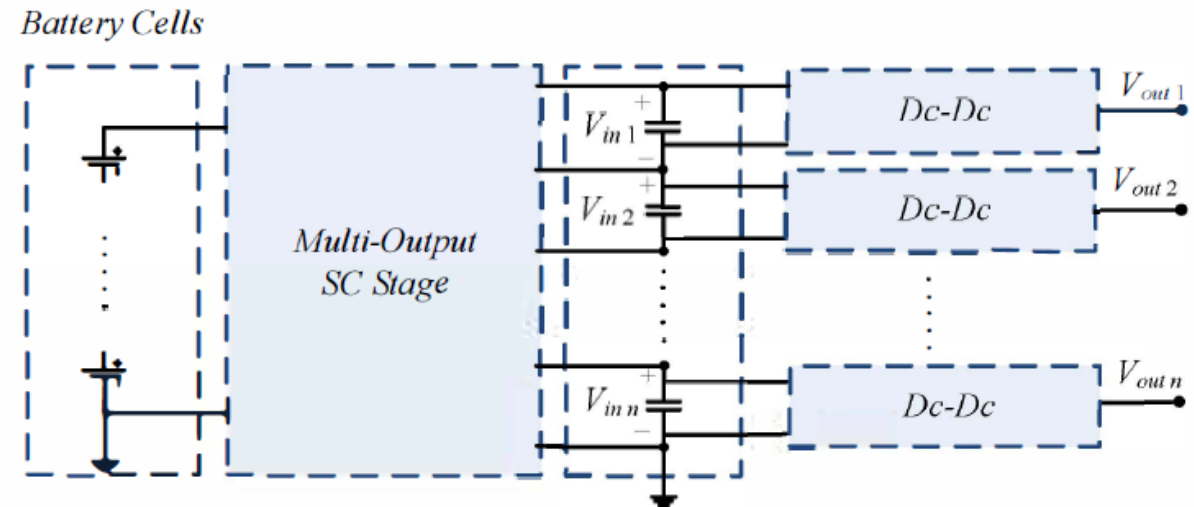
So many choices, so little time

- Which DC-DC Converter architecture?
- Which Control scheme?
- Which Process technology?
- Which Passive Components?
- Which Package solution?



Which DC-DC Converter architecture?

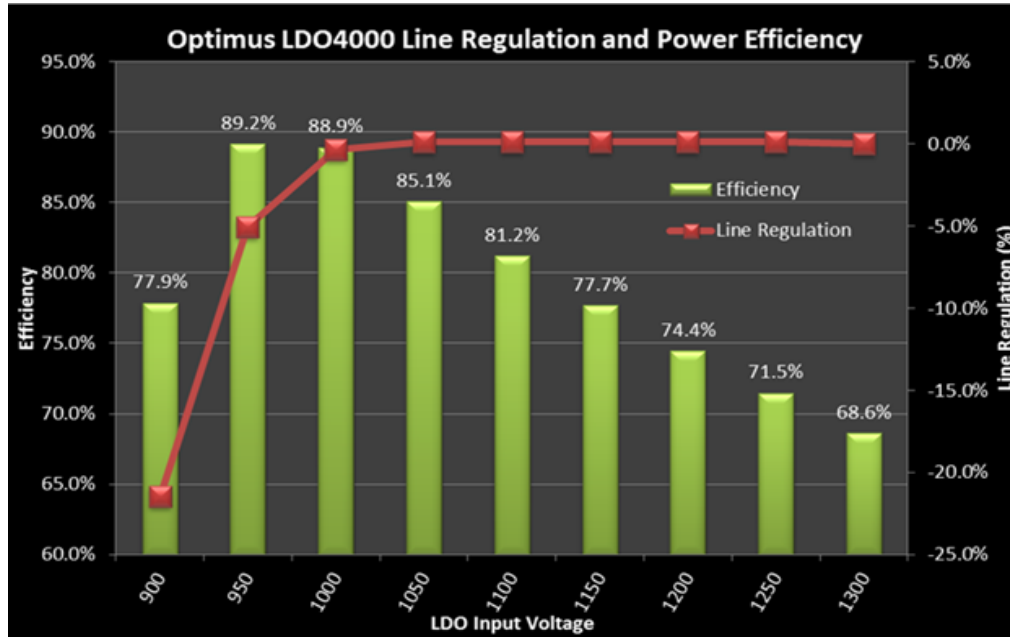
- LDO – can be very fast in deep sub-micron!
- Switch-Capacitor Charge Pump has higher energy density, but 12% output voltage granularity requires 16 switches in series → good for low power, cell-level embedded power management, or for coarse supply regulation
- Buck: in order to integrate and reduce inductor size, voltage has to go down.
- Q in high frequency inductors is ~10's, while capacitors can have 10x or higher Q
- Combination of capacitors and inductors may achieve the appropriate compromise
- Fine-grain power management – a combination of all of the above techniques!



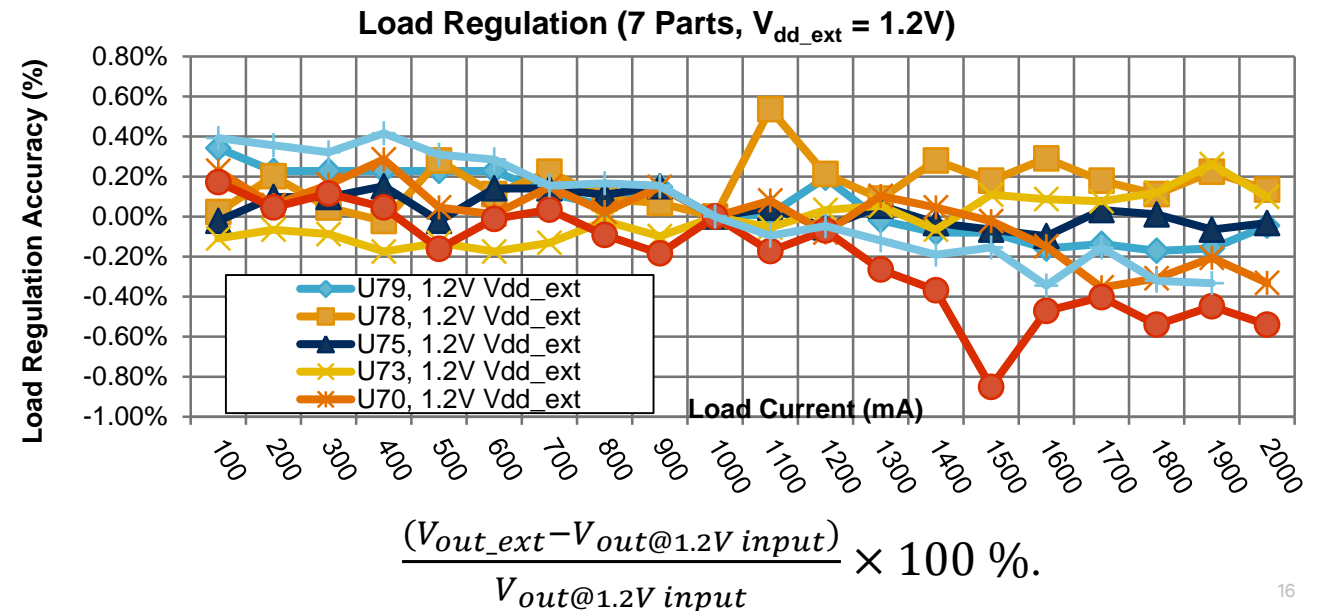
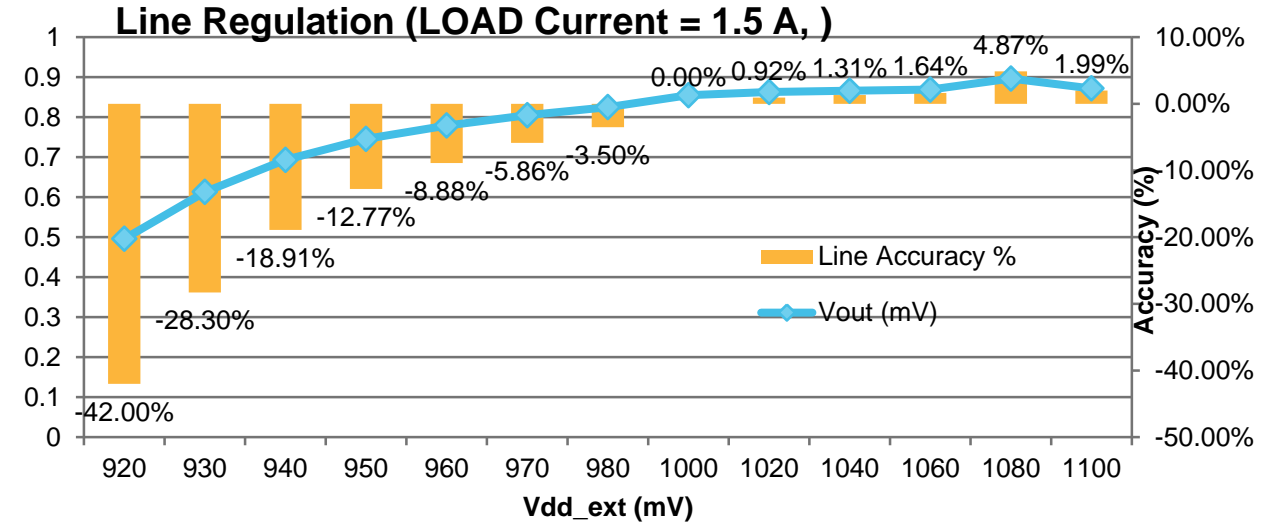
Aleksandar Radic et al., "High-Power Density Hybrid Converter Topologies for Low-Power Dc-Dc SMPS", 2014 International Power Electronics Conference

Performance of an LDO in 20nm

Output Voltage: 0.9V – Load: 2 Amp

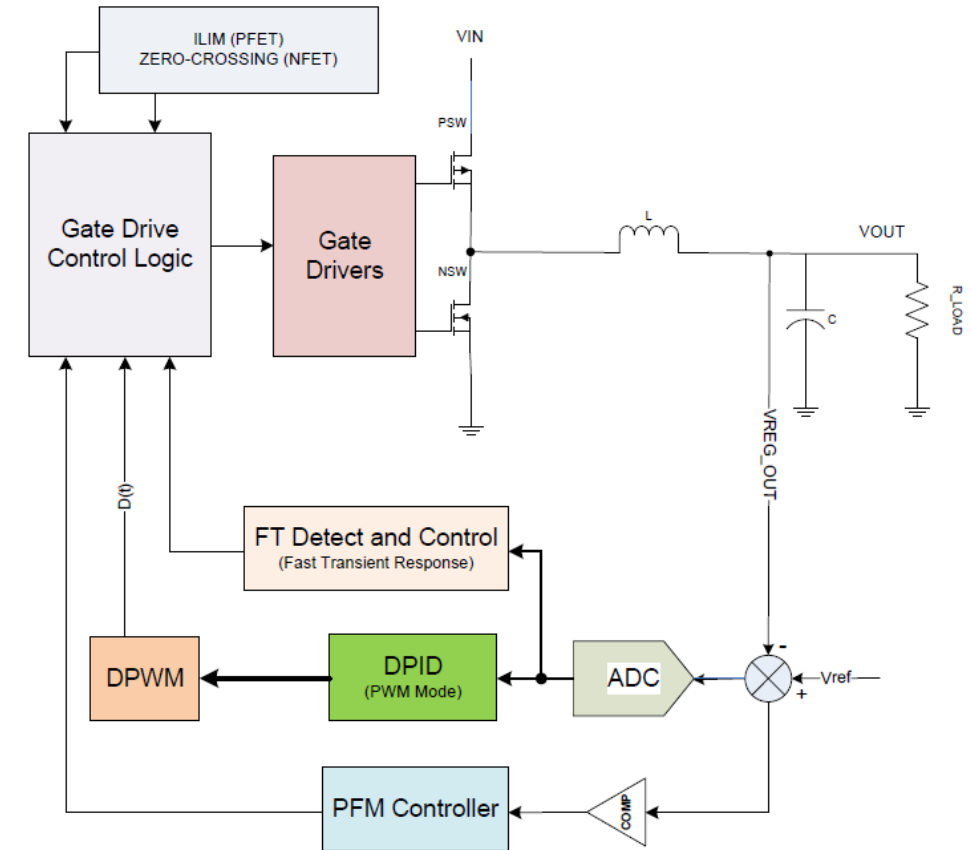
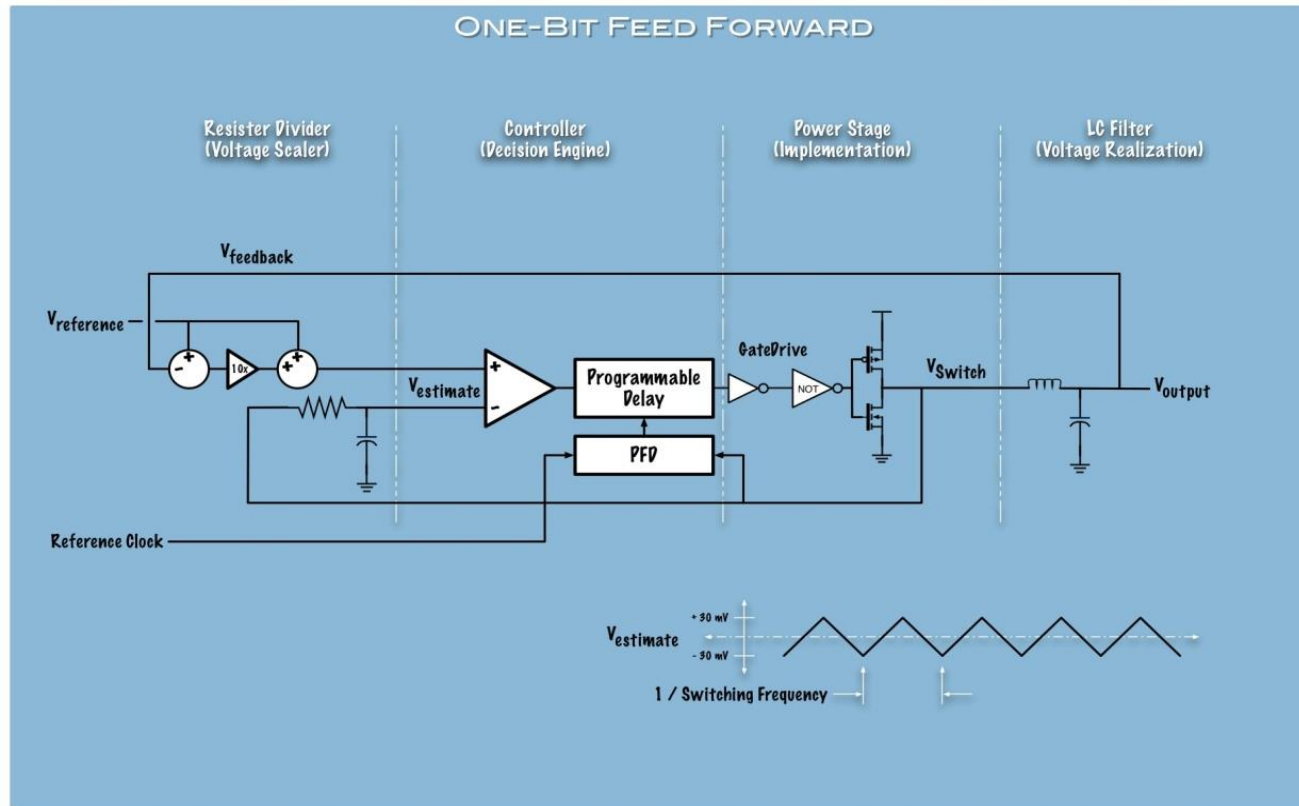


$$\text{Power Efficiency} \equiv \frac{V_{out} \times I_{load}}{V_{ext} \times (I_{load} + I_{quiescent})}$$



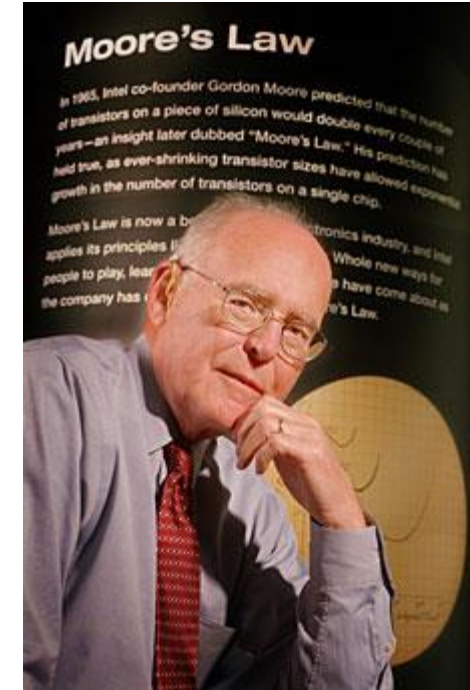
Control loop is no longer the limiting factor

Both Analog and Digital solutions can provide proximate time-optimal response



Which Process technology?

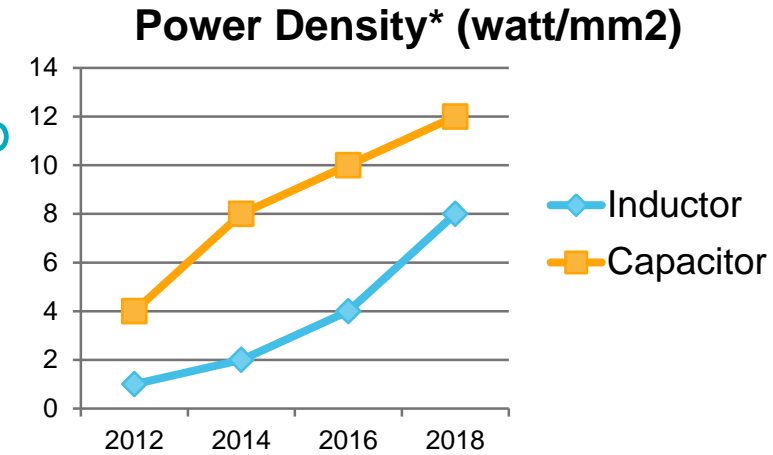
- Semiconductor processes and components:
 - Silicon remains the workhorse, but traditional Silicon is no longer yielding significant performance gains
 - Improvements are required in the next decade (SOI), GaN (GaN on Si)



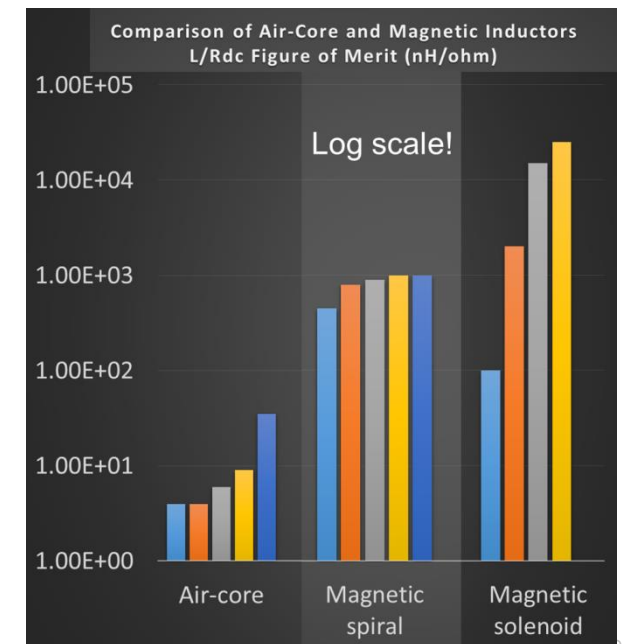
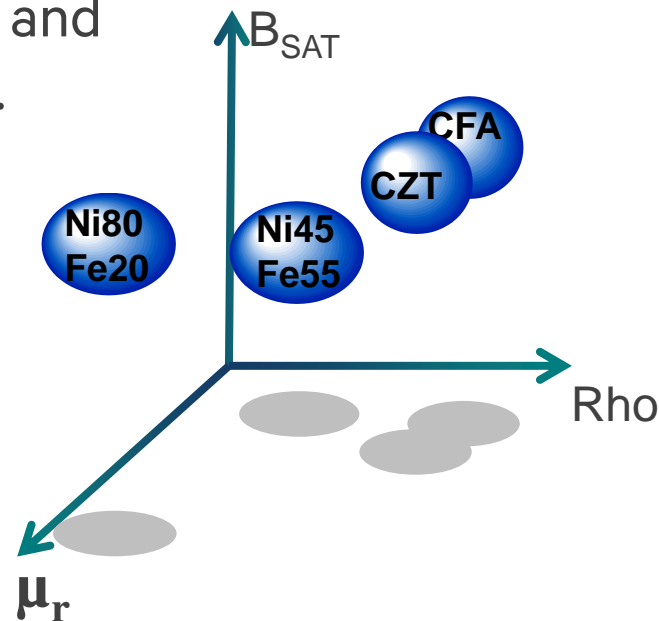
Passive Components evolutions

Capacitors have higher energy density, but inductors are catching up

- Capacitance density continues to make progress thanks to multi-layer insulators and trench technology
- 100+ MHz Buck converters can be implemented with air core, but in the long term magnetics win
- Ideal magnetic material has highest B_{sat} and resistivity with sufficiently low coercivity.



* Achievable in production process for >1W applications

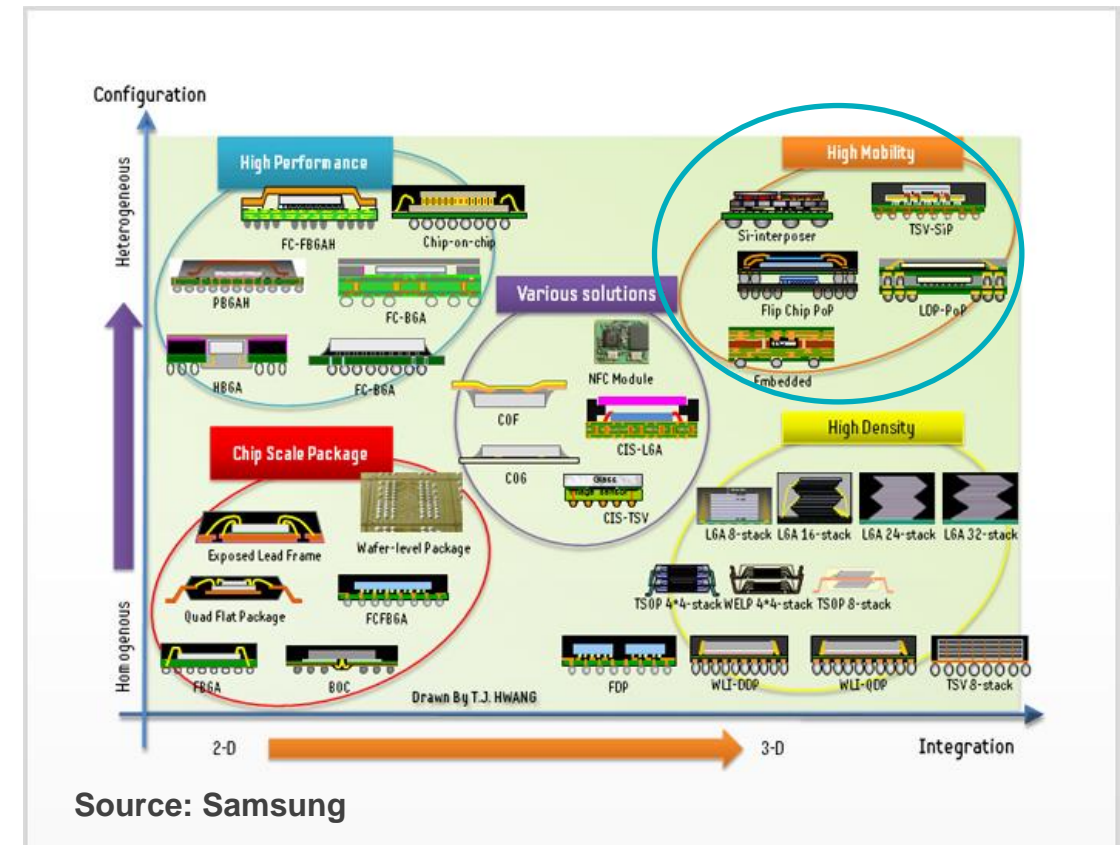


The biggest challenge: integration. Those d*#@n parasitics!

Integration is required because of physical dimensions' impact on performance

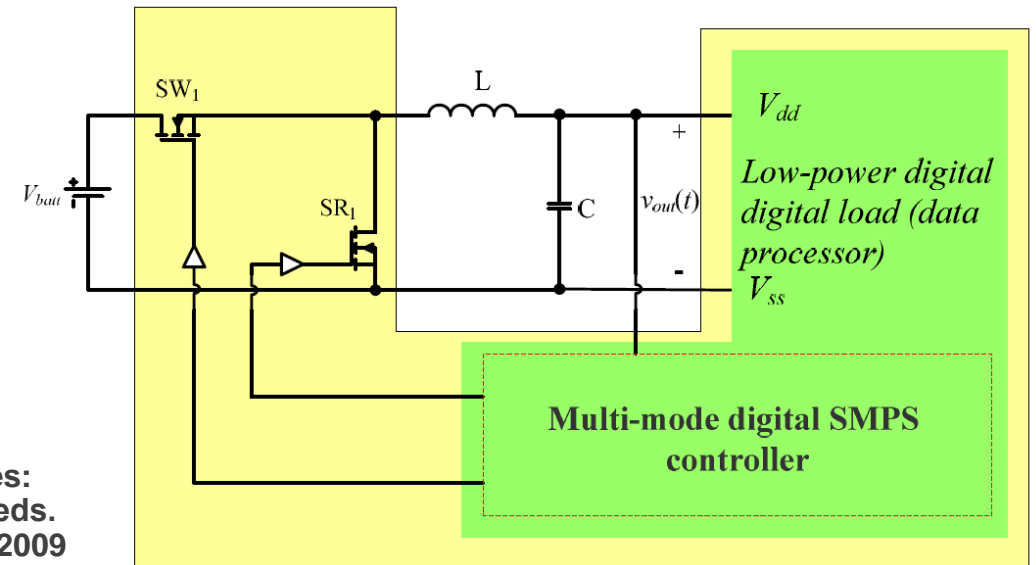
- Lateral current flow exacerbates L
- Vertical current flow pushes 3-D integration
 - Passives on silicon:
 - $\text{Cost} = \text{Die} * (1 + \Delta\text{area}) * (1 + \Delta\text{masks})$
 - Multi-die:
 - Passives on top \rightarrow lots of vias (area) on processor
 - Passives below \rightarrow Lots of vias on interposer for I/Os

I meant... the biggest challenge is cost



Fine-Grained Power Control

- DVFS benefits are well understood, but not easy to implement effectively
- VR integration yields many benefits
 - Voltage regulators can have multiple modes of operation, optimized for efficiency in different load ranges
 - Accurate auto-detection of load current is still “expensive”
 - Low-power modes may have significantly reduced transient performance which cripples auto-detection
 - However, power consumption of many loads is easily characterizable (modem, analog, dedicated DSP, etc.)
 - Fast and cheap same-die communication with regulators allows for dynamic optimization of a large number of individual voltage domains
 - Prediction is very difficult on standard processors, but many dedicated functions are “predictable”



Power aware system architectures:
the load knows “best” what it needs.
A. Prodic, University of Toronto, 2009

Conclusions

- From Power Management to Energy Management
- Integration of Computing and Power Management
 - Control of di/dt
 - Power profiles and Prediction of energy demand
 - Power-aware HW/SW implementation of system (VR + Processor)
- Process: GaN on Si?
- Integrated passives (FoM is looking good)
- 3-D integration – at low cost!
- Tools
 - Multi-physics co-simulation of power and thermals
 - Measurements of fast transient loads

Thank you

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