# *The Road to Integrated Power Conversion via the Switched Capacitor Approach*

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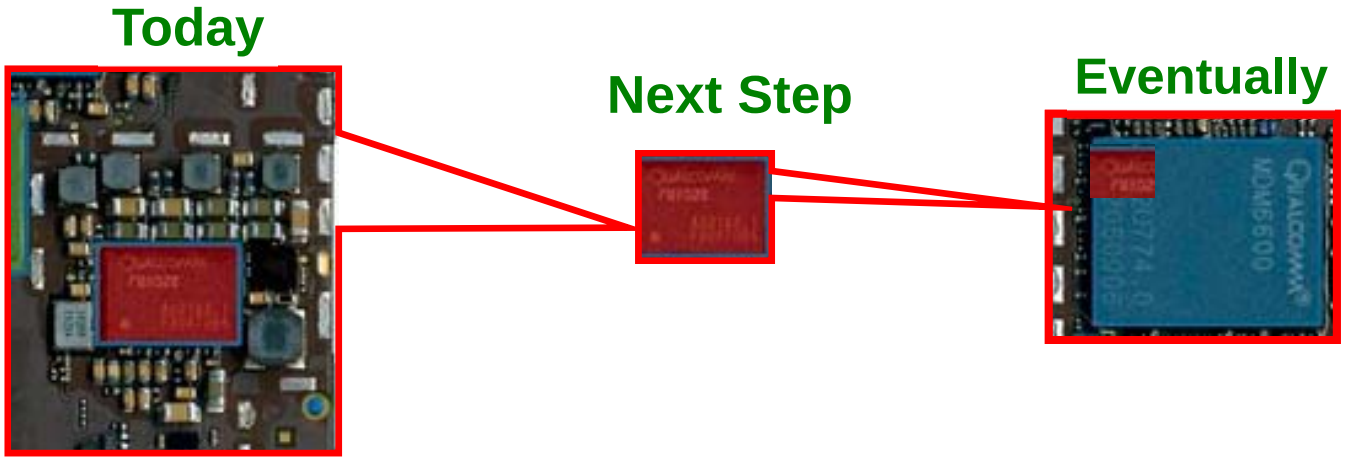
# Integrated Power

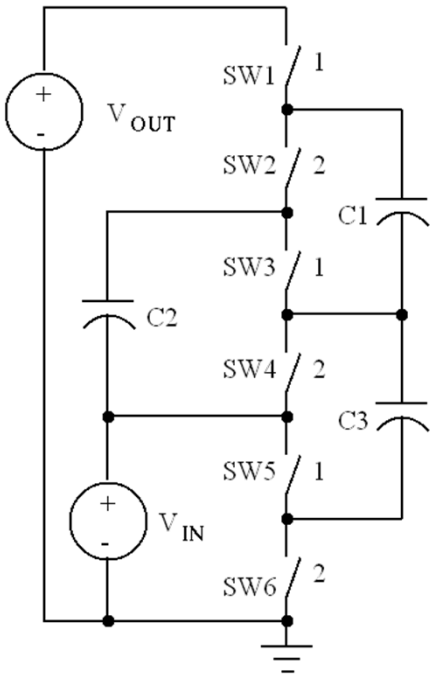
- ***Integration has benefits:***
  - *Reduce passives -> save board real estate, passive cost*
  - *More voltage domains on-die, improve efficiency in multi-core processor*
  - *Efficiency + fine-grain power management -> **battery life***
- ***and challenges:***
  - *Aim for ~10W/mm$^2$*
  - *Wide input range: eg. Li-type battery voltage discharge range*
  - *Limited on-die resources in standard CMOS*
  - *Efficiency over wide load voltage and current range*
  - *Ultra-low-power modes*

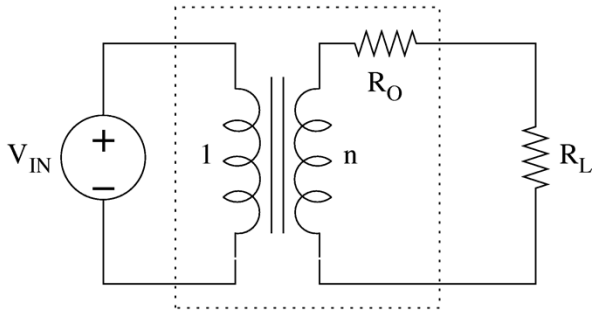



> 25% board area

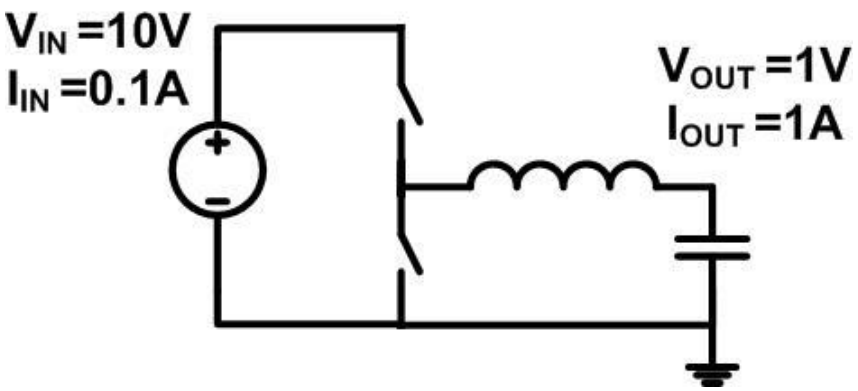
# Switched Capacitor Power Converters

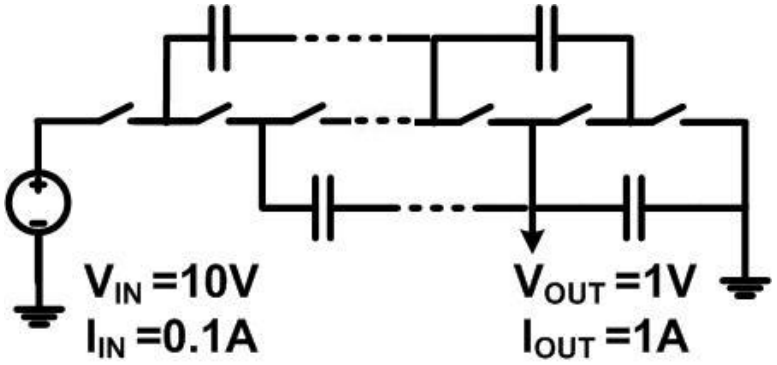
- Only switches and capacitors
- Can support multiple input or output voltages/terminals
- Simple full integration in standard process
- Works well over a wide power range
  - Single mode, can adjust clock rate
  - No minimum load
- No inductive switching losses
- Stacked devices enable high voltage with low voltage processes
- Simple low freq model as an ideal transformer with Thevenin impedance
  - freq dependent loss and leakage



# First Look



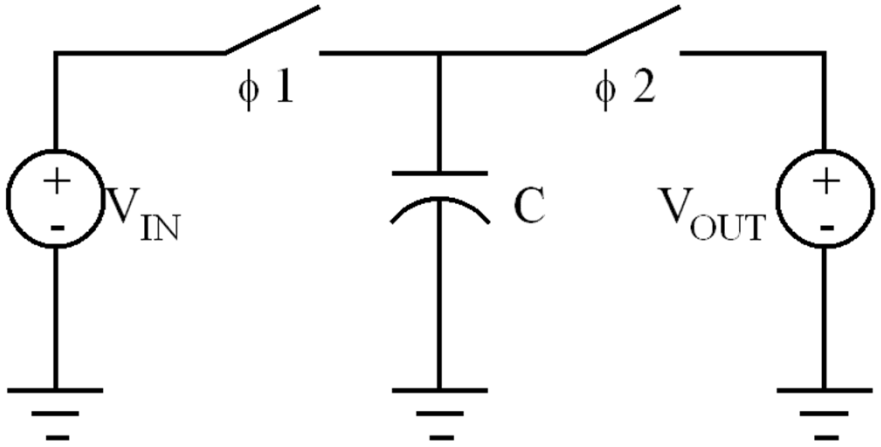

**Magnetic boost/buck:**

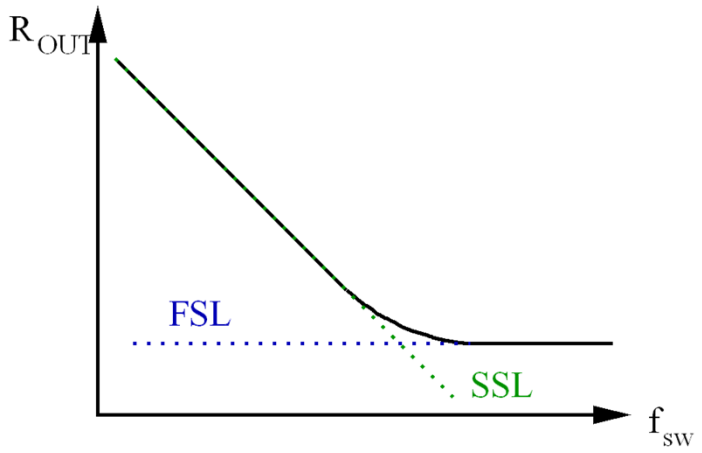
- **10-to-1 V conversion, 1A @ 1V**
- **S1,S2 rated for V-A product of V*I = 10 V-A**
- **Sum up to 20 V-A**
- **Need inductor, inductor loss, Inductive switching**

**10-to-1 Ladder Switched-Cap:**

- **10-to-1 V conversion, 1A@1V**
- **20 switches, each blocks 1V**
- **18 switches handle 1/5 A**
- **2 switches handle 9/5 A**
- **V-A product sums up to 36/5 =7.2 V-A**
- **Intrinsic CMOS device convenient**

# SC Analysis: Simplest Example




- Slow Switching Limit (SSL):
  - Impulsive currents (charge transfers)
  - Resistance negligible (assume R = 0)
  - This (SSL) impedance is the switching loss!
- Fast Switching Limit (FSL):
  - Constant current through switches
  - Model capacitors as voltage sources (C → ∞)

$$i = f_{sw}\Delta q = \boxed{f_{sw}C\Delta v}$$

$$i = \boxed{\frac{1}{4}\frac{1}{R}}\Delta v$$

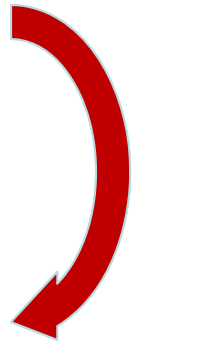
$$(\Delta v = V_{IN} - V_{OUT})$$

# Why Not S-C ?

- Difficult regulation?
- Interconnect difficulty for many caps?
- Voltage rating of CMOS processes?
- Magnetic-based ckts = higher performance?
- Ripple?
- Fundamental charge sharing losses?

# Discrete Inductors vs. Discrete Capacitors

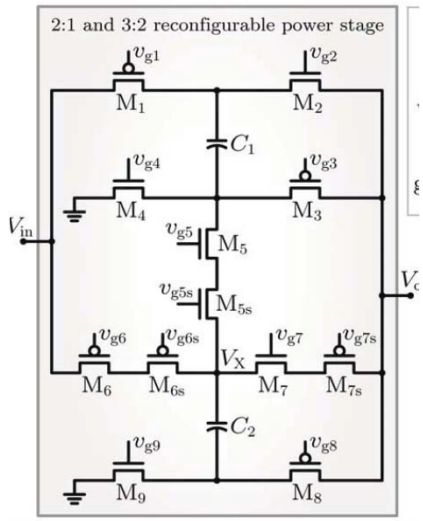
| Type | Manufacturer | Capacitance | Dimension | Energy Density |
|---|---|---|---|---|
| Ceramic Cap | Taiyo-Yuden | 22µF @4V | 1.6 x 0.8 x 0.8 | **344** |
| Ceramic Cap | Taiyo-Yuden | 1µF@35V | 1.6 x 0.8 x 0.8 | **1196** |
| Tantalum Cap | Vishay | 10µF@4V | 1.0 x 0.5 x 0.6 | **533** |
| Tantalum Cap | Vishay | 100µF@6.3V | 2.4 x 1.45 x 1.1 | **1037** |
| Electrolytic Cap | Kemet | 22µF@16V | 7.3 x 4.3 x 1.9 | **94** |
| Electrolytic Cap | C.D.E | 210mF@50V | 76φ x 219 | **172** |
| Shielded SMT Inductor | Coilcraft | 10µH @ 0.21A | 2.6 x 2.1 x 1.8 | **0.045** |
| Shielded SMT Inductor | Coilcraft | 100µH @ 0.1A | 3.4 x 3.0 x 2.0 | **0.049** |
| Shielded inductor | Coilcraft | 170µH @ 1.0A | 11 x 11 x 9.5 | **0.148** |
| Shielded inductor | Murata | 1 mH @ 2.4A | 29.8φ x 21.8 | **0.189** |



**>1000x**

- Capacitors have >1000x higher energy density than inductors
- Same holds with on-die scale devices/technology

# Recent Work, Example 1: TM Andersen et al., ISSCC 2014




2:1 and 3:2 topology

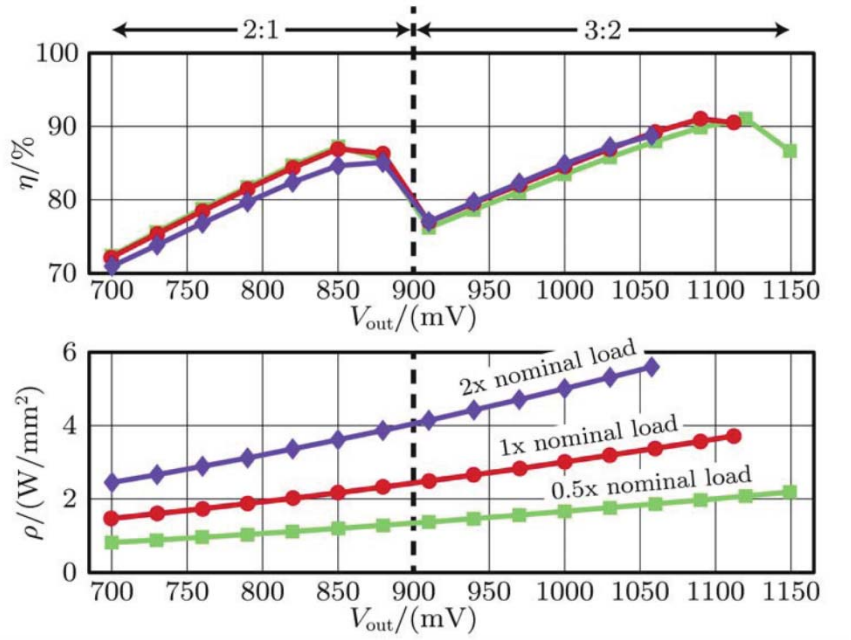
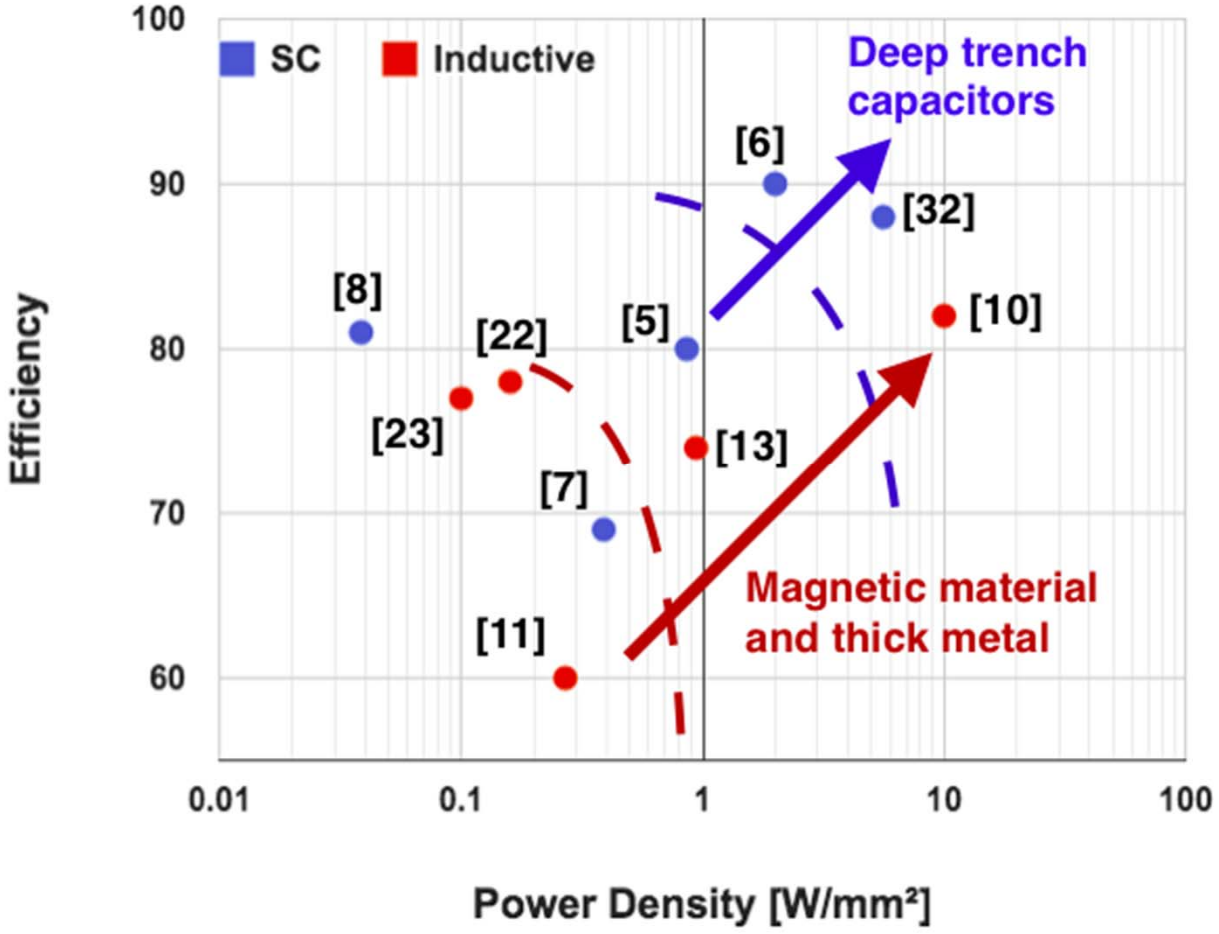



**Figure 4.7.5: Measured efficiencies and power densities for $V_{in}$=1.8V over the full output voltage range.**

- ~290 nF/sq.mm deep trench cap
- 16 phase, with 125 MHz per phase
- ~6 W/sq.mm @ 88-89% eff

# Performance with advanced passives




References in fig: [6] L. Chang, "A fully integrated switched capacitor …" *VLSI*, 2010

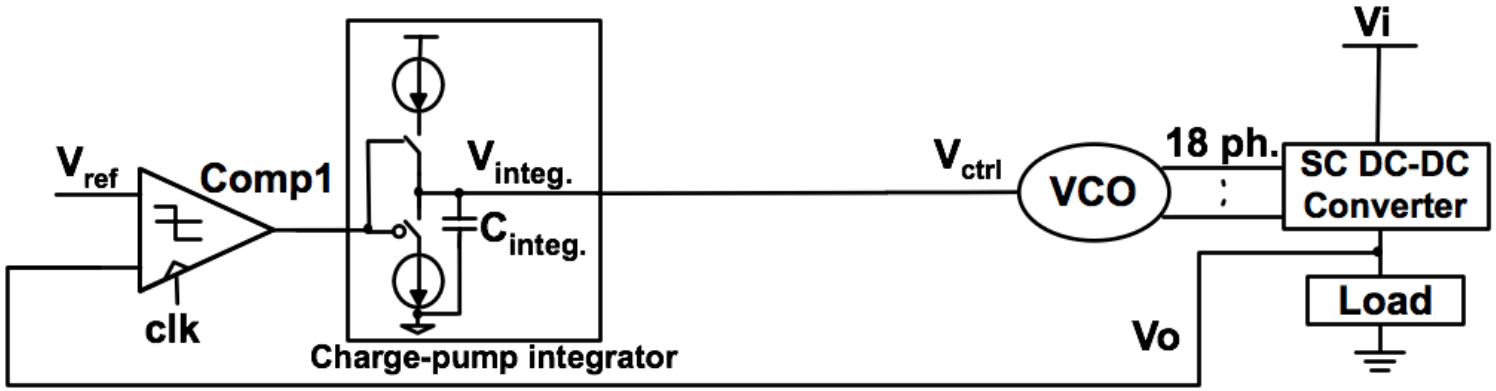
[5] HP Le, ISSCC 2010

[10] J. Dibene, "A 400A fully integrated silicon ..." *APEC*, 2010

[32] T.M. Anderson et al., ISSCC 2014

***(Sanders et al., IEEE T-PELS 2013, "The Road to …")***

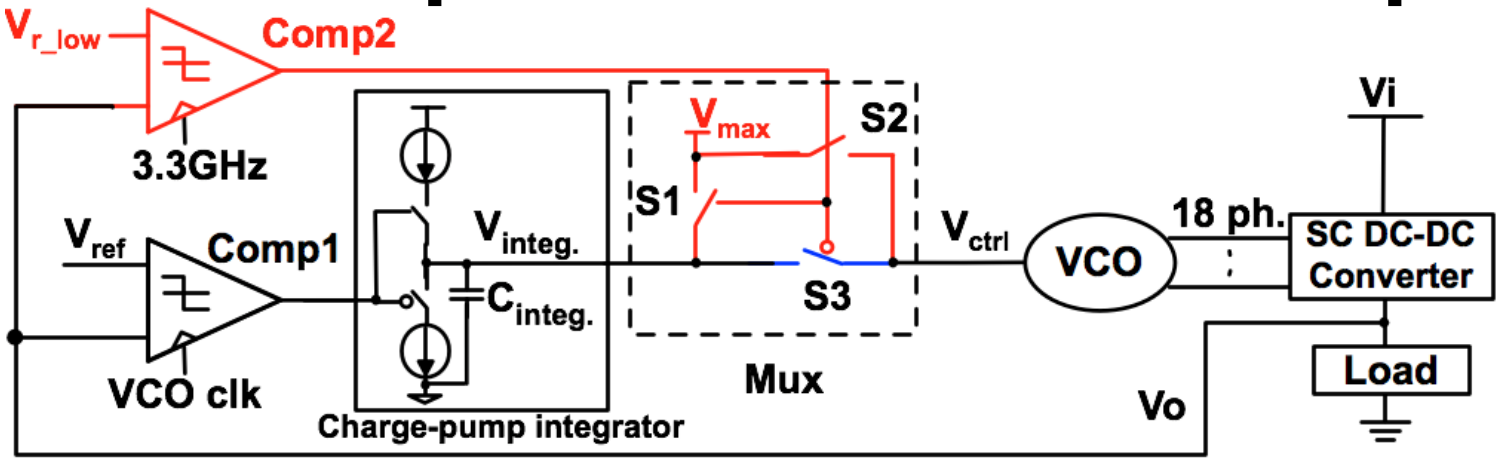
# Simple Closed-Loop Control (Ex. 1 cont.)

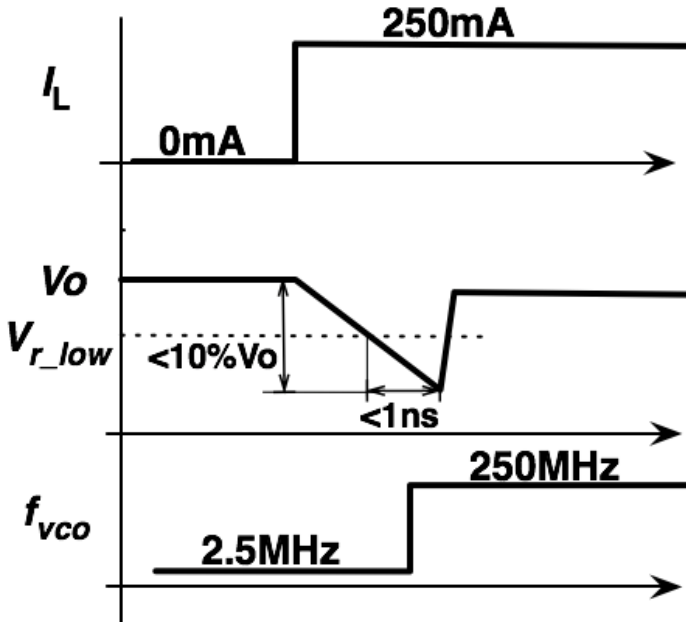



- **Output impedance of the regulator set by $f_{vco}$**
  - Rout α $1/(f_{vco}C_{fly})$
- **Switching frequency set by (slow) integral control loop**
- **Key challenge: response to 0 → $I_{max}$ load step**

***(Ref: H-P Le et al, ISSCC 2013)***

# Control Loop with Fast Load Response

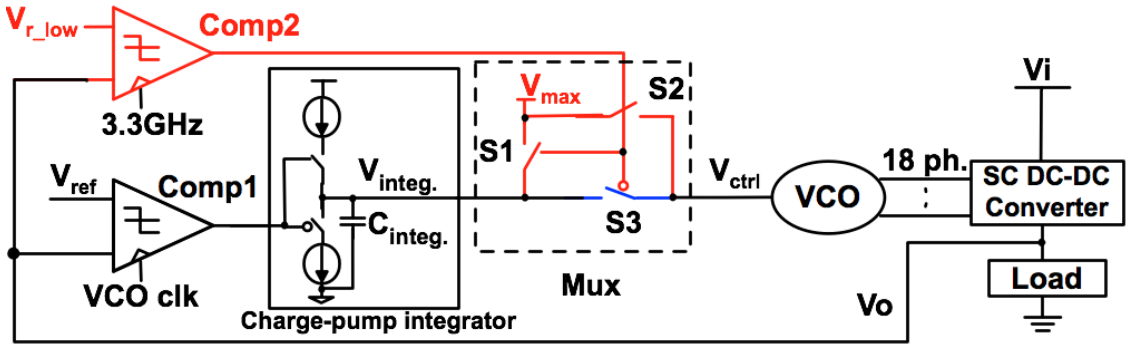


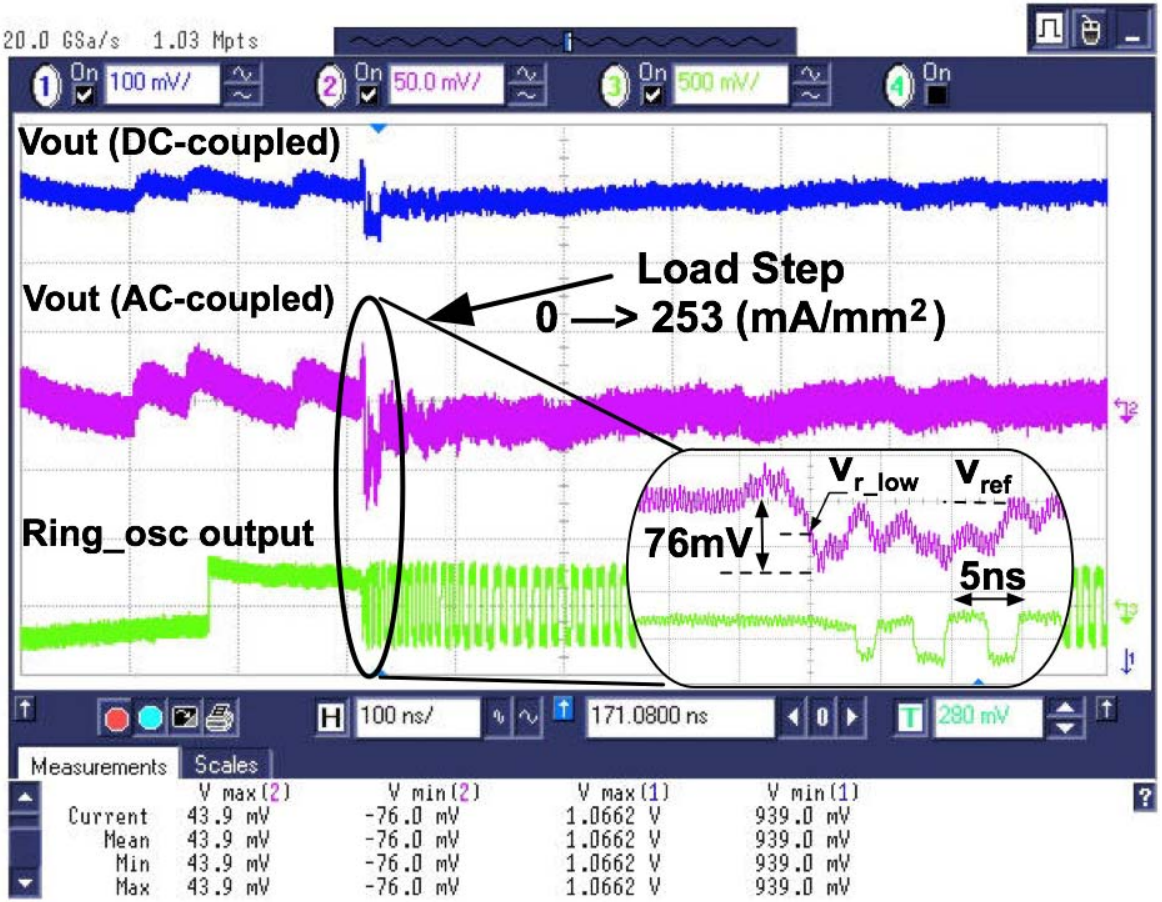




- **Additional comparator "jumps" $f_{vco}$**
- **Need sub-ns response time for <10% droop**
  - Comparator must sample Vo at high frequency

***(Ref: H-P Le et al, ISSCC 2013)***

# Load Step Measurement



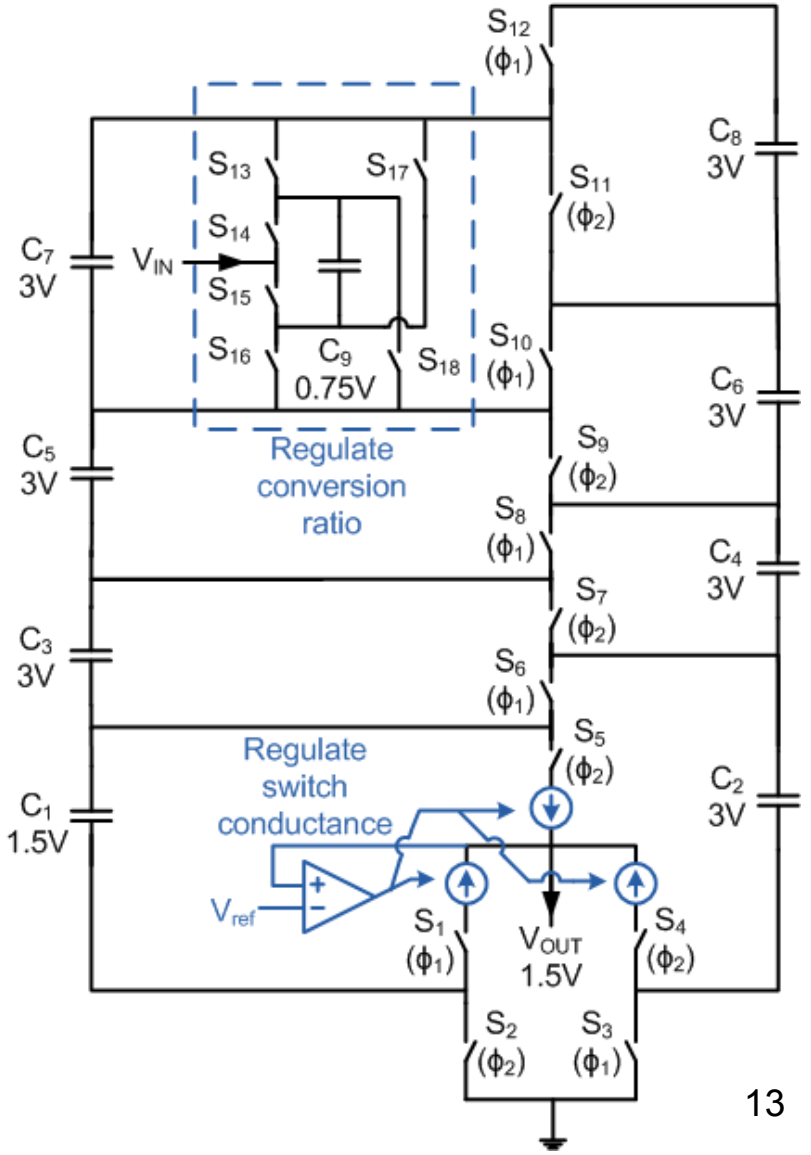

- **Load step generated by on-die load circuitry**
- **Achieves 7.6% droop under a full load step (50ps rise time) of 253mA/mm²**
  - Indicates response time of < 1ns

***(Ref: H-P Le et al, ISSCC 2013)***

# Example 2 – Point-of-Load:12V-to-1.5V Dickson Type Circuit

Illustrates "tap-changing" technique for line regulation.

- Dickson converter with nominal conversion ratios: 5-to-1, 5.5-to-1, … , 8-to-1
- Modulate switch conductance for fine regulation
- Modulate switching frequency for high efficiency at light load
- Illustrates wide range conversion and voltage domain stacking




***(Ref: V.W. NG et al, IEEE T-PELS 2013)***

# Transient measurement – load step

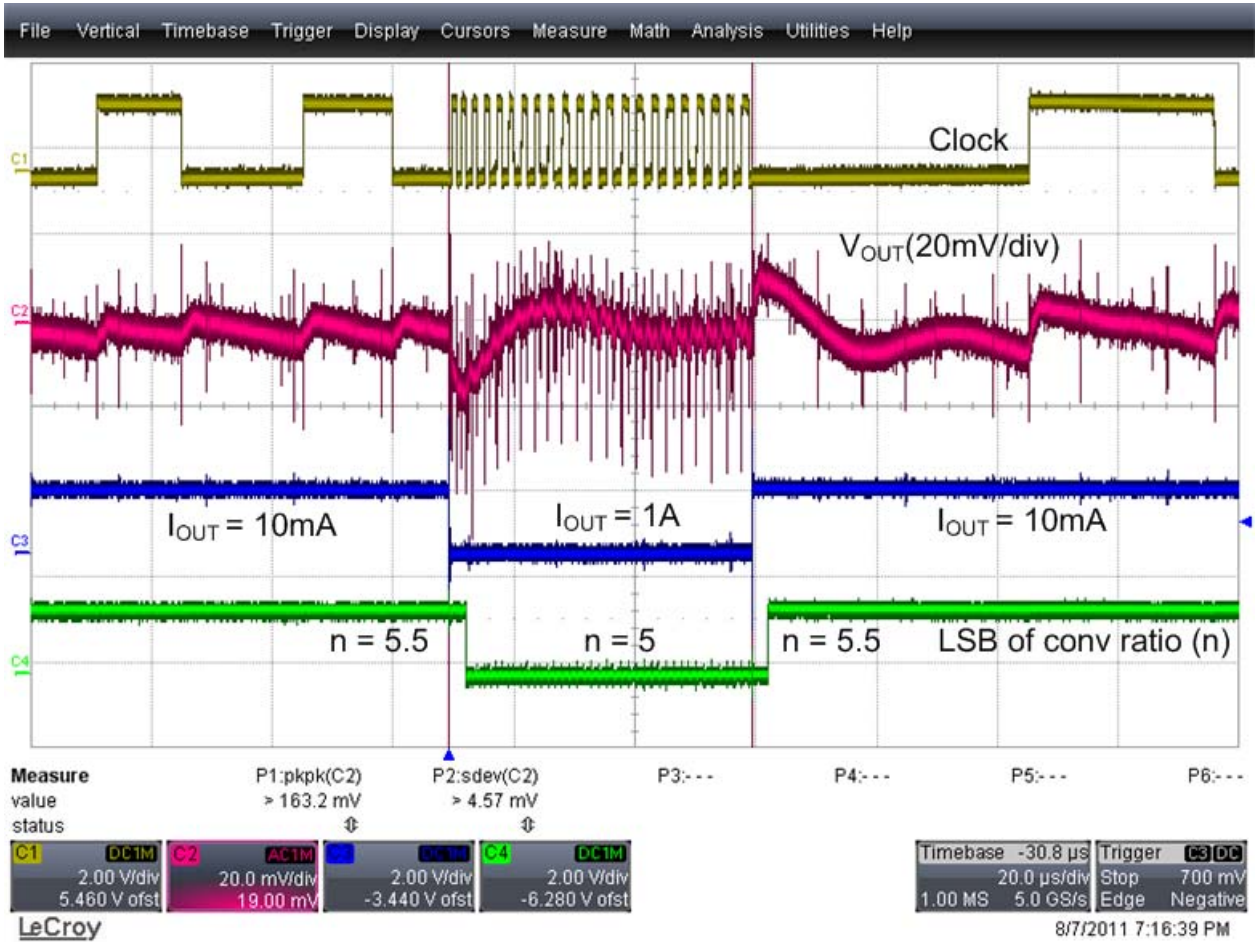
clock

Vout: 20 mV/div

Load Current:

10mA-1A-10mA

LSB (ratio)




- $V_{OUT}$ variation within 30mV during full loading and unloading transient
- $C_{IN}$=12µF, $C_{OUT}$=110µF, typical to 1A buck converters

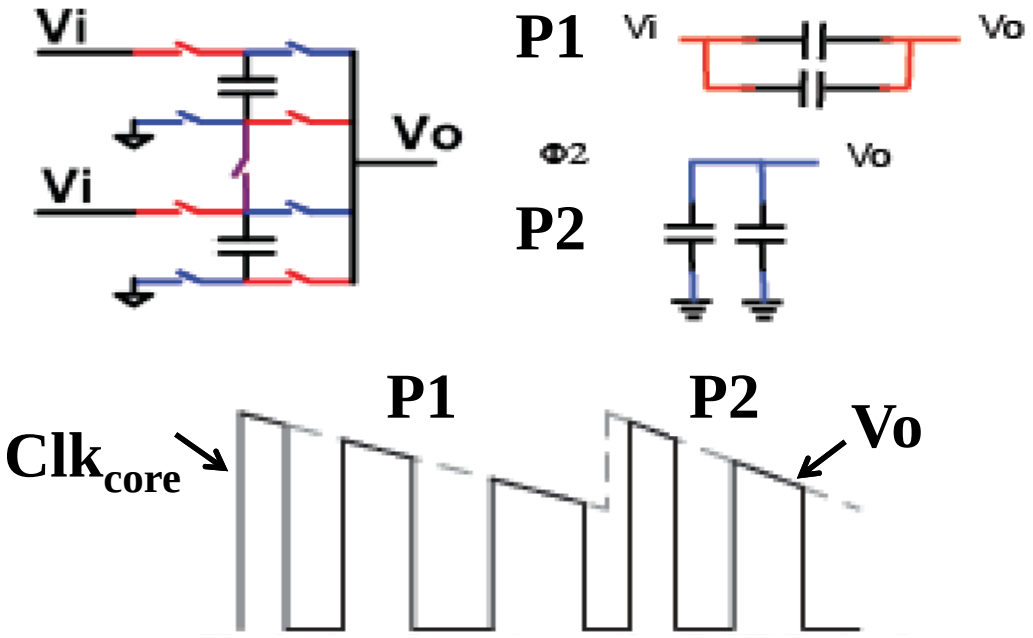


***(Ref: V.W. NG et al, IEEE T-PELS 2013)***

# Ex. 3: Raven Processor Project (2014)– BWRC (UC Berkeley), Alberto Puggelli poster

- Each digital unit is powered by a dedicated single-phase SC converter:
  - fine-grained DVFS
  - power gating
- Innovation: combine and exploit SC voltage ripple with DVS to adiabatically consume ripple energy

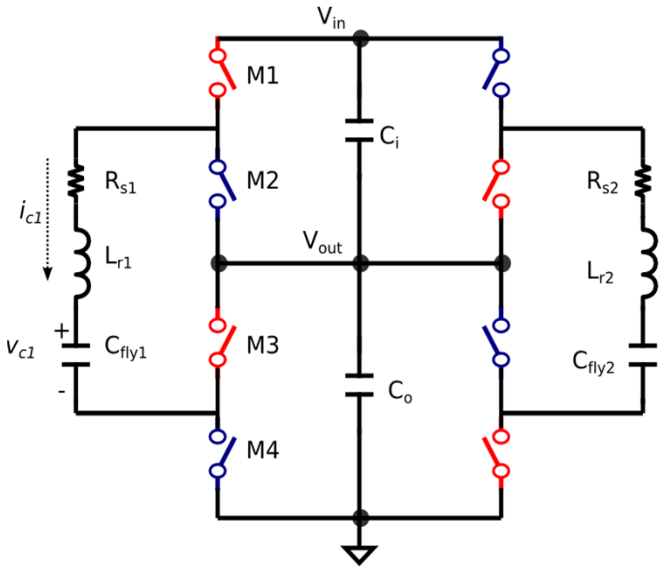
Basic unit cap cell and its functionality in 2:1






(***Ref: IEEE T-VLSI 2014***)

# What's next? ResSC Topology(s)




Small on-die inductance resonates out working (flying) caps

- Avoid charge sharing losses
- Much larger swing on working caps, better use of valuable cap resources
- Net inductor V-A utilization superior to "conventional buck", etc.
- Opportunities for lossless regulation
- Refs: Stauth et al. (ISSCC 2013,14), many others + on-going efforts

Related:

- "Soft charging" methods that adiabatically combine inductor-based and SC ckts
- Ex. Pilawa et al, IEEE PESC 2008

# Why Not S-C ?

- Difficult regulation? X
- Interconnect difficulty for many caps? X
- Voltage rating of CMOS processes? X
- Magnetic-based ckts = higher performance? X
- Ripple? X
- Fundamental charge sharing losses? X