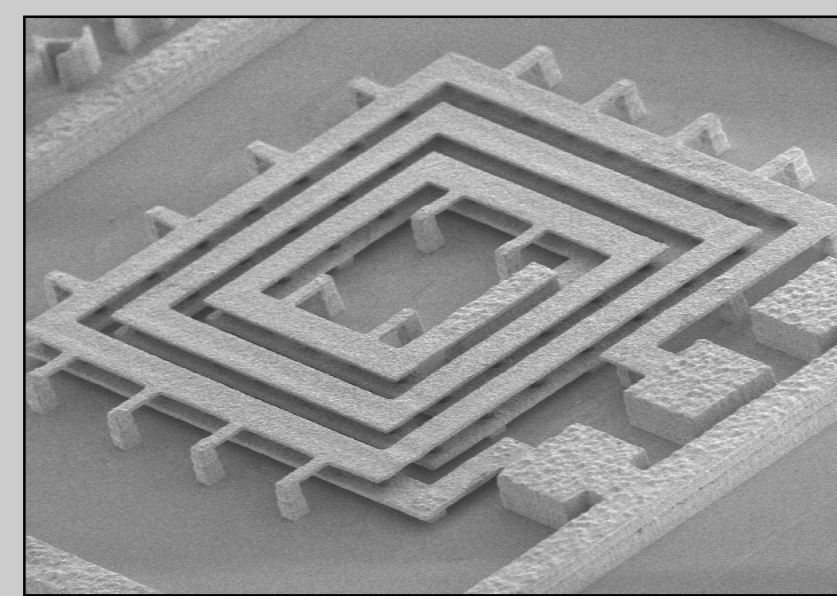


# Integrated Components for Chip Scale Power Management

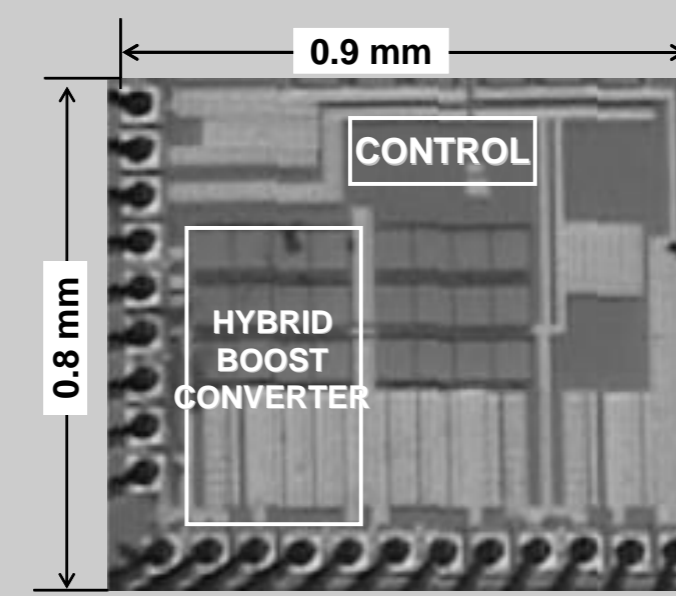
Christopher D. Meyer<sup>1</sup>, Sarah S. Bedair<sup>1</sup>, Jeffrey S. Pulskamp<sup>1</sup>, Ronald G. Polcawich<sup>1</sup>, Nathan S. Lazarus<sup>1</sup>, Iain M. Kierzewski<sup>1</sup>, Xue Lin<sup>2</sup>, Christopher Dougherty<sup>2</sup>, and Rizwan Bashirullah<sup>2</sup>

<sup>1</sup>U.S. Army Research Laboratory  
<sup>2</sup>University of Florida

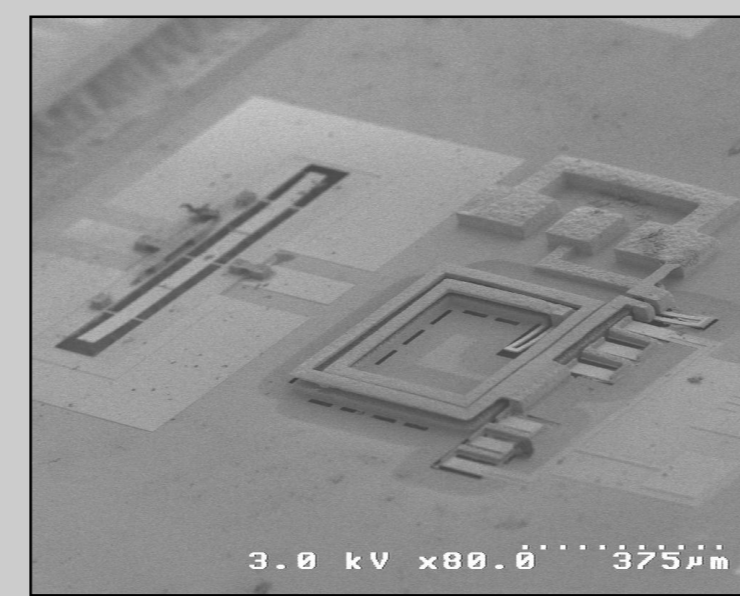
## Miniature power converters



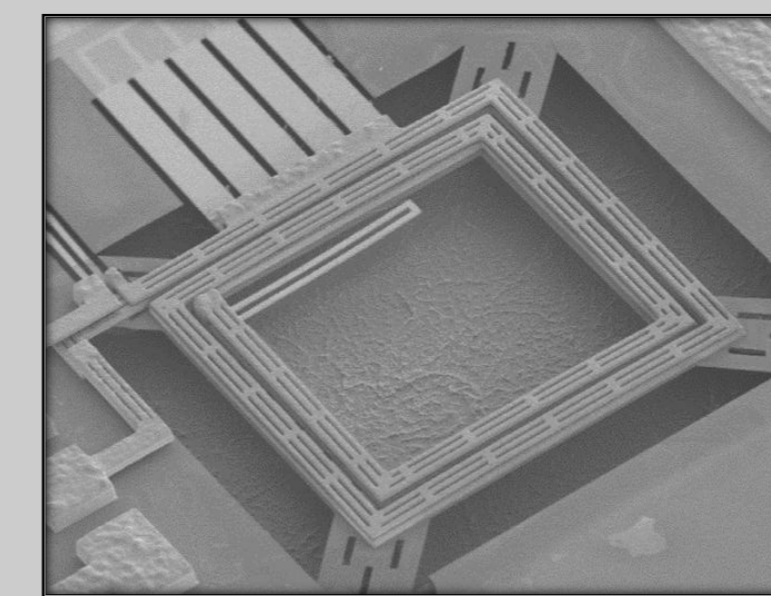
High frequency RF power inductors



CMOS switching / control

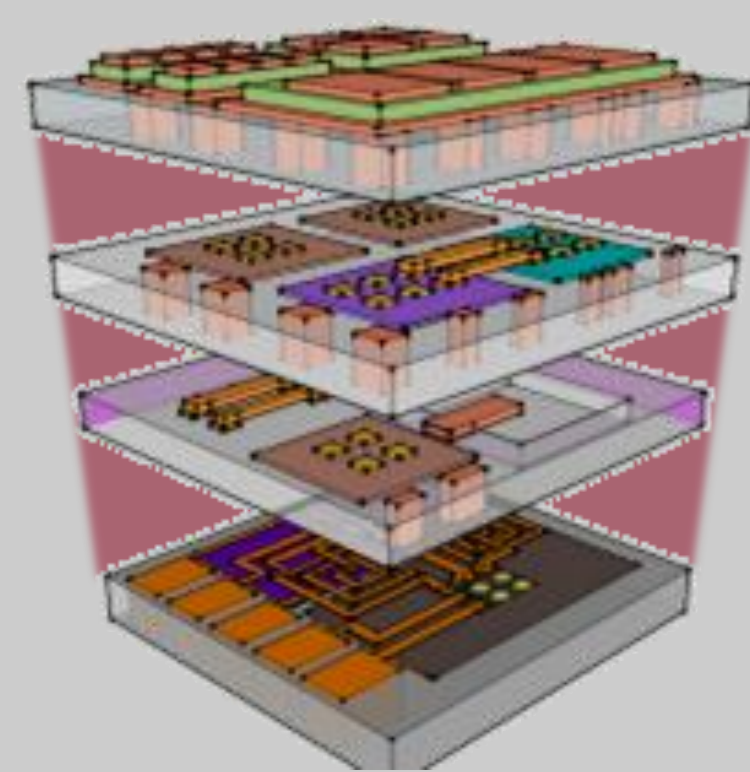


Tunable components

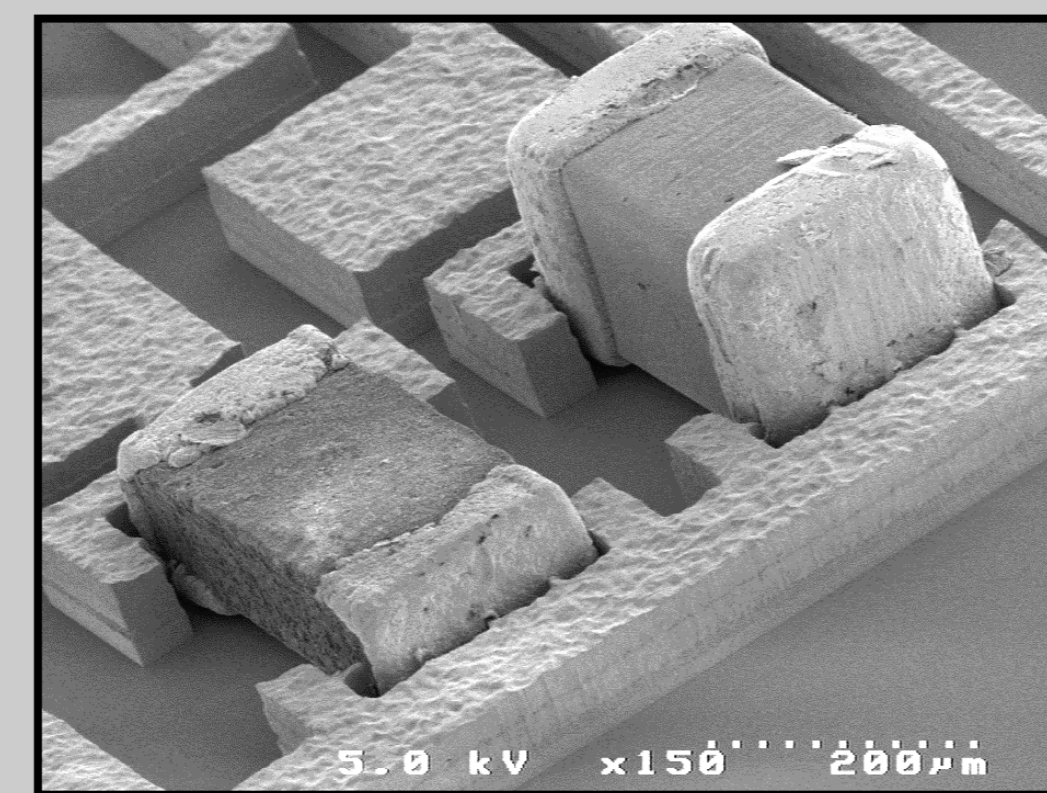


Mechanical transformers

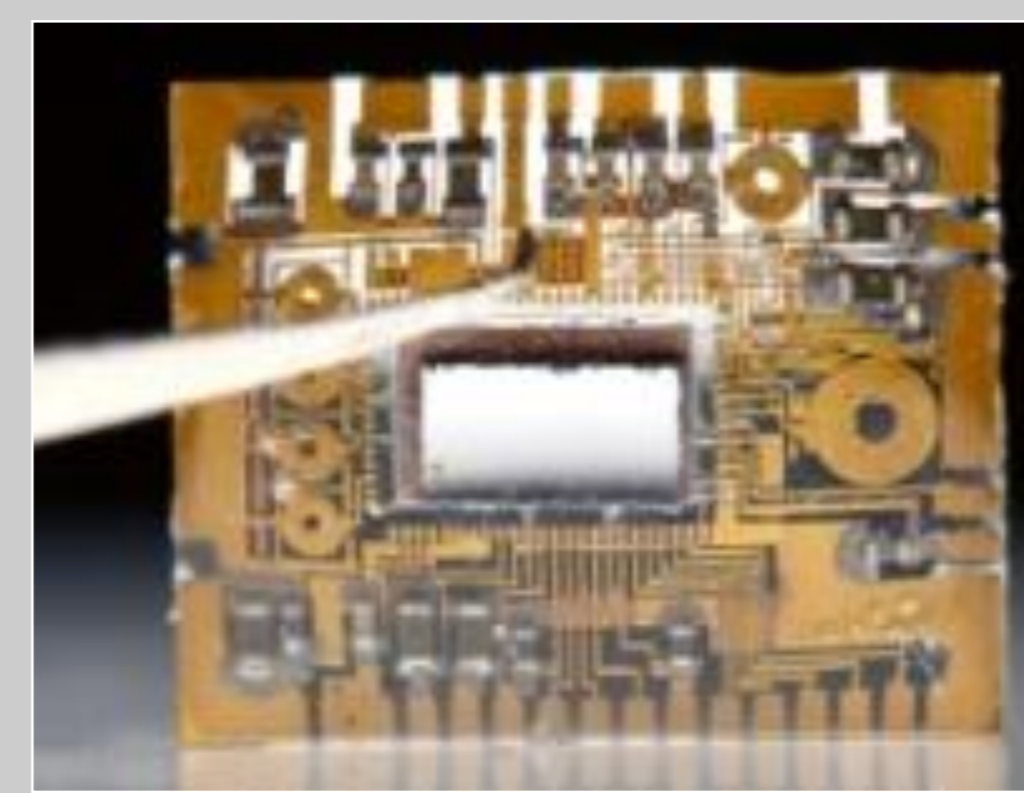
## Monolithic / hybrid integration



3D integration for SWAP constrained systems



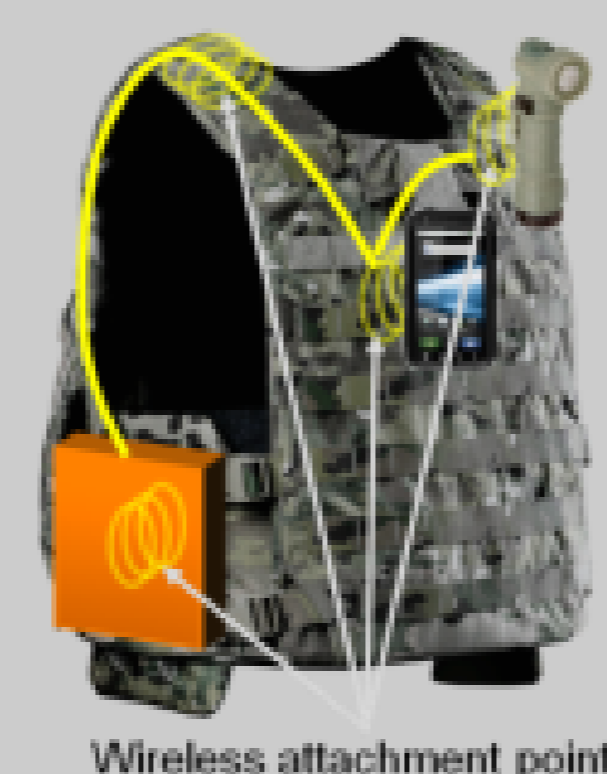
Hybrid component integration



## Wearable power components

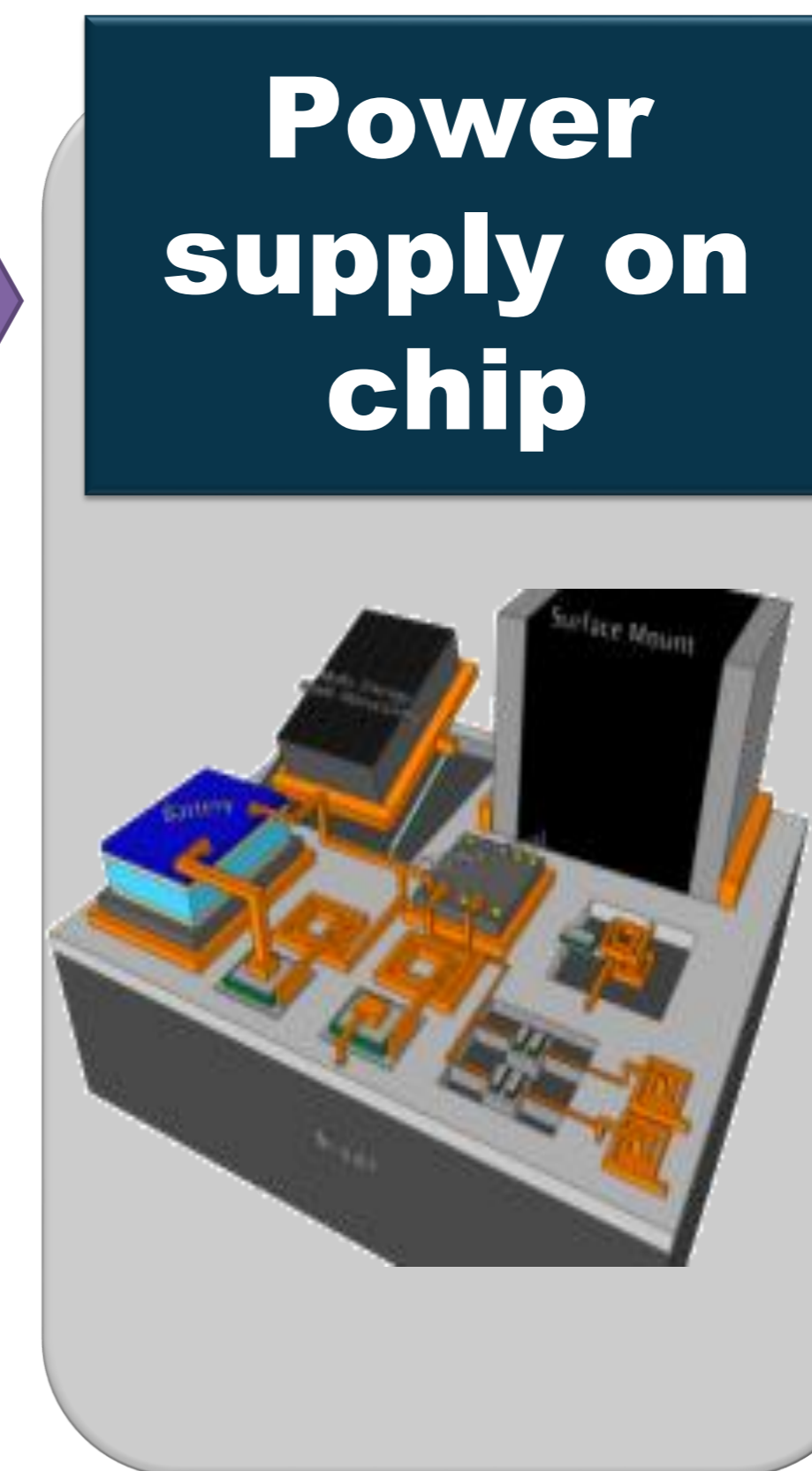


Stretchable power inductor and components



Wireless attachment points

Wireless power coupling for integrated soldier power



- ARMY Applications**
- Microrobotics
  - Small munitions
  - Radios
  - Portable electronics
  - Soldier power
  - ...

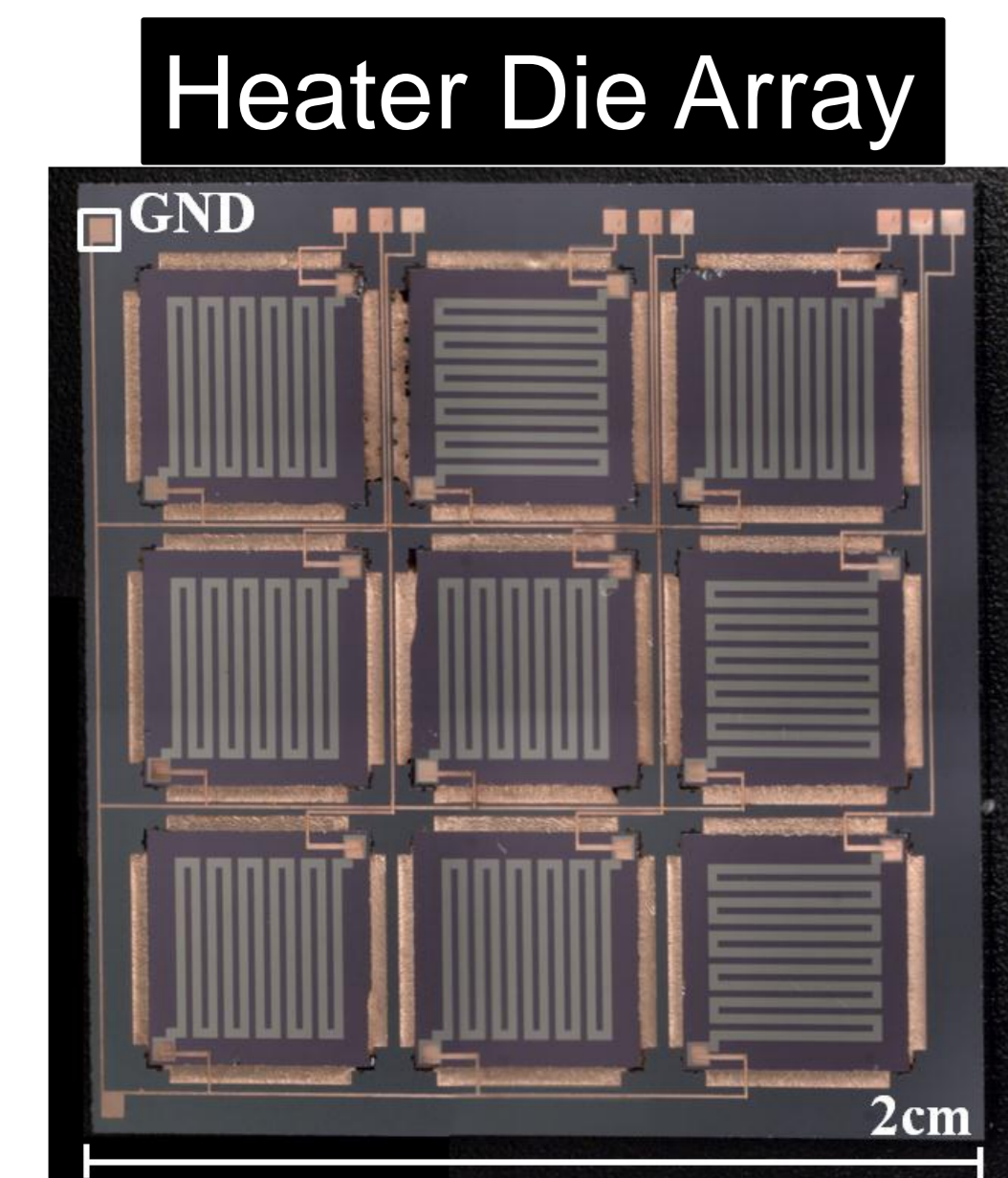
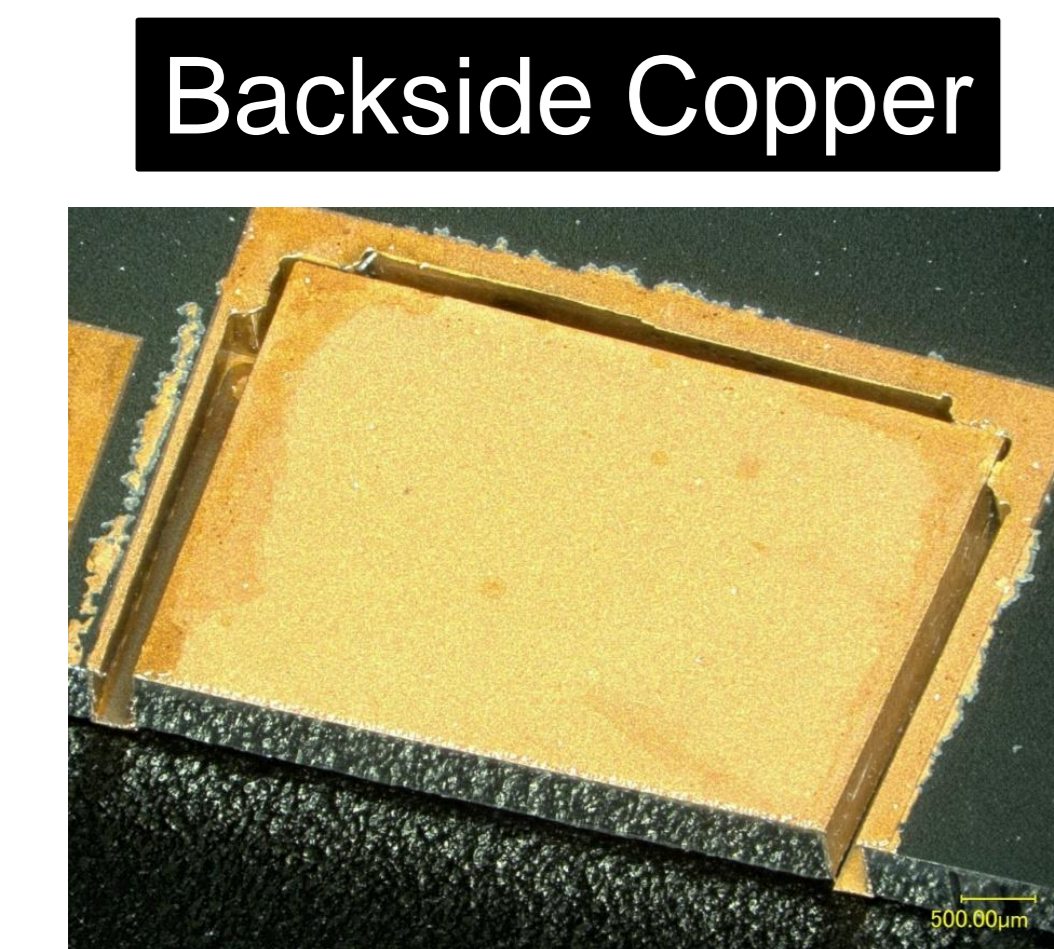
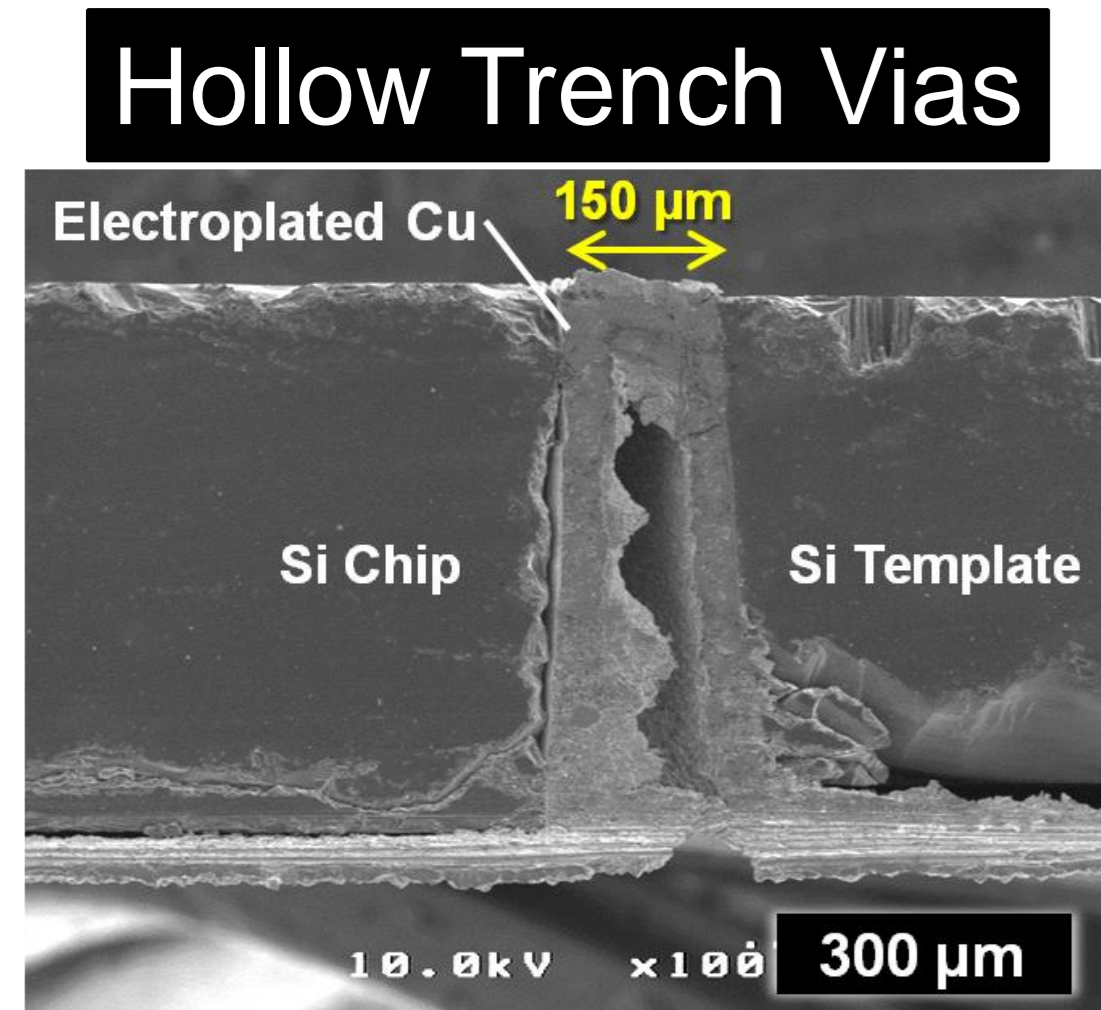
# Integrated Components for Chip Scale Power Management

Christopher D. Meyer<sup>1</sup>, Sarah S. Bedair<sup>1</sup>, Jeffrey S. Pulskamp<sup>1</sup>, Ronald G. Polcawich<sup>1</sup>, Nathan S. Lazarus<sup>1</sup>, Iain M. Kierzewski<sup>1</sup>, Xue Lin<sup>2</sup>, Christopher Dougherty<sup>2</sup>, and Rizwan Bashirullah<sup>2</sup>

<sup>1</sup>U.S. Army Research Laboratory  
<sup>2</sup>University of Florida

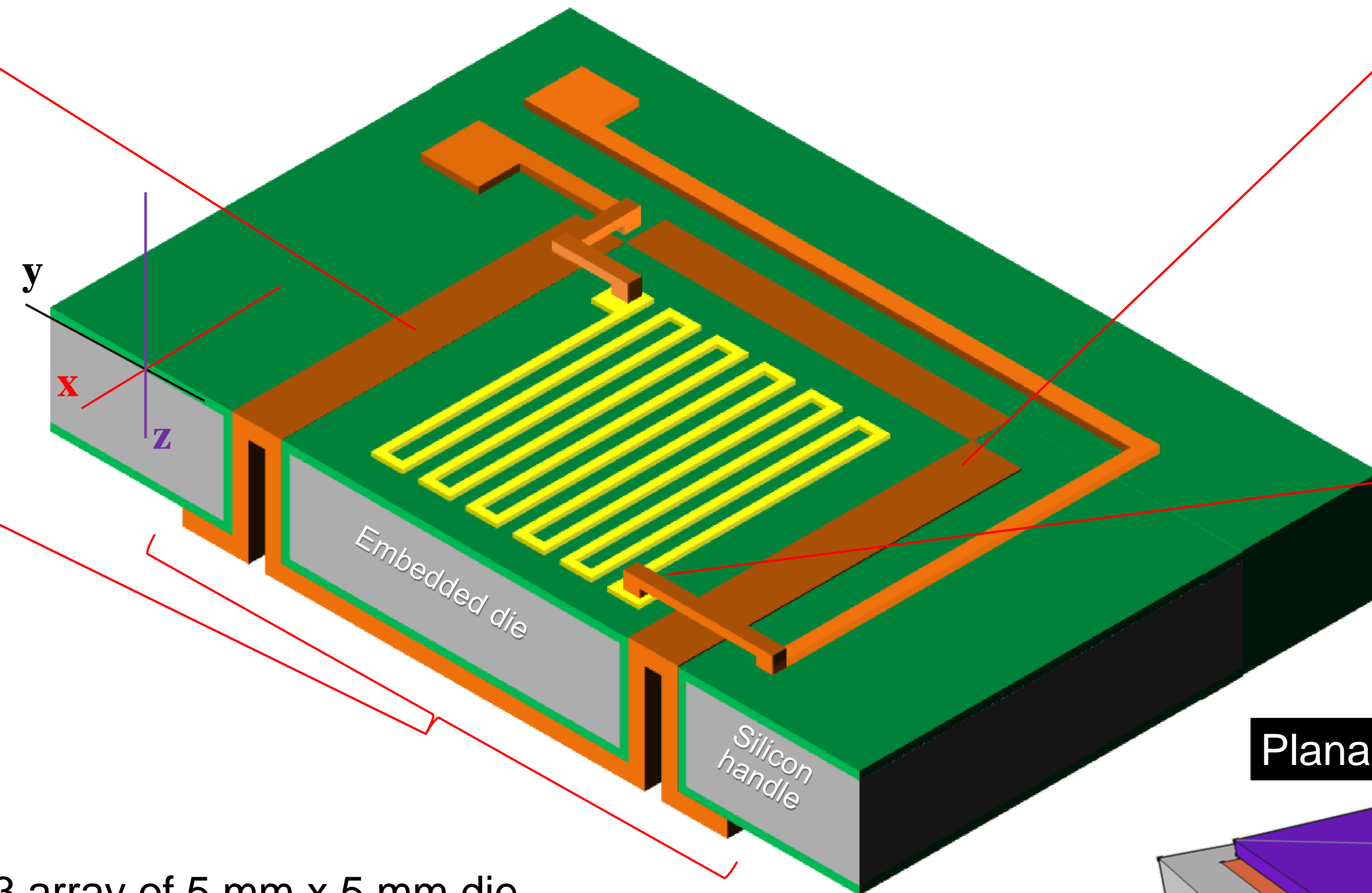
## Heterogeneous Die Integration Process

- Electroplated copper holds die in place in silicon wafer
- Simultaneously yields electrical vias with 125-326  $\mu\Omega$  resistance through 525  $\mu\text{m}$  thick silicon handling wafer

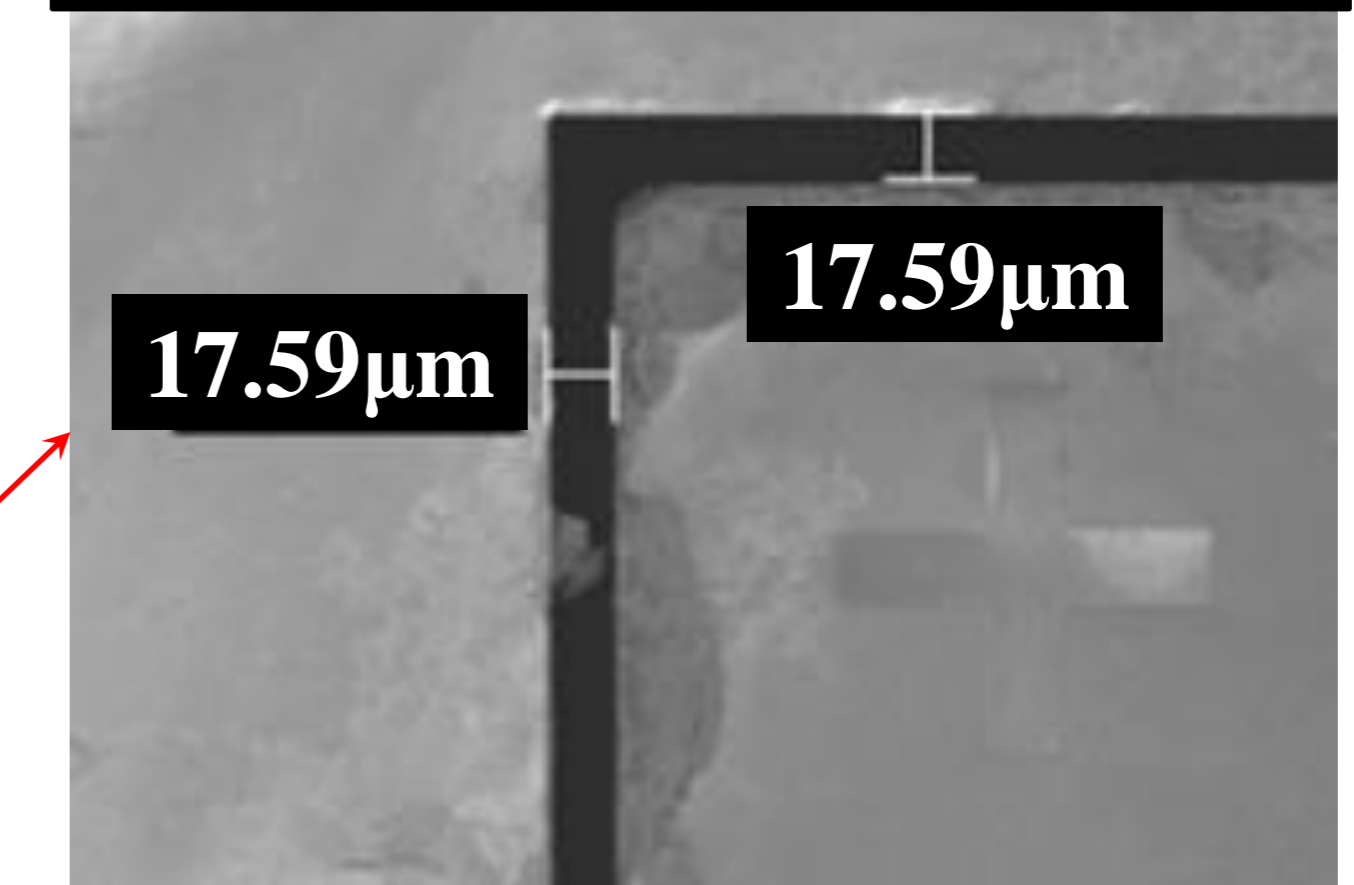


- 3x3 array of 5 mm x 5 mm die
- 200  $\Omega$  surface heaters
- 280  $\mu\text{m}$  inter-die spacing

CD Meyer et al., "Heterogeneous Chip Integration into Silicon Templates by Through-Wafer Copper Electroplating," in *ECS Transactions*, vol. 45, no. 6, pp. 163-169, 2012.

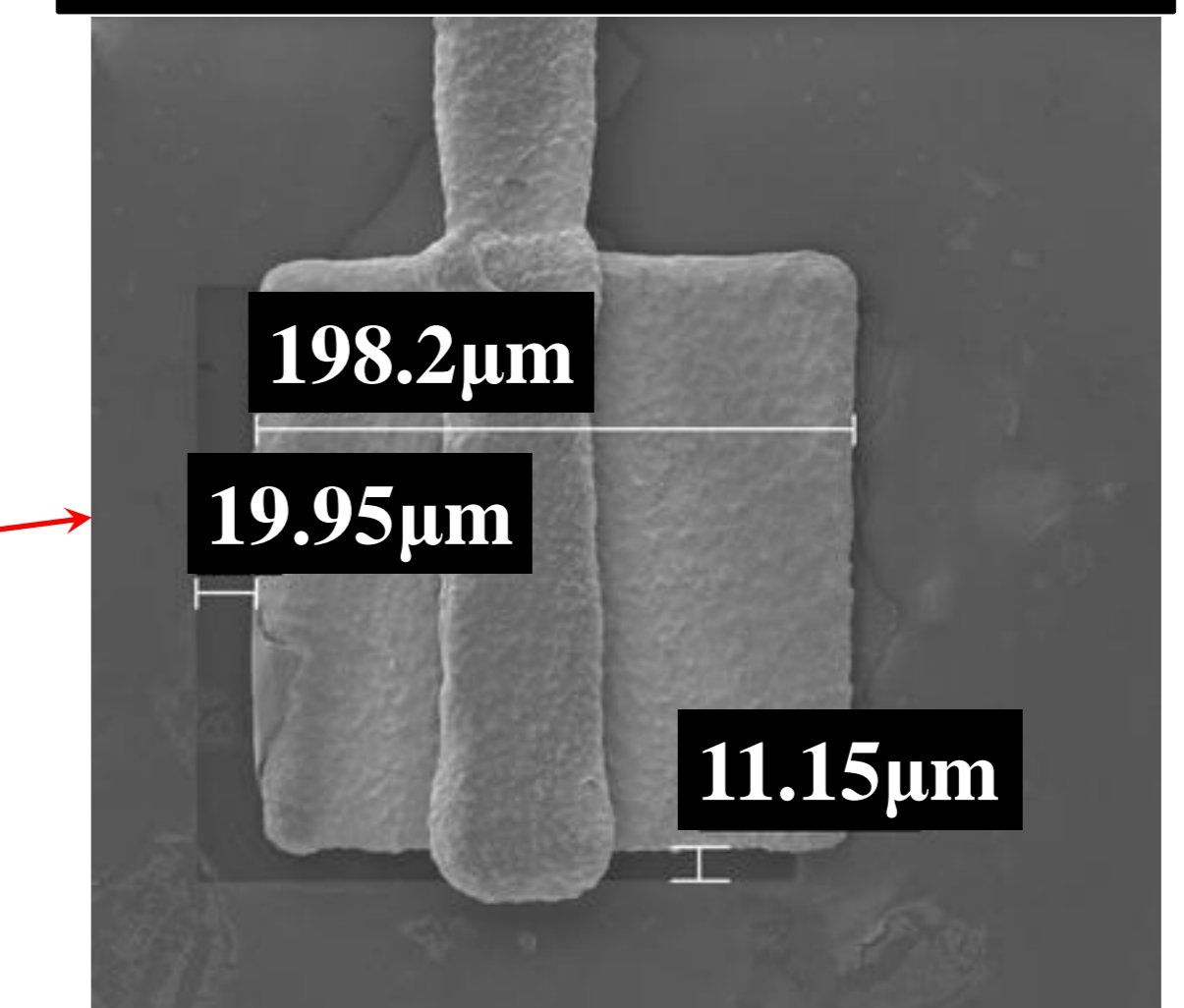


## Corner Alignment Notches



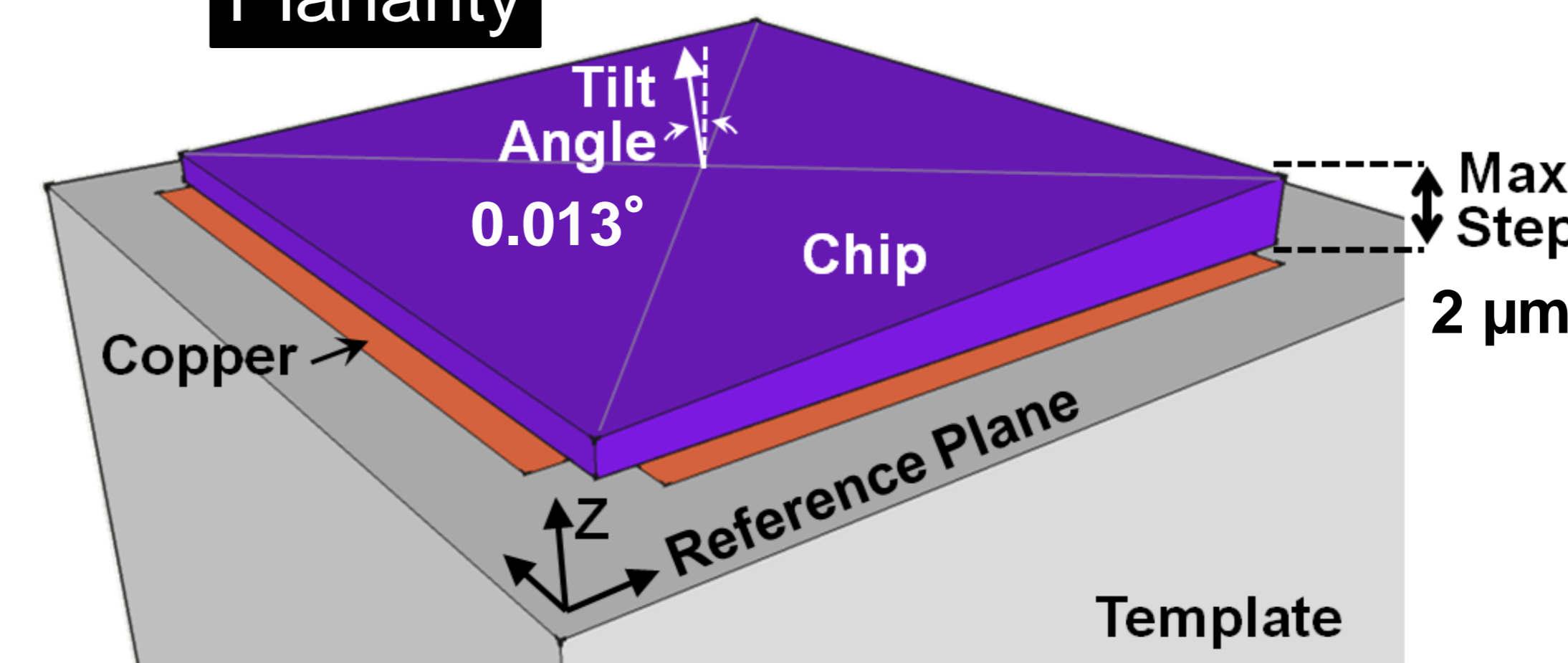
- Corner notches give hand-placed lateral alignment within 20  $\mu\text{m}$

## Topside Pad Alignment



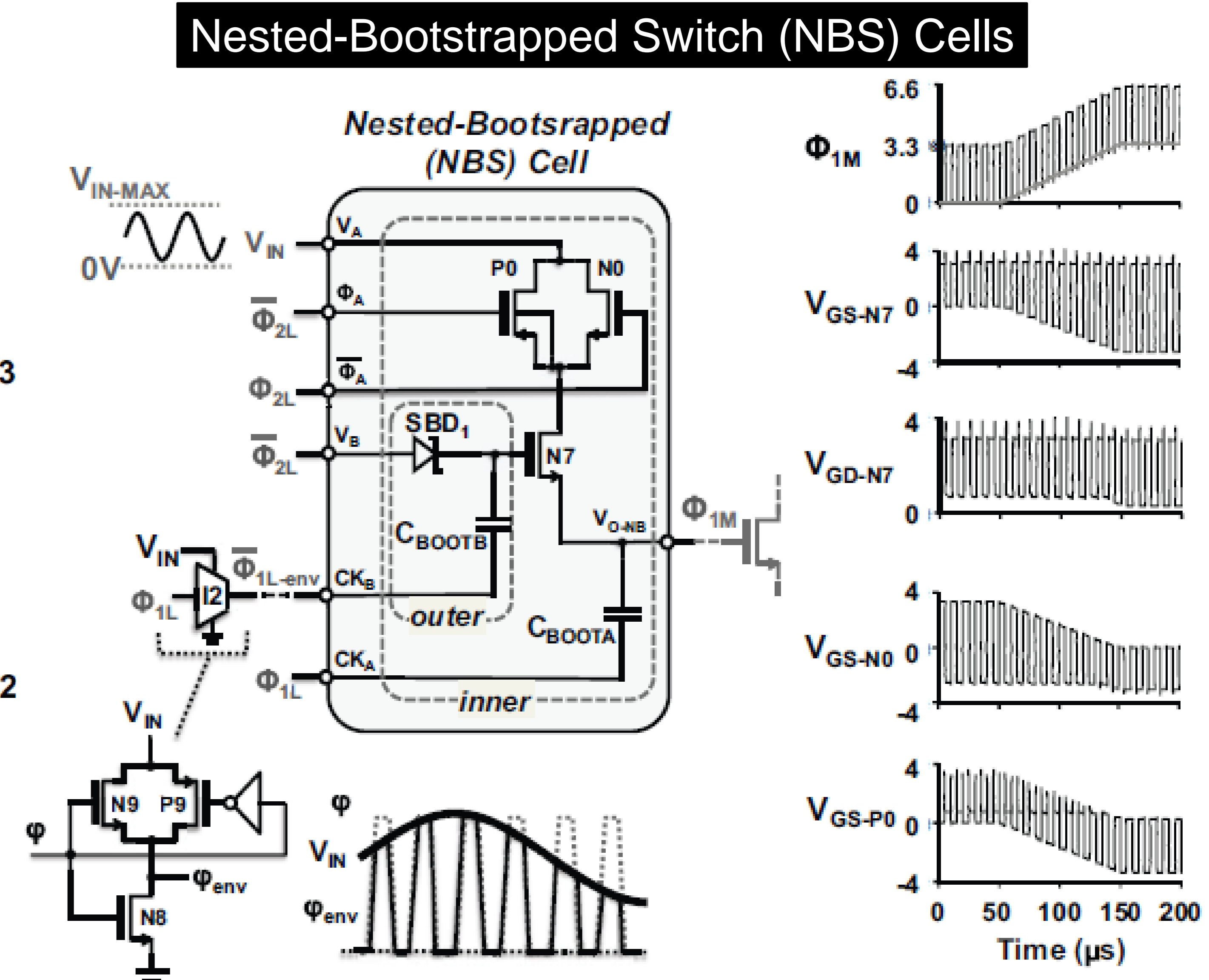
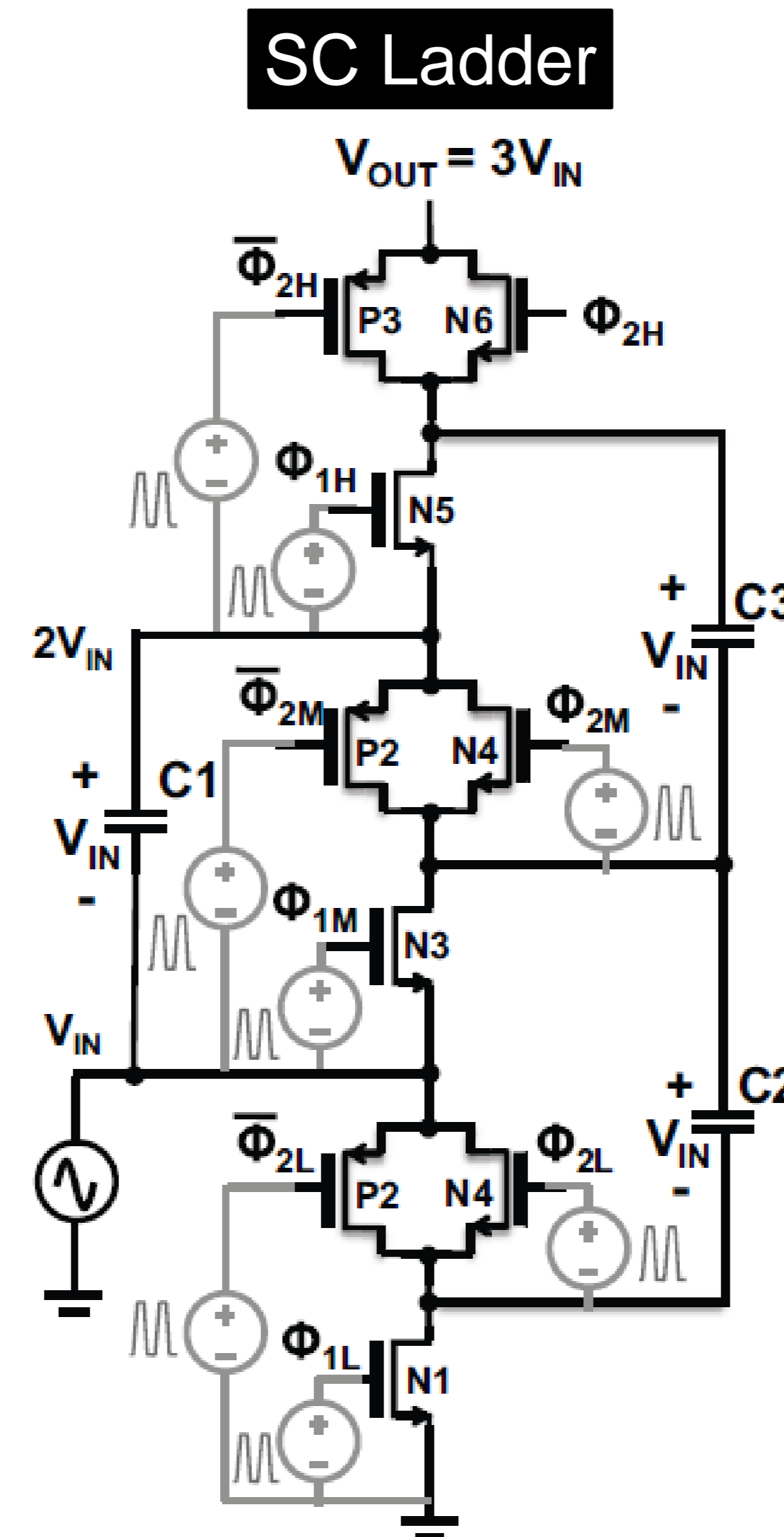
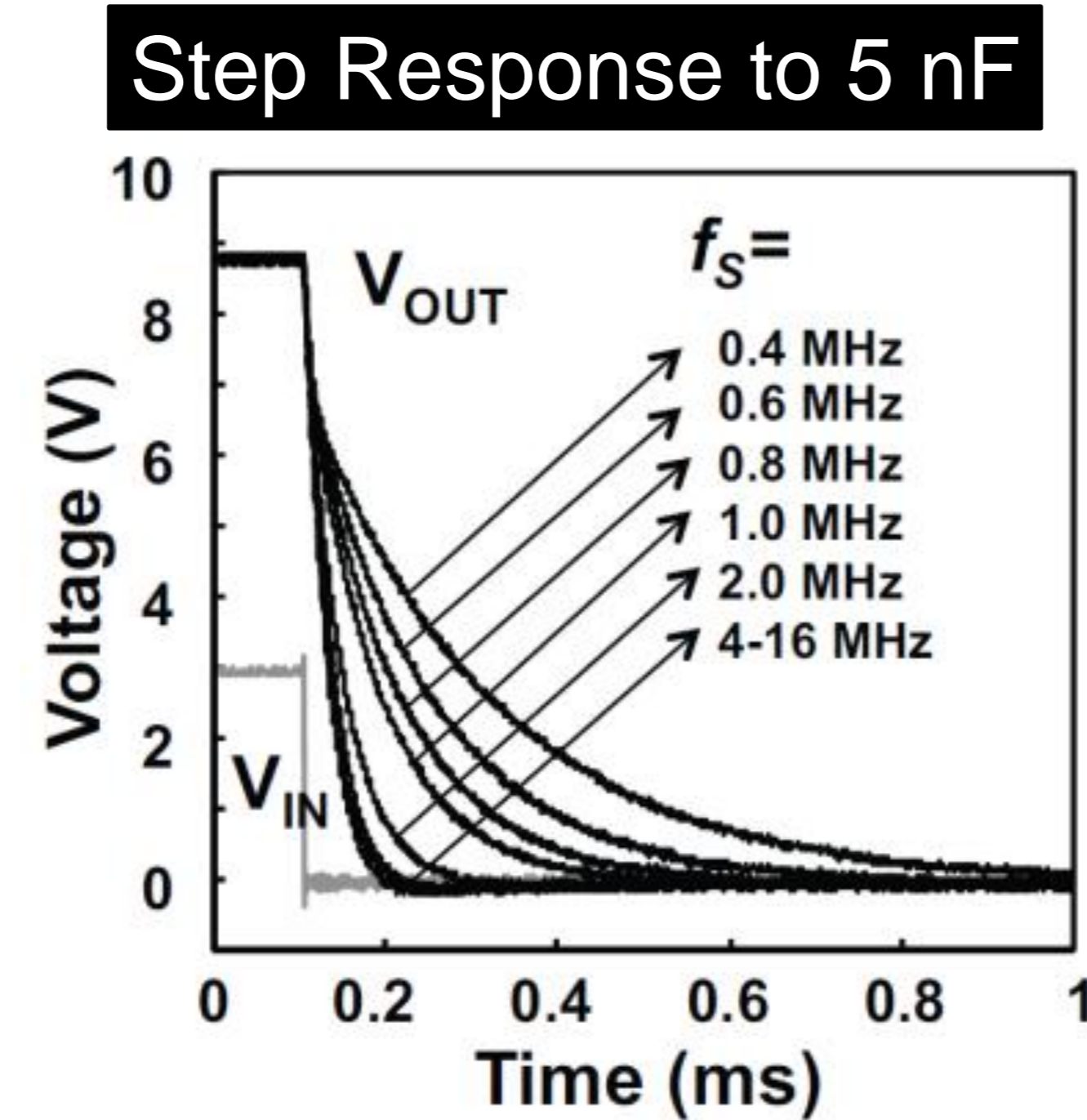
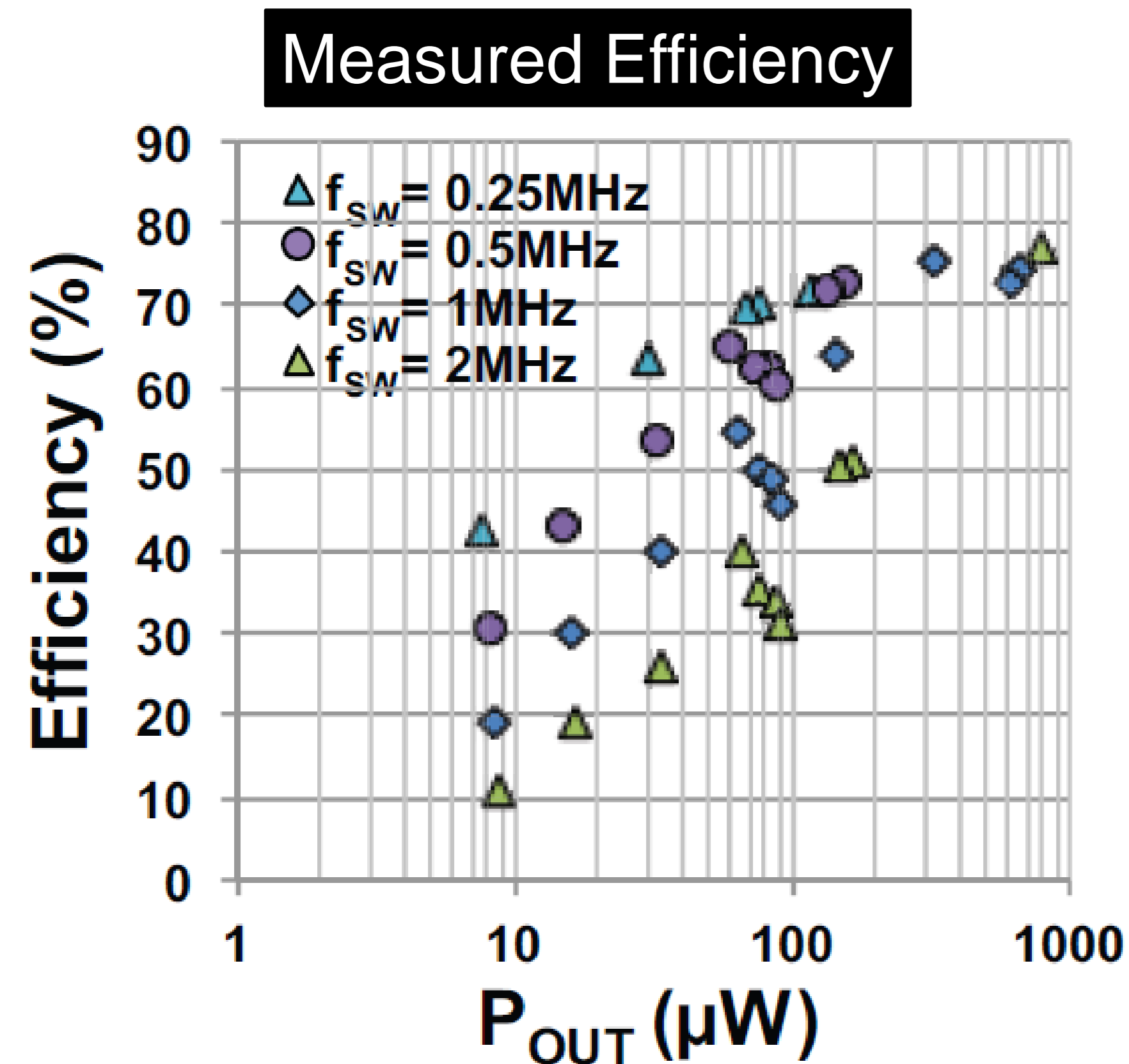
- Frontside 3 layer 10  $\mu\text{m}$  copper with spray-coated AZ4999 for interconnects and passives

## Planarity



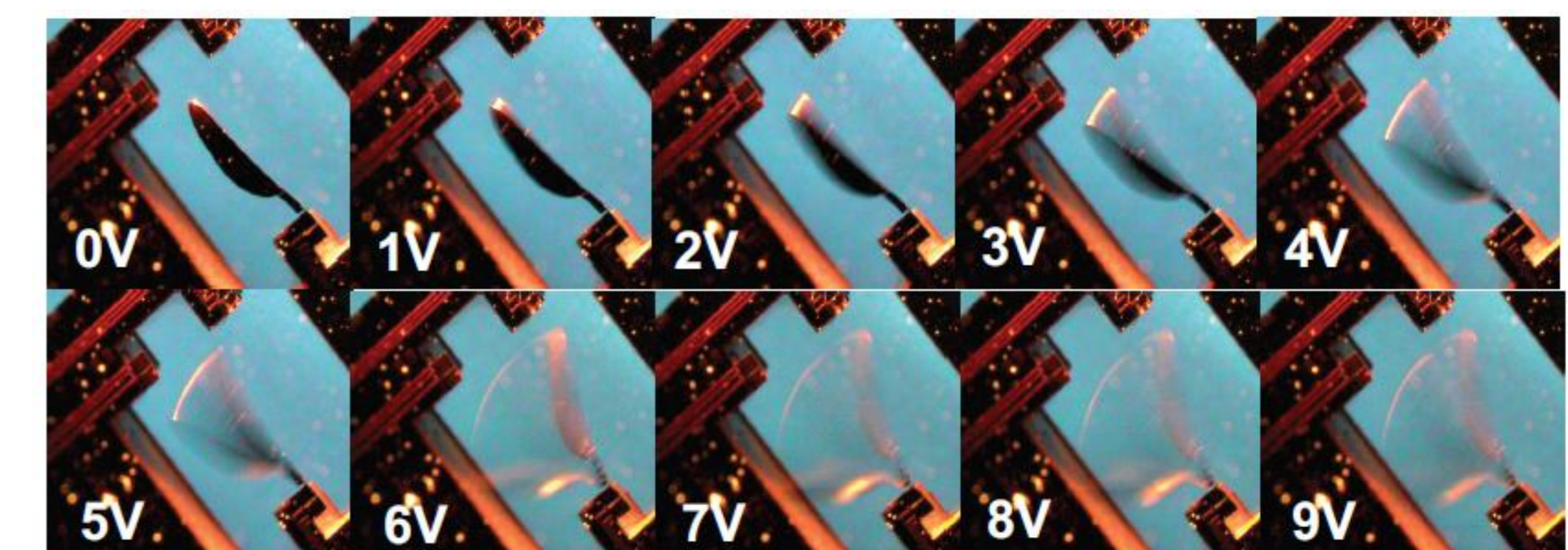
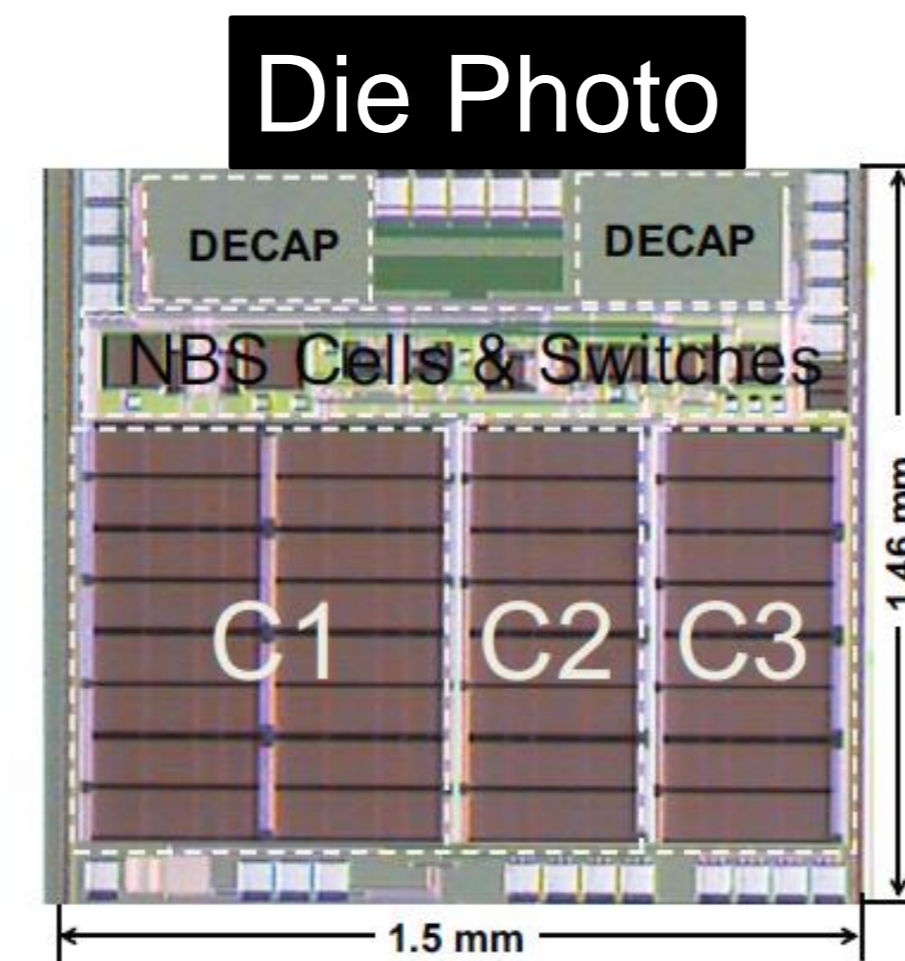
- Frontside alignment against photoresist-coated wafer for micron-level planarity over mm-scale die

- Fully-integrated (mm<sup>3</sup>) bi-directional converter driving ARL mm-scale robot wing
  - PZT actuated, 10 V, DC-500 Hz, CL=2-5 nF
- Design, model & test of switched-capacitor ladder converter w/ new voltage distributed nested bootstrap technique
- Fabricated in 0.13 μm 1.2/3.3V triple-well CMOS
- Demonstrated 3x voltage boost
- Achieved 77% efficiency with 800 μW load



mm<sup>3</sup> Converter Driving ARL's Micro-flyer

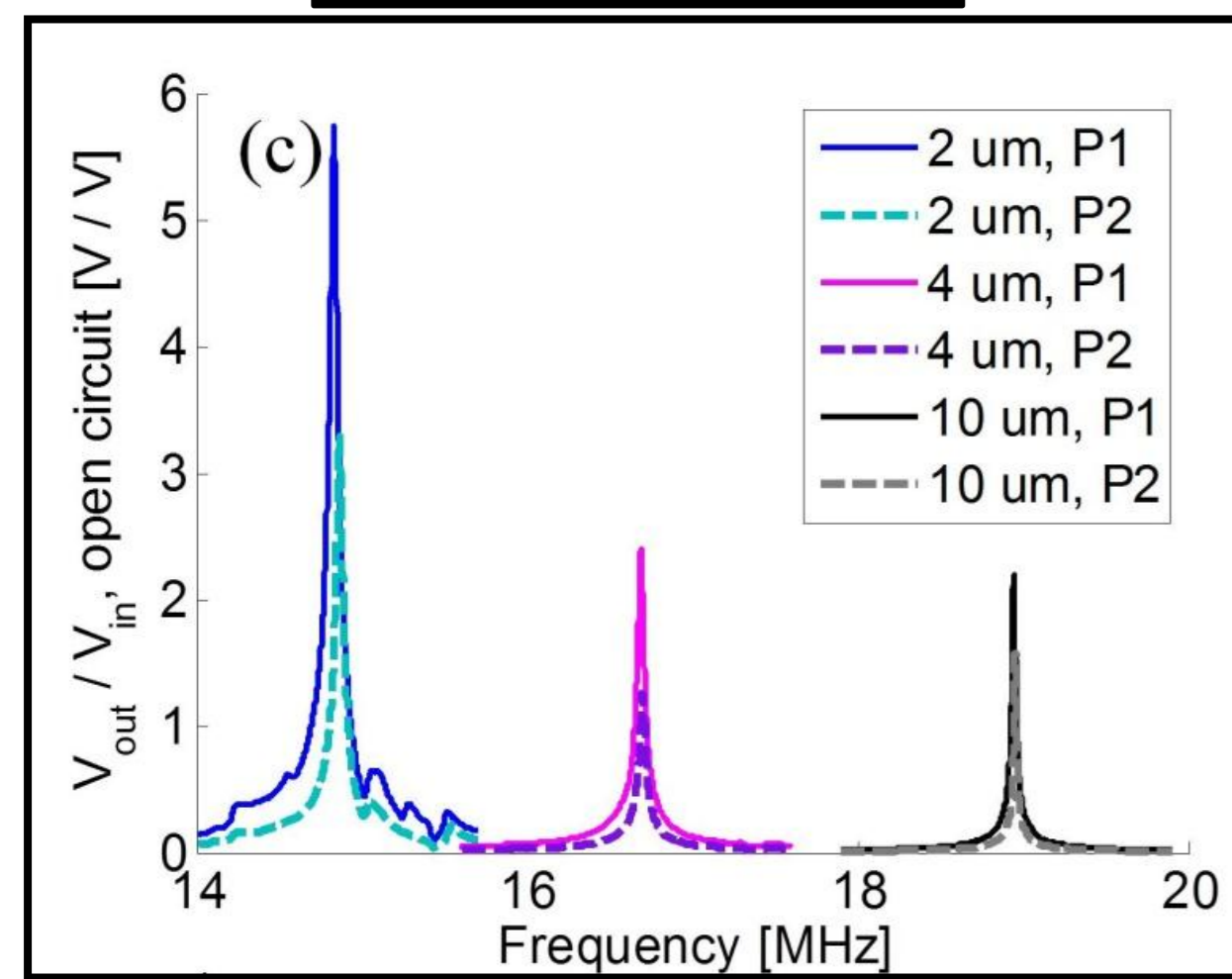
CM Dougherty, et al., "A 10V Fully-Integrated Bidirectional SC Ladder Converter in 0.13μm CMOS using Nested-Bootstrapped Switch Cells," in Symposium on VLSI Circuits Digest of Technical Papers, 2013.



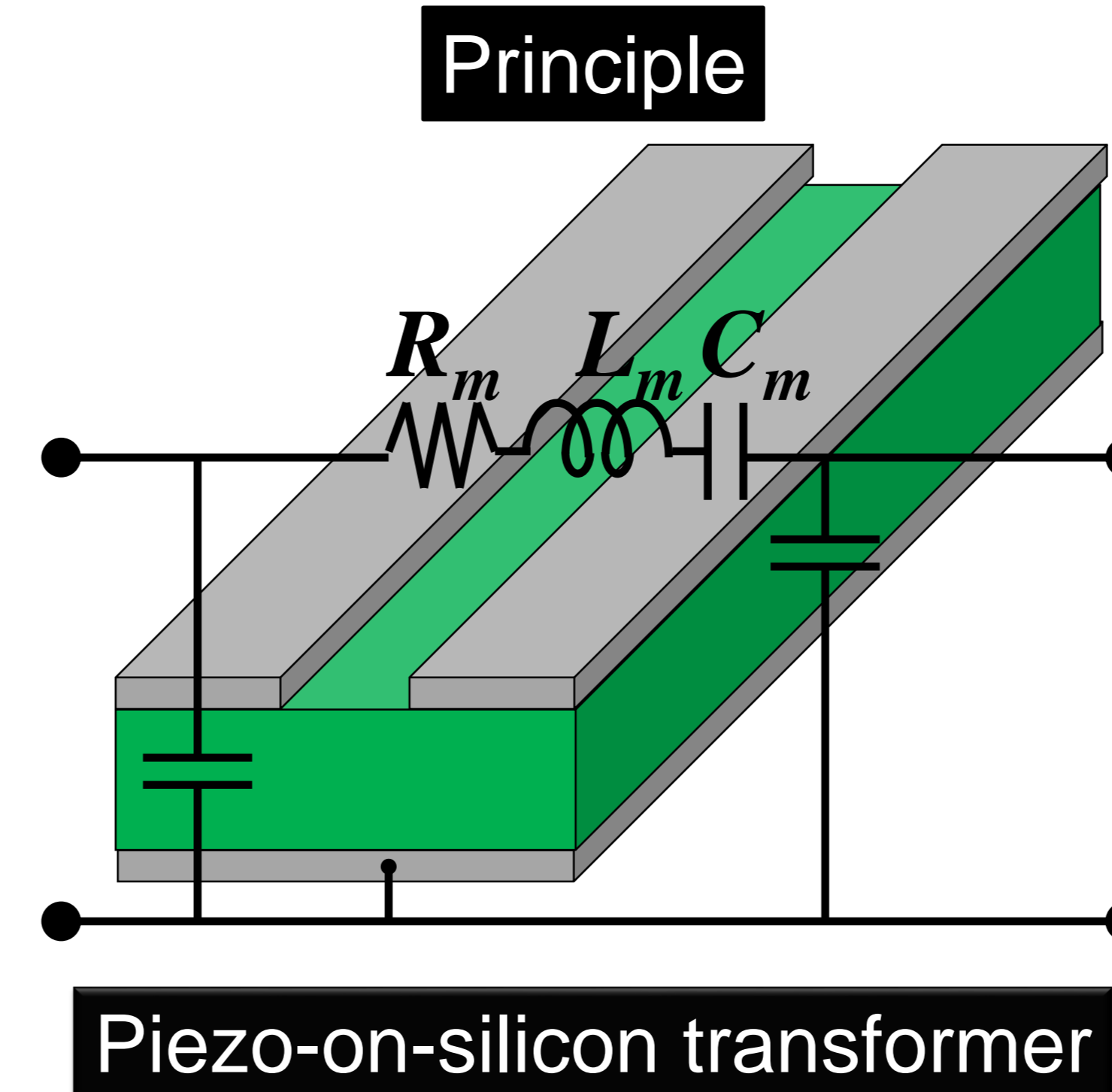
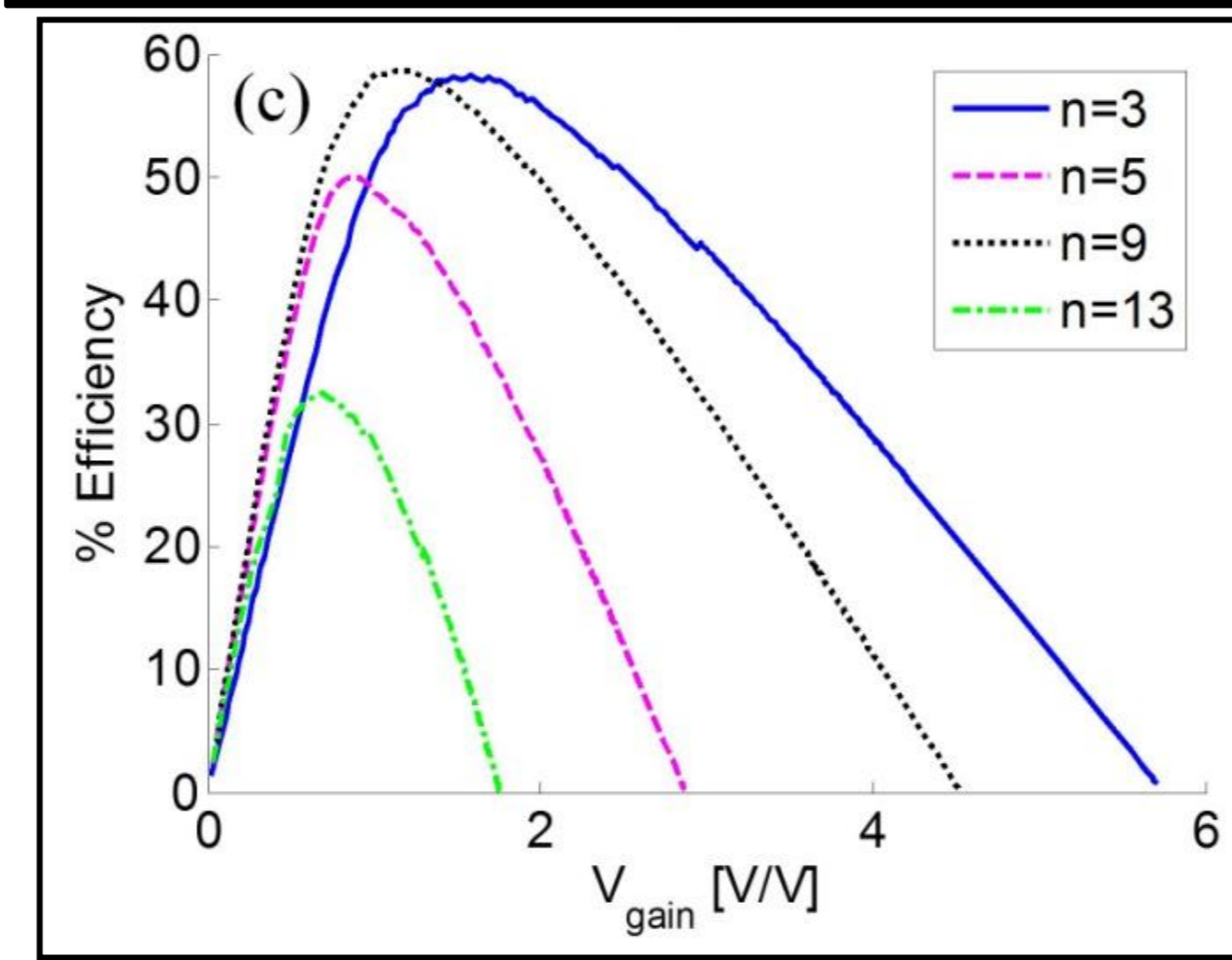
## Thin Film Piezo Transformers

- Developed analytical models describing both efficiency & voltage gain for piezo-on-silicon (composite) transformers
- Measured 6:1 voltage gain and 60% efficiency
- ~100 mW power through 30 x 70 x 4 μm thick (3 μm SOI) device, leading to > 10 Watts / mm<sup>3</sup>

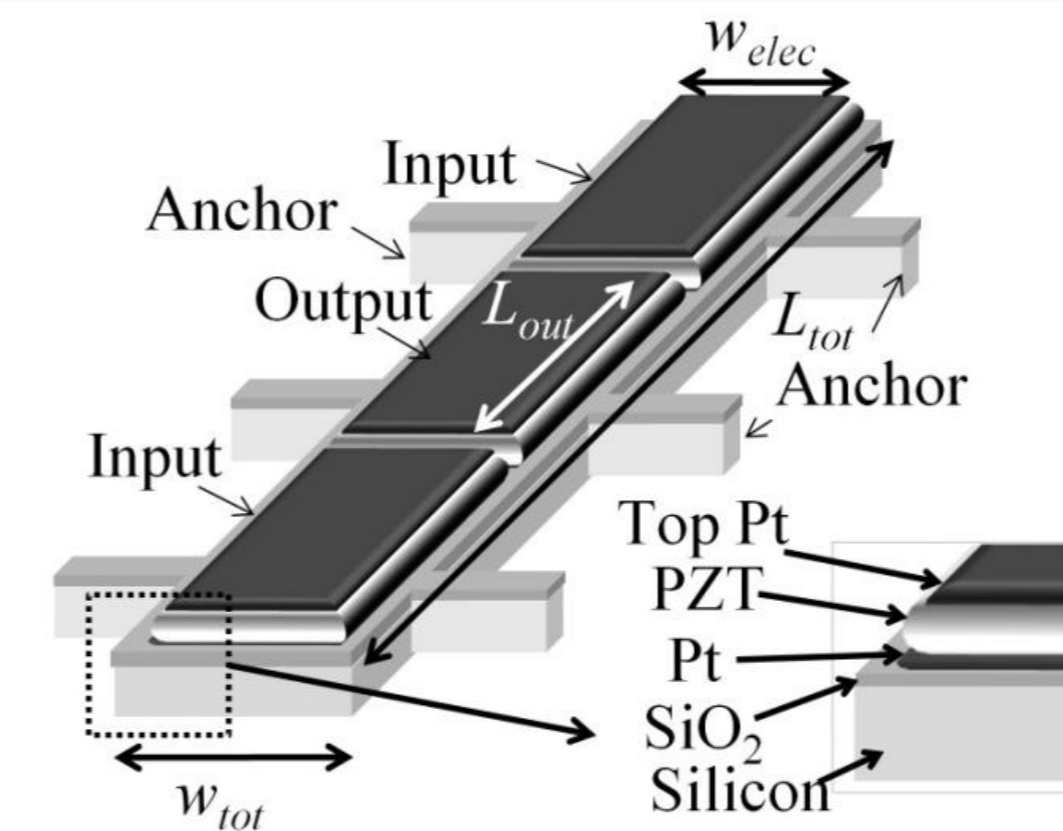
### Voltage Gain



### Voltage Gain vs. Efficiency



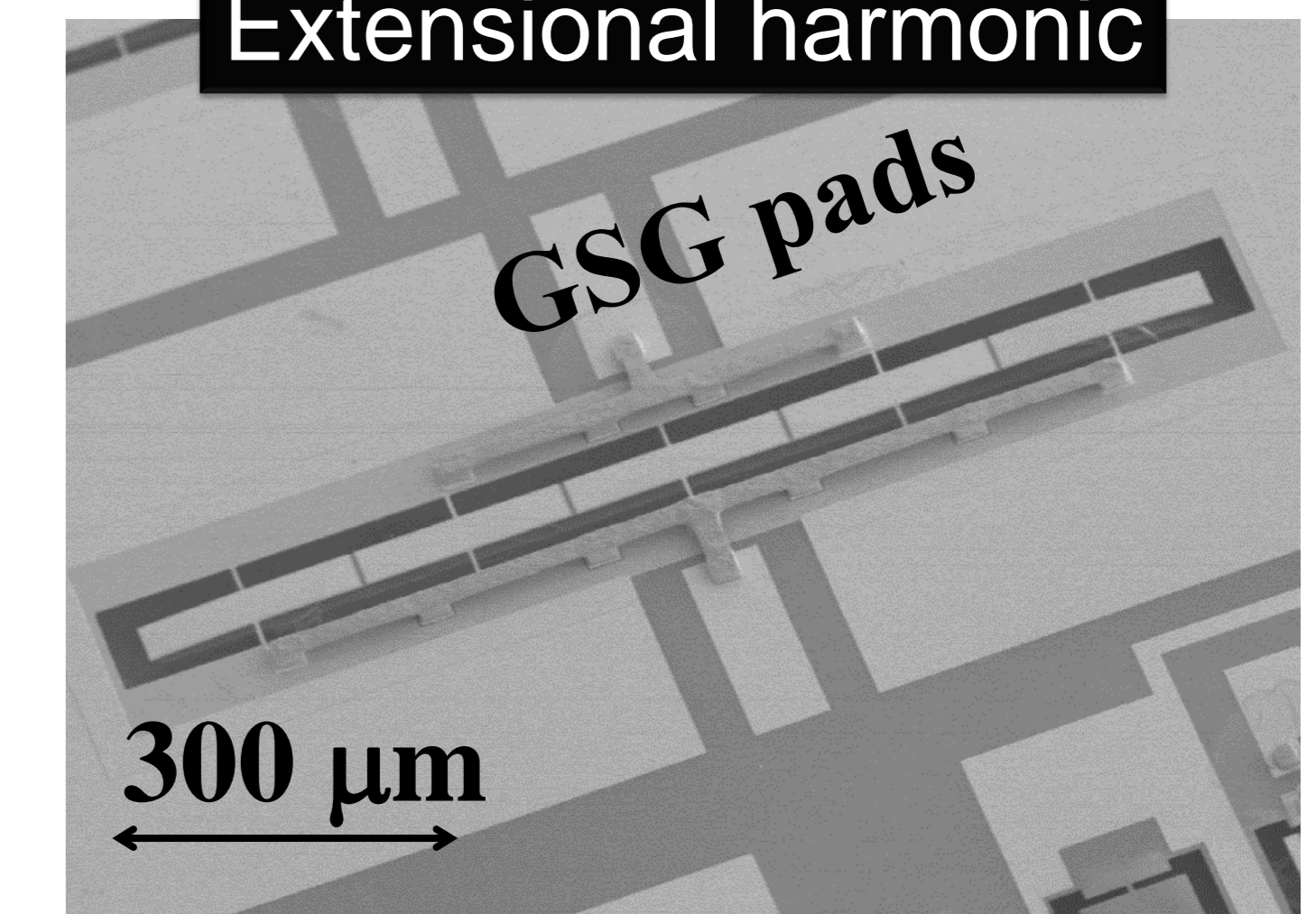
Piezo-on-silicon transformer



## Electromechanical vs. Magnetic

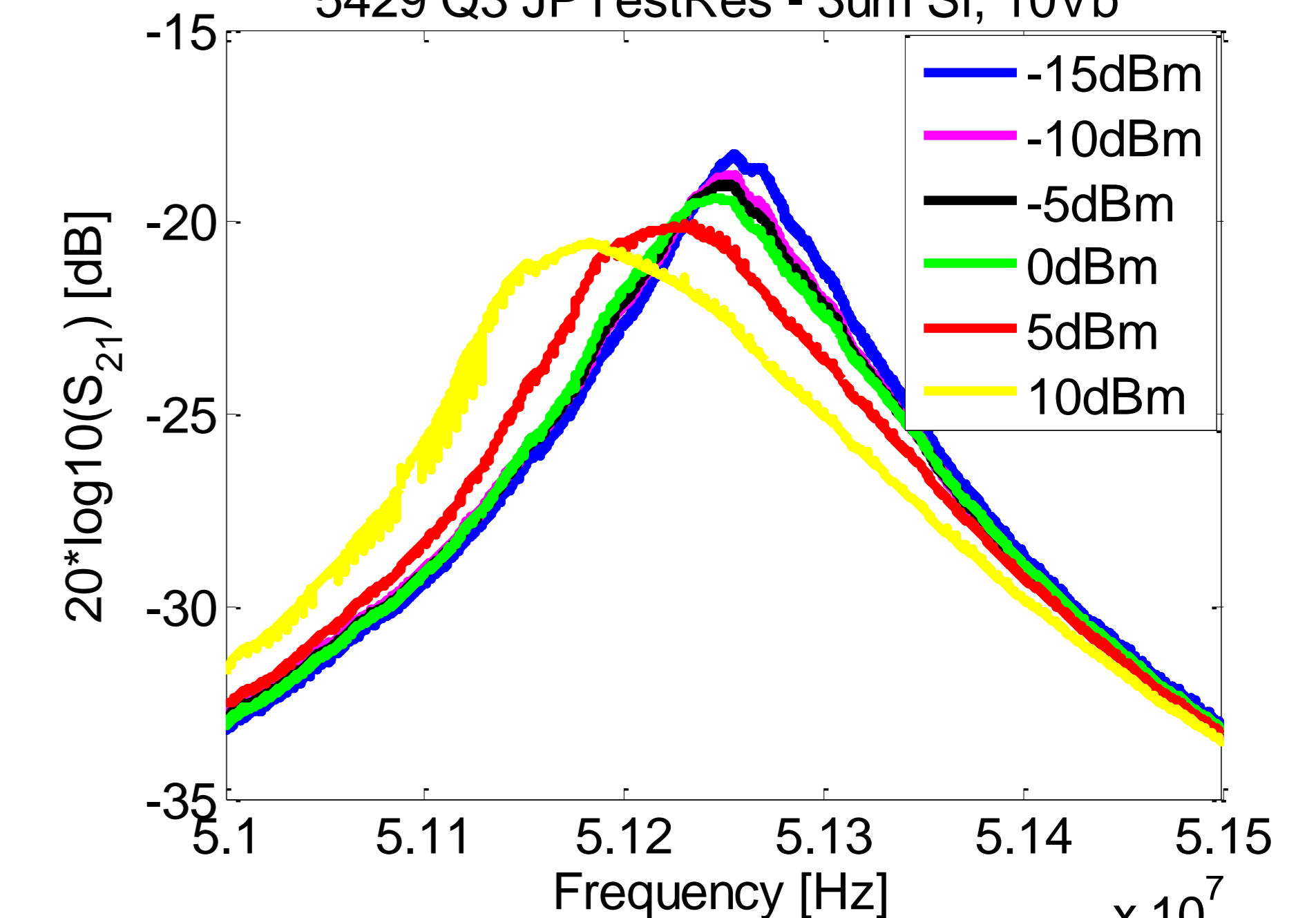
Energy Storage	Energy density	Limits	Theor. Limit
Magnetic field	$\sim \mu H^2$	Magnetic saturation	$\sim 10^4 \text{ J/m}^3$
Strain	$\sim Y \epsilon^2$	Fracture	$\sim 10^7 \text{ J/m}^3$

## Fabricated device

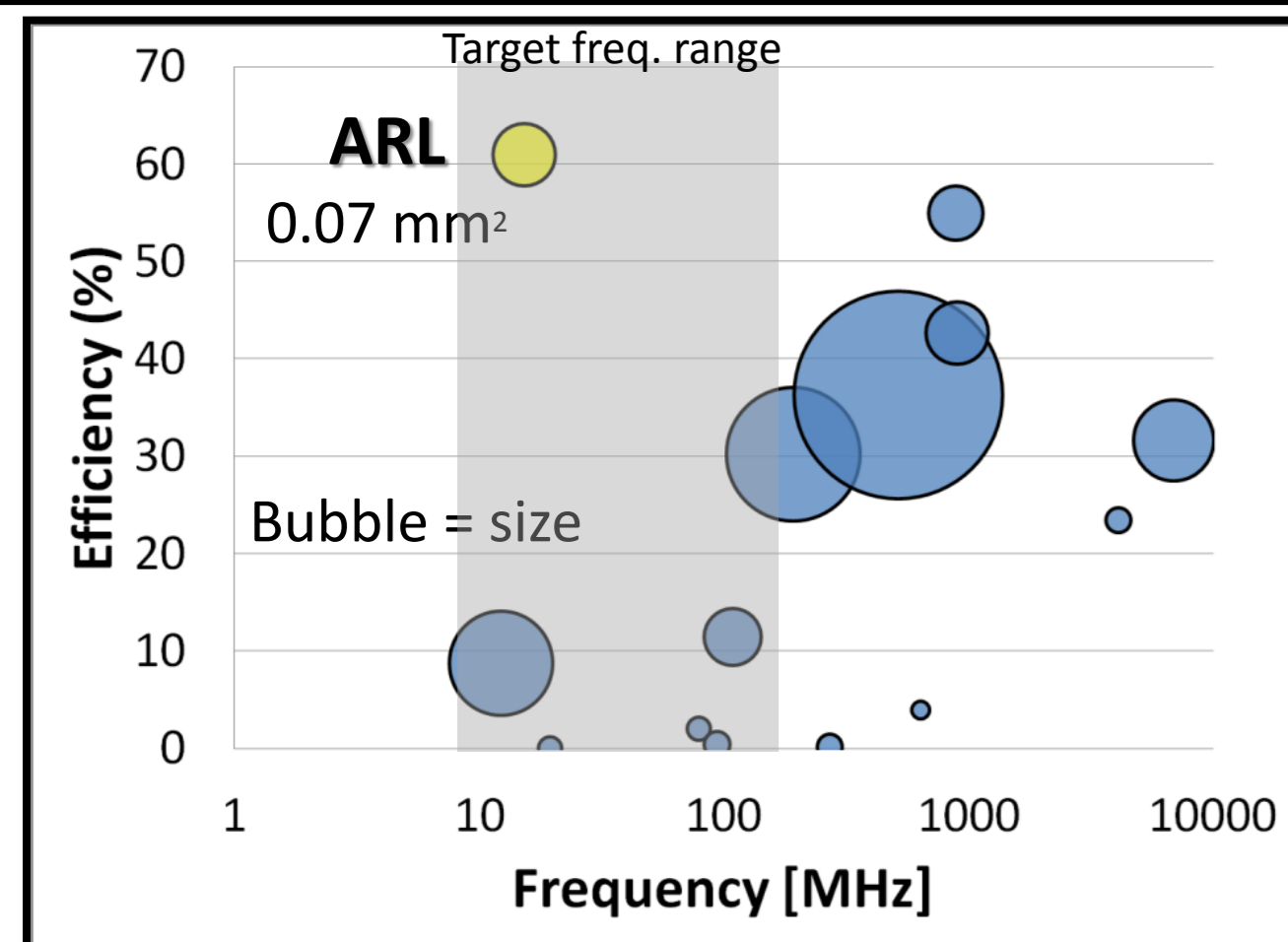


## Power Handling on Si

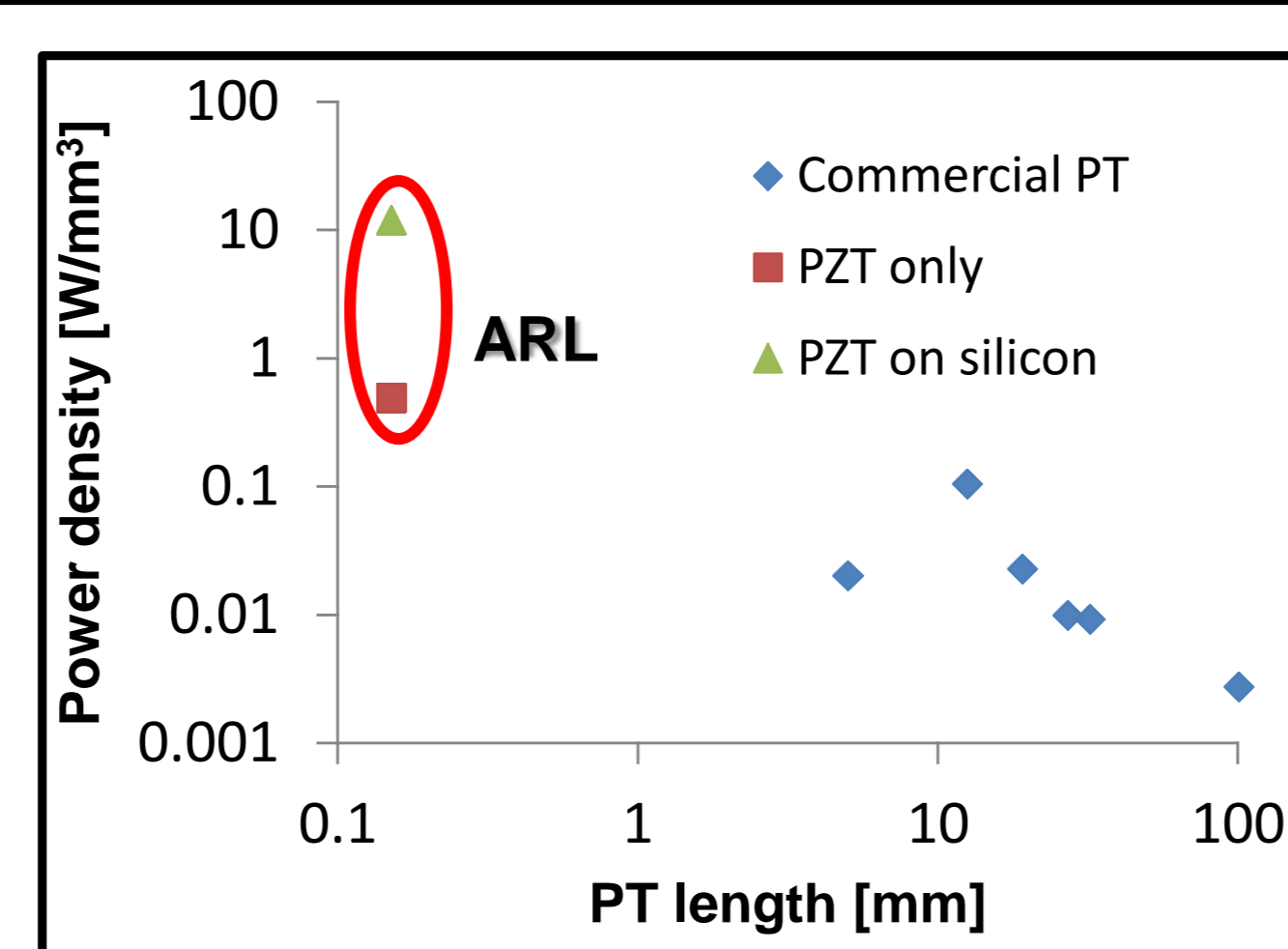
5429 Q3 JPTesRes - 3um Si, 10Vb



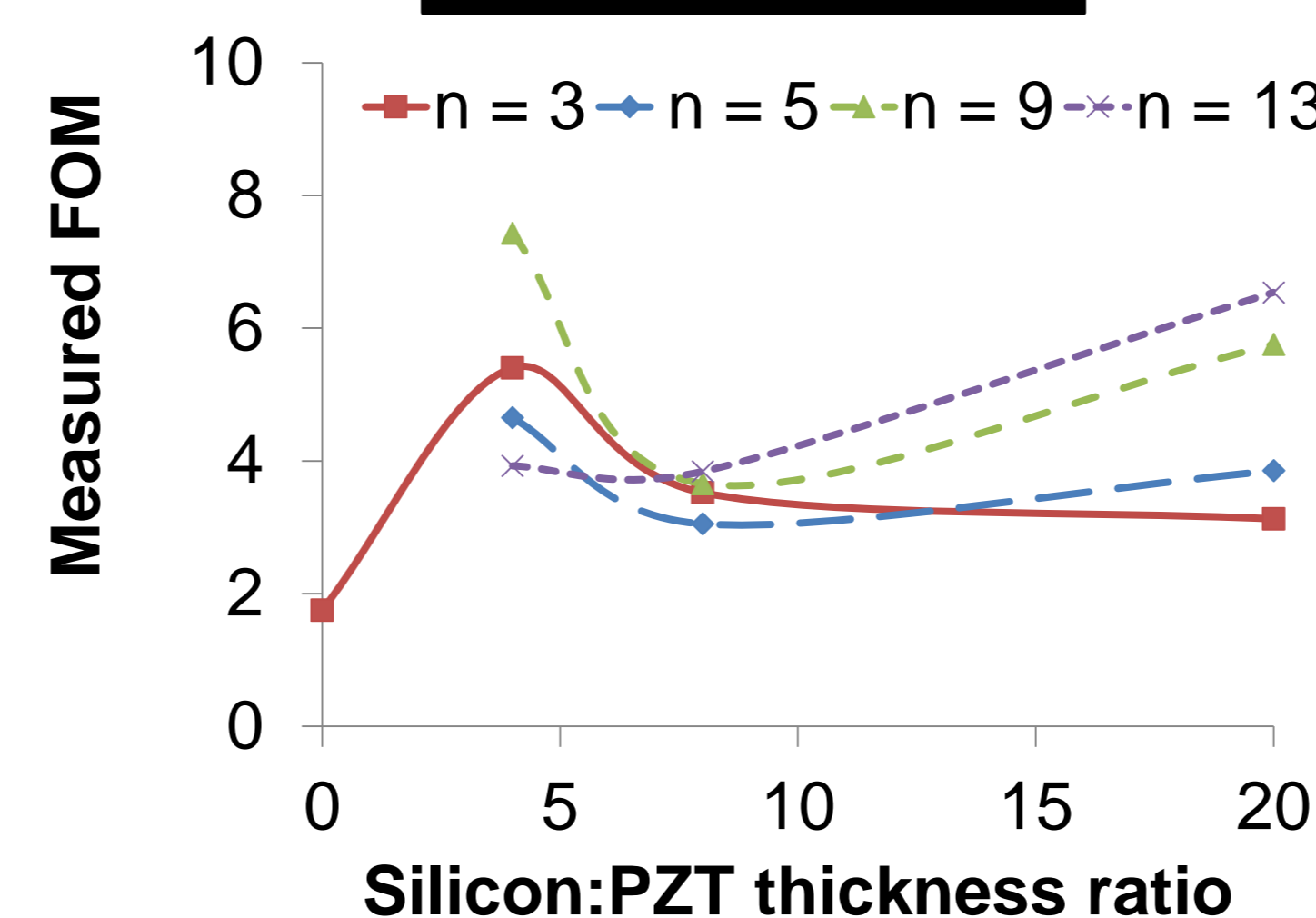
## Comparison to MEMS resonators



## Comparison to commercial PT's



## FOM = keff<sup>2</sup> Q



SS Bedair, et al., "Thin-Film Piezoelectric-on-Silicon Resonant Transformers," *IEEE J. MEMS*, vol. 22, no. 6, pp. 1383-1394, 2013.

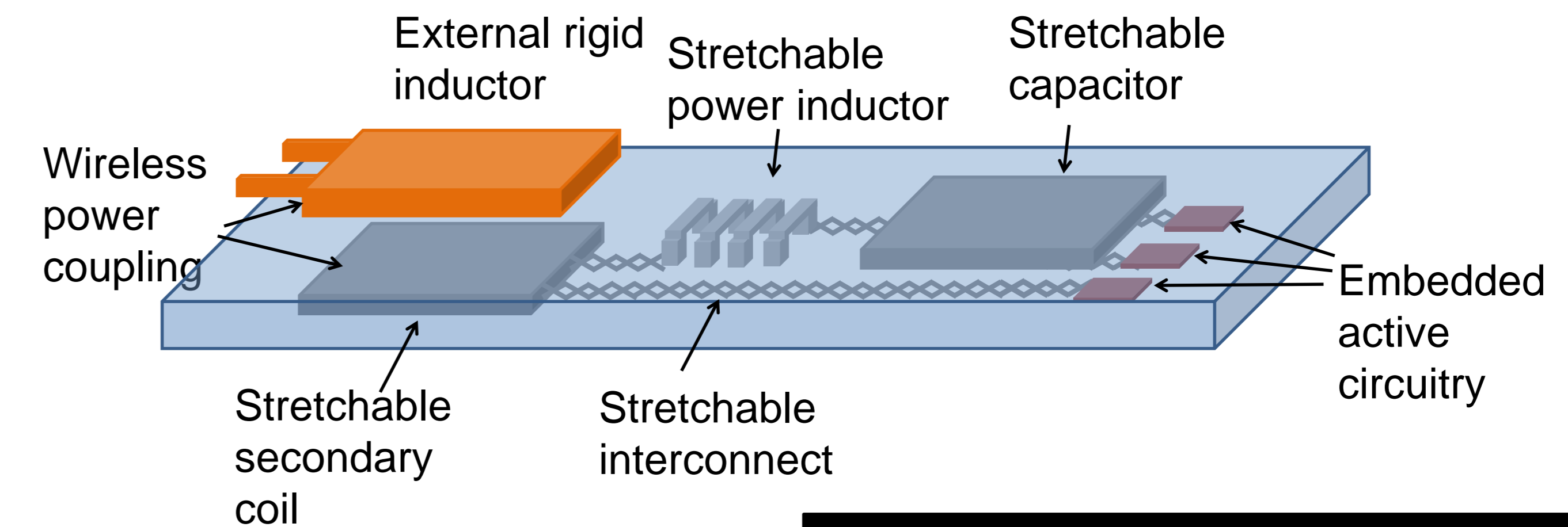
# Integrated Components for Chip Scale Power Management

Christopher D. Meyer<sup>1</sup>, Sarah S. Bedair<sup>1</sup>, Jeffrey S. Pulskamp<sup>1</sup>, Ronald G. Polcawich<sup>1</sup>, Nathan S. Lazarus<sup>1</sup>, Iain M. Kierzewski<sup>1</sup>, Xue Lin<sup>2</sup>, Christopher Dougherty<sup>2</sup>, and Rizwan Bashirullah<sup>2</sup>

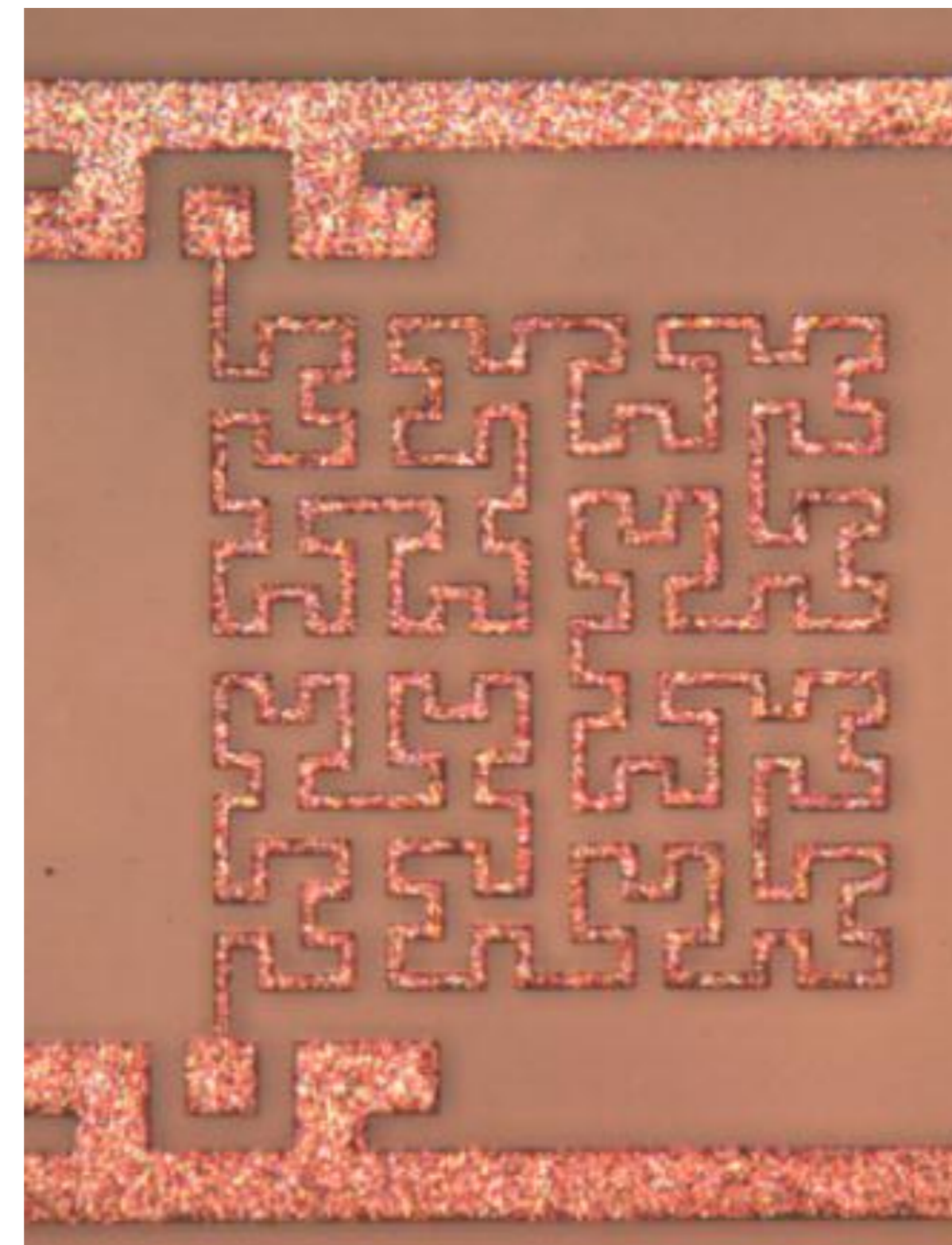
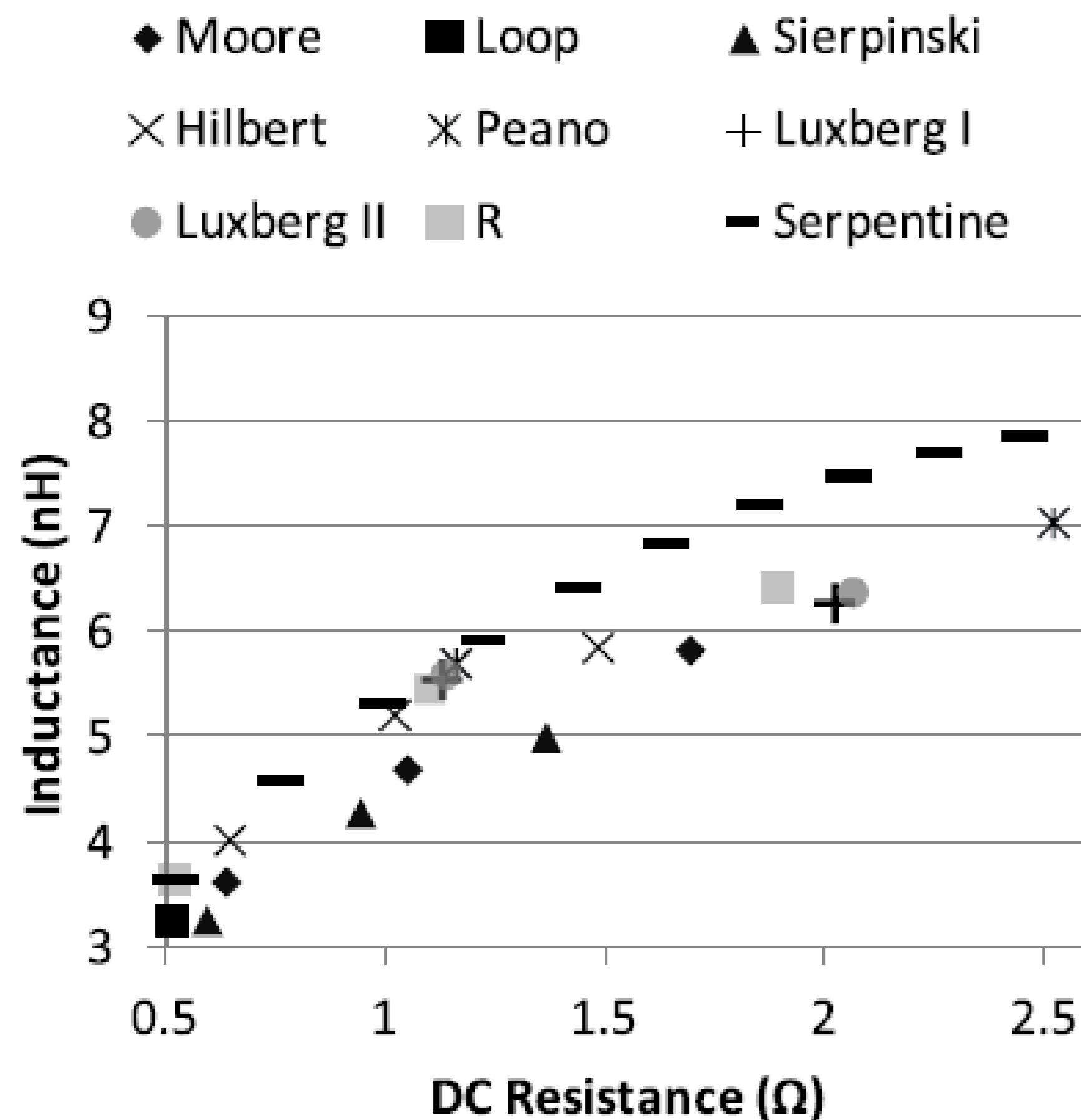
<sup>1</sup>U.S. Army Research Laboratory  
<sup>2</sup>University of Florida

- Develop power systems to allow highly efficient wireless power of stretchable systems
- Multilayer inductors based on liquid metal galinstan for 150%+ strain
  - 250 nH stacked spiral and 55 nH solenoid
- Characterization of space-filling fractal inductors with solid metal traces
  - Lower order fractals similar performance to serpentine, higher order worse
  - 10x lower peak stress than serpentine

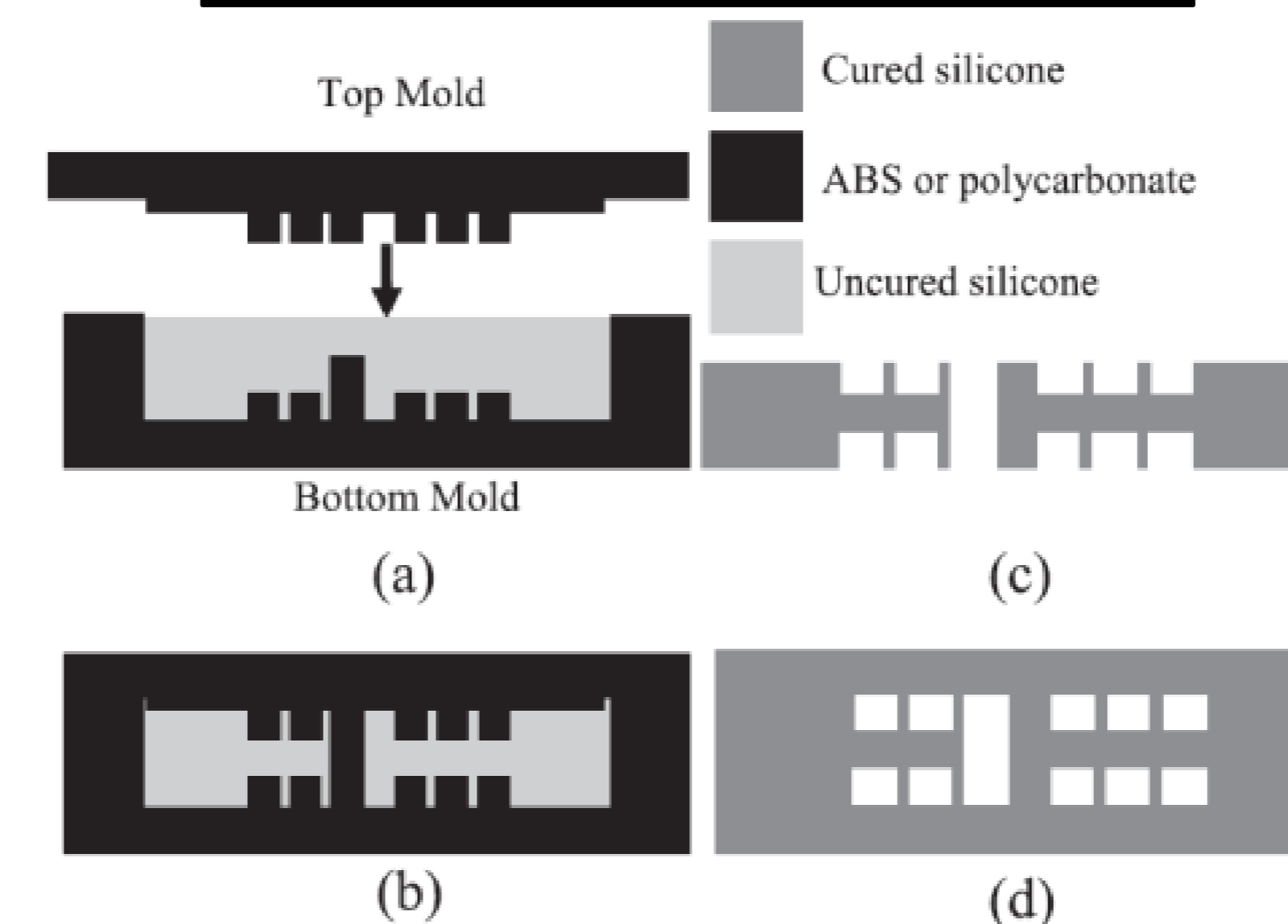
## Stretchable Power System



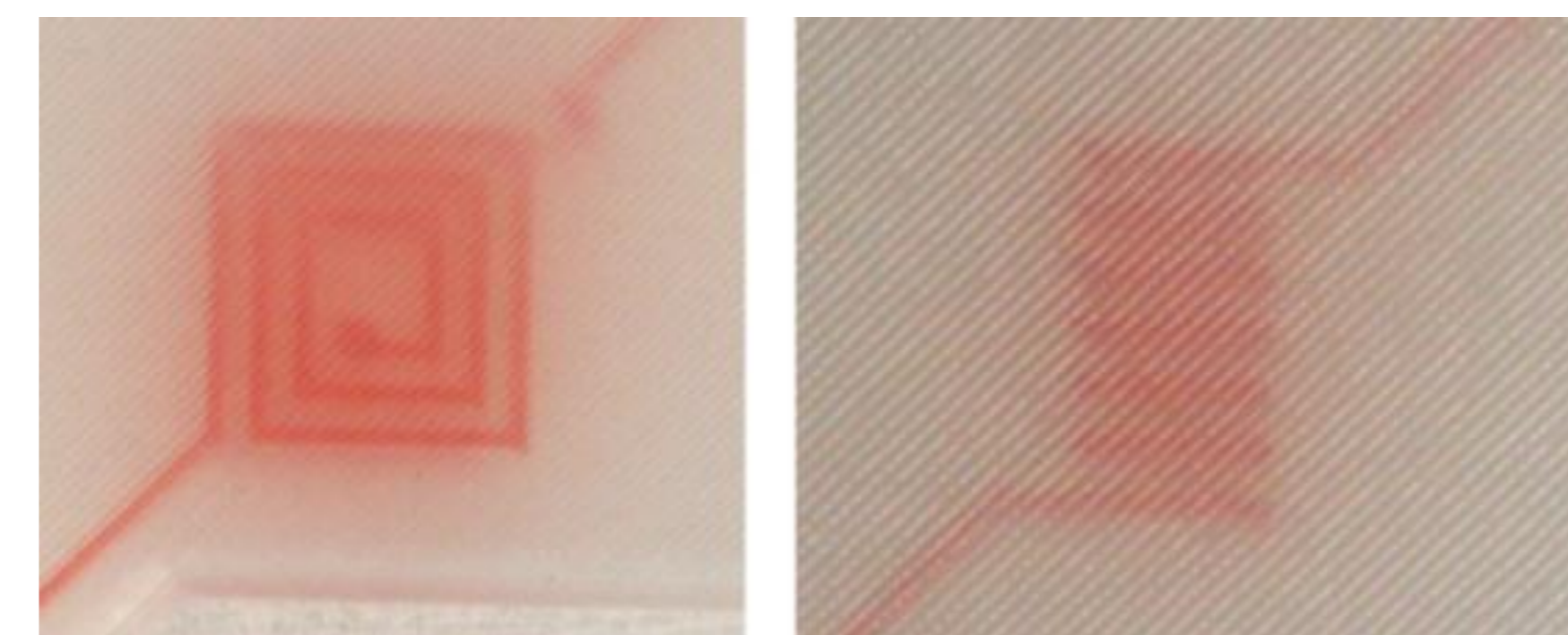
## Fractal Inductors



## Silicone molding process

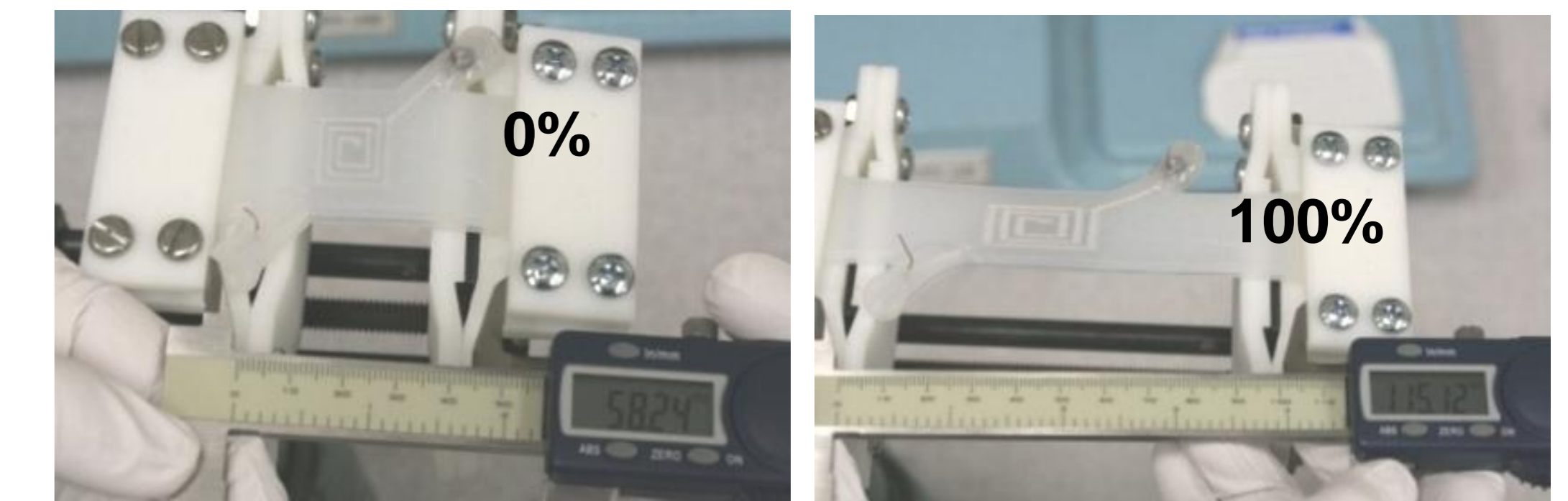


## Multilayer Inductors

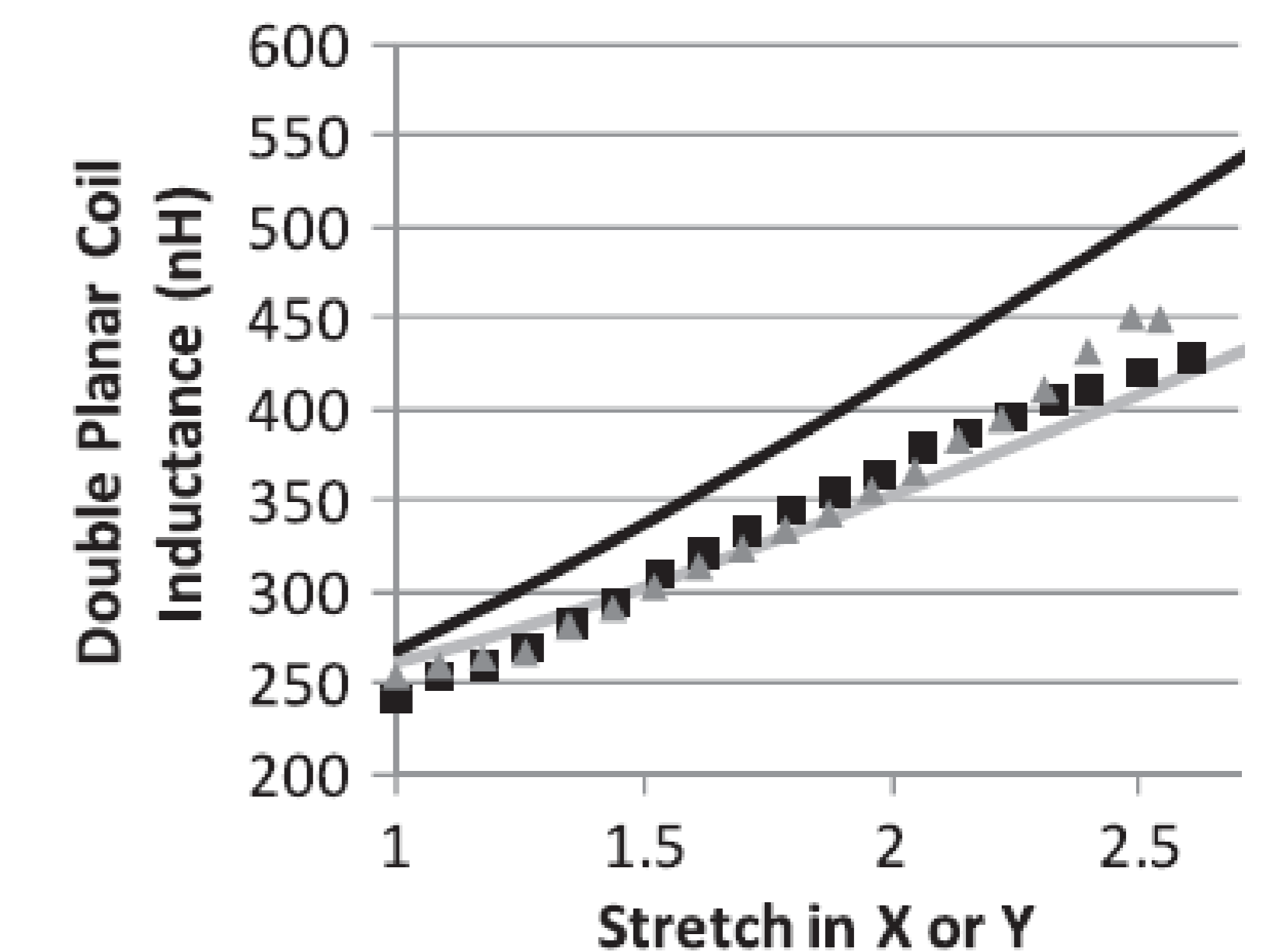


N Lazarus et al., "Multilayer liquid metal stretchable inductors," *Smart Materials and Structures*, vol. 23, no. 8, 2014.

## Liquid Metal Inductor Strain Testing



■ X direction ▲ Y direction  
— Model — Numerical



N Lazarus et al., "Fractal Inductors," *IEEE Trans. Magnetics*, vol. 50, no. 4, pp. 1-8, 2014.