Topology Comparison between Inductor, Capacitor and Resonant-based Fully Integrated DC-DC Converter in CMOS 65nm Technology

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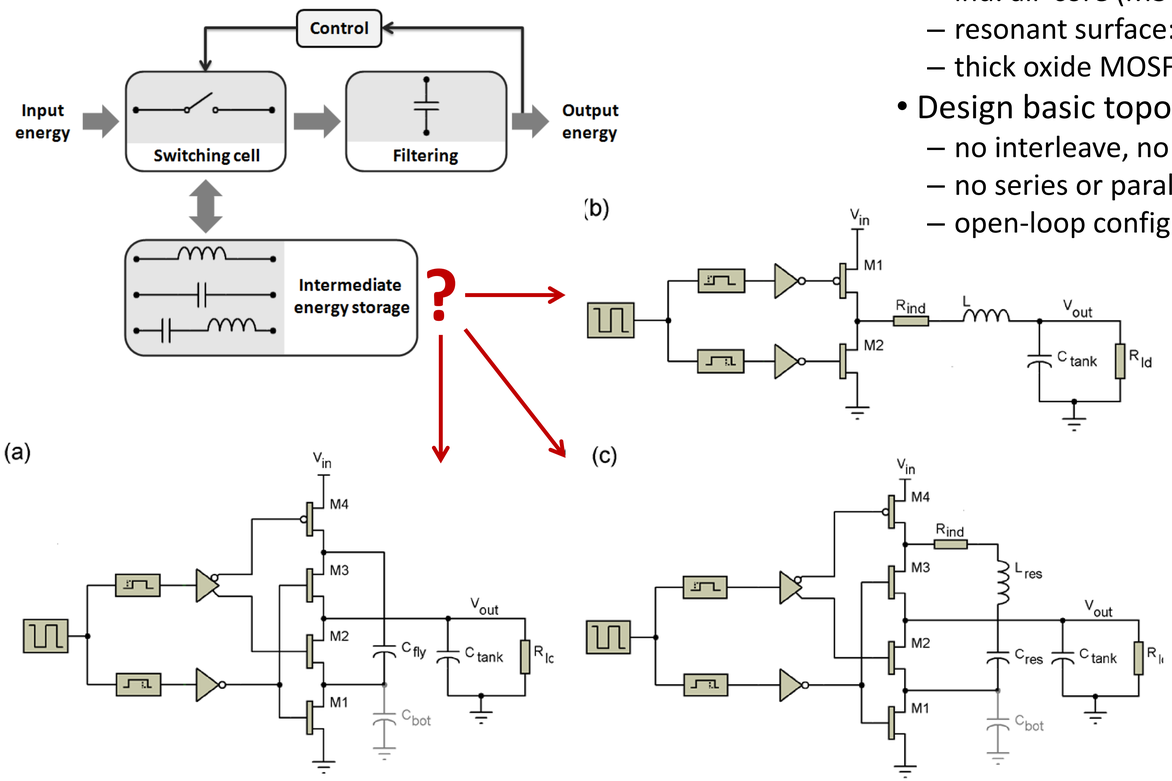
Objective

What is the "best" topology
for the full integration of DC-DC converters
in CMOS technology
to achieve the highest efficiency
on a fixed silicon die area?



(a) capacitive (b) inductive and (c) resonant-based converter under study

Methods

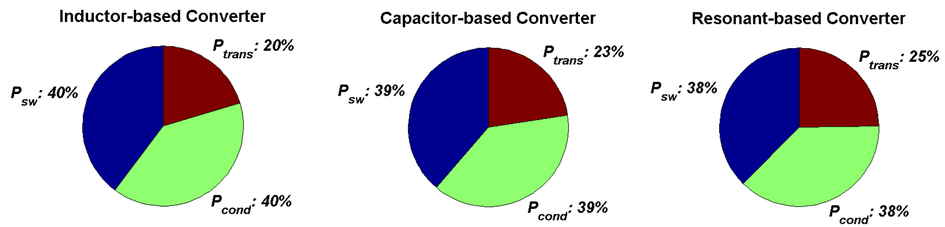
- Perform 3x3 comparisons
  - for three topologies (a,b,c)
  - for three load resistor value (0.08,0.8,8Ω)
- Use standard CMOS 65nm (ST)
  - no external component
  - cap: nw/poly and metal/metal (M1-5)
  - ind: air-core (M3-7, 1 spire)
  - resonant surface: 1/3 ind, 2/3 cap
  - thick oxide MOSFET
- Design basic topology (no refinements)
  - no interleave, no coupled ind
  - no series or parallel connection
  - open-loop configuration

Modeling & Optimization

- Identify loss mechanism
  - Switching loss P_{sw}
  - Conduction loss P_{cond}
  - Energy transfer related loss P_{trans}
- Optimize the sizing $\{W,\theta_i,f_{sw},L,C\}$
  - Efficiency driven optimization
  - First based on analytical equations
  - Then based on transitor-level simulation

Converter	Inductive	Capacitive	Resonant
P_{sw}	$Af_{sw}W$	$Af_{sw}W$	$Af_{sw}W$
P_{cond}	$\frac{F}{W}(\theta_1+G\theta_2)\left(1+\frac{H}{L^2f_{sw}^2}\right)$	$\frac{B}{W}\sum\theta_i$	$\frac{\pi^2}{8}\frac{B}{W}\sum\theta_i$
P_{trans}	$JL\left(1+\frac{H}{L^2f_{sw}^2}\right)$	$C\left(1+Df_{sw}+\frac{E}{f_{sw}}\right)$	$\frac{K}{\alpha}\left(1+\frac{N}{f_{res}^2\sqrt{1-\alpha}}\right)+Q\alpha f_{res}$

Losses analytical expressions



Losses distribution @Rld=0.81Ω

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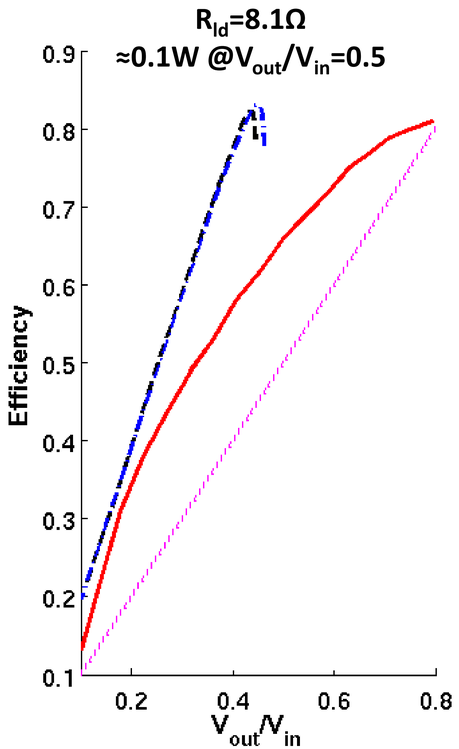
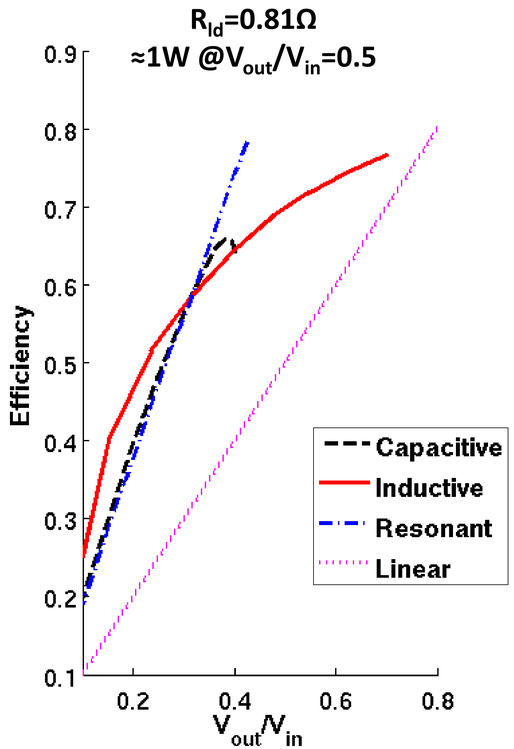
Results

Process /design parameters	Value
Input voltage	1.8V
Passive area	1mm²
Optimized point	0.9V
Switch voltage rating	2.5V
Bypass capacitor (C_{tank})	300nF
Switch resistivity	1.3kΩ.µm
Switch capacitance	1fF/µm
Capacitance density	16fF/µm²
Bottom plate capacitance	2%
Indutance FoM	7nH/Ω



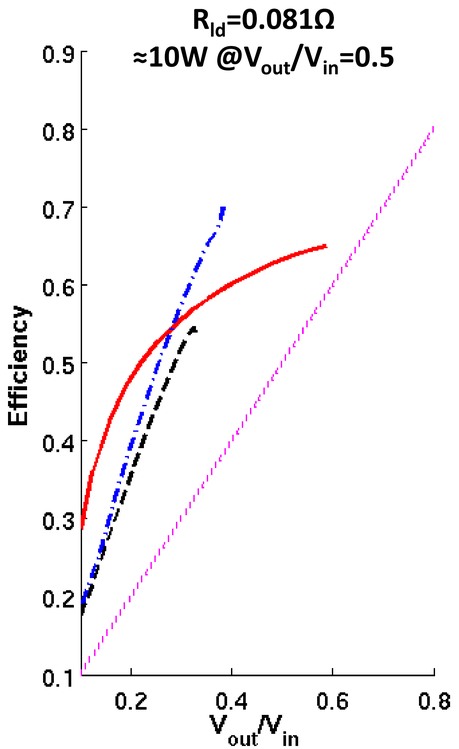
inductive < capacitive ≈ resonant

Optimal Sizing ➔	Inductive	Capacitive	Resonant
Passive value (on 1mm²)	4.2nH	16nF	0.5nH / 11nF
Switching frequency [MHz]	160	15	67
Active area overhead [%]	2	2	3
Passive energy density [nJ/mm²]	0.07	6.5	4.5



inductive ≈ capacitive < resonant

Inductive	Capacitive	Resonant
0.9nH	16nF	0.3nH / 11nF
170	50	88
6	11	6
0.3	6.5	4.7



capacitive < inductive < resonant

Inductive	Capacitive	Resonant
0.2nH	16nF	0.06nH / 11nF
145	400	200
60	56	140
0.9	6.5	6.0

Efficiency vs conversion ratio over three nominal loads - results from transistor-level simulation

Conclusion

- Passive energy density is not directly linked to efficiency
- Capacitive switching converter seems to be a relevant solution up to 0.1W/mm²
- At higher power density, resonant achieves better performance
- ¡Results strongly depend on the technology capability to integrate passive!

Discussion is open…

References

Many thanks to previous works in this topic
[1] S. R. Sanders et al. "The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach," 2013
[2] C.R. Sullivan et al., "Integrating Magnetics for On-Chip Power: A Perspective," 2013
[3] T. Andersen et al., "A 4.6W/mm² Power Density 86% Efficiency On-Chip Switched Capacitor DC-DC Converter in 32nm SOI CMOS," 2013
[4] Y.K. Ramadass et al., "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter with Digital Capacitance Modulation in 45 nm CMOS," 2010
[5] J. Wibben, R. Harjani, "A High-Efficiency DC-DC Converters Using 2nH Integrated Inductors," 2008
[6] F. Neveu et al, "Review of High Frequency, Highly Integrated Inductive DC-DC Converters," 2014
[7] K. Kesarwani et al. "A 2-Phase Resonant Switched-Capacitor Converter Delivering 4.3W at 0.6W/mm²," 2014
[8] M.D. Seeman, "A Comparative Analysis of Switched-Capacitor and Inductor-Based DC-DC Conversion Technologies," 2010
[9] R. Aparicio, A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," 2002
[10] S. Osmanaj, E. Nasufi, "Design of an Integrated Planar Inductor Using 0.35µm Fabrication Technology," 2013
..and others

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