# Quilt Packaging<sup>®</sup> Microchip Interconnect Technology

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#### Overview

- Introduction to IIC
- Quilt Packaging (QP)
  - Concept
  - Electrical Performance
  - Fabrication
  - Advantages
- IIC as an R&D partner



# Quilt Packaging (QP) Technology

- Edge-connections joined to create multi-chip "quilt," developed at Notre Dame
- "Monolithic" assemblies from same or disparate materials & process technologies
- Enables optimization for cost and functionality
- Alternative or complementary technology
- Industry-standard tools and fabrication processes







#### **QP-Interconnect Structures**

- Edge connection structures called "nodules"
- Solid metal, typically 10-200 um wide, ~ 20-50 um thick
- Customizable shapes-including interlocking-enables sub-micron chip alignment





### QP Customizable I/O



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### Sub-Micron Chip Alignment





Interior (left) of four-chip quilt (above)

QP enable extremely accurate alignment



**—** = 30 micron

### **QP** Microwave Performance



Less than 0.1 dB insertion loss from 50 MHz past 100 GHz, with no resonances. Recent unpublished results under 0.9 dB at 180 GHz



## QP Eye diagrams

- Measurement of 12 Gb/s eye pattern (Anritsu MP1763B)
  - Horiz. 100 mV/div
  - Vert. 20 ps/div
- Data stream: 2<sup>31</sup>-1 pseudorandom bit sequence
- Nearly ideal interconnect performance; indistinguishable from PG.
- Error-free operation
  - SNR (Q) = 12.9 for pattern generator alone, 12.4 after chip-to-chip interconnect



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### **QP** Time-Domain Performance

**/oltage** (V)

- Single-ended GSG CPW configuration
- Picosecond Pulse Labs 4022 TDR pulse enhancement module:
   < 9 ps risetime</li>
- Total delay including probe pads, launcher: 7 ps (820 µm length)
- Delay due to QP nodules: 2.7 ps



Time (ps)

100  $\mu m$  nodule compared with pads/launcher, GSG



## Advantages of Quilt Packaging

- Optimized integration of disparate materials and process technologies (Si, GaAs, GaN, AlN, more)
- Chip partitioning for optimal yield/functionality
- Increased cross-sectional area vs. WBs, bumps
- Better thermal management & failure modes compared to WB
- Reduced design time due to applicability of current 2-D tools, design re-use
- IP flexibility, security



### **QP** Process Flow Overview

- Very similar to "via-middle" TSV process
- Utilizes industry-standard tools & processes
- At least 2 additional mask steps
  - Nodule definition
  - Separation
- Most unique feature is dry etch step for singulation
- After assembly, handle as if "normal" chip



#### **QP** Fabrication-Nodule Definition





#### **QP** Fabrication- Nodule Metallization





### **QP** Fabrication-Die Singulation





## QP Assembly

- Multiple approaches to connecting die
  - Solder, solder paste, and reflow
  - Laser welding
  - Solder-free (gold coating, epoxy in place)
- Can be automated with modifications to pick & place tools
  - Sub-micron chip-to-chip alignment





# "3D-QP" and "Interposers"

- QP can enable multiple
  3D configurations
- 3D-QP retains many advantages of 2D-QP
- "Quilting" interposers can decrease formfactor
- Systems benefit from QP without having to redesign chips



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## **IIC Fabrication Services**

Contract R&D Experience:

- Materials Deposition
- E-Beam Lithography
- Specialty Plating
- DRIE & ICP etching
- IC & MEMs prototyping
- Magnetics/nanomagnetic fabrication & testing
- SEM, AFM, EDX, FIB analysis
- CMP & wafer grinding





## **Additional Material**

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### Thank You!

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