Fine-Grain Power Management in Multicore SoCs using Integrated Voltage Regulators

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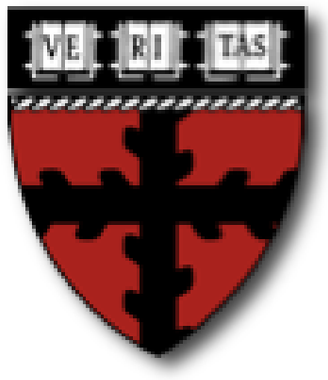
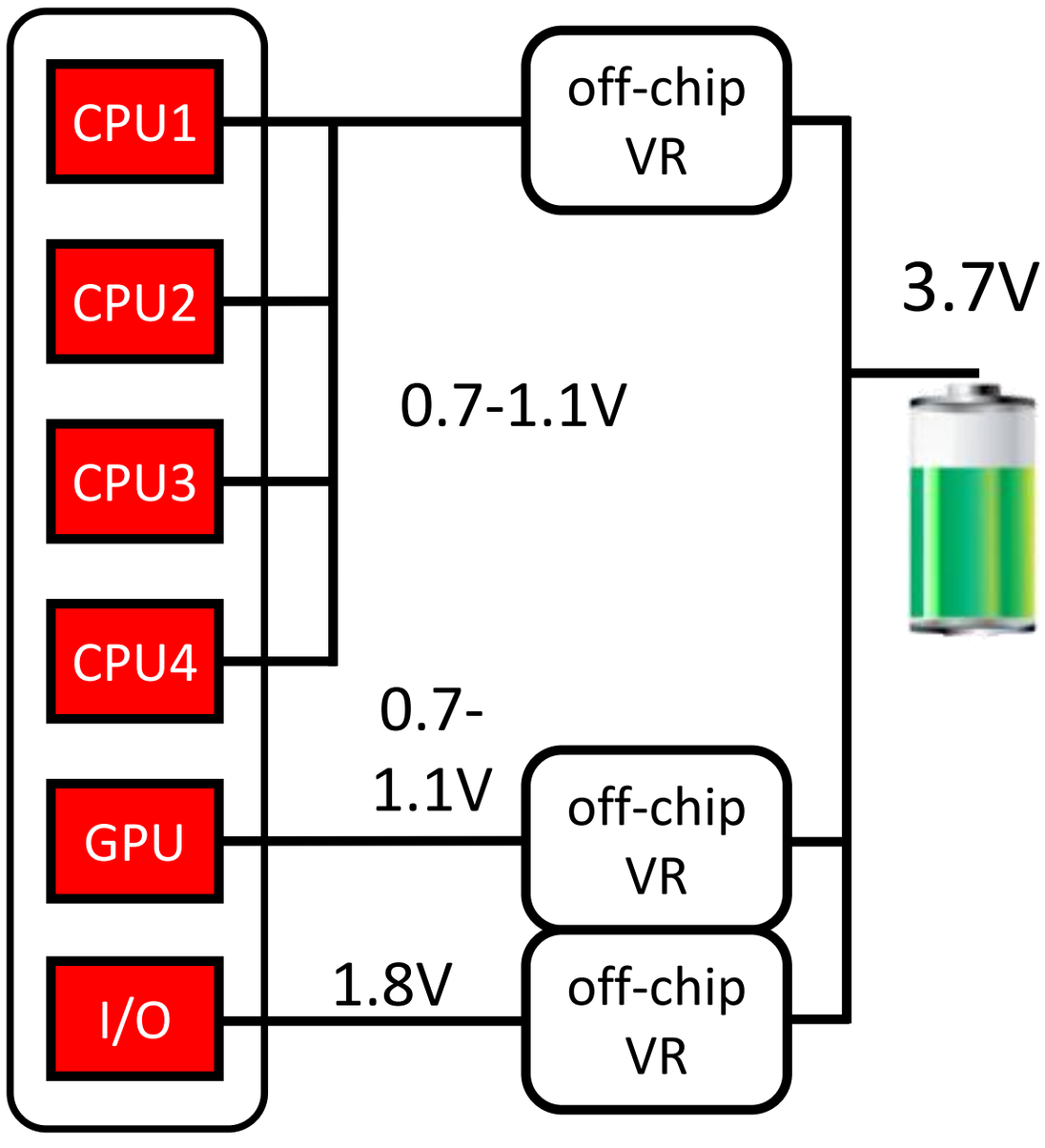
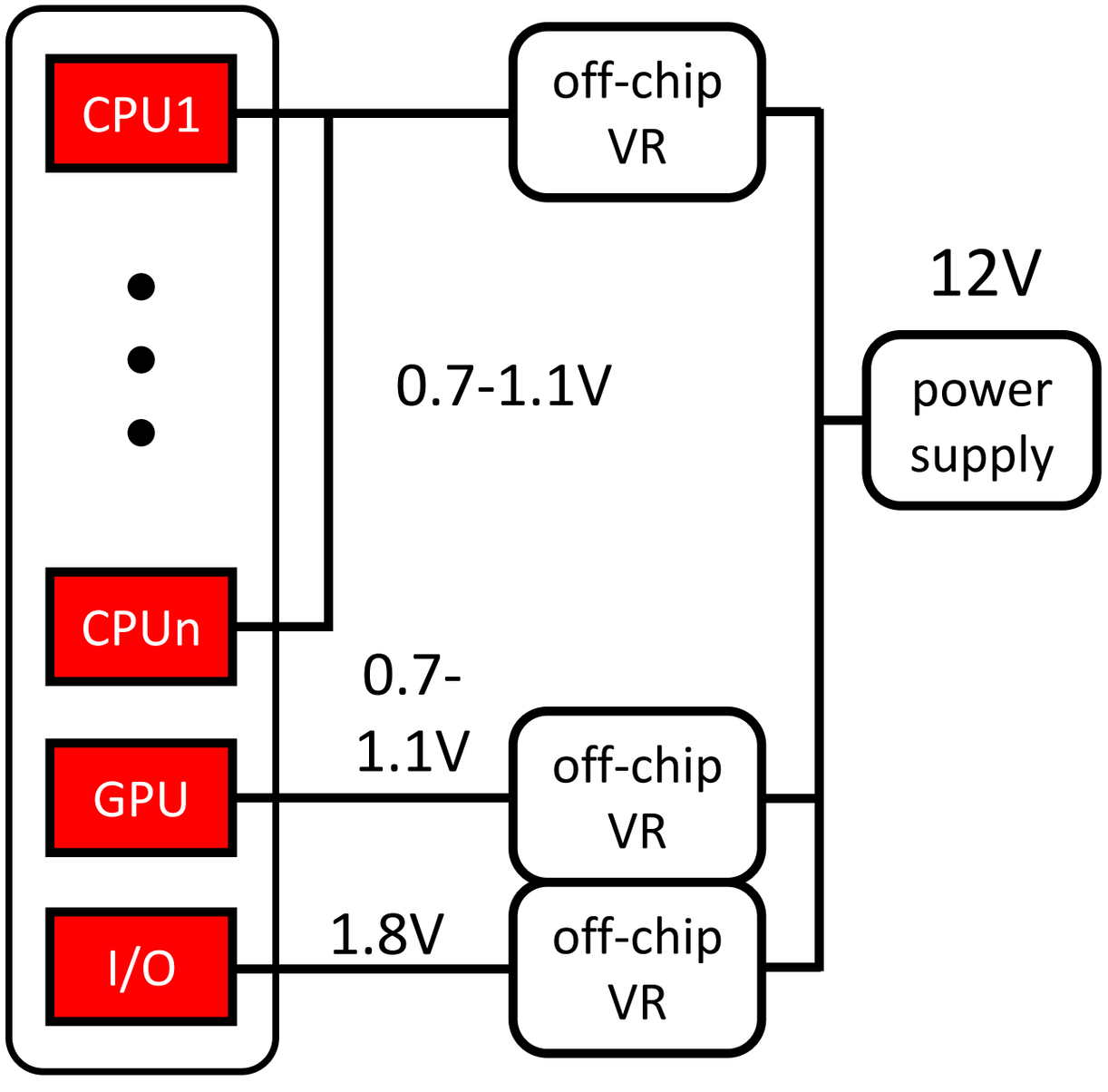


Power delivery in mobile and server systems look similar



mobile SoC

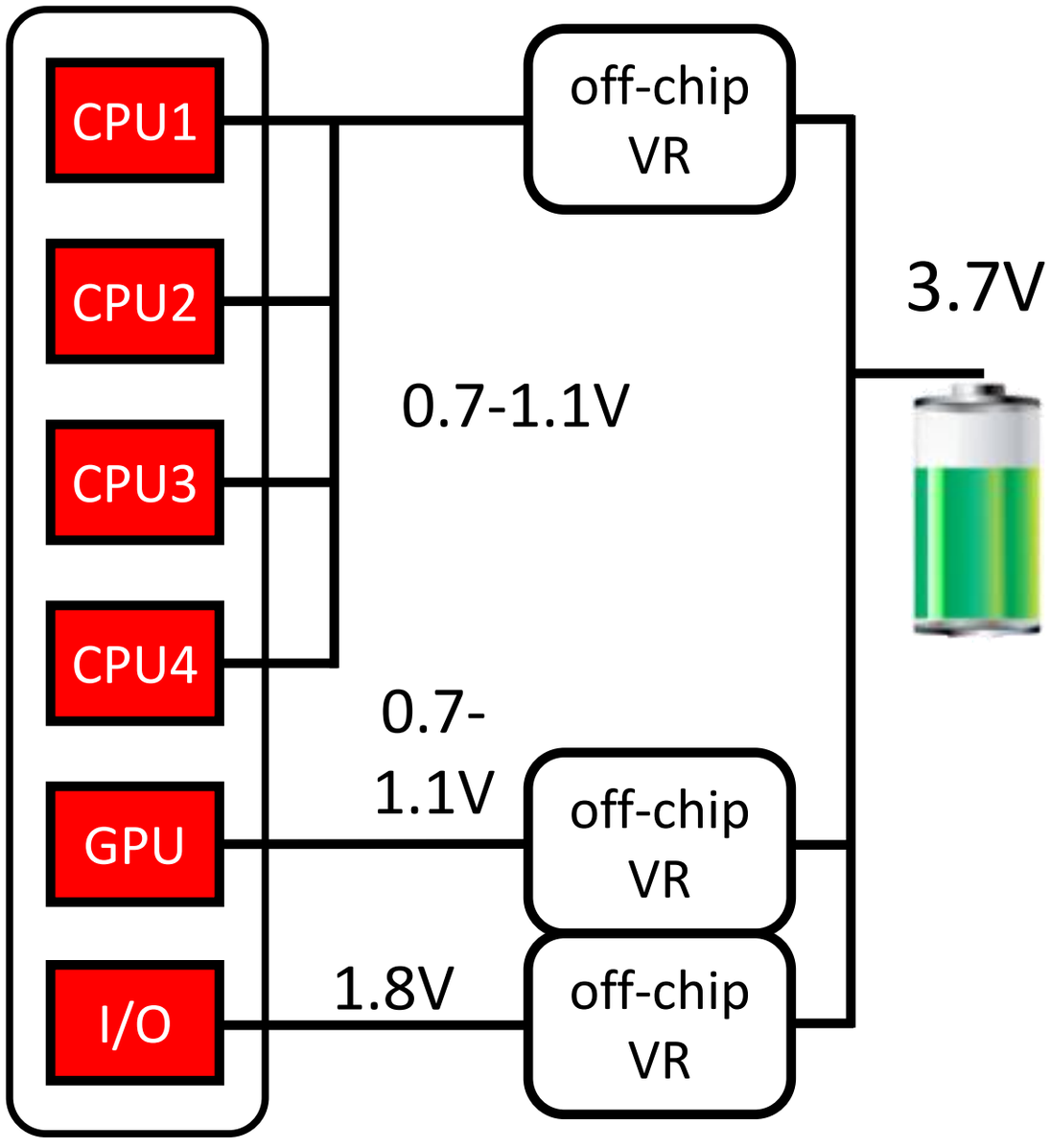


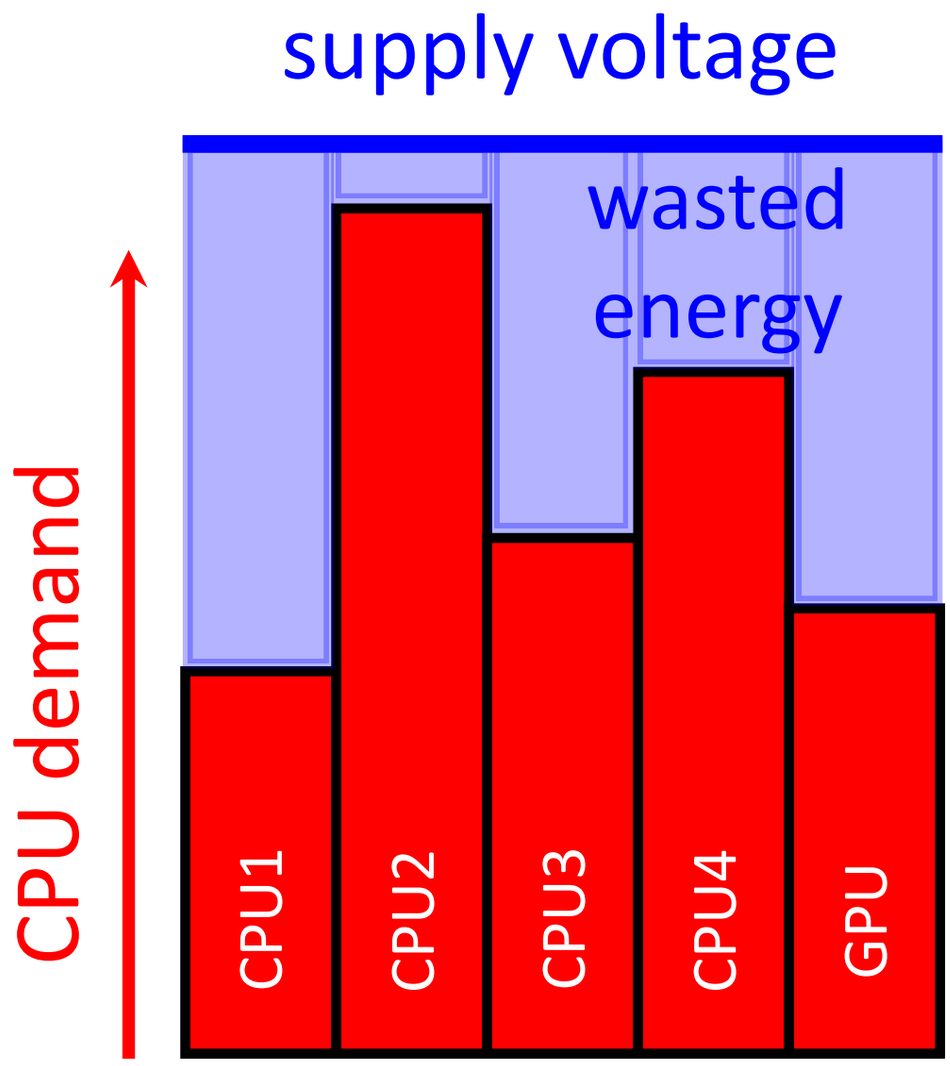
server processor

Problems with conventional off-chip power delivery

- Inefficient energy usage
- Board area and cost

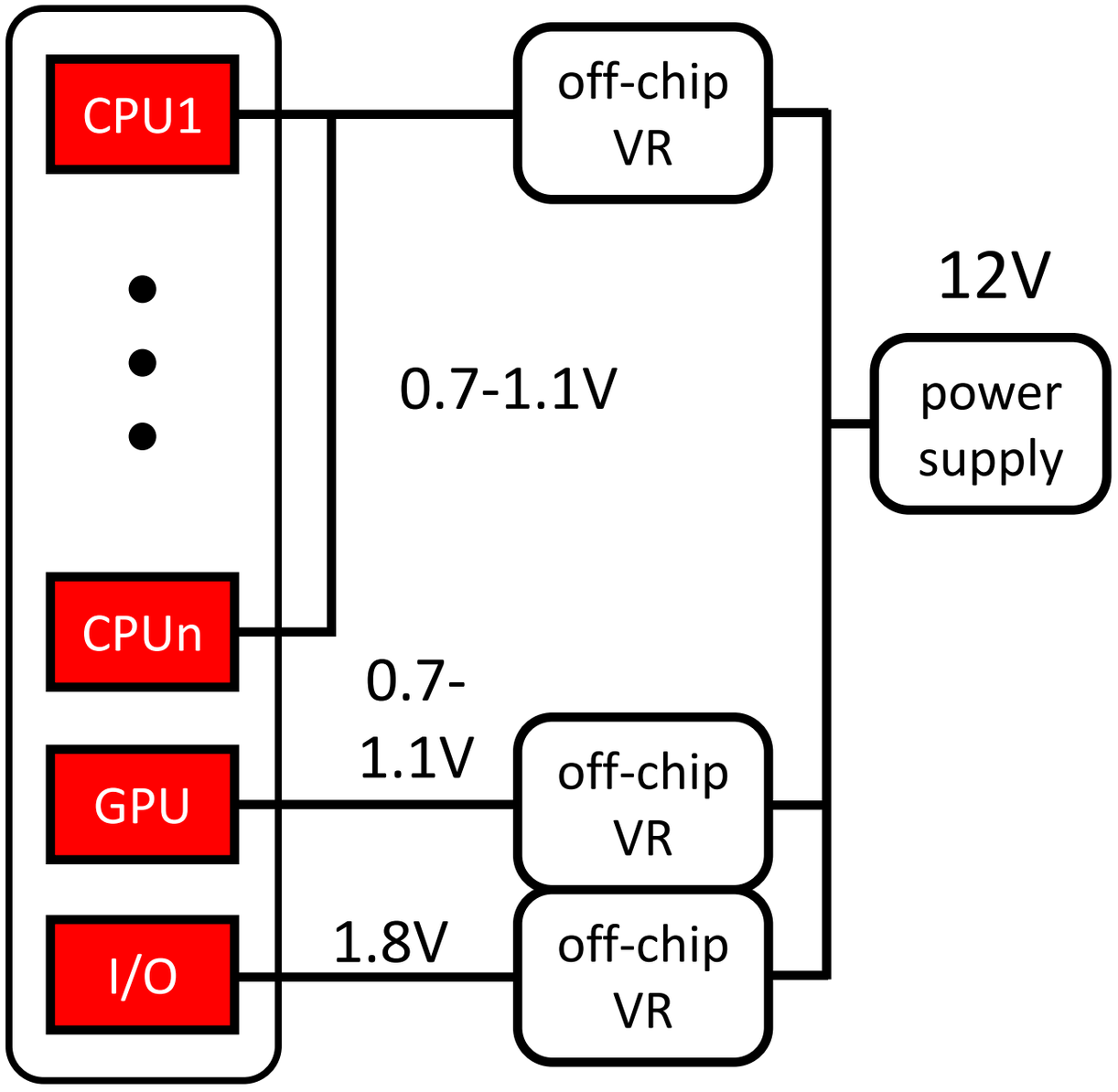
Problem 1: Sharing single voltage across multiple cores wastes energy





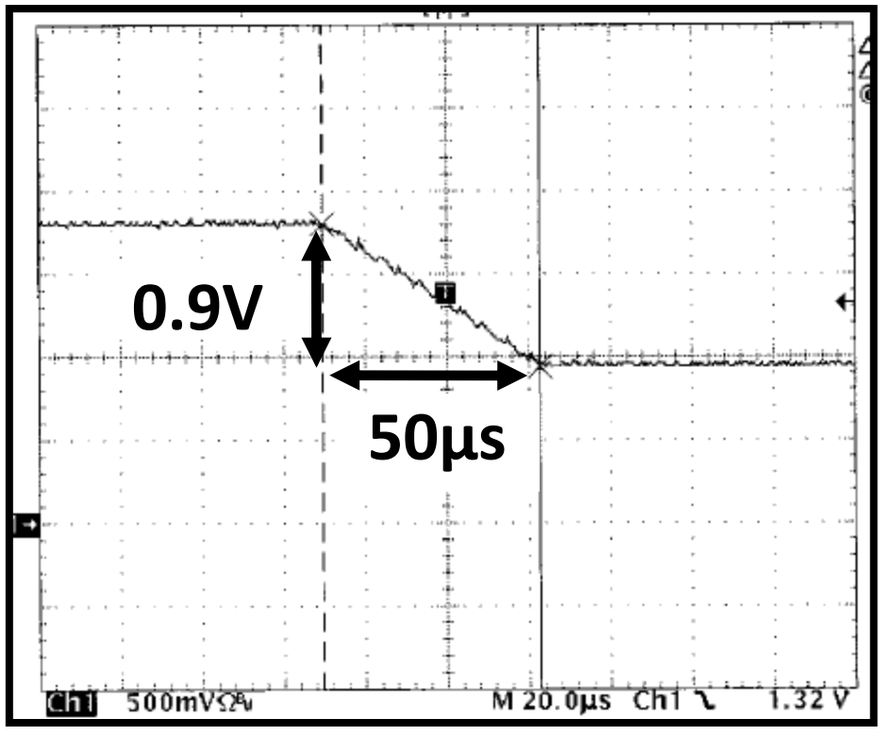
But… complex board design/cost for per-core voltage control

Impractical to route many voltage domains through PCB and package

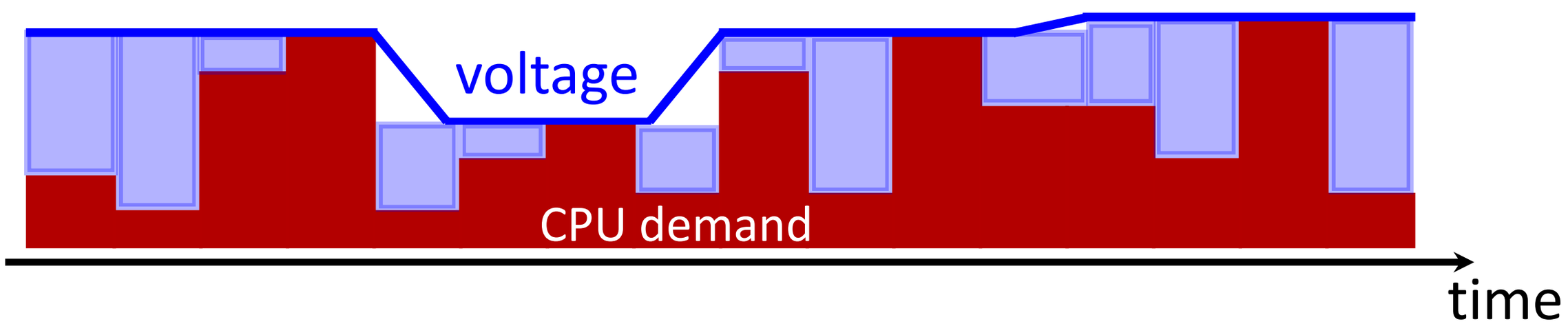


server processor

Problem 2: Inefficient SoC energy usage with slow (µs) voltage scaling

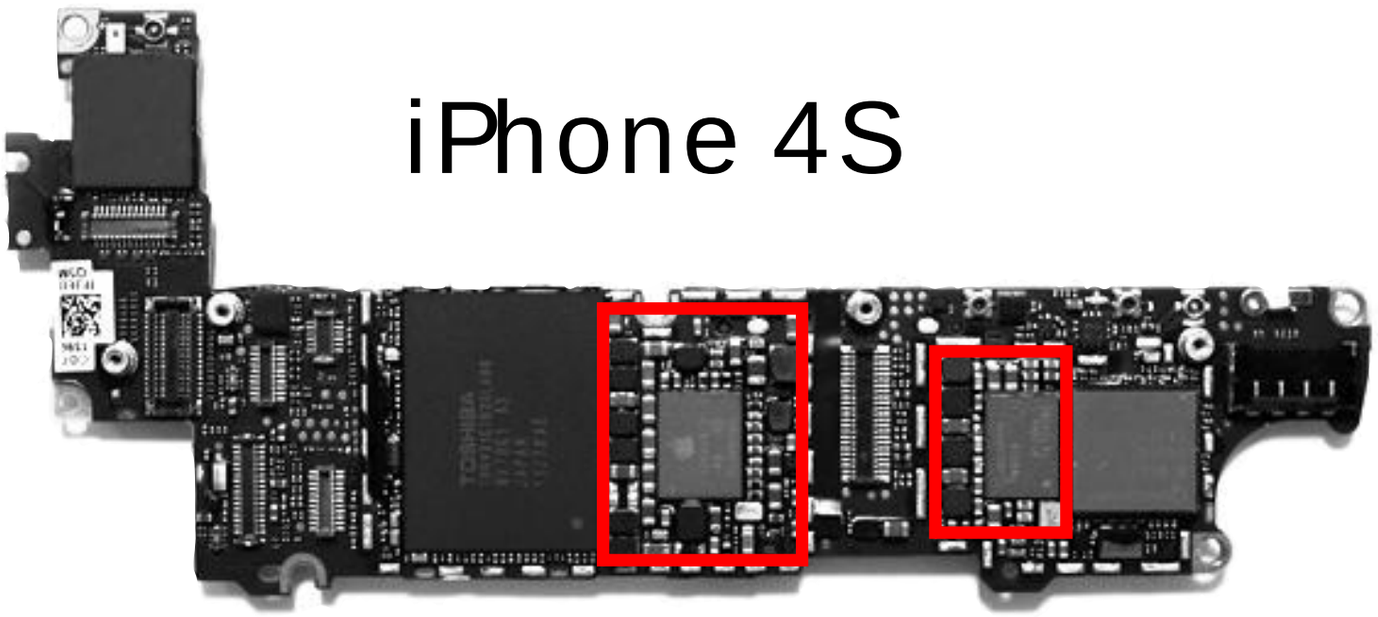


L.T. Clark et al, JSSC 2001



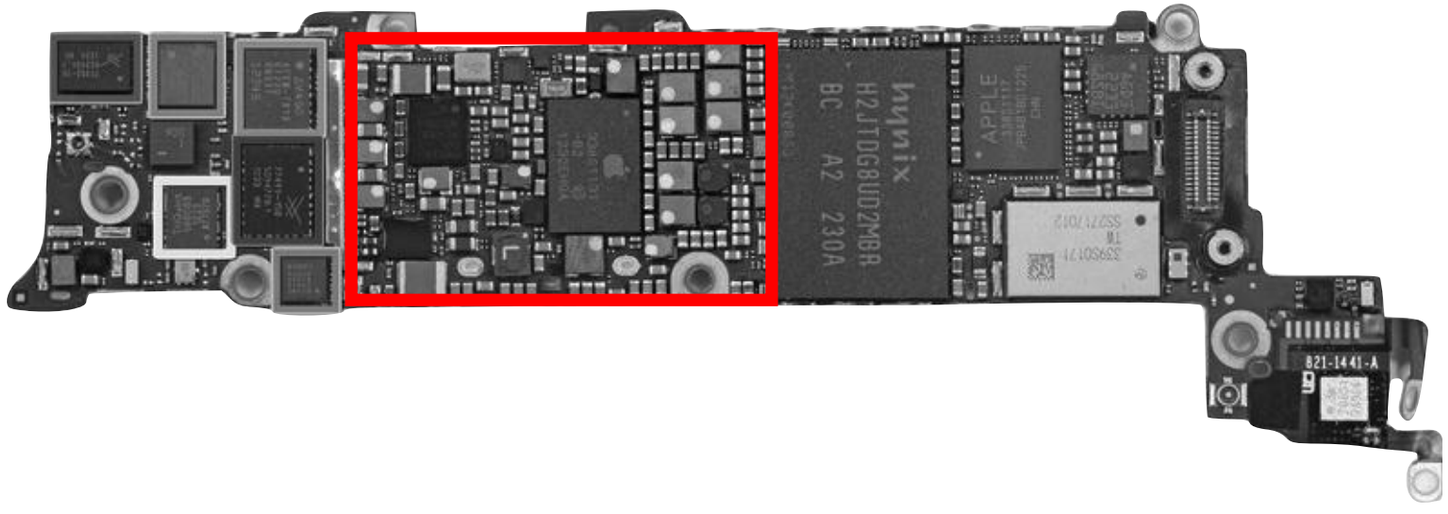
Problem 3: Requires large PCB area

iPhone 4S



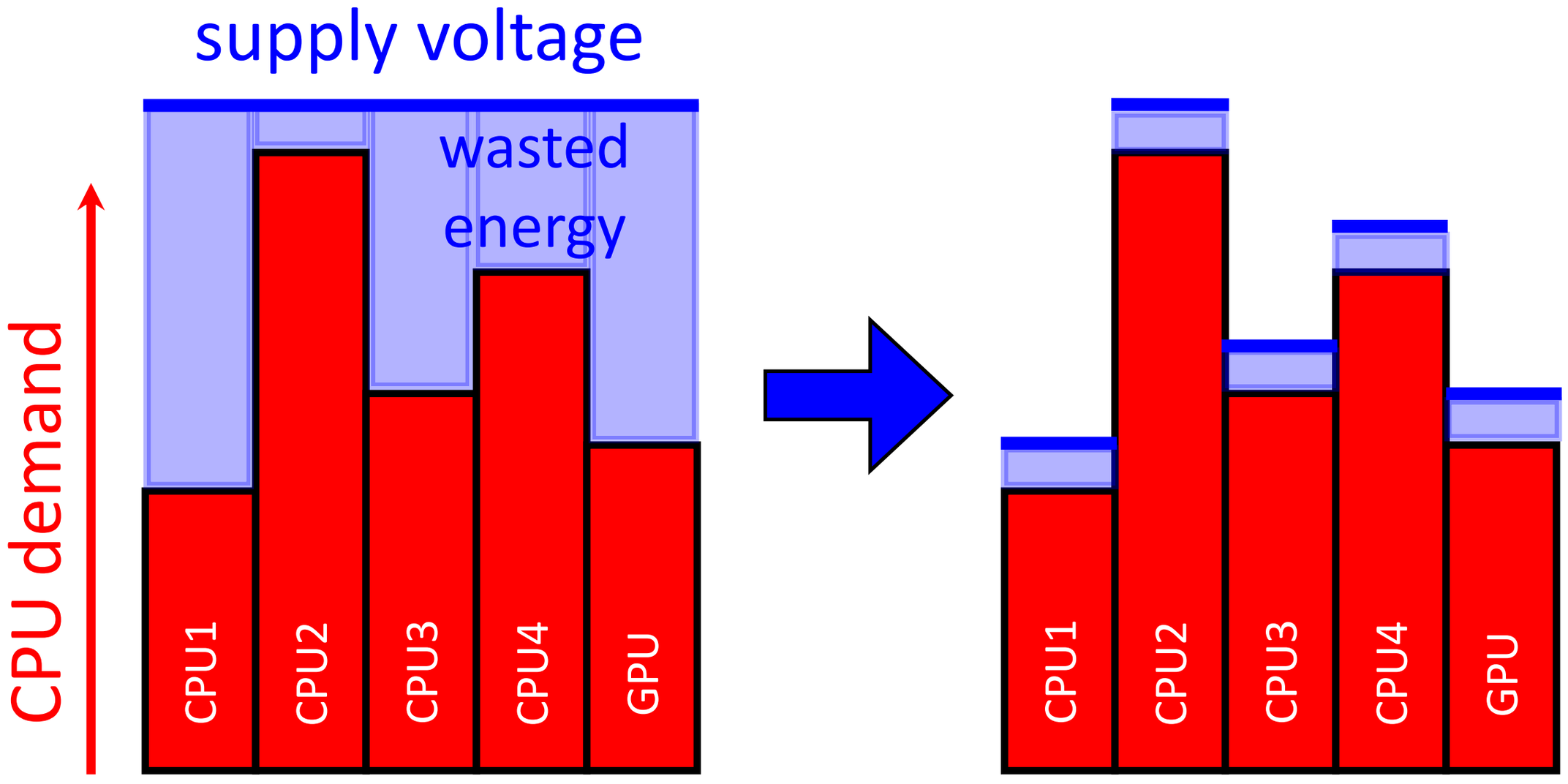
DC- DC + passive elements

iPhone 5



Solution: Replace off-chip VRs with IVRs

Advantage 1: IVR saves SoC energy with per-core voltage control



shared voltage

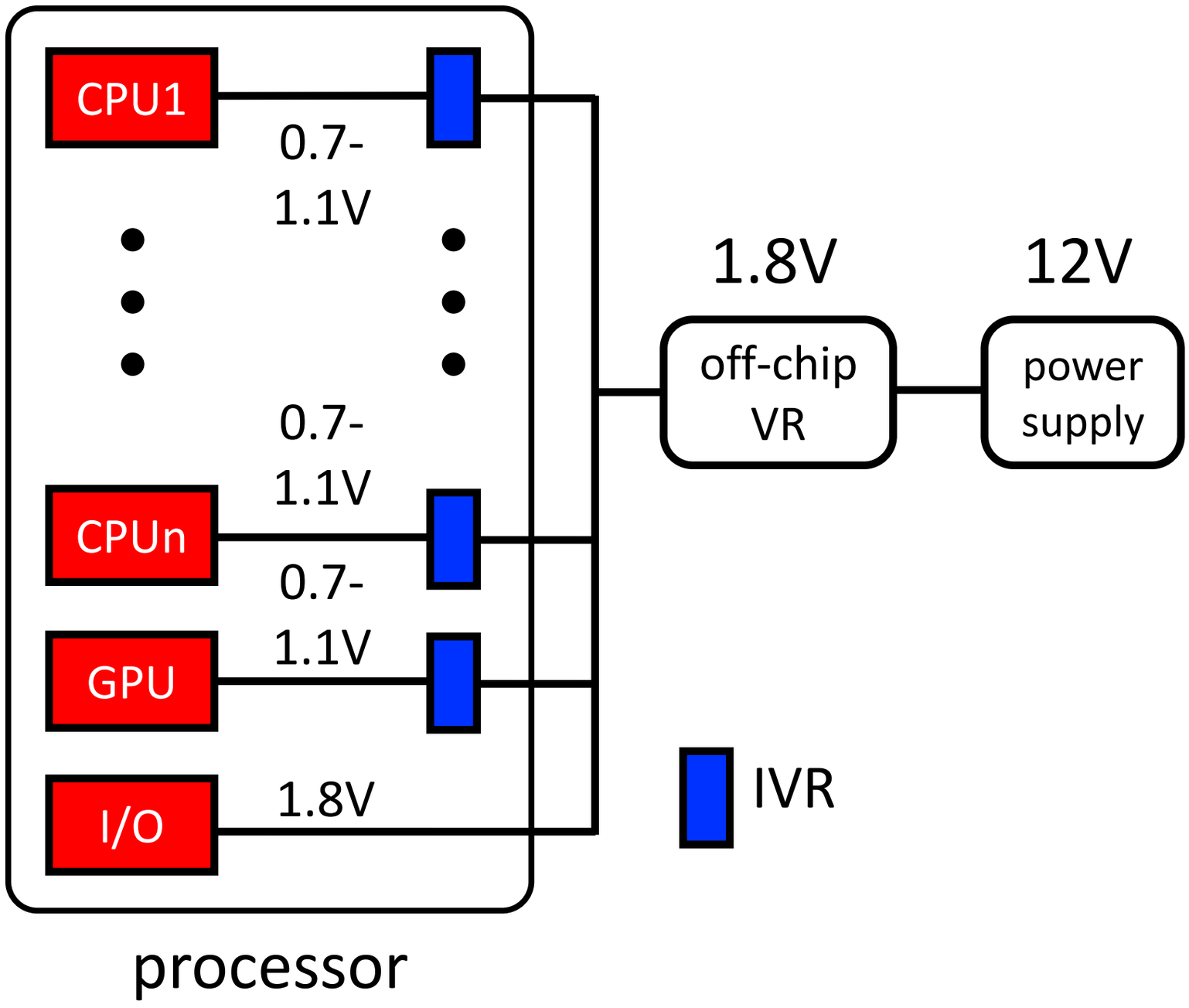
per-core voltage

Per-core voltage control simplifies otherwise complex board design

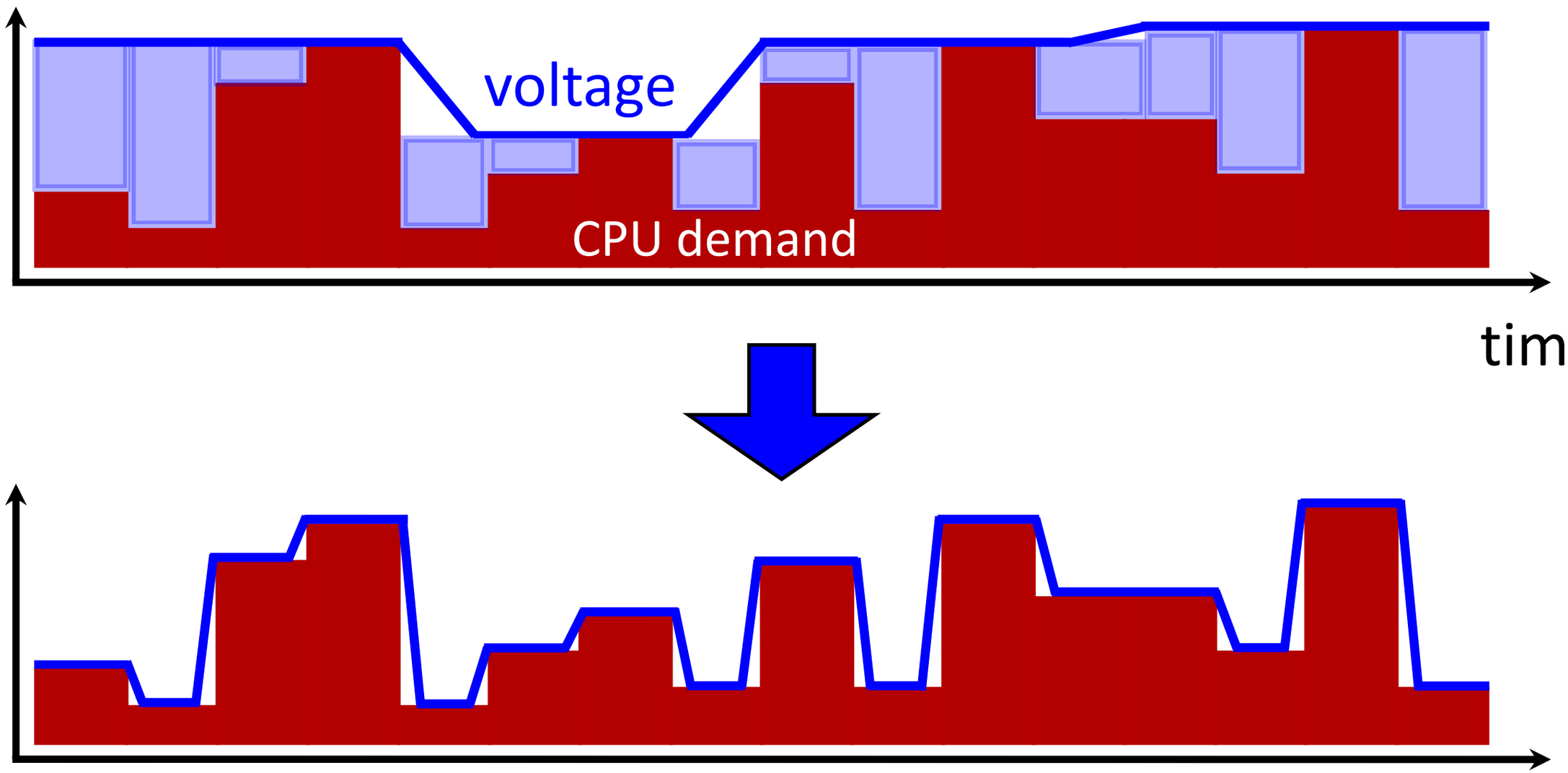
Reduce off-chip VR with bulky passive elements

Integrate IVRs and cores together in a single die

Multiple copies of IVRs for per-core voltage control

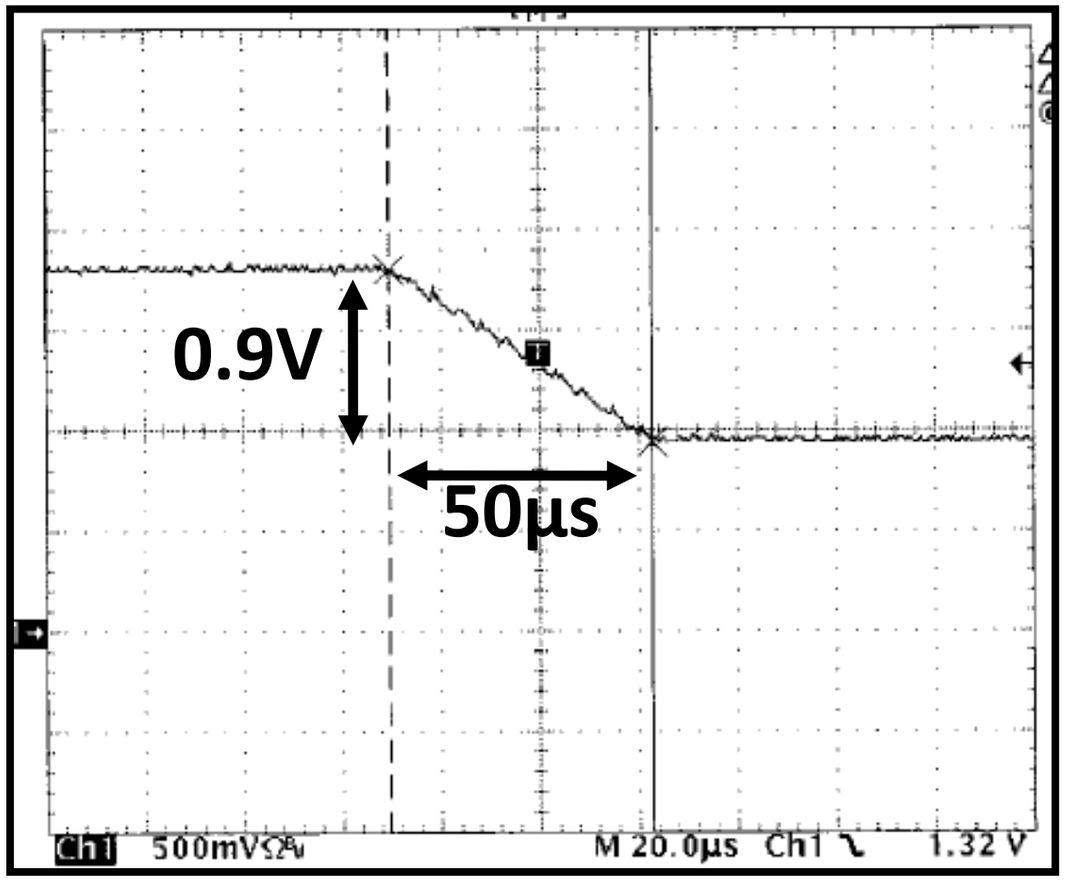


Advantage 2: IVR saves SoC power via nanosecond-scale voltage scaling



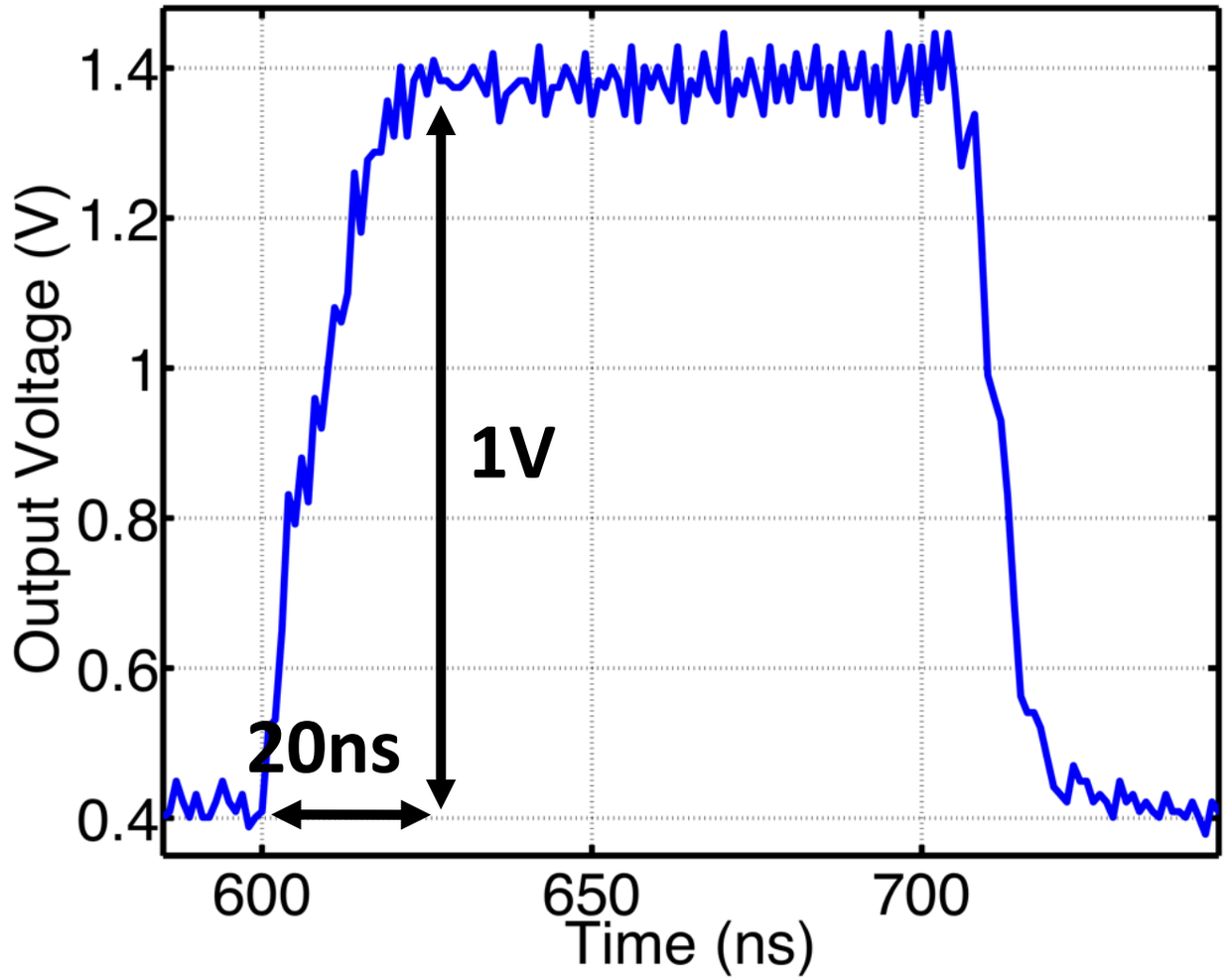
IVR offers 1000x faster voltage scaling

L.T. Clark et al, JSSC 2001



Off-chip (µs-scale)

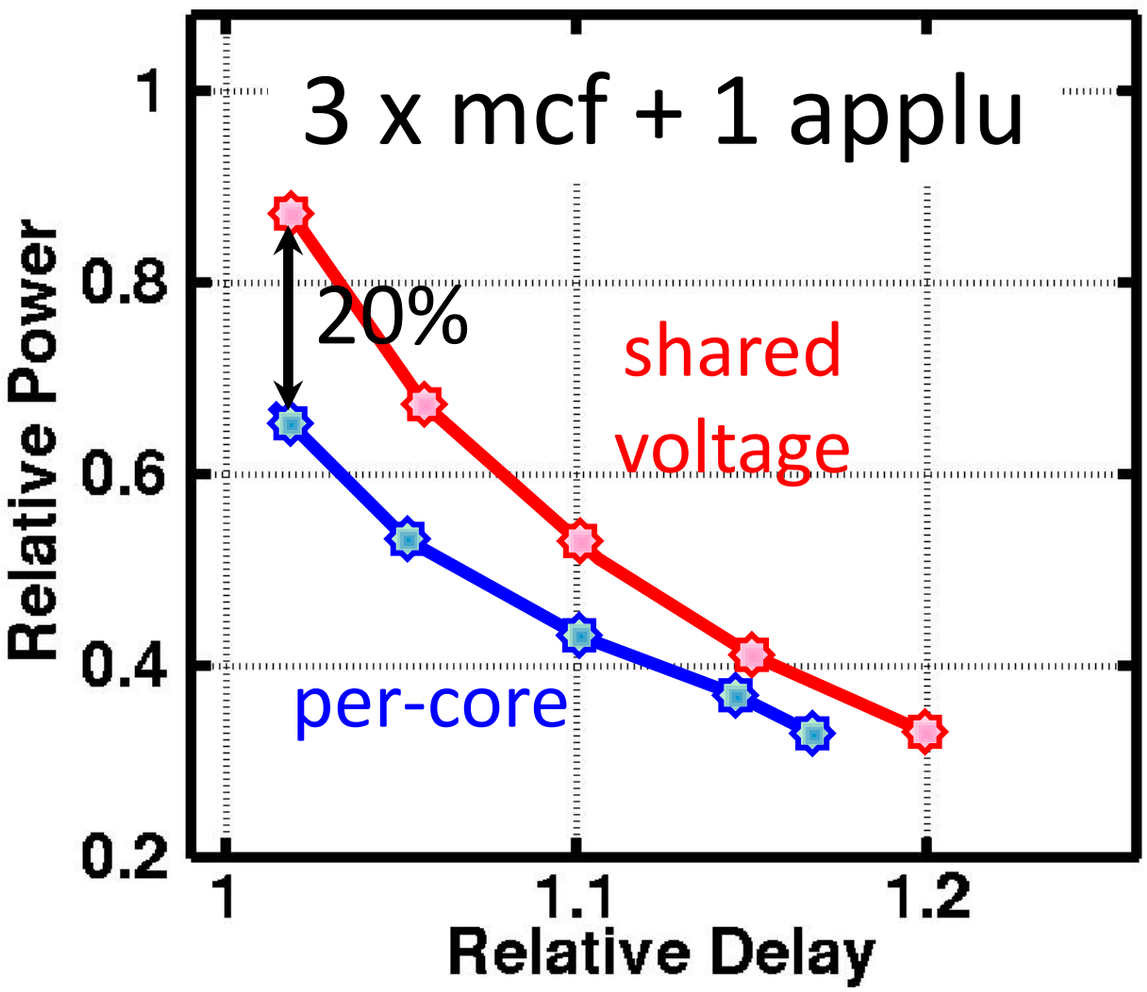
W. Kim et al, ISSCC 2011



IVR (ns-scale)

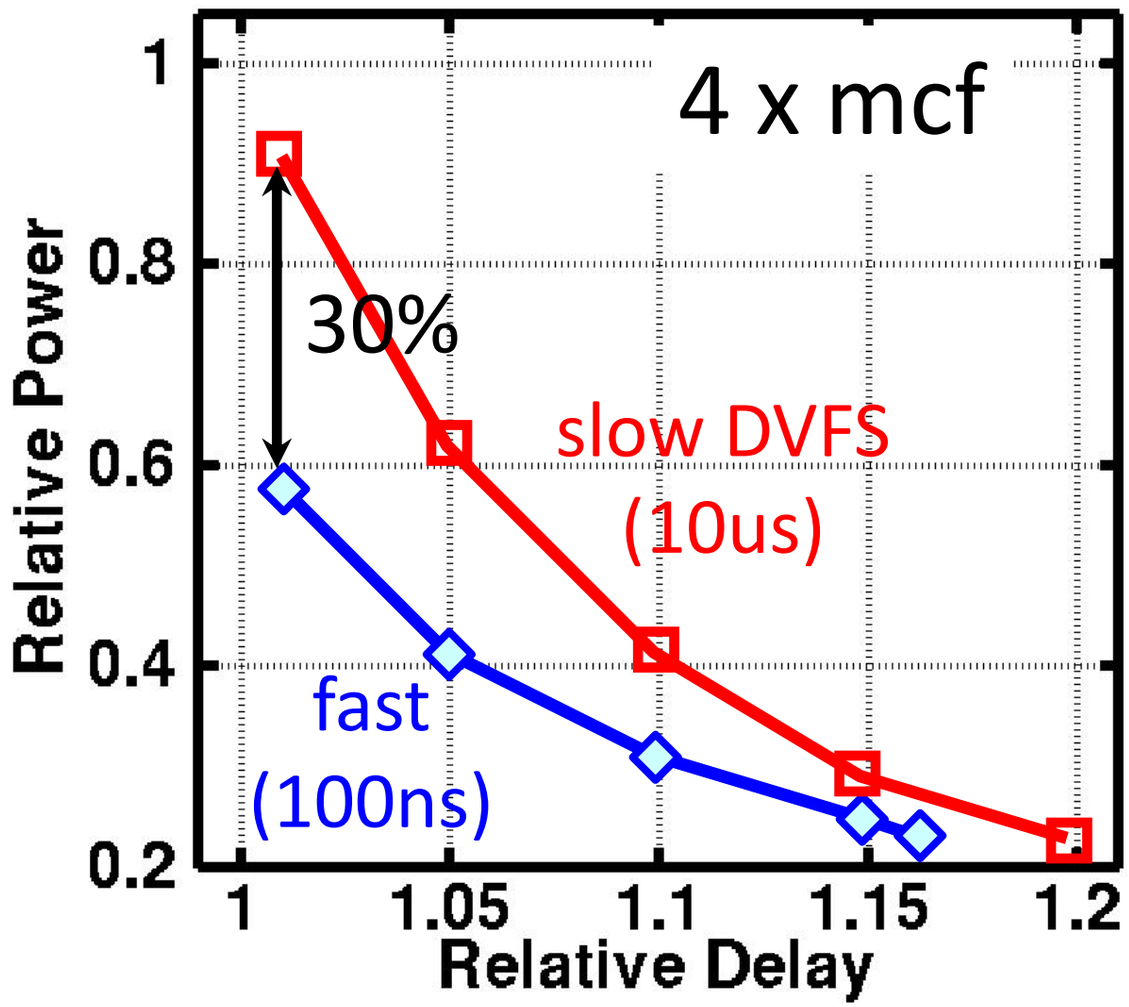
Architectural simulations show 20-30% power savings with fast, per-core DVFS

Per-core DVFS



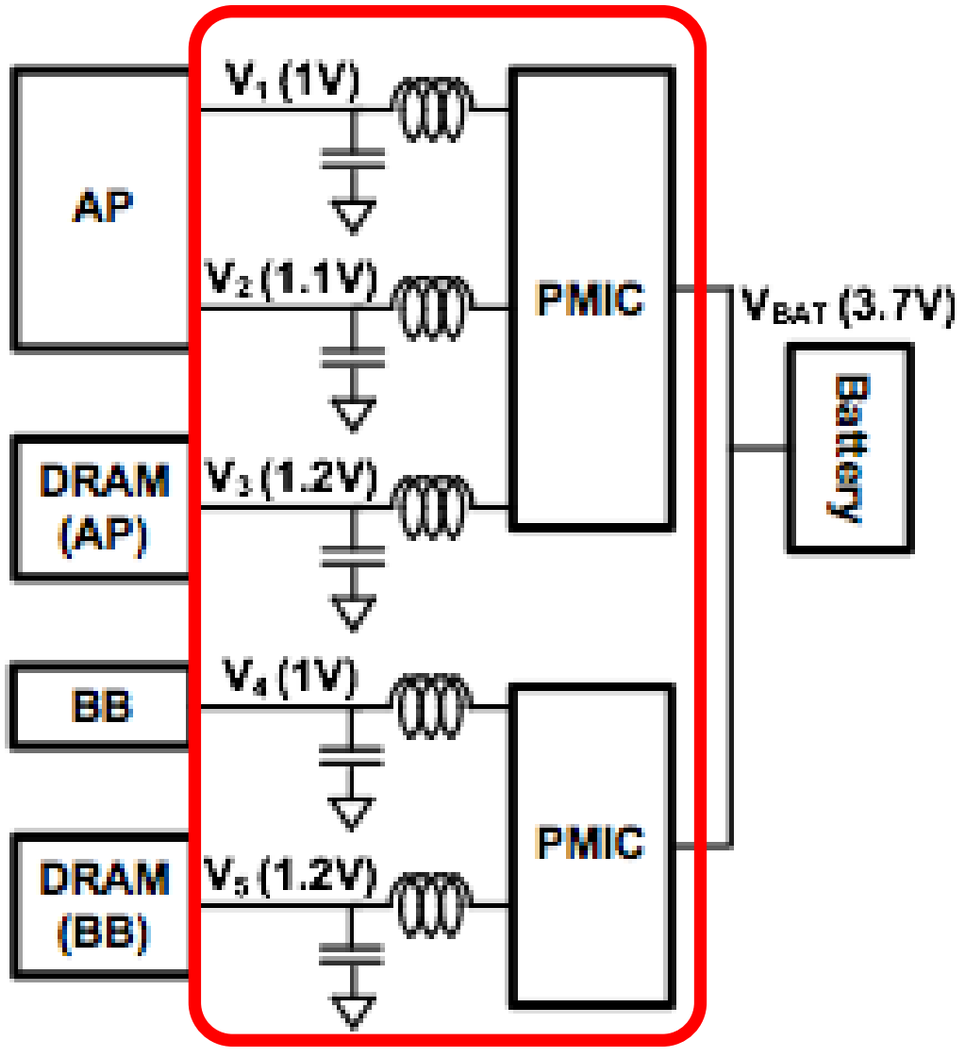
1.6W 4-core processor

Fast DVFS

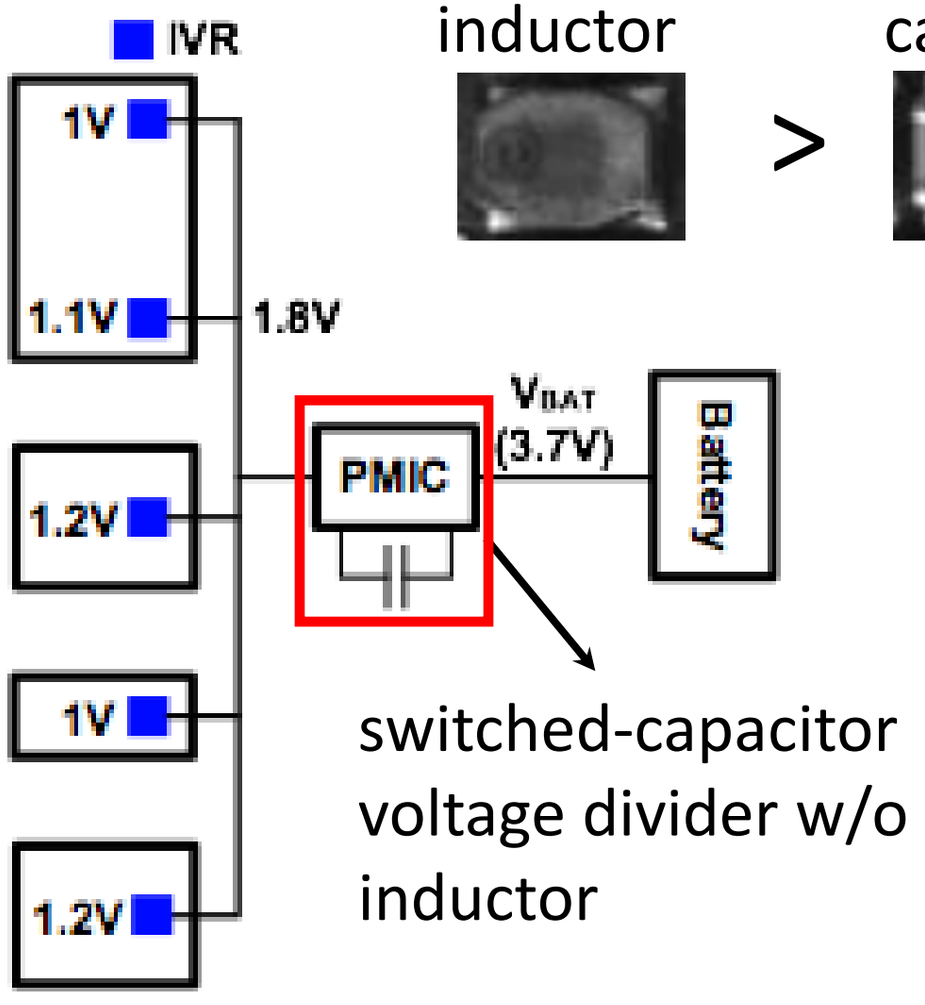


W. Kim et al, HPCA 2008

Advantage 3: IVR reduces PCB area

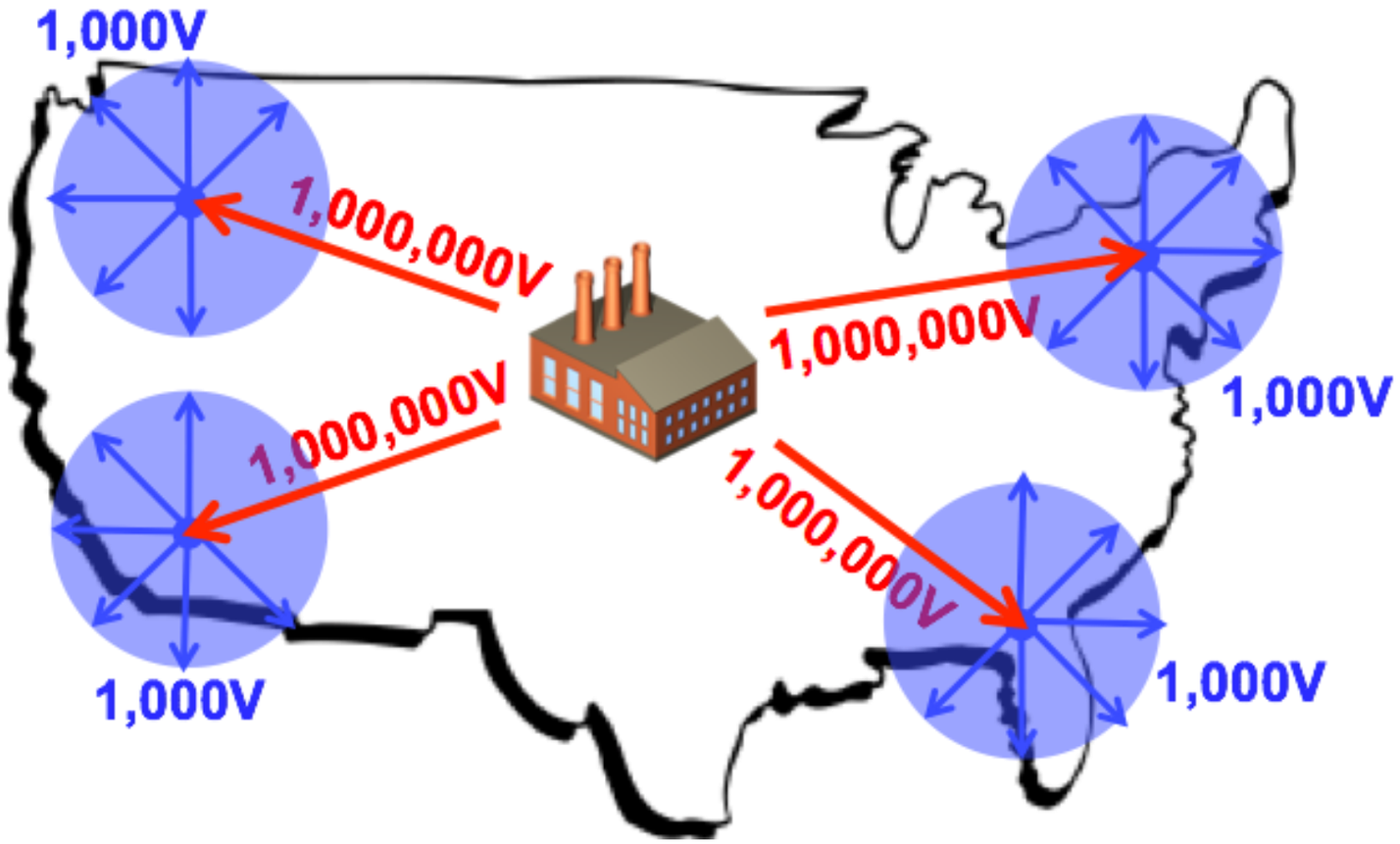


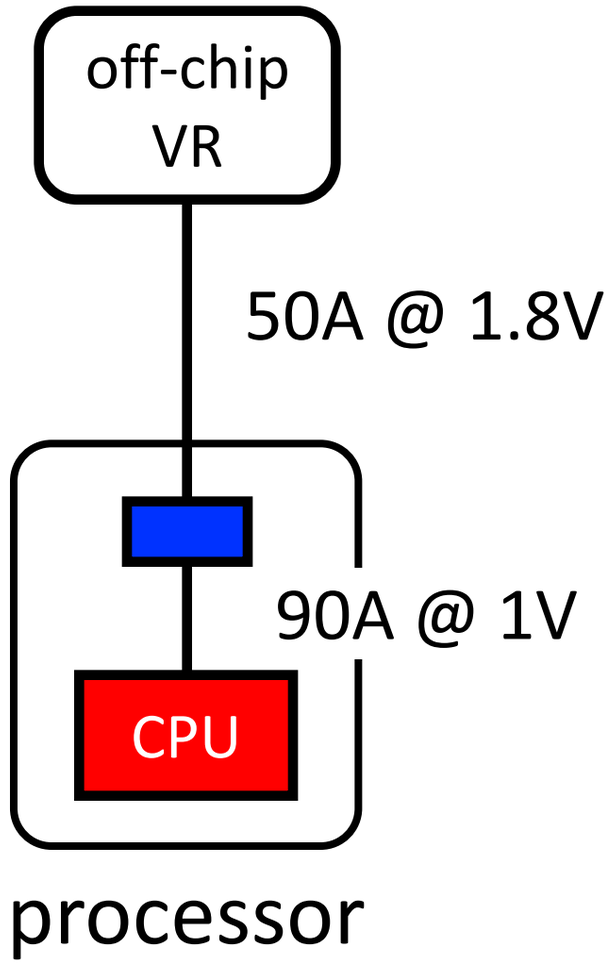
Conventional



Integrated Voltage Regulators

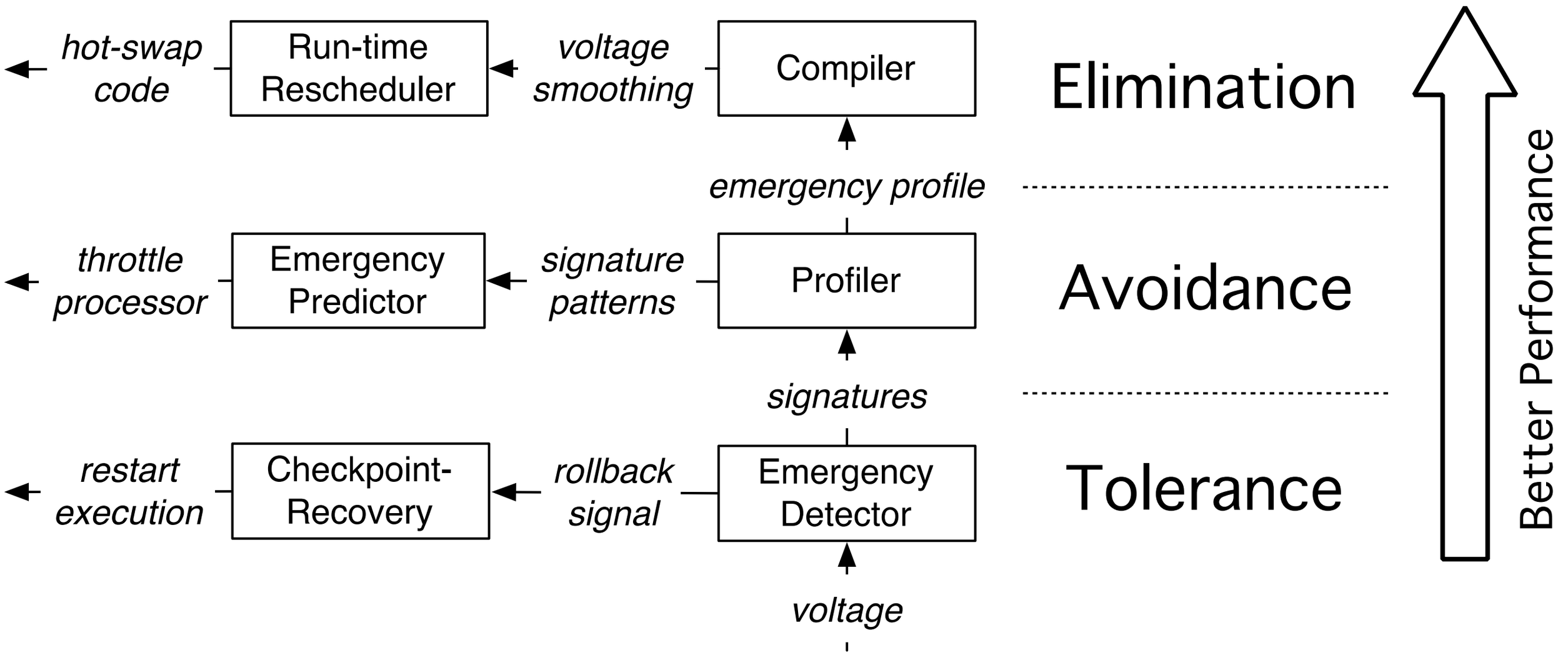
Advantage 4: Distribute power at high voltage and low current to reduce IR loss





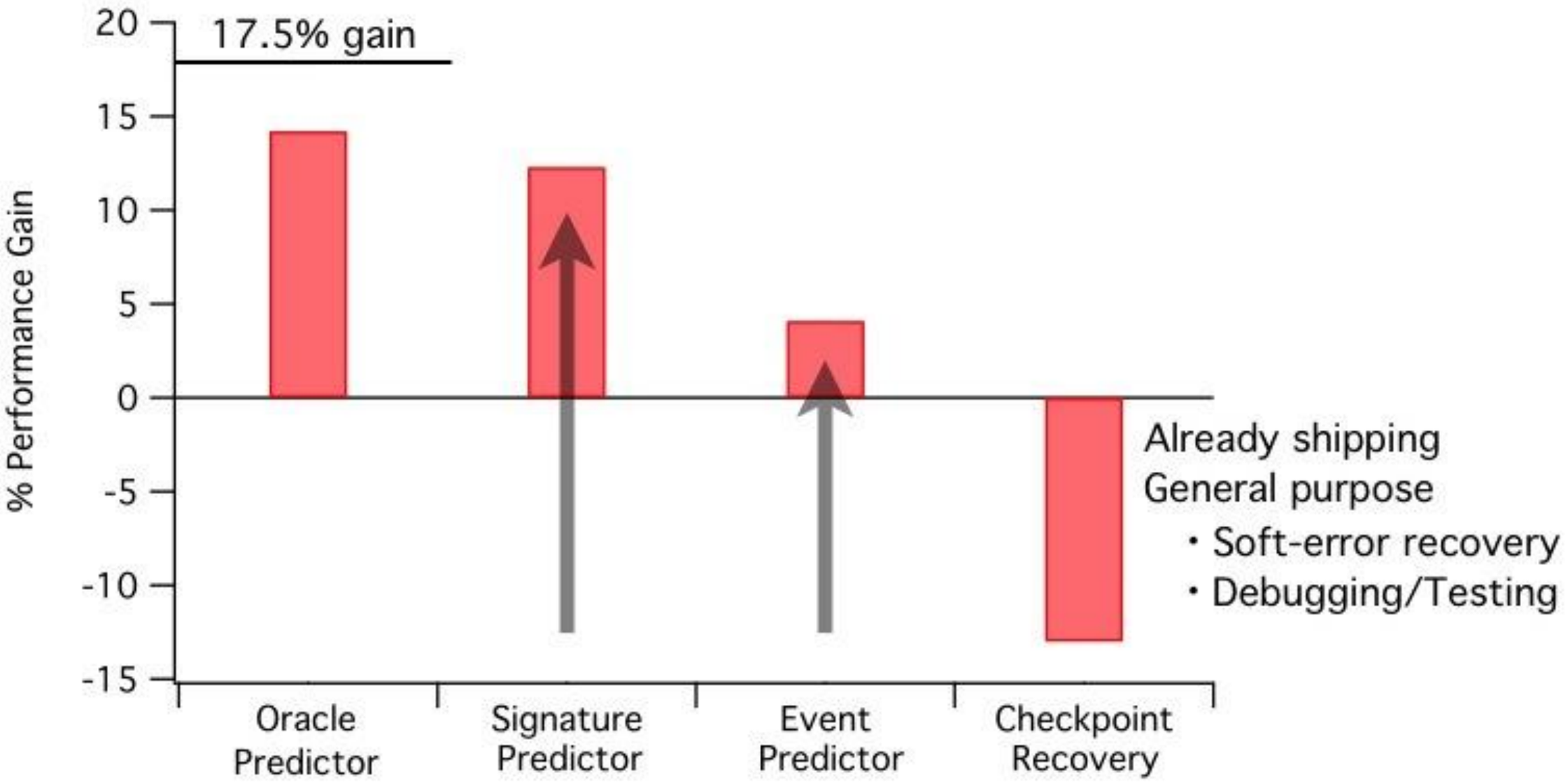
Especially important for high performance server systems

Opportunity 1: Leverage architecture & SW to combat voltage noise



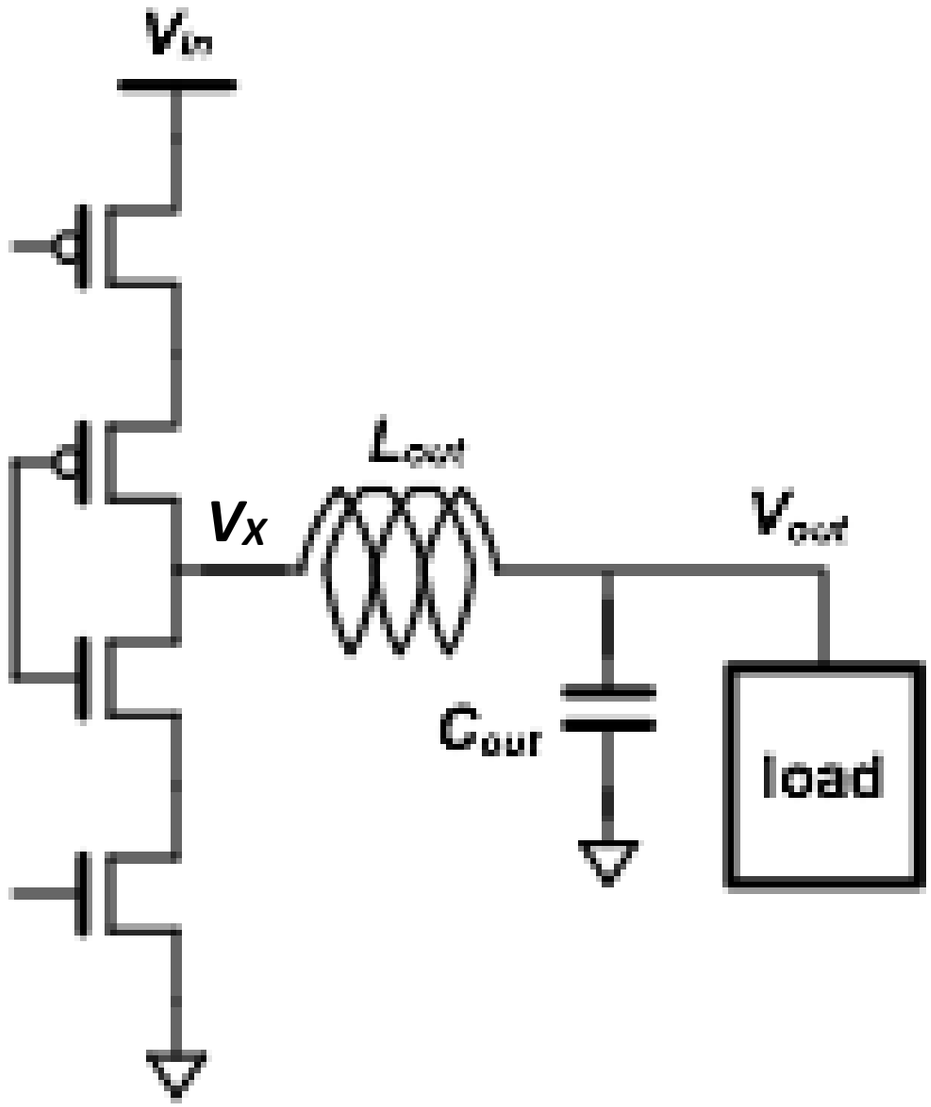
V.J. Reddi, et al., Symp. Micro 2009 & 2010

Performance gained by reducing voltage noise margins



V.J. Reddi, et al., Symp. Micro 2009 & 2010

Buck converter

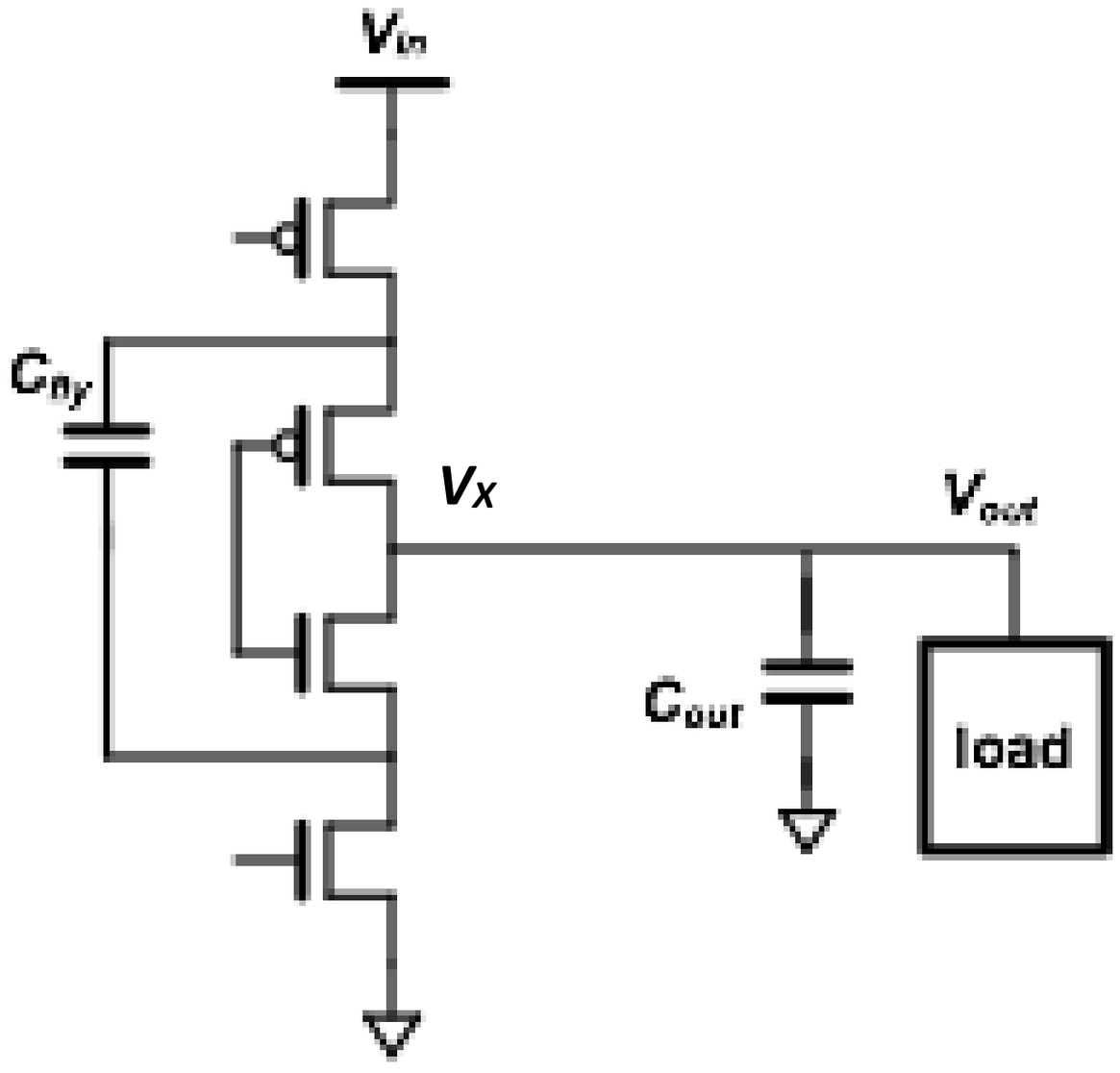


buck

- Wide output voltage range
- Large inductor difficult for on-die integration

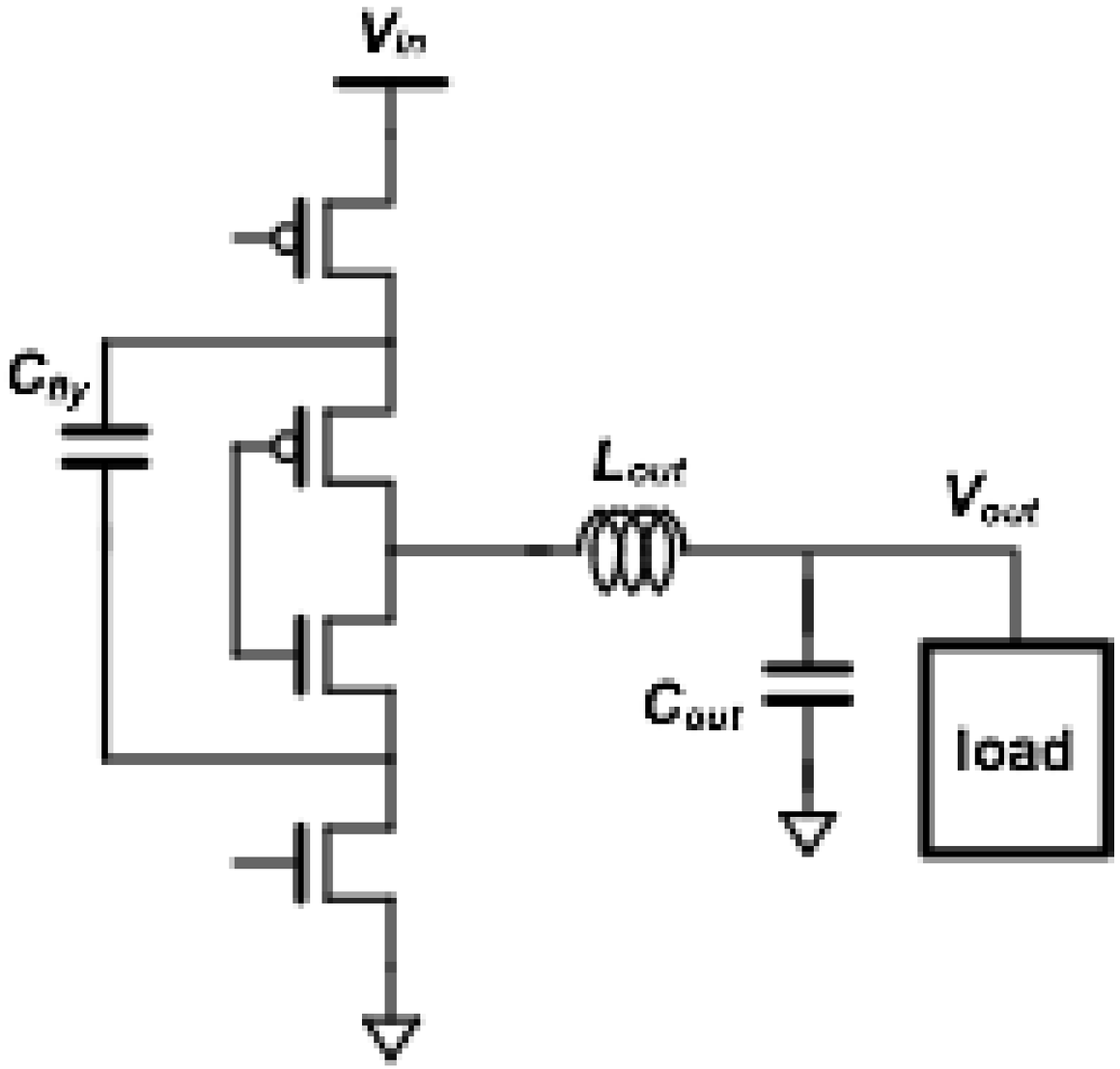
Switch-capacitor converter

- No inductor
- High efficiency for output voltages that are integer ratios of the input voltage (e.g., 1/2, 1/3, 2/3)



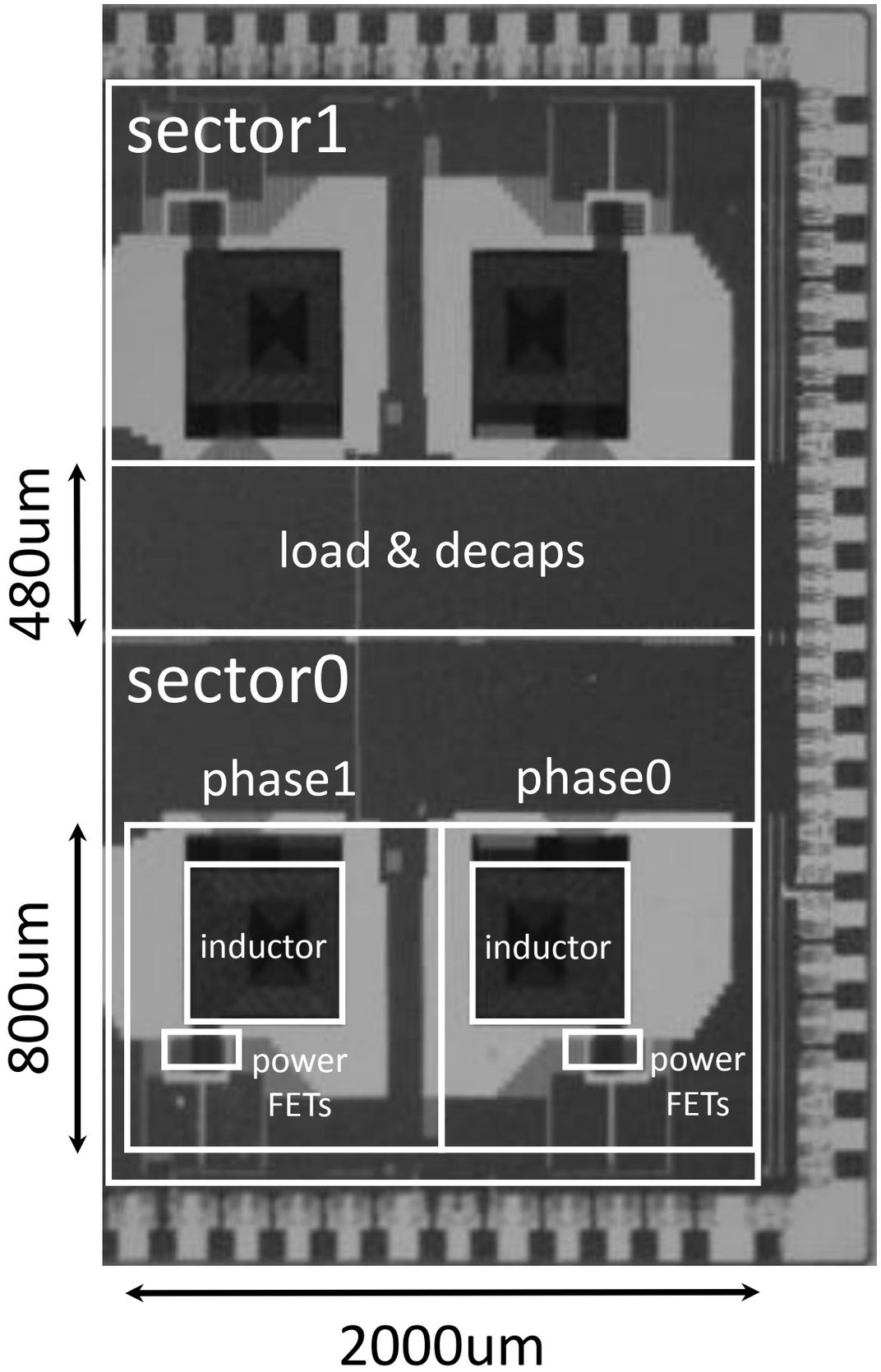
switched-capacitor (SC)

3-Level VR: Hybrid of buck and switched-cap



- Requires smaller inductor than buck (2x switching frequency & ½ swing)
- Can generate wide range of output voltages

W. Kim et al, ISSCC 2011 & JSSC 2012

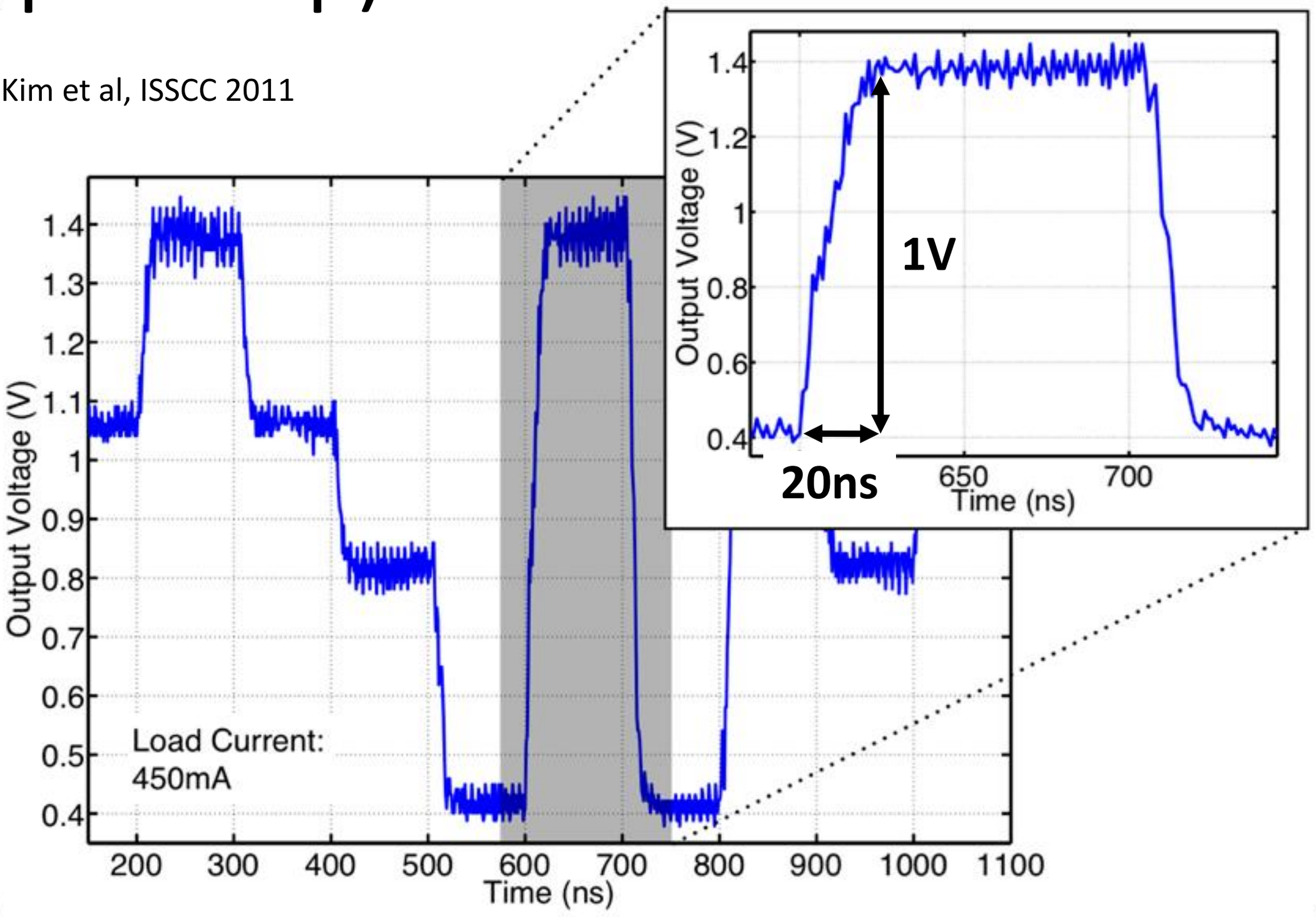


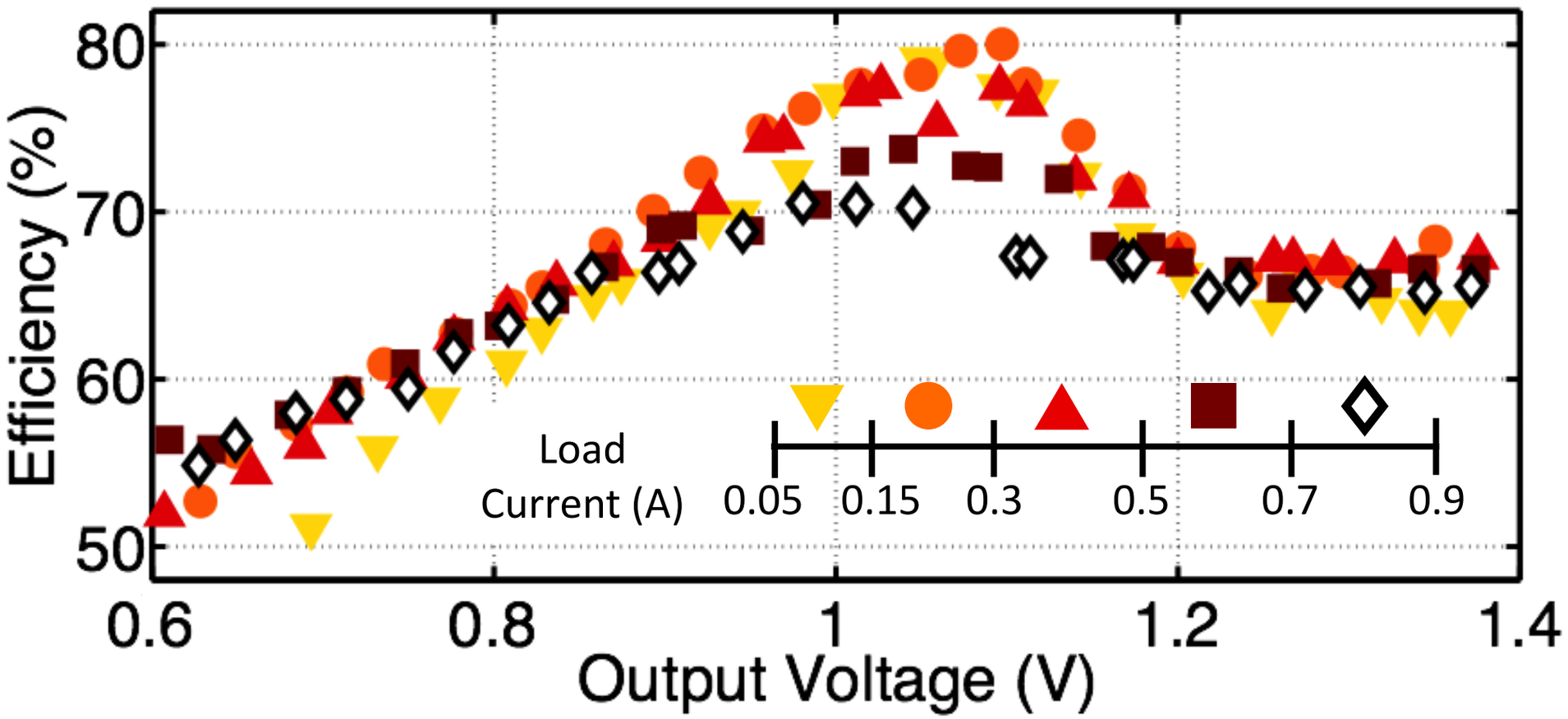
- UMC 130nm CMOS
- Integrated spiral inductors (1nH)
- 2.4V to 0.4-1.4V conversion
- 0.9A max load current

W. Kim et al, ISSCC 2011

Nanosecond-scale voltage transition (open loop)

W. Kim et al, ISSCC 2011





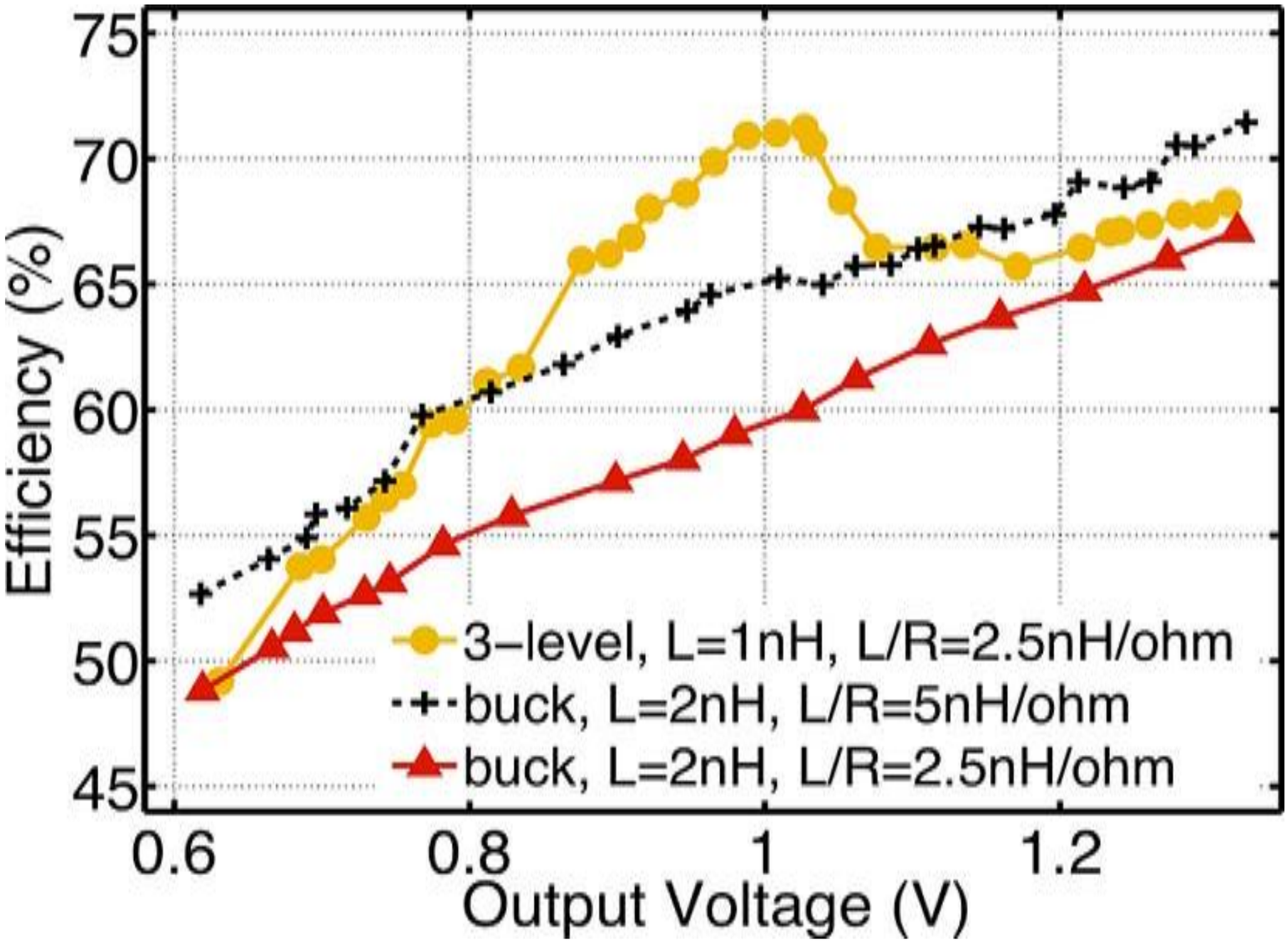
Efficiency $= P_{OUT} / P_{IN}$

$= P_{OUT} / (P_{OUT} + P_{LOSS})$

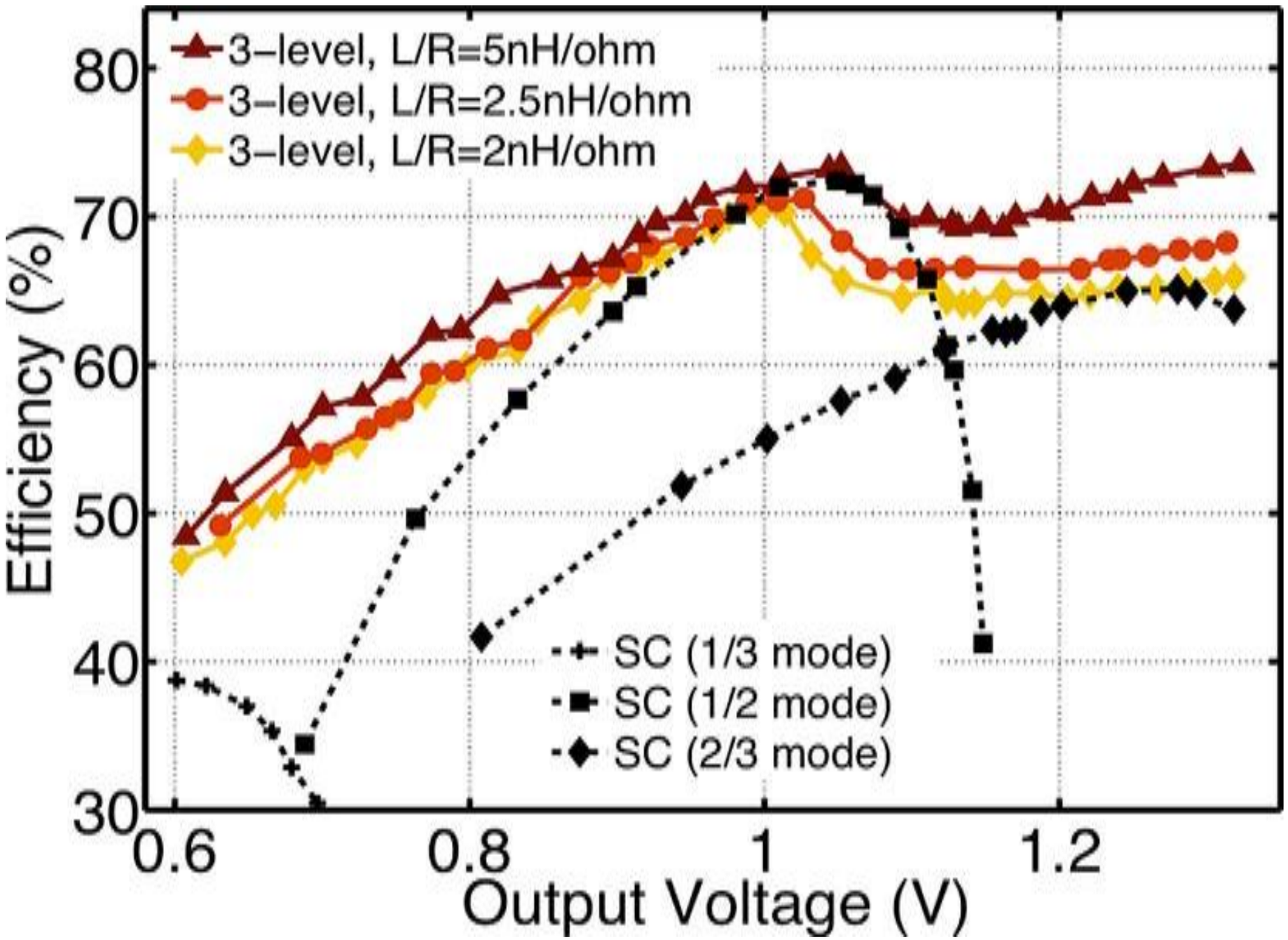
P_{OUT} increases with output voltage

P_{LOSS} increases as duty cycle deviates from 50%

Comparison to buck (simulated)



Comparison to SC (simulated)



Summary of design

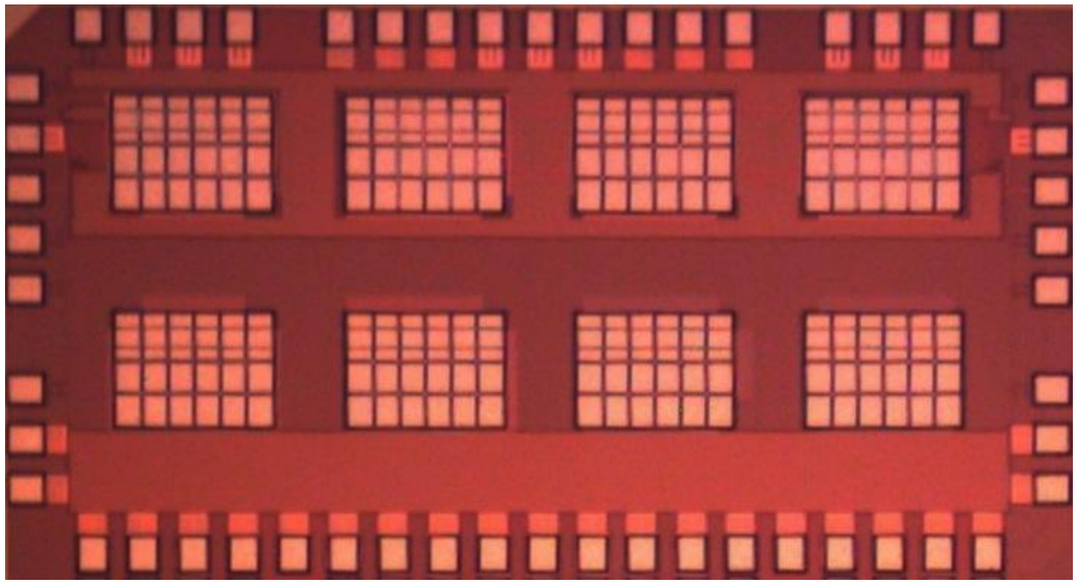
- Generate 0.4-1.4V output voltage
- Nanosecond-scale voltage scaling

- ~80% peak efficiency
- 3mm^2 die area for 1A delivery

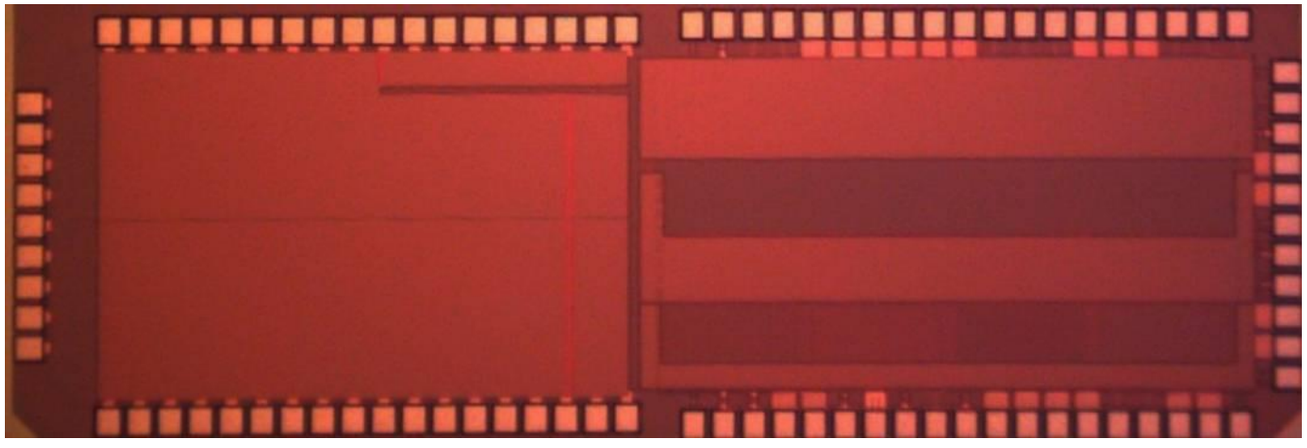
Room for improvement!

On-going IVR projects in TSMC 40nm CMOS

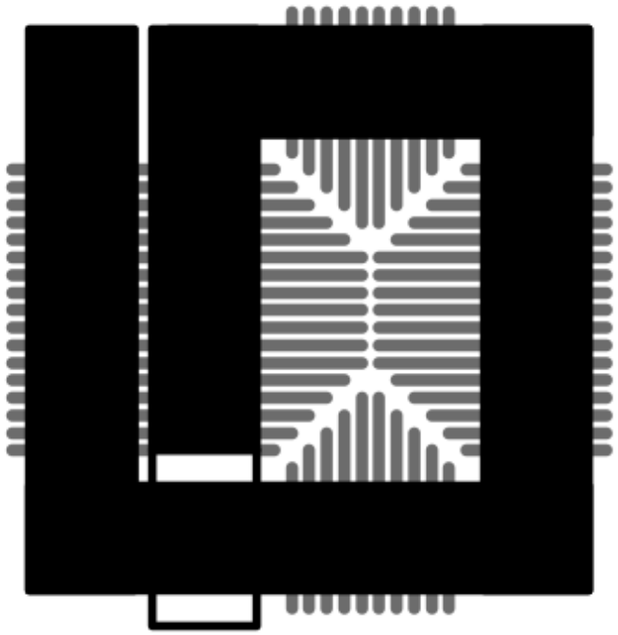
- 3-level IVR ver.2
  - Pads for mounting SMT inductors
  - Dual-loop control



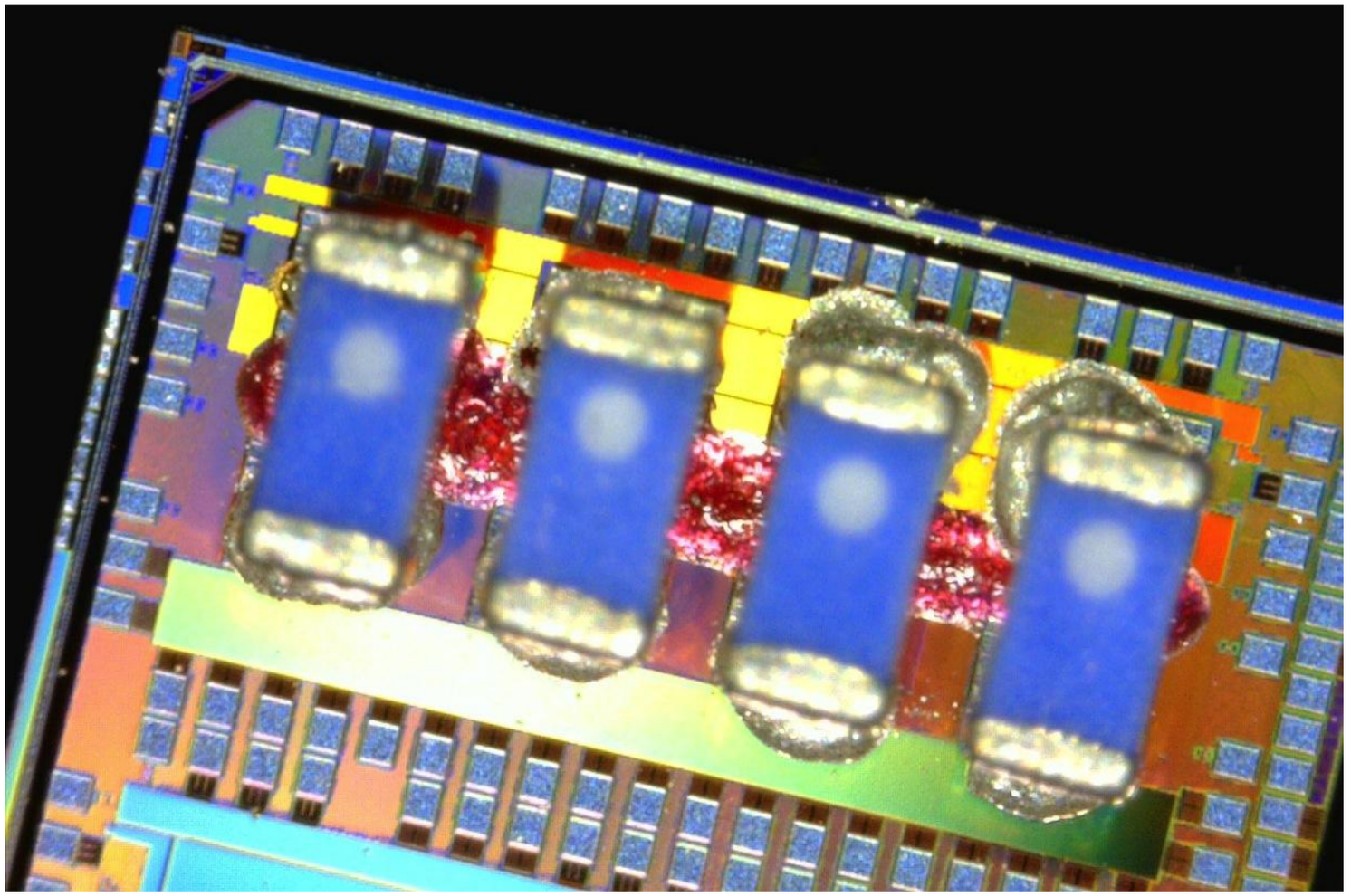
- IVR for Robobee brain chip



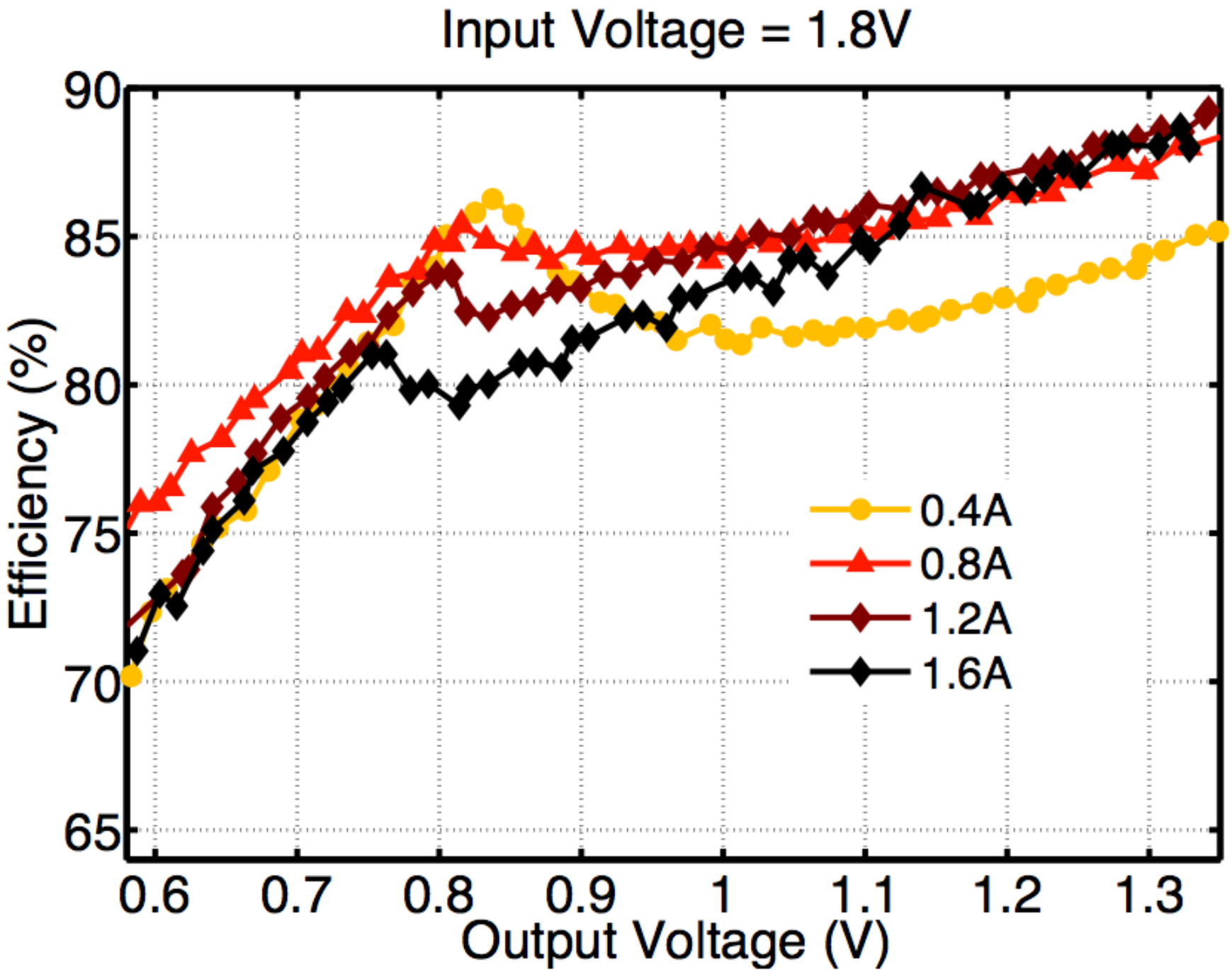
Increase efficiency by mounting SMT inductors on top of the die?



on-chip spiral inductor

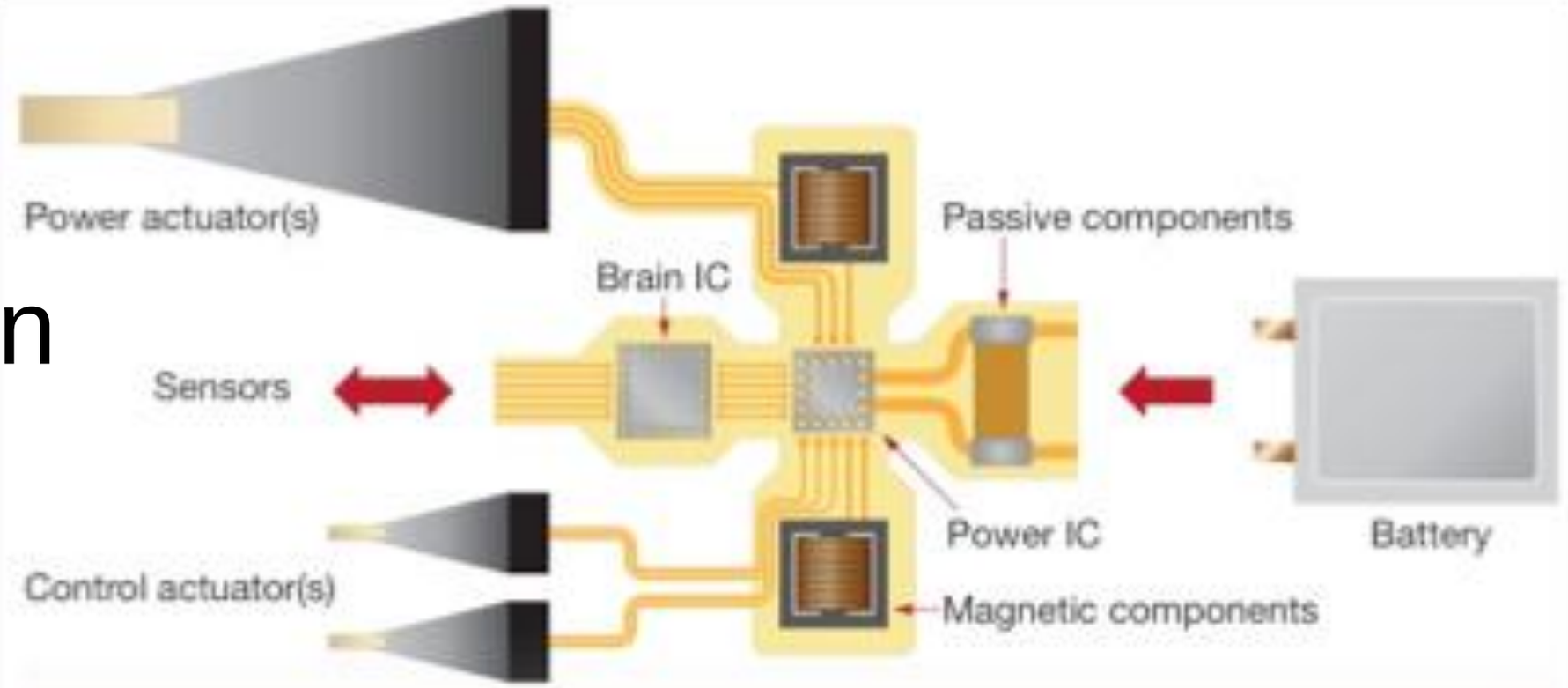


Murata 1nH 0201 inductors
(chip coil. HF thin film, DCR=0.1ohms)



Simulated efficiency w/ SMT inductors and TSMC 40nm CMOS, 1.8mm x 0.8mm, ~1W/mm^2 @ V_{out} = 1V

Power converters in Robobees

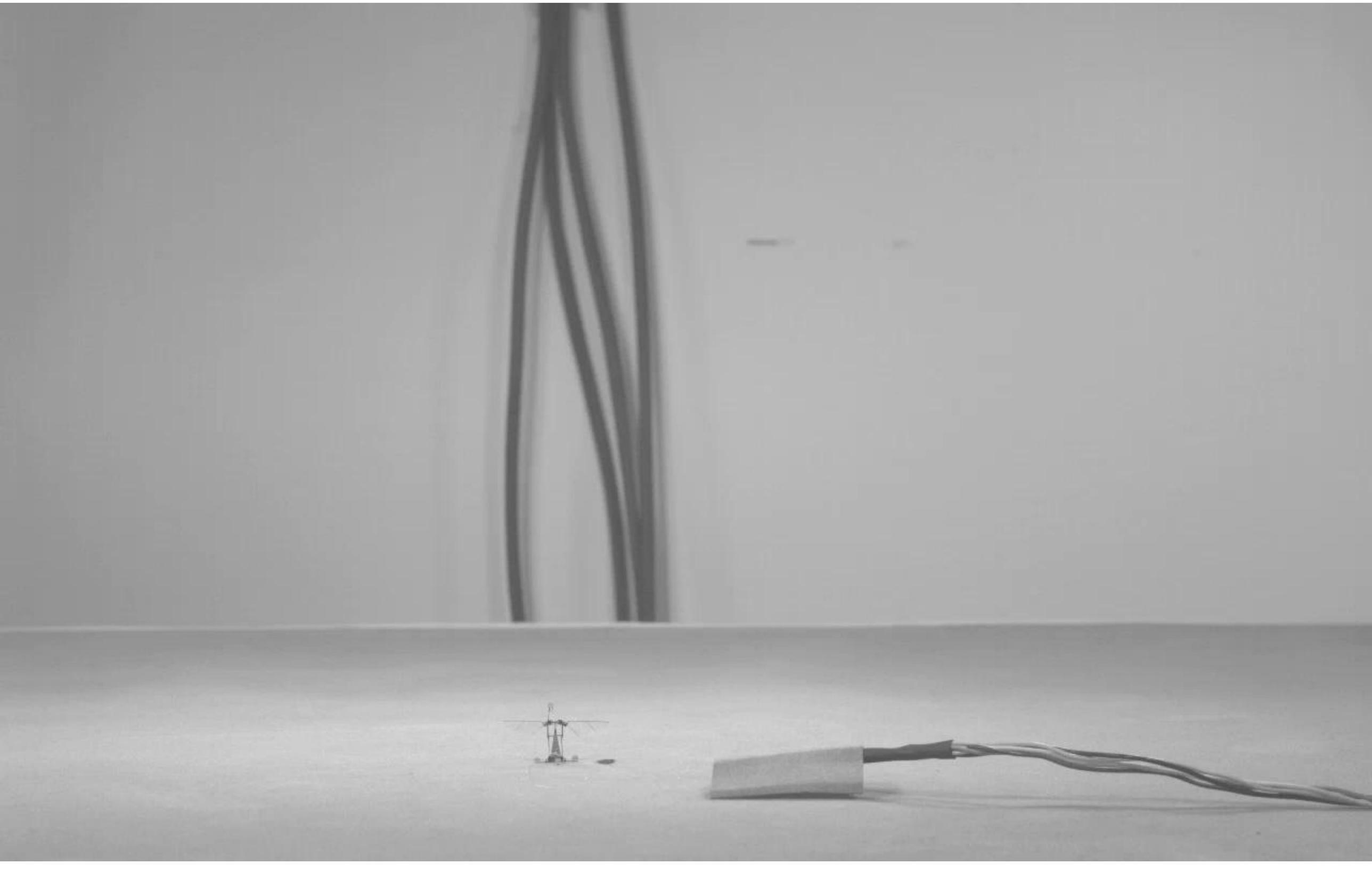


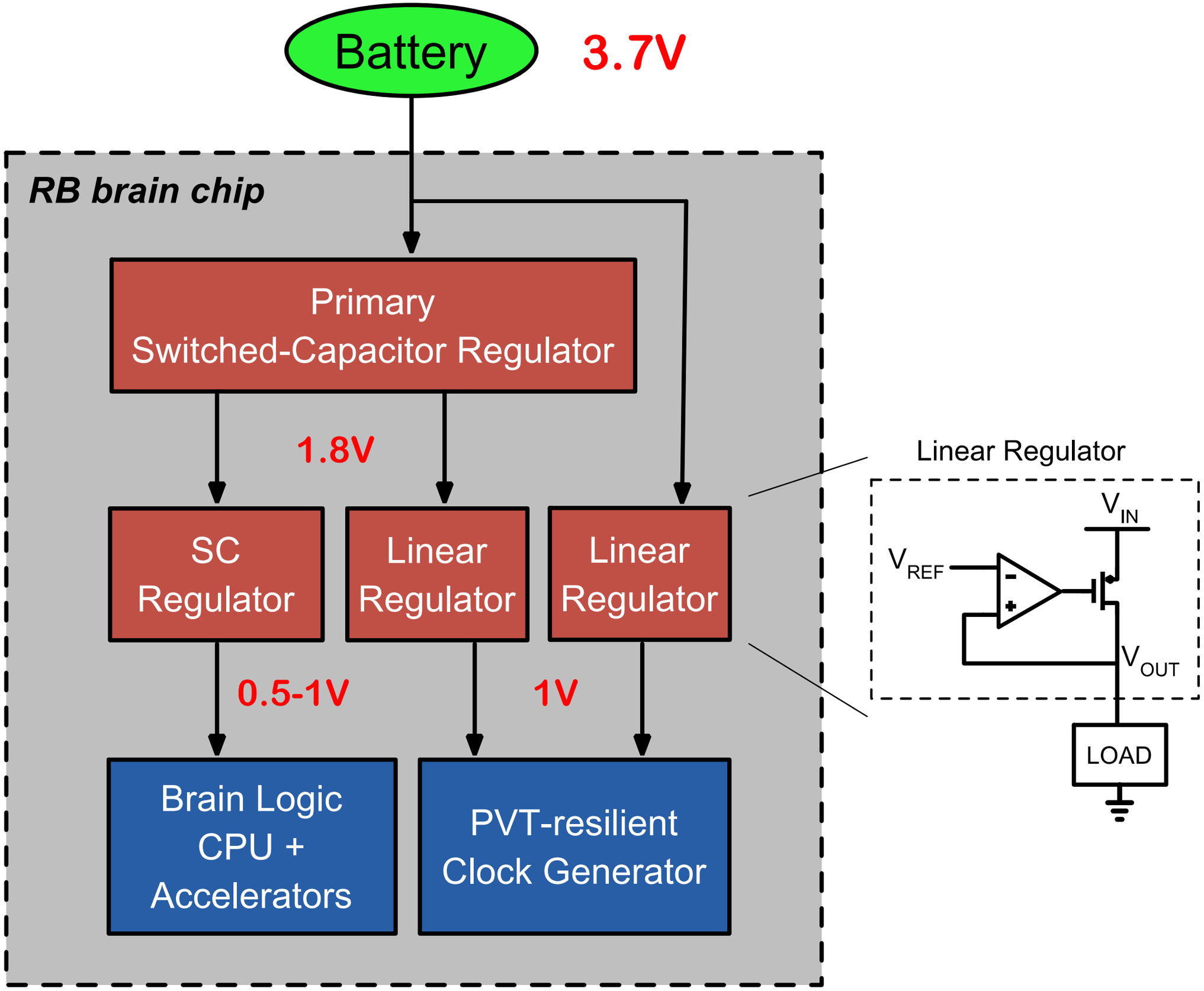
PZT actuators: 3.7V → 300V boost

Brain IC: 3.7V → 0.9V

Objective:

Embed brain and power electronics into body scaffold with minimal size and weight overheads




Battery
3.7V
RB brain chip
Primary
Switched-Capacitor Regulator
1.8V
SC
Regulator
Linear
Regulator
Linear
Regulator
0.5-1V
1V
Brain Logic
CPU +
Accelerators
PVT-resilient
Clock Generator
Linear Regulator
V_{IN}
V_{REF}
V_{OUT}
LOAD

Future directions

- Explore different packaging/process technologies to improve IVRs
  - SMT passives on top of die
  - Package/System-in-Package (P/SiP)
  - 2.5D silicon interposers
  - 3D stacking
- Architectural IVR models to facilitate design-space exploration