

An abstract geometric graphic on the left side of the slide, consisting of several overlapping squares and rectangles in shades of gray, creating a complex, layered effect.

# ***POWER DELIVERY CHALLENGES FOR NEXT GENERATION HIGH PERFORMANCE SOCS***

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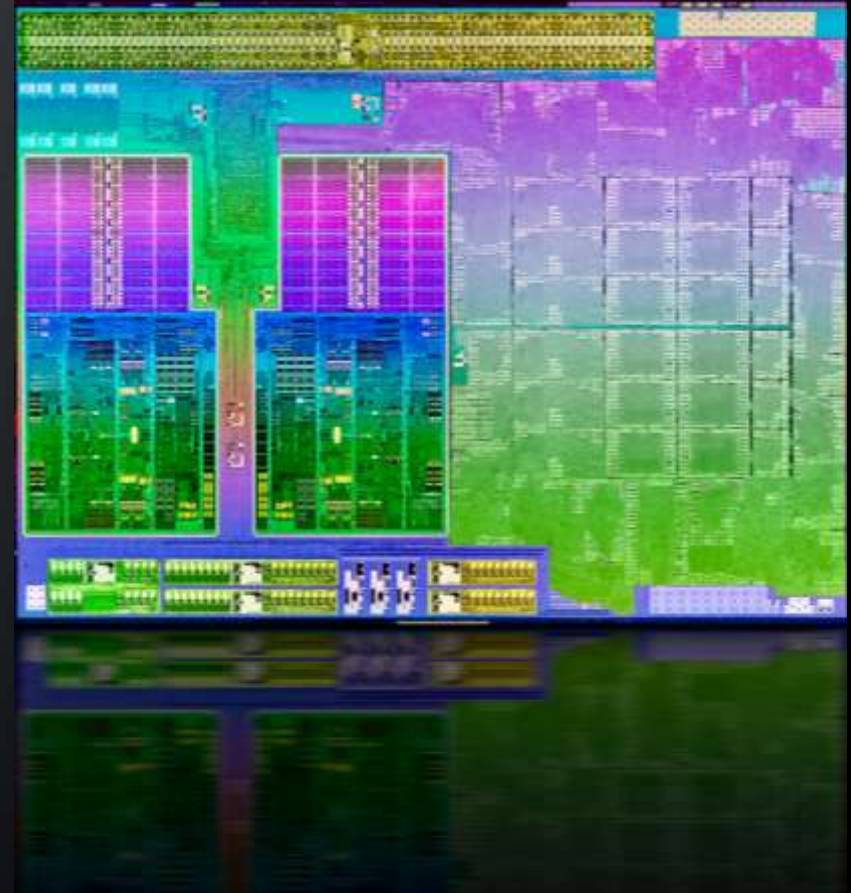
# AGENDA

- High Performance APU Overview
  - Voltage rail requirements
  - IP components
  - Fine grain power gating
  - SVI2 interface
- Package Power Delivery Constraints
  - Physical constraints
  - Potential issues for integrated voltage regulator (IVR) solutions
- System AC Response
  - Simplified power distribution model
  - Variable frequency clocks
- Minimal IVR efficiency requirement
- Concluding remarks



# HIGH PERFORMANCE APU “TRINITY”

- “Piledriver” Cores
  - Quad CPU Core with total of 4MB L2
- 2nd-Gen AMD Radeon™ with DirectX® 11 support
  - 384 Radeon™ Cores 2.0
- HD Media Accelerator
  - Accelerates and improves HD playback
  - Accelerates media conversion
- Enhanced Display Support
  - 3 Simultaneous DisplayPort 1.2 or HDMI/DVI links
  - Up to 4 display heads with display multi-streaming



	Nominal Voltage (V)	TDC (A)	Max Load Step (A)
VDD	Variable	50	42
VDDNB	Variable	29	37
VDDIO	1.5	3.2	-
VDDR	1.2	3.5	-
VDDP	1.2	4	-
VDDA	2.5	0.75	-

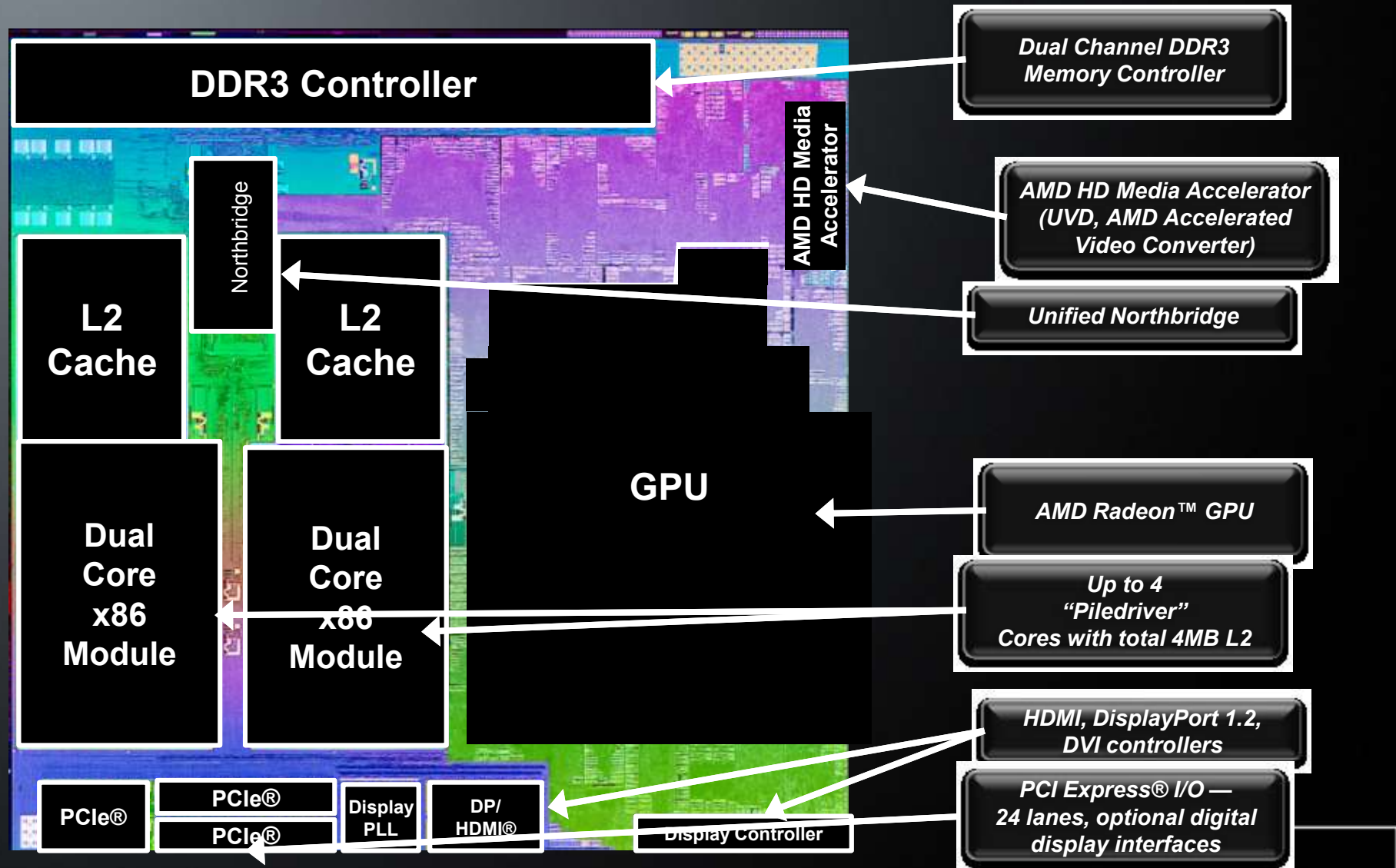
← 6 voltage rails



# "TRINITY" APU

32nm SOI, 246mm<sup>2</sup>, 1.303BN TRANSISTORS

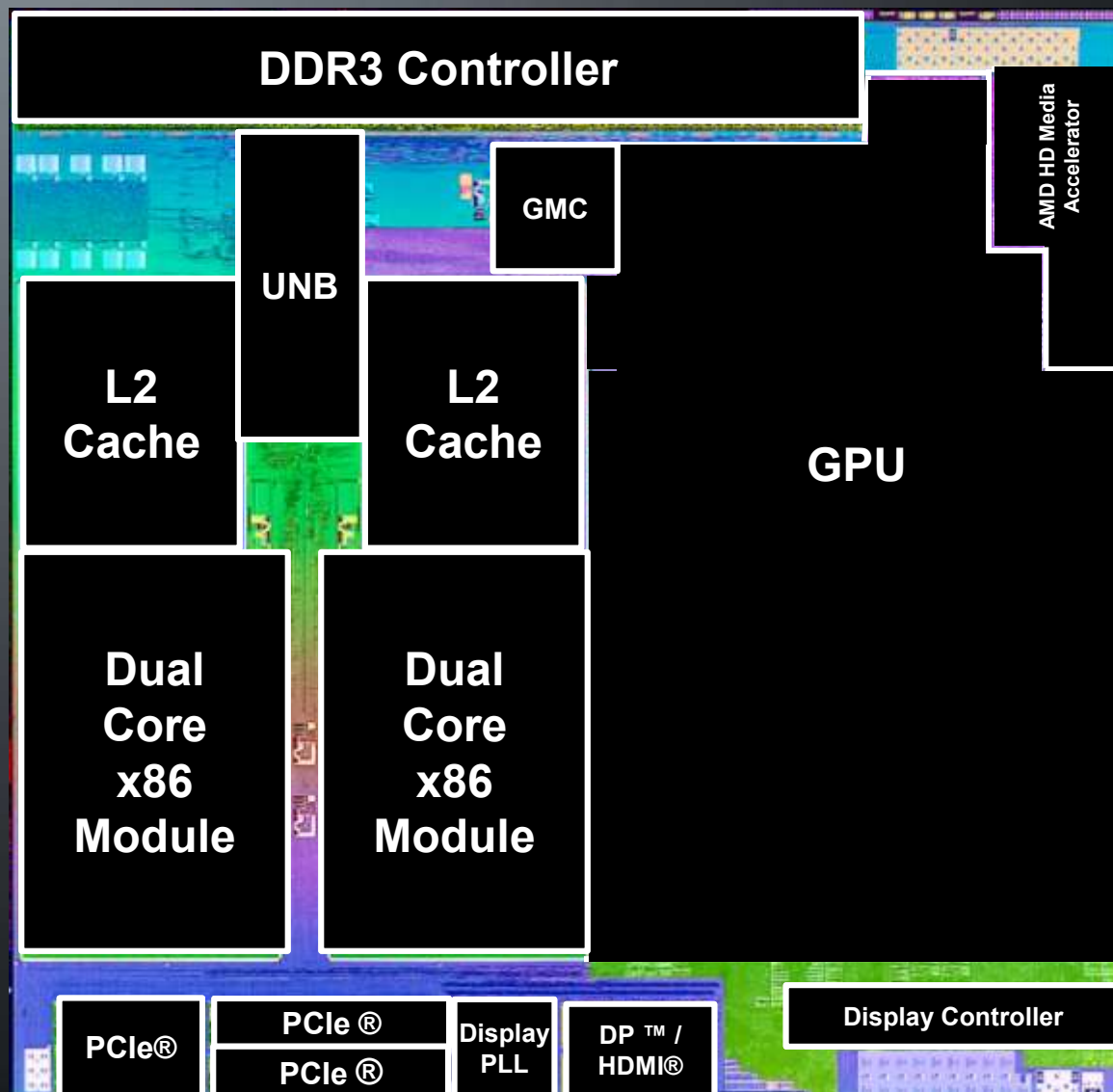
**Multiple, mode configurable IP blocks**  
**Provides performance on demand**



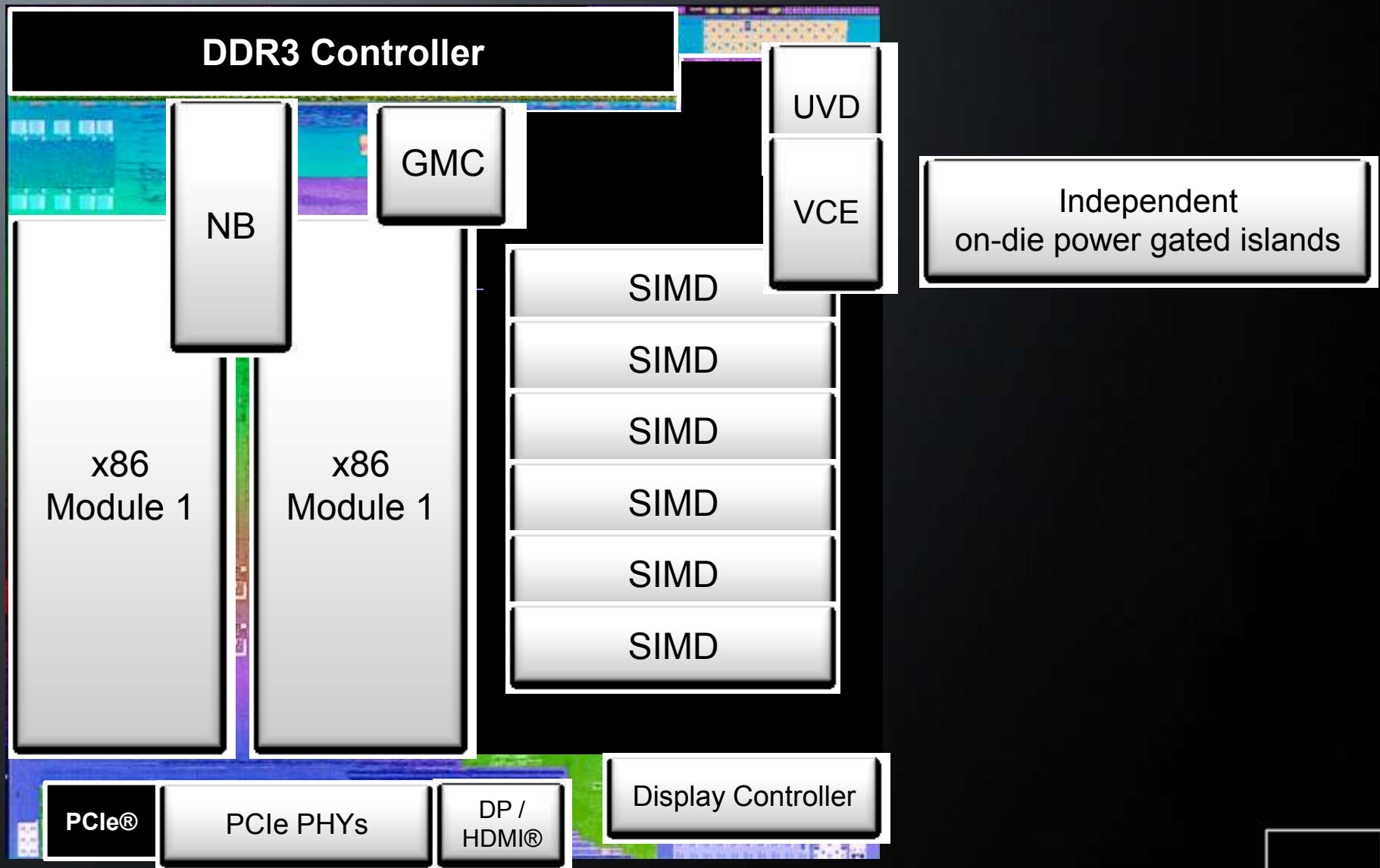
Sebastien Nussbaum, Hot Chips, Palo Alto, 2012



# ***“TRINITY” APU FINE-GRAIN POWER GATING ISLANDS***

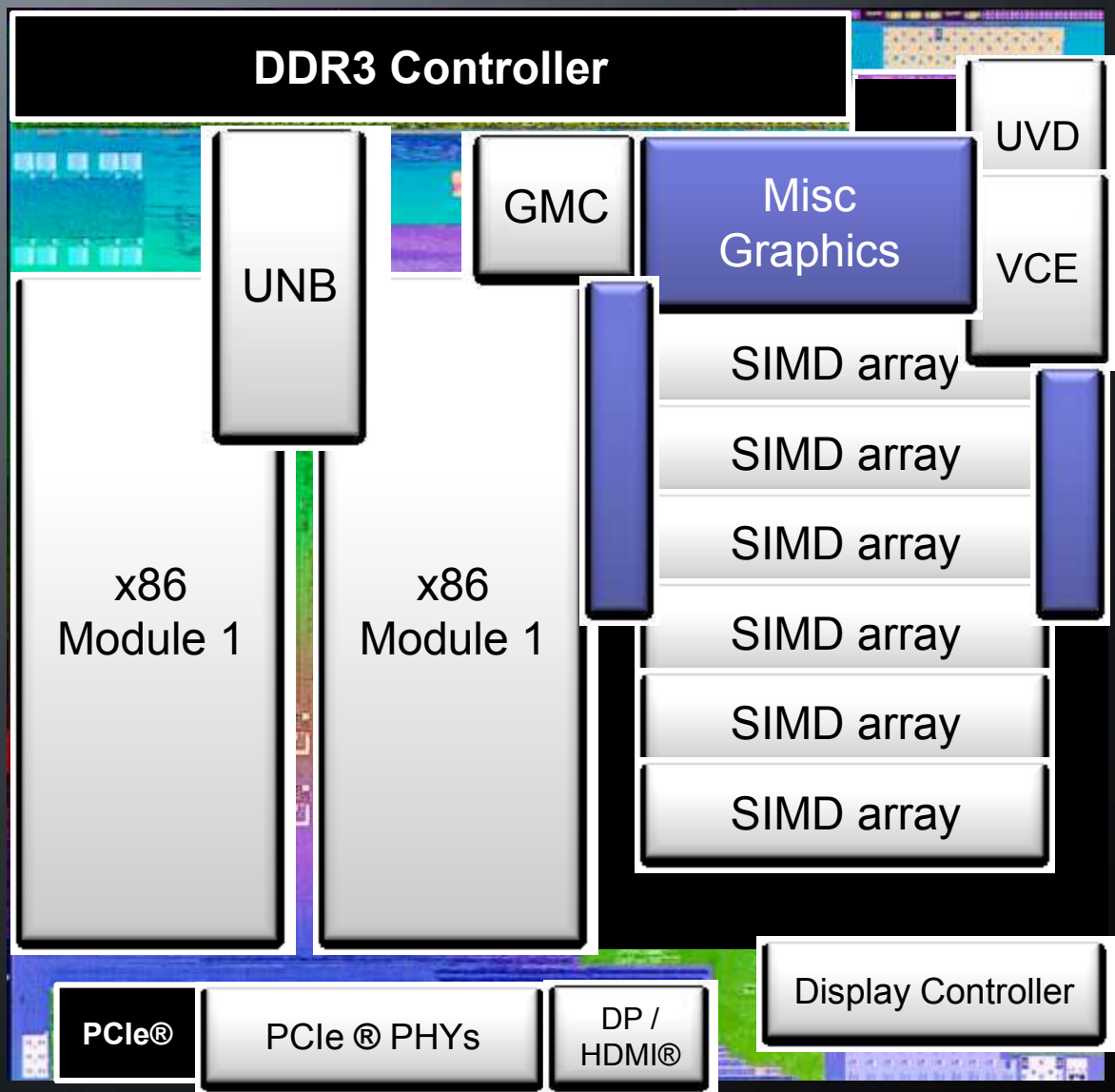


# ***“TRINITY” FINE-GRAIN POWER GATING ISLANDS (2)***





# "TRINITY" FINE-GRAIN POWER GATING ISLANDS (3)



Independent  
on-die power gated islands

Additional power-down  
region when all graphics  
functions are shut down

***Power gating is very  
effective for configuring  
the power rails for different  
operating modes!***

***> 20X leakage current  
reduction***



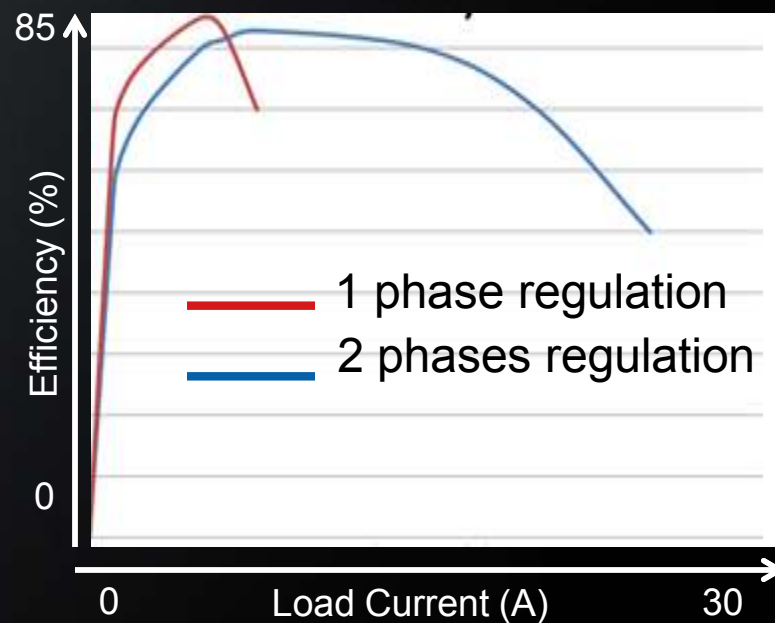
# PLATFORM POWER SAVINGS

## AMD SERIAL VOLTAGE INTERFACE 2.0 (SVI2)

- SVI is the interface which allows the system power management unit to communicate information to and from voltage regulator
- SVI2 enables quicker power state transitions
  - Faster data transmission rates (33Mhz)
  - Adds regulator response when transition is complete
  - 80+% improvement in 500mV set point change latency over SVI1
- Power efficiency features
  - Multiple Power State Indicators sent to regulator
    - PSI0 – Current low enough that regulator can shed phases
    - PSI1 – Current low enough that regulator can use pulse skipping / diode emulation
  - Load Line trim, offset
    - Ability to adjust DC offset and load line slope based on APU state

***SVI2 provides a fast power management control path***

Regulator Efficiency vs. Load



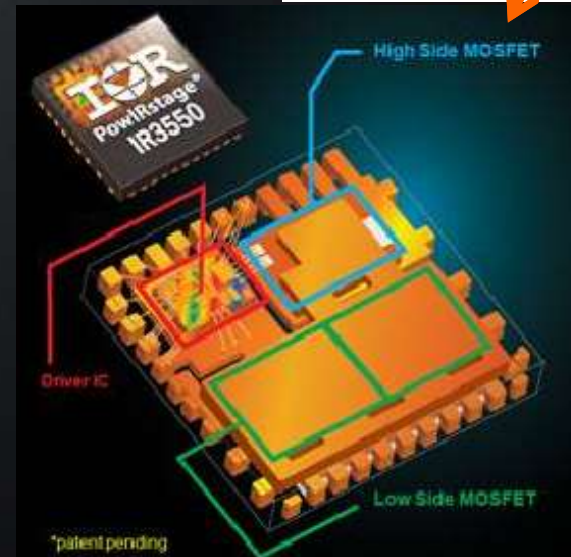
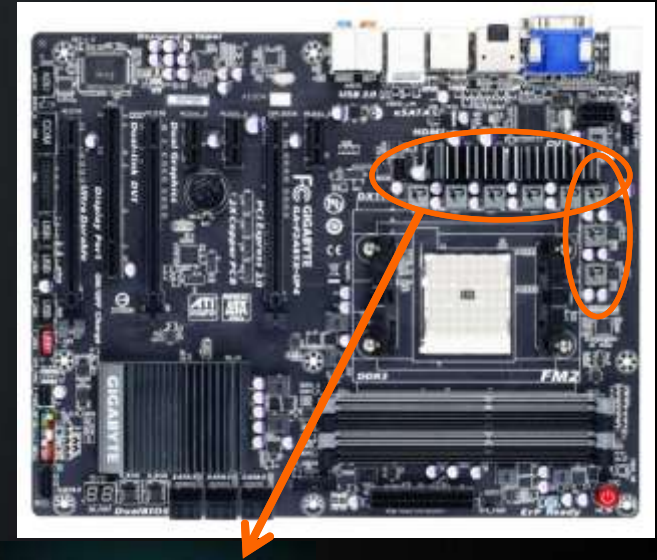


# CLIENT FM2 MOTHERBOARD

- Example Client configuration
  - IR3550 “PowIRstage” ICs from International Rectifier
  - 2X Copper PCB routes
  - High current Ferrite Core Chokes rated up to 60A
- Minimal resistive losses from VRM to APU are possible

$R_s < 1\text{m}\Omega$  typical  
(as seen in similar systems)

**Today's system power delivery solutions are highly optimized for low loss and efficiency**



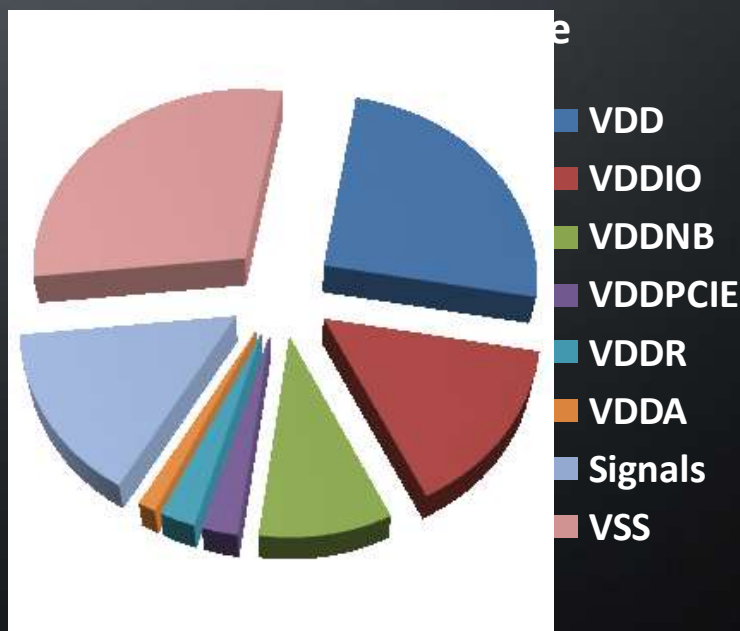
<http://www.irf.com>

<http://www.pcp.com/news/Motherboards/GIGABYTE-Unveils-Exclusive-Ultra-Durable-5-Technology-Computex-2012>

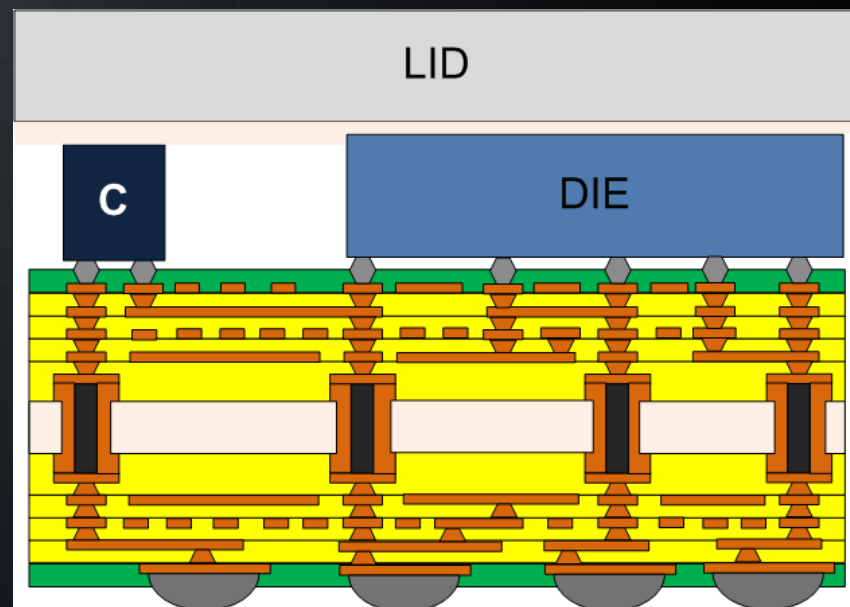


# TYPICAL PACKAGE CONSTRUCTION

- Package resources limitations
  - Limited number of metal layers
  - Competing resources
  - z-height constraints
  - Dielectric maximum voltage limits
- Additional layers or size increase costs



## Typical package cross-section

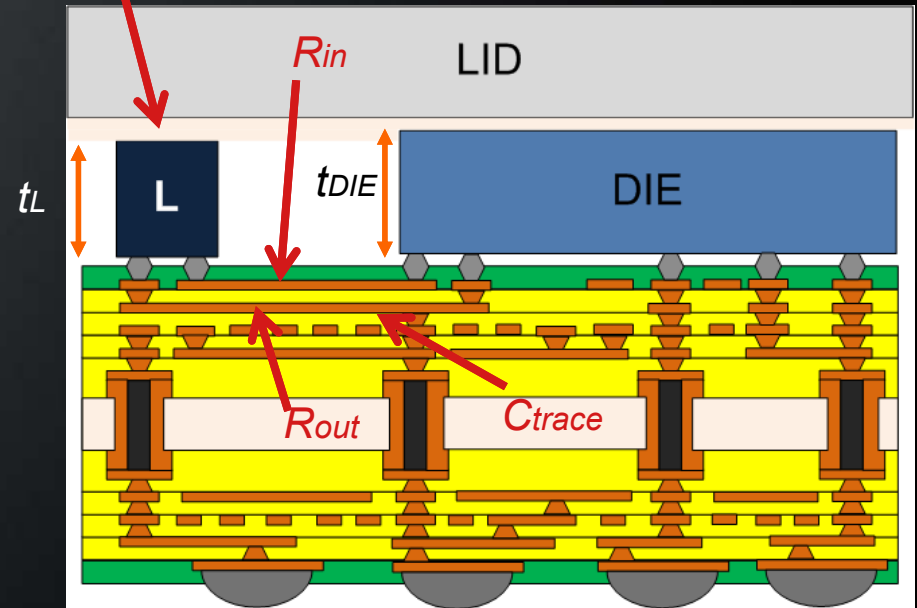


***Package design is optimized for power delivery and signal integrity***

# PACKAGE LEVEL DISCRETE SURFACE MOUNT INDUCTOR

- Not as simple as it sounds
  - Thermal heating of inductor
    - $I^2R$  heating in inductor can be significant
    - Physical height should match die
      - Variations can cause problems
      - Can have poor thermal conduction to heat spreader
  - Power loss of route
    - $I^2R$  loss in package trace
    - $CV^2f$  loss in package trace
    - Skin effect loss at high  $F_{sw}$

Thermal Conduction

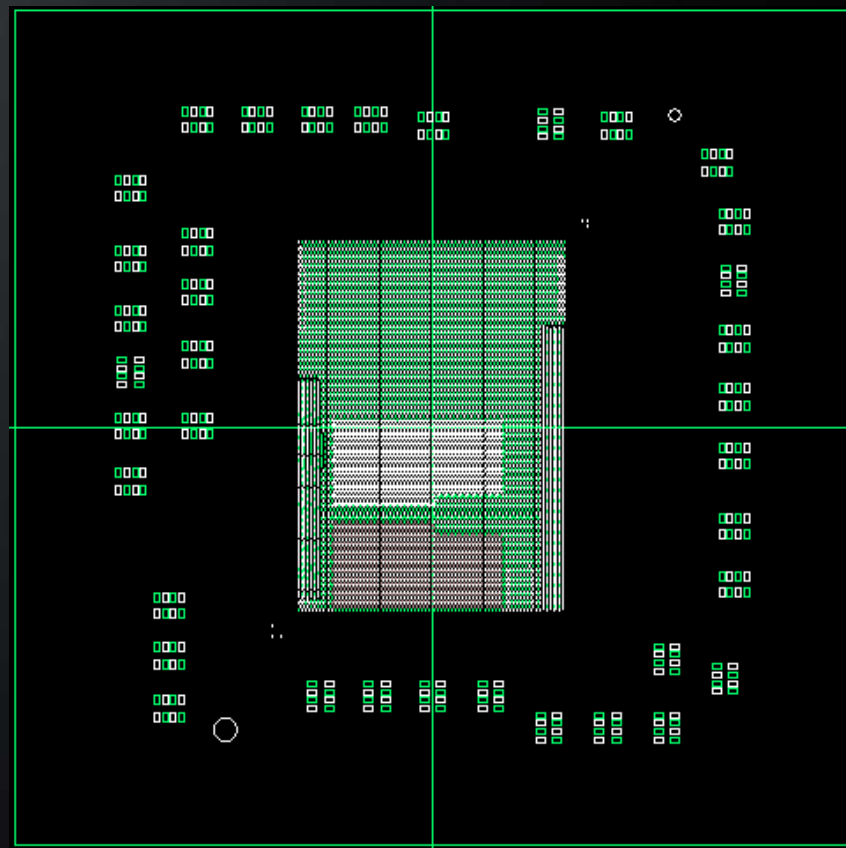


***Integrated voltage regulation presents numerous challenges***



# PACKAGE SPACE CONSTRAINTS

- Limited number of locations available for passive components
- Keep-out regions add further limitations
- Back-side cavity locations can provide some relief
  - At the cost of inductive connections
- Multi-chip packages
  - Additional cost and complexity
- Possible IVR components
  - Controller IC
  - Power FETs
  - Inductors
  - Capacitors

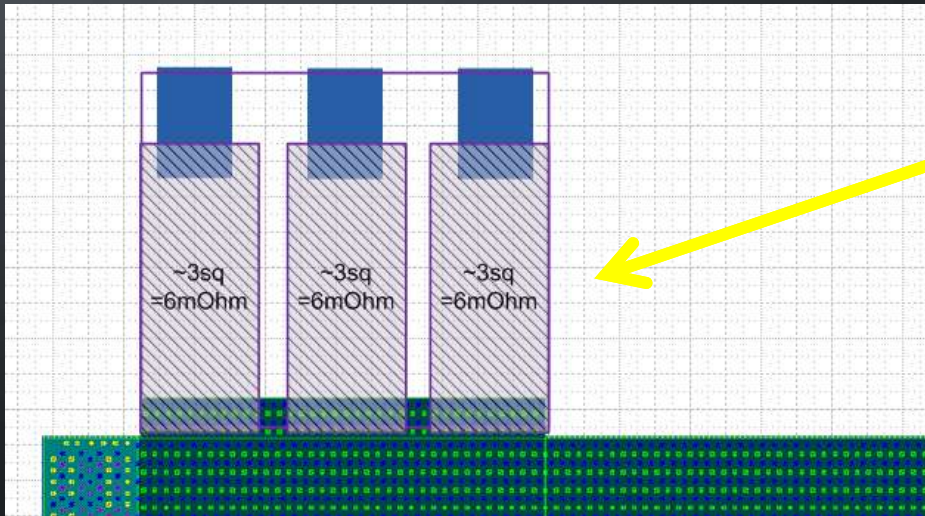


***Physical package size is a major constraint for an integrated voltage regulator solution***

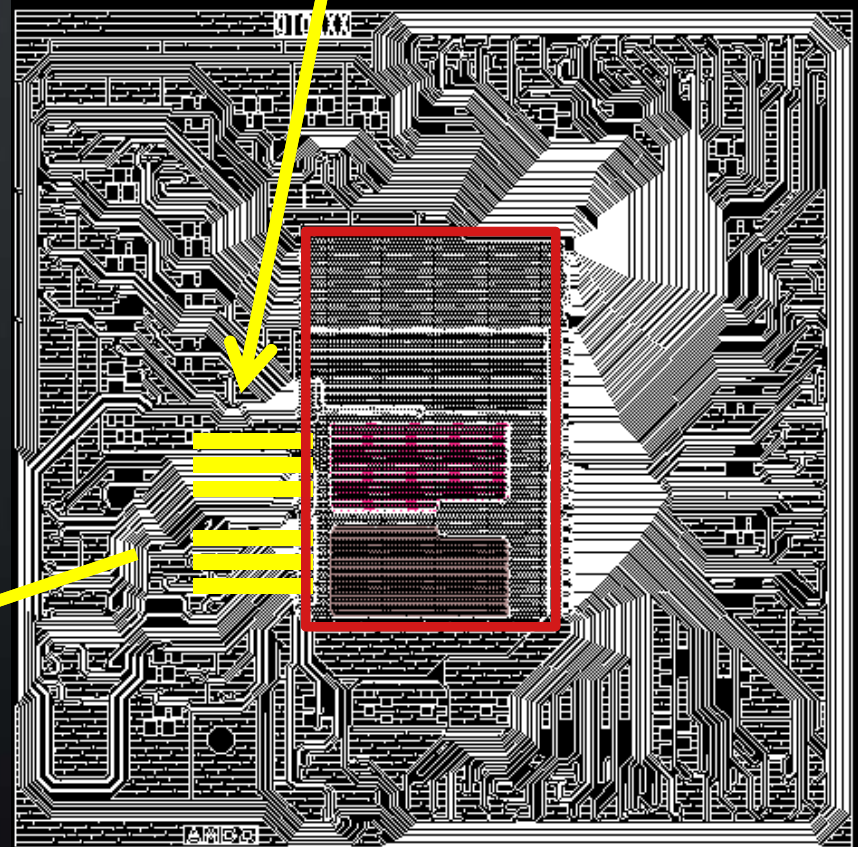


# IVR ROUTING CONSTRAINTS

- Top level metal already very congested with I/O routing
- New chip floorplans are required to optimize connections to discrete components
- Package routes still have significant resistance
  - Resistance in the single digit mOhm range for reasonable metal usage

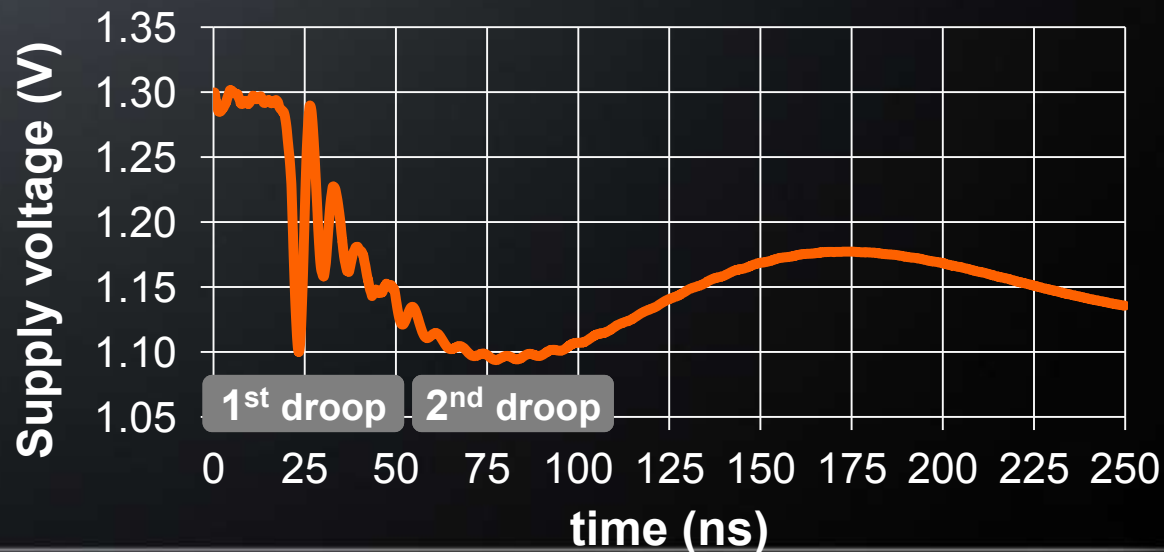
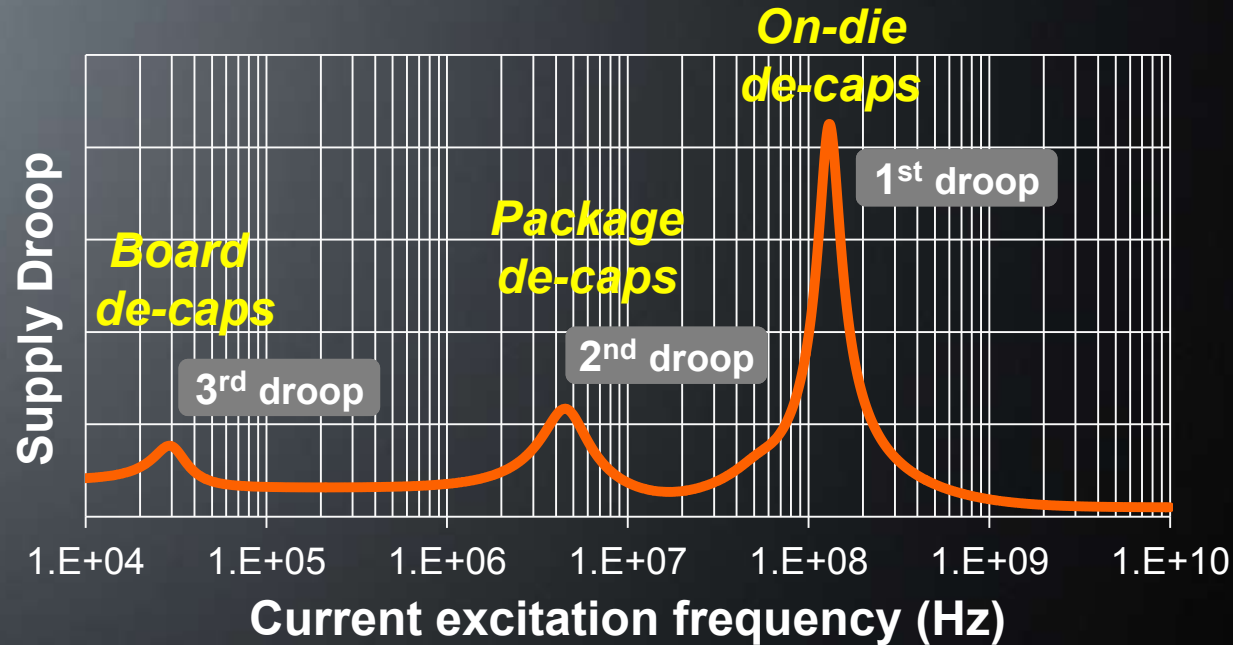


Potential routes to discrete inductors



**An IVR solution must compete with signal routes and external supplies**

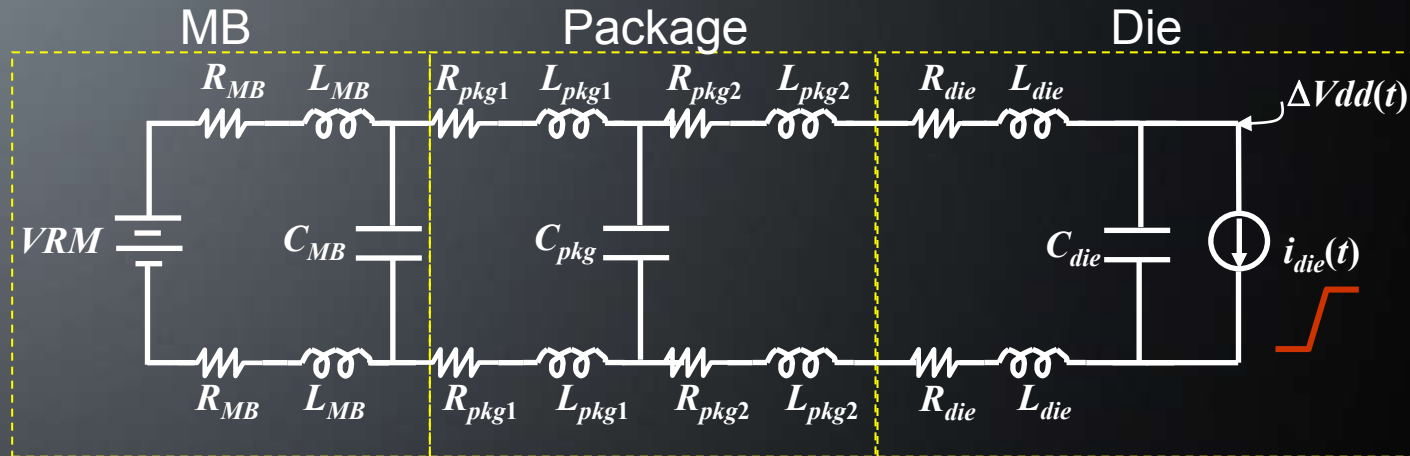
# TYPICAL FREQUENCY AND TRANSIENT STEP RESPONSE





# TYPICAL MICROPROCESSOR POWER DELIVERY NETWORK

## Simplified power distribution lumped model



- Different resonance frequencies (100s of MHz – KHz)
- Sudden changes in load ( $i_{die}(t)$ ) cause undershoot/overshoot in supply
  - De-cap added at different levels to suppress this supply noise
- On-die de-cap typically < 100nF per voltage rail
  - Not enough to satisfy the demands of a high performance processor
  - Significantly more will require expensive MIM cap technology
- IVR designs will require large filter capacitance
  - Package mounted capacitors would have similar ESL as today's VRM based designs

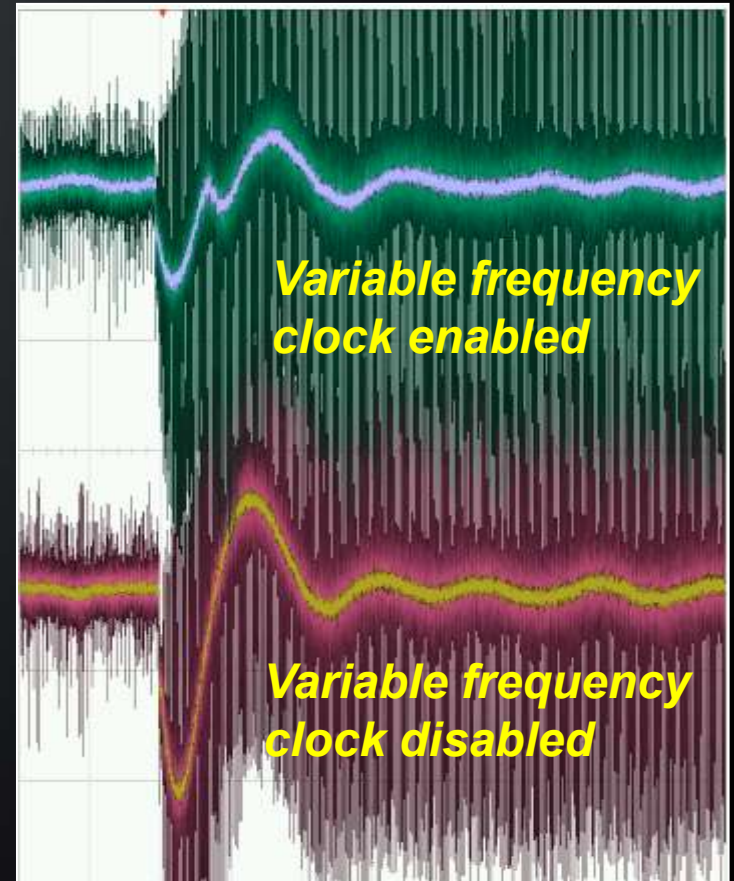
***Transient response to noise would be very similar  
between an IVR and non-IVR solution***



# NON-IVR SOLUTIONS FOR DI/DT NOISE

- 1<sup>st</sup> droop occurs very fast
  - ~5ns from onset of current step
  - Caused by the depletion of the low ESL on-die decoupling capacitance
- Variable frequency clocks can provide high speed adaptation to di/dt events at low cost
  - VFCG PLL dynamically reduces the CPU clock when supply goes below a threshold
  - > 5% performance increase for same power supply
  - > 10% power saving at same performance level

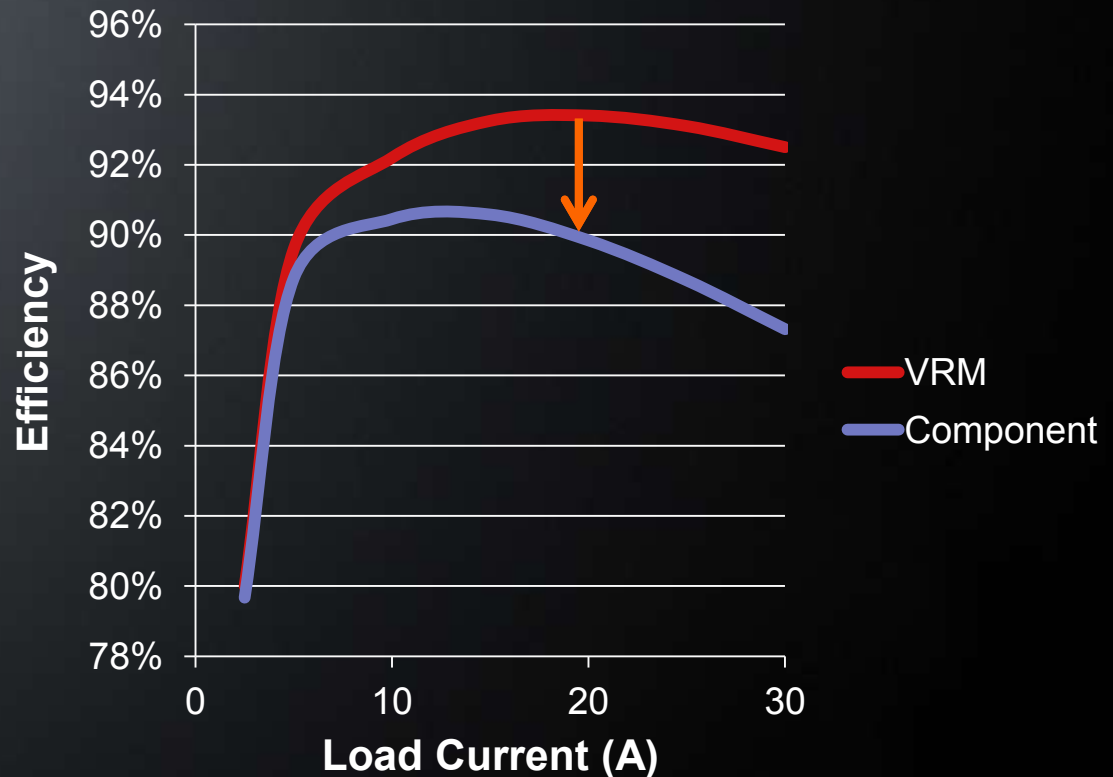
***Techniques like variable frequency clocks can reduce the need for very high speed regulator response***



Alain Artieri: “Embedded Multicore in Mobile Platforms”, presented at the Power/Performance Optimization of Many-core Processor SoCs, ISSCC Forum, San Francisco, Feb 2012.

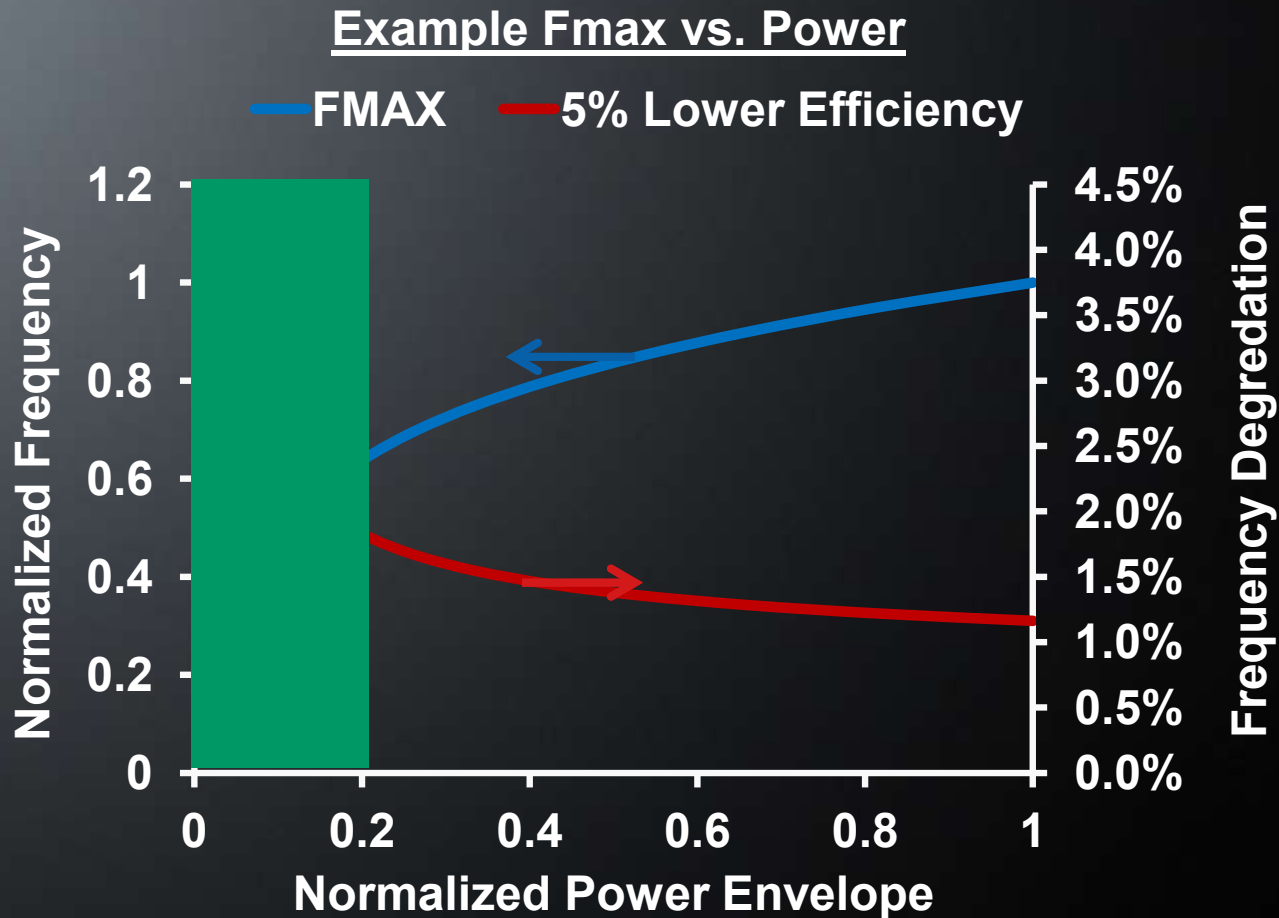
# SINGLE PHASE POWER DELIVERY EXAMPLE

- Today's VRM efficiencies can be very high
  - Does not include PWM controller power
  - High quality power components
  - Low DCR inductor
  - Low loss PCB routes
- Switching Frequencies
  - 200KHz – 1MHz
- Losses to board component
  - $I^2R$  DCR loss
  - $I^2R$  PCB route loss
- Multiple phases can further reduce losses



**+90% Efficiency across wide load range typical today**

# SYSTEM CONSTRAINED POWER SENSITIVITY TO VRM POWER EFFICIENCY

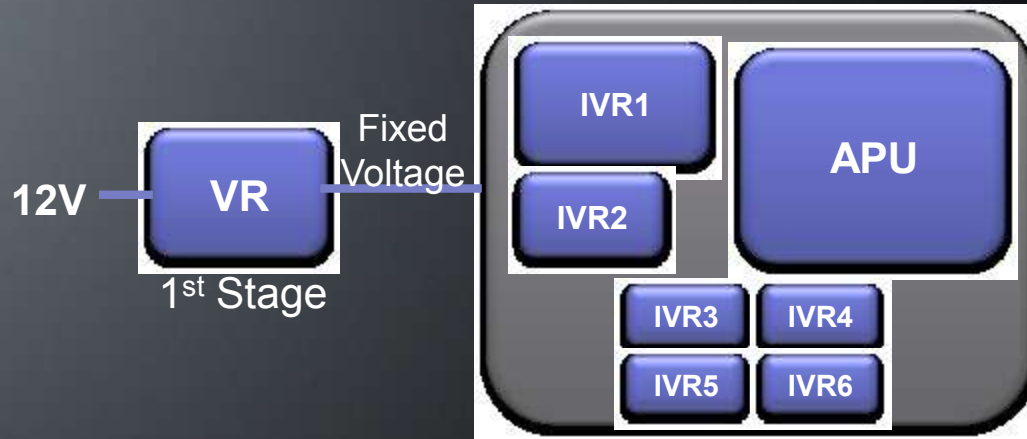


***Performance impact of power  
delivery efficiency can be significant,  
especially at low power points***

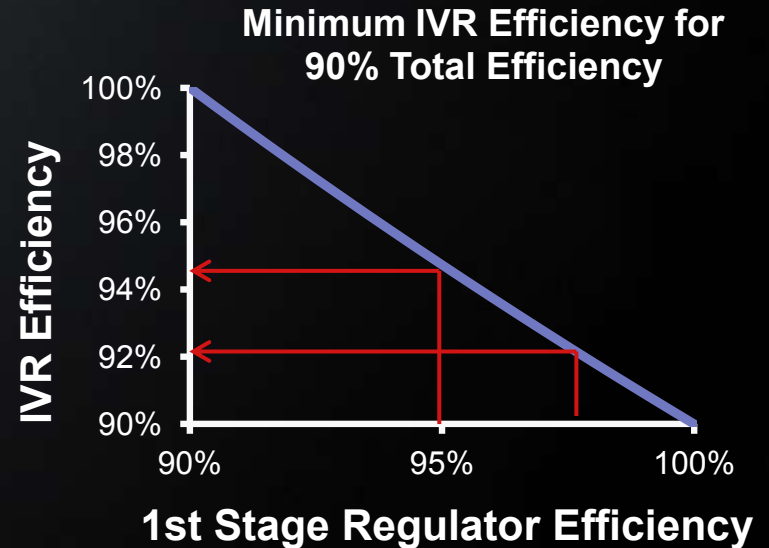


# HIGH CURRENT IVR REQUIREMENT

## Potential IVR based system



- Break Even Requirement
  - Assume Today's VRM Efficiency > 90%
  - 1<sup>st</sup> stage regulation efficiency needs to be very high to avoid excessive loss
- Need enough package space to support components for all rails
  - +2 High current rails, +4 low current rails
  - Difficult to accommodate many high current multi-phase designs



# CONCLUDING REMARKS

- High performance SOC's are integrating more and more IP blocks
  - Additional voltage rails will open up more possibilities for advanced power management
- Fine grain power gating has proven to be an effective solution for powering down unused IP blocks
  - IVR solutions must compete with computational sprinting techniques
- SVI2 provides fast power state transitions and power management control
  - Phase shedding
  - Pulse skipping
  - Load line trimming
- State-of-the-art external VRMs and good board design can provide a high efficiency power delivery solution
  - Present solutions set a very high bar, integrated solutions need a high ROI
- Package constraints limit number and placement of discrete components on package
  - We don't have unlimited space
- Variable frequency clocks can provide a low cost solution to  $di/dt$  droops
  - High speed regulator response is not a large motivation





## *CONCLUDING REMARKS (CONTINUED)*

- The three most important criteria for an integrated voltage regulator solution:
  1. Efficiency
  2. Efficiency
  3. Efficiency
  
- At low cost



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