3D Integrated Voltage Regulator Architectures

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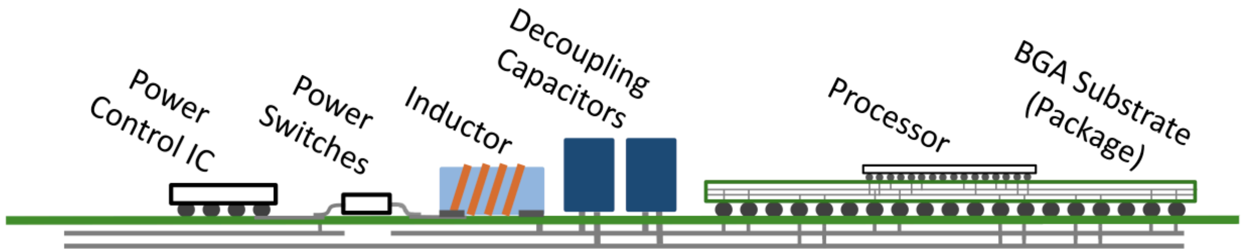
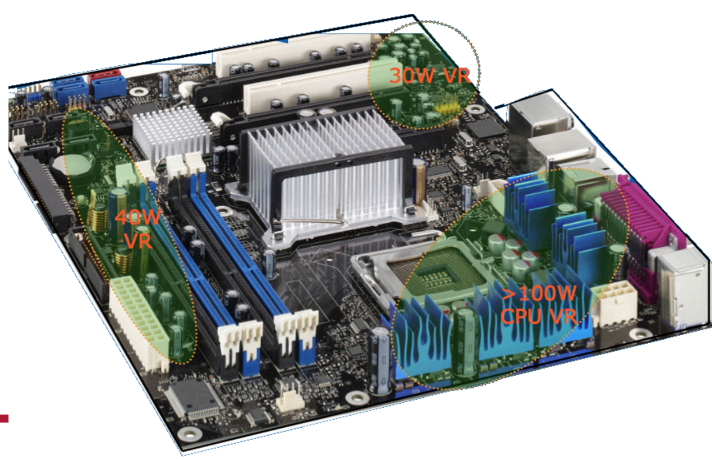
Current state-of-the-art

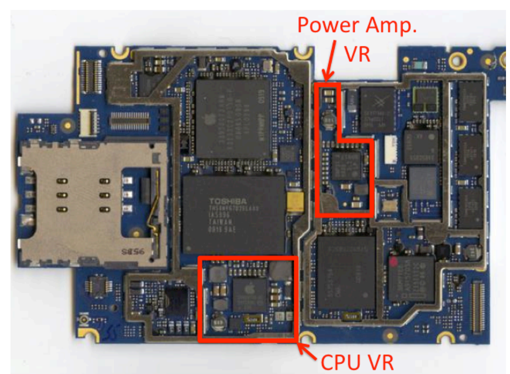
- Typical voltage regulator configuration on a motherboard



- **These regulators consume an enormous amount of real estate**



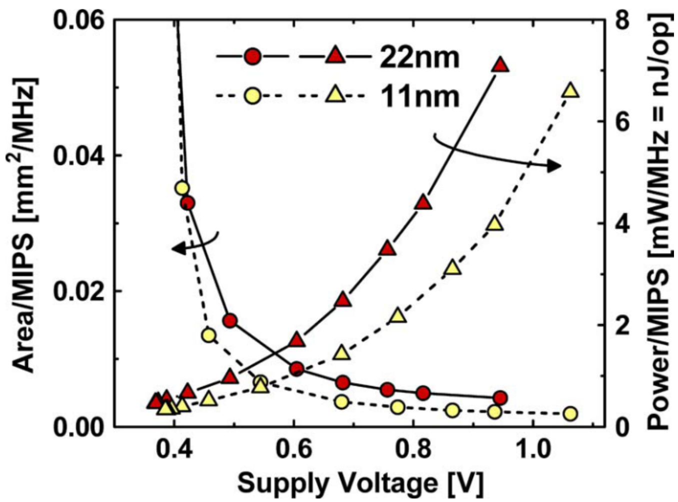
High-performance processor (40%)

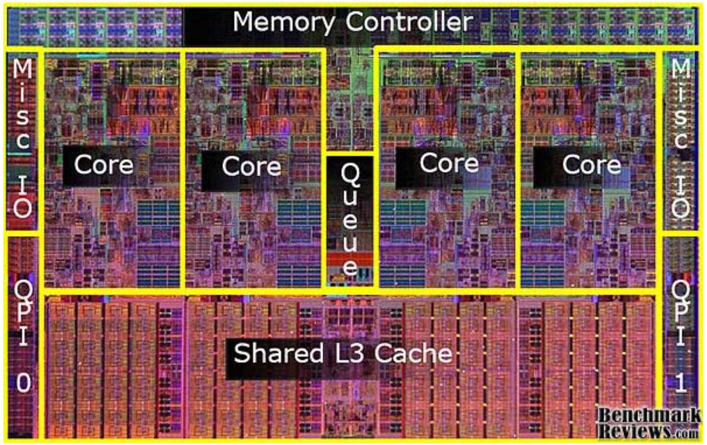


Mobile platform (20%)

Scaling challenges

- Energy-efficient operation requires aggressive, granular voltage scaling with the exploitation of parallelism. Potentially hundreds of voltage domains required, operating typically < 0.5 V.

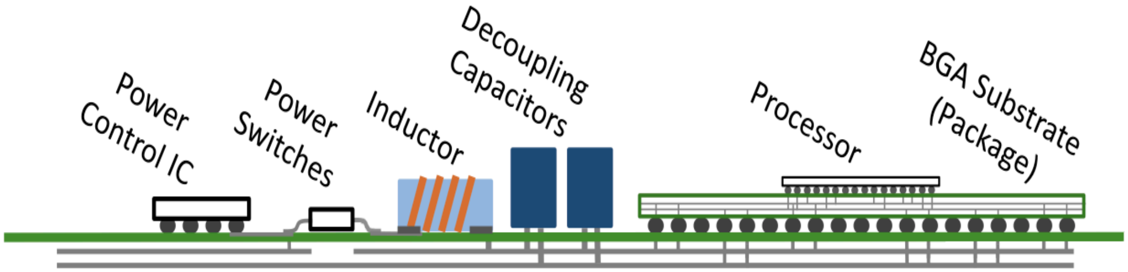




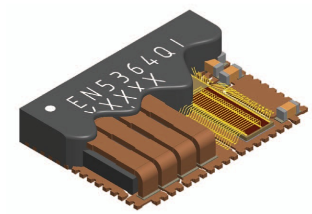
- **Very low impedance requirements on power distribution network.**

P = V I

Vision

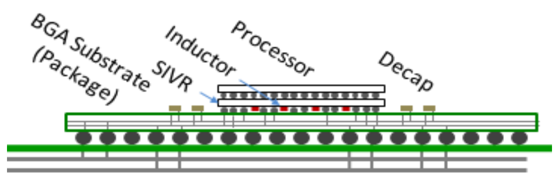


Typical motherboard configuration



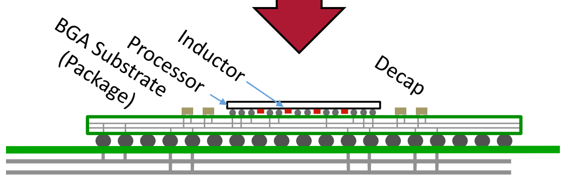
Power supplies in packages (PSIP)

- Isotropic bulk magnetics
- Densities of 40 mA/mm^3
- Single output



3D integration

- Thin-film magnetics
- 100 A +
- Multiple outputs



Monolithic integration?

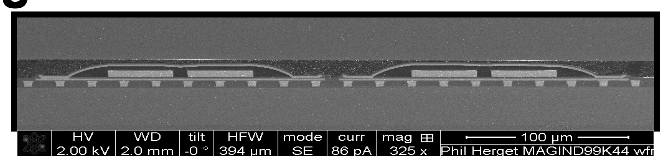
Outline

Converter specifications such as:

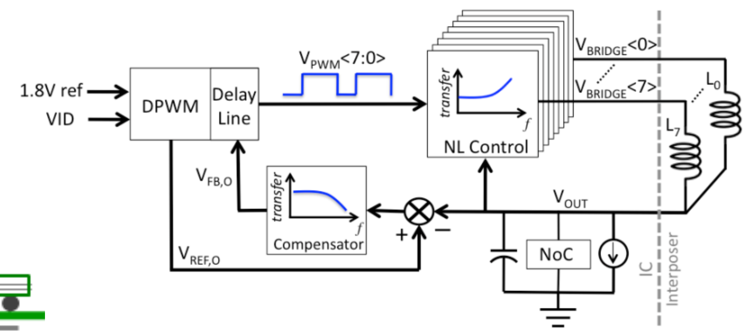
Input voltage
Maximum load current
Maximum load step and load step time constant
Maximum transient overshoot

depend on co-design of:

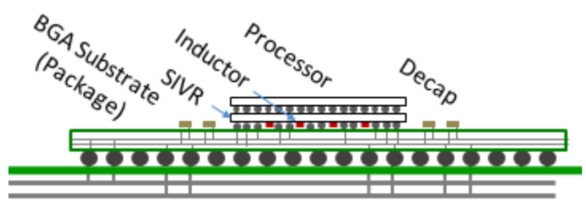
- Power inductors



- Circuits (power train and controllers)

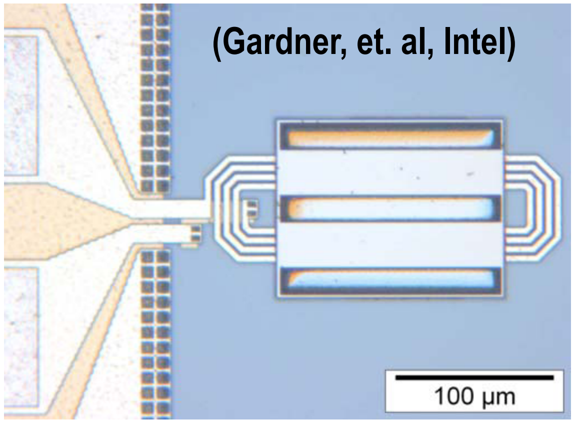


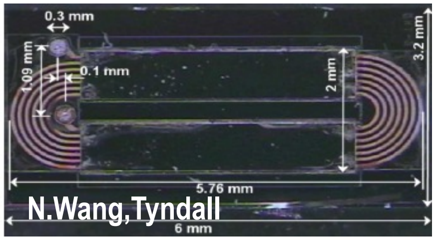
- Packaging

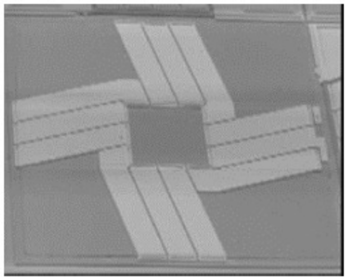


Thin-film inductors

- Structures
  - Yoke-based. Magnetic material surrounds windings.
  - Toroid. Magnetic material core
- Materials
  - $Ni_{80}Fe_{20}$, $Ni_{45}Fe_{55}$, CoZrTa, FeN, CoFe, powder composites
  - Electroplating, sputtering, packing

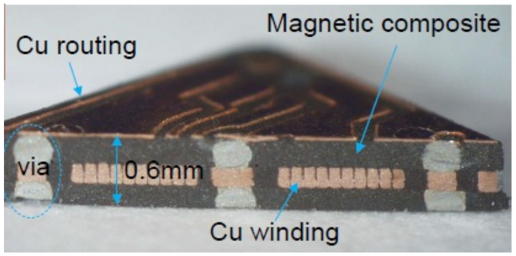






B.Orlando, STMicroelectronics

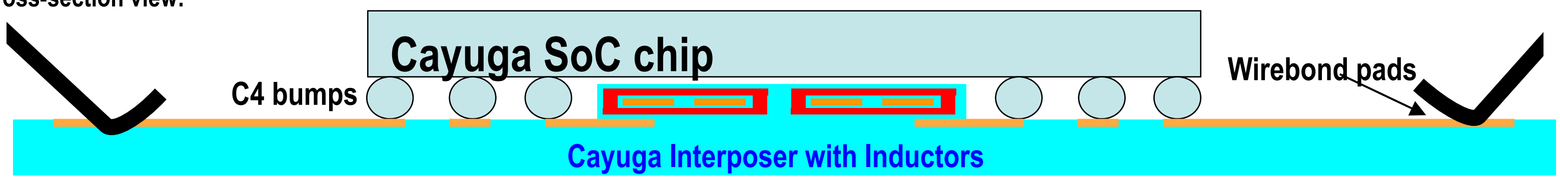
M. Wang, UF, 2010



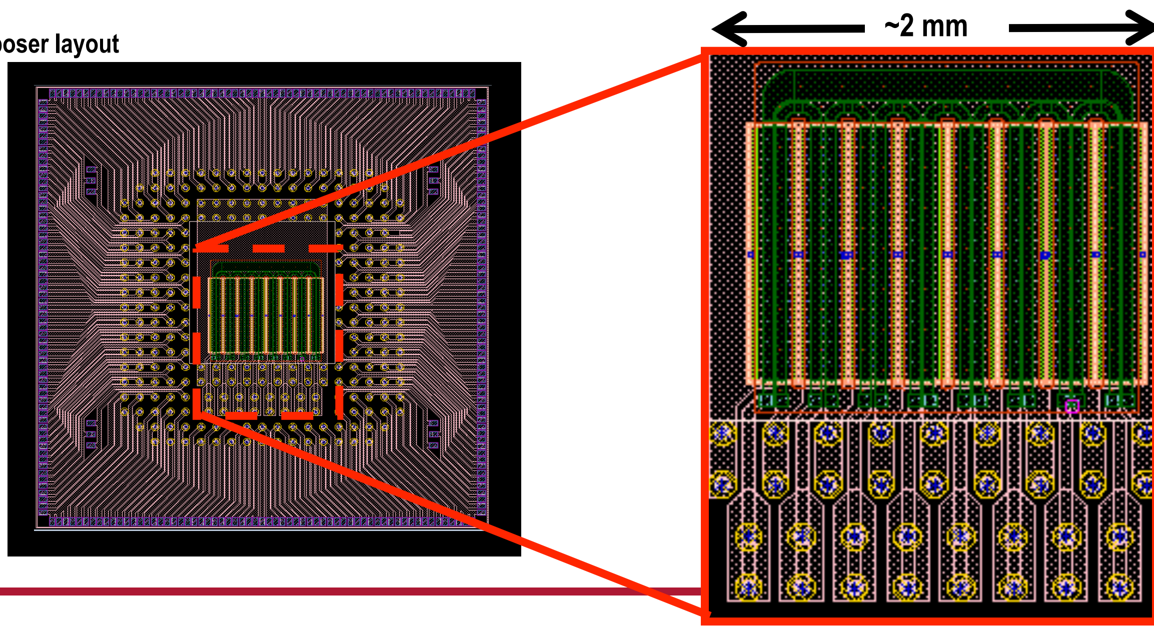
Test site: Overview

- **Control logic, switches, trench capacitors on SoC processor chip**
- **Magnetic inductors on interposer**

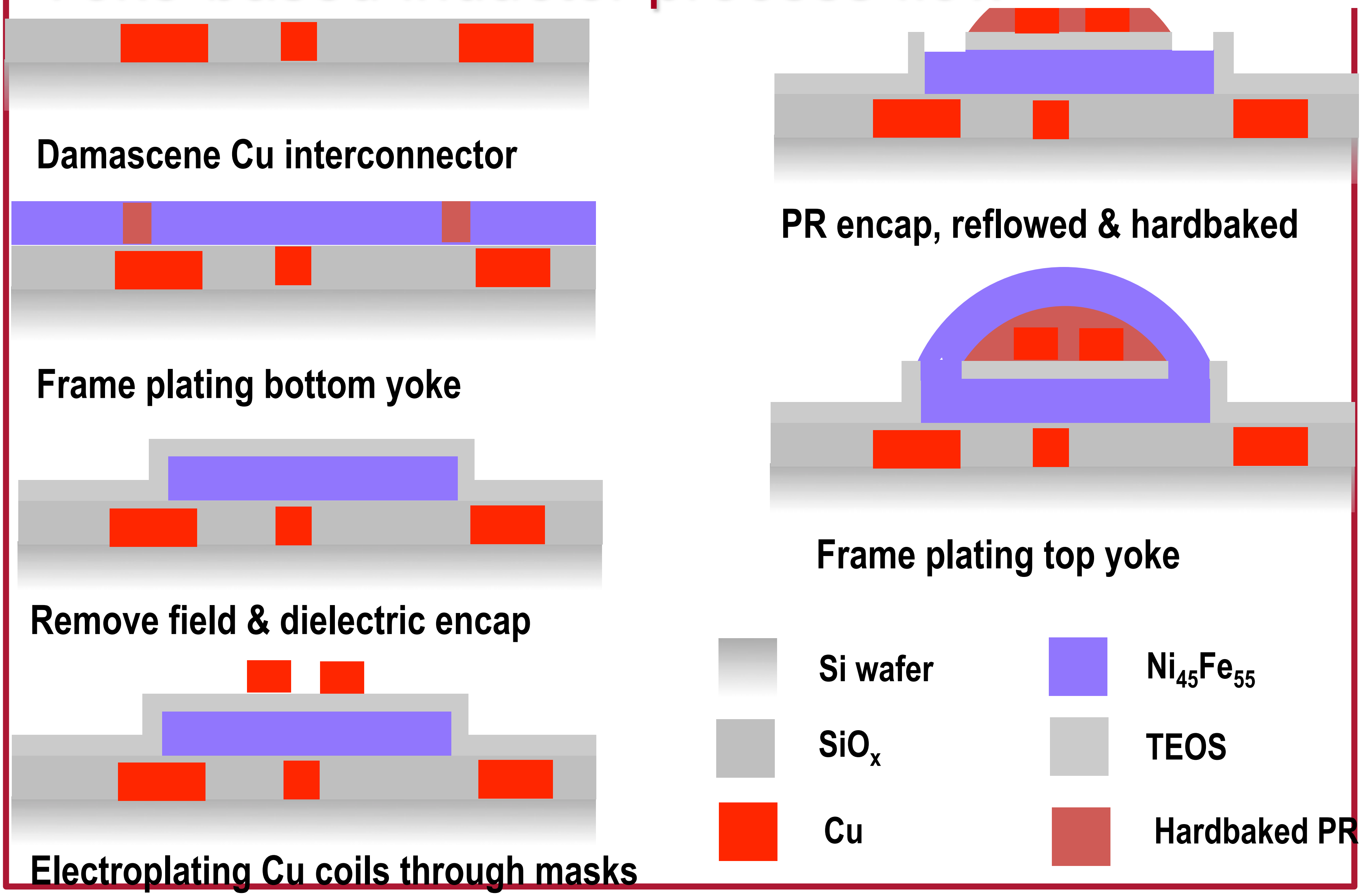
Schematic cross-section view:



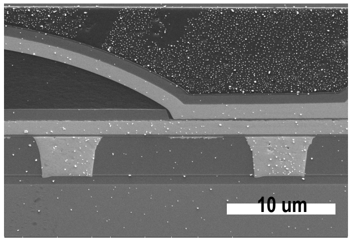
Top down view of Cayuga interposer layout

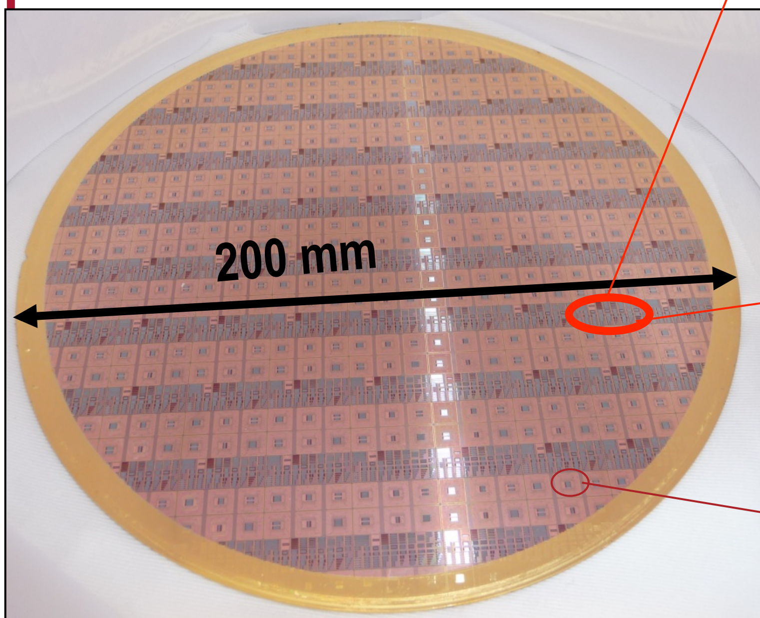


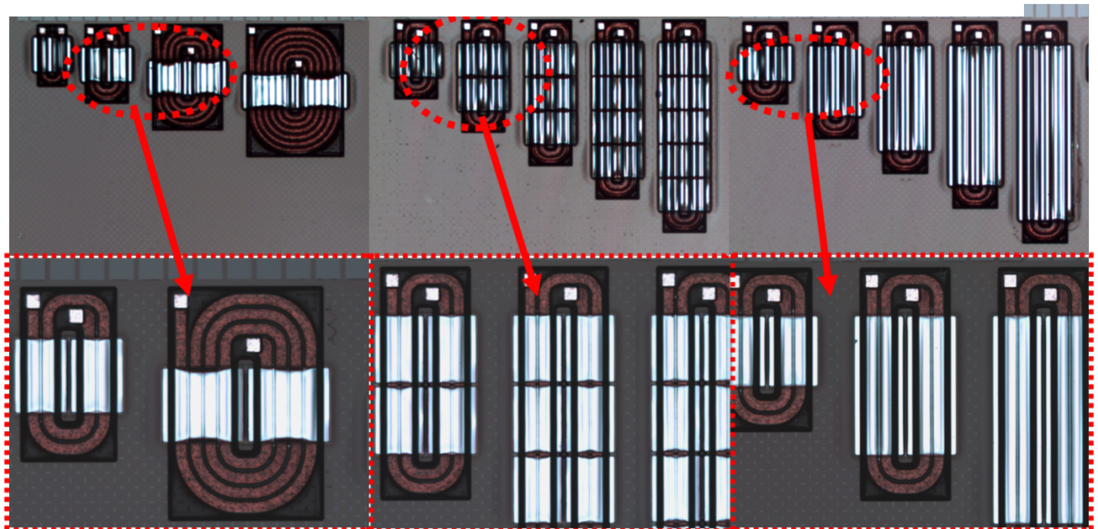
Yoke-based inductor process flow

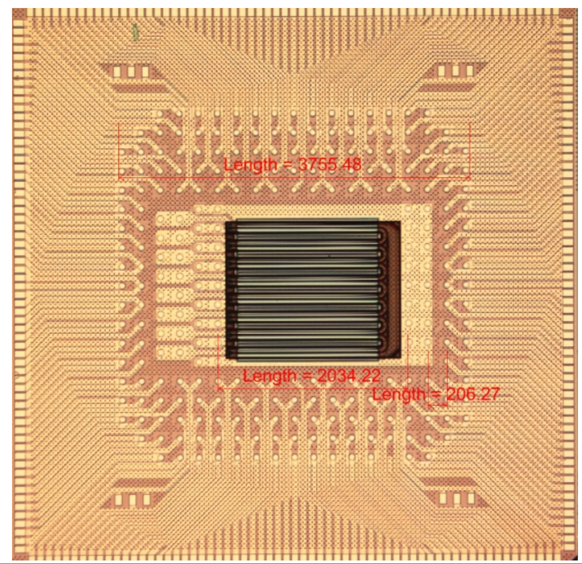


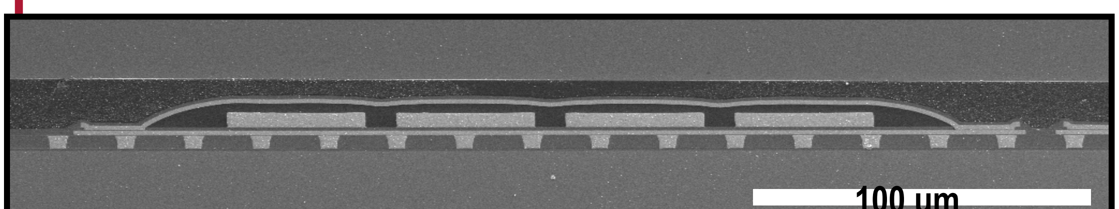
Inductor structures





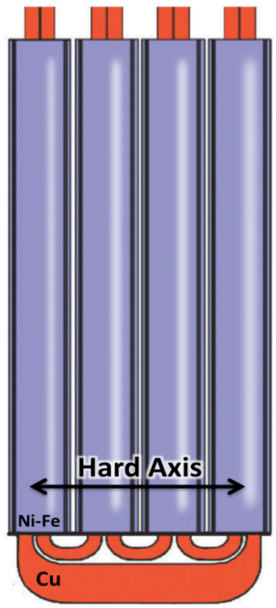


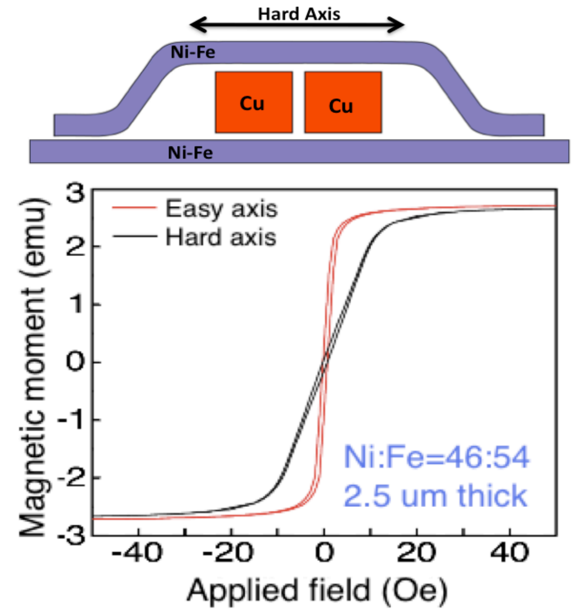




Magnetic material properties

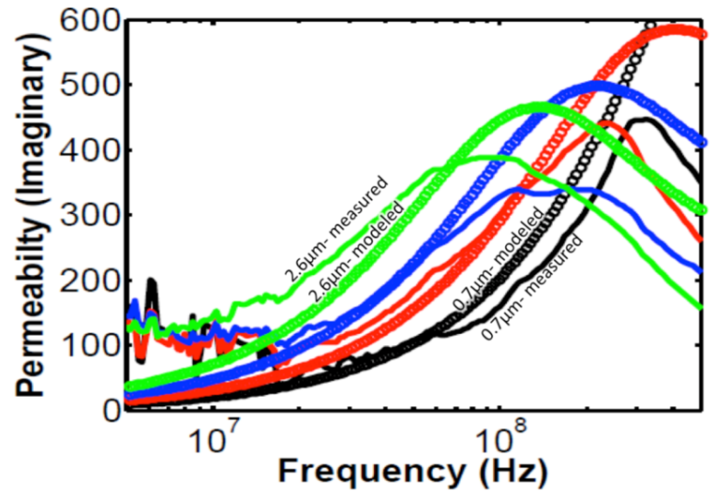
- Magnetic hysteresis loops measured by vibrating sample magnetometry (VSM)
- Coercivity of 0.2 Oe
- Saturation magnetization of 1.5 T
- Anisotropy field of 13 Oe.
- Inductor long and skinny to maximize magnetic field orientation along hard axis.

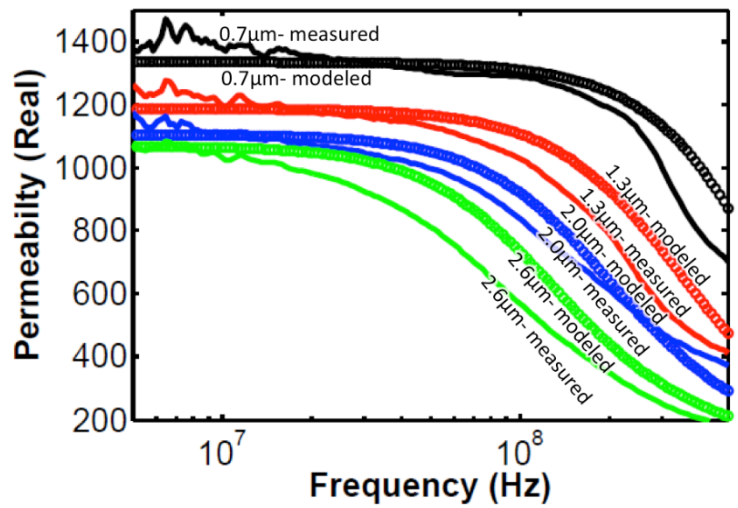




Magnetic material properties

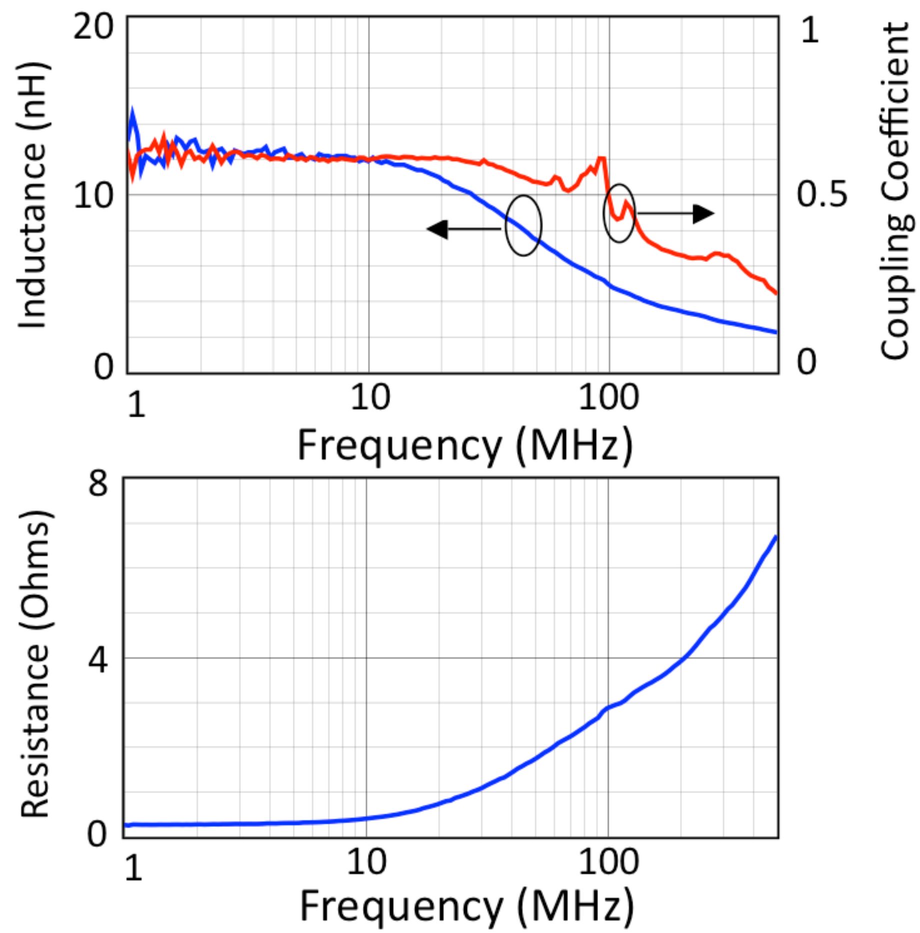
- Complex permeability spectrum obtained by measuring the the impedance of a single-stripe loop fixture loaded with $Ni_{45}Fe_{55}$
- As the thickness of the film increases, the permeabillity decreases due to shape anisotropy in the thicker films.
- The roll-off frequency also decreases with increasing thickness due to eddy currents from 200 MHz to 50 MHz.



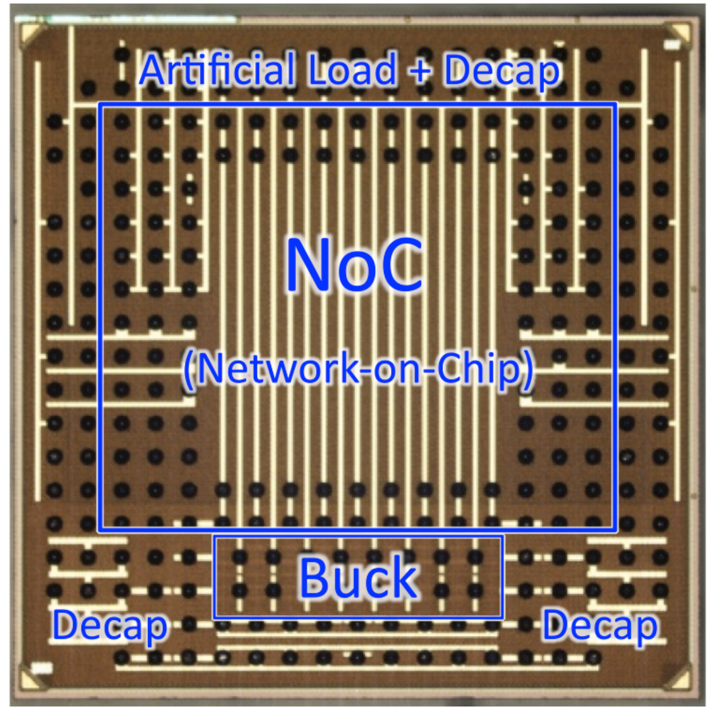


Measured Coupled Inductors Design

- $Ni_{45}Fe_{55}$ core, amenable to electroplating
- Currently, no insulation laminations to suppress eddy currents and domain wall motion; but work on this is proceeding

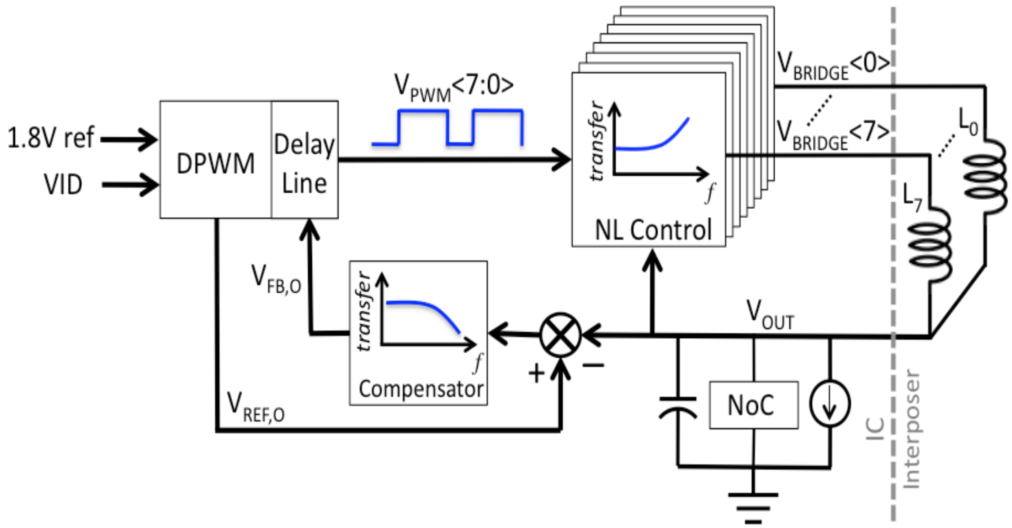


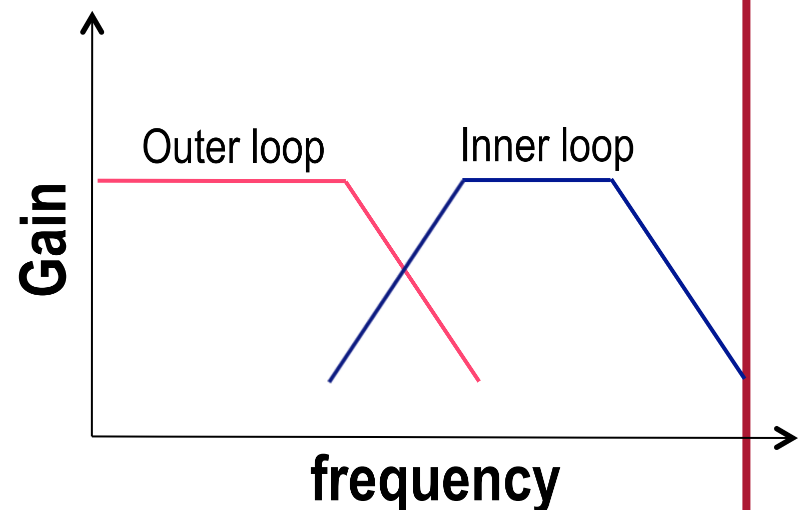
SoC: Overview



- Chip Specs
  - IBM 45nm, 4mm X 4mm, C4 IO
- 64 Tile NoC
  - Clock Gating, Diagnostics, DVFS
- 8-Phase Buck DC-DC Converter
  - Fast inner control loop (step response)
  - Digital outer control loop (adjustable load-line)
- Power Density
  - 8-phase topology reduces required C_{out}, boosts current density ~1.2X
  - Flip-chip packaging reduces package impedances, improves efficiency
- Inductors
  - Designed to mate with interposer inductors for complete integrated power chip-stack, also can incorporate package SMT air-core inductors

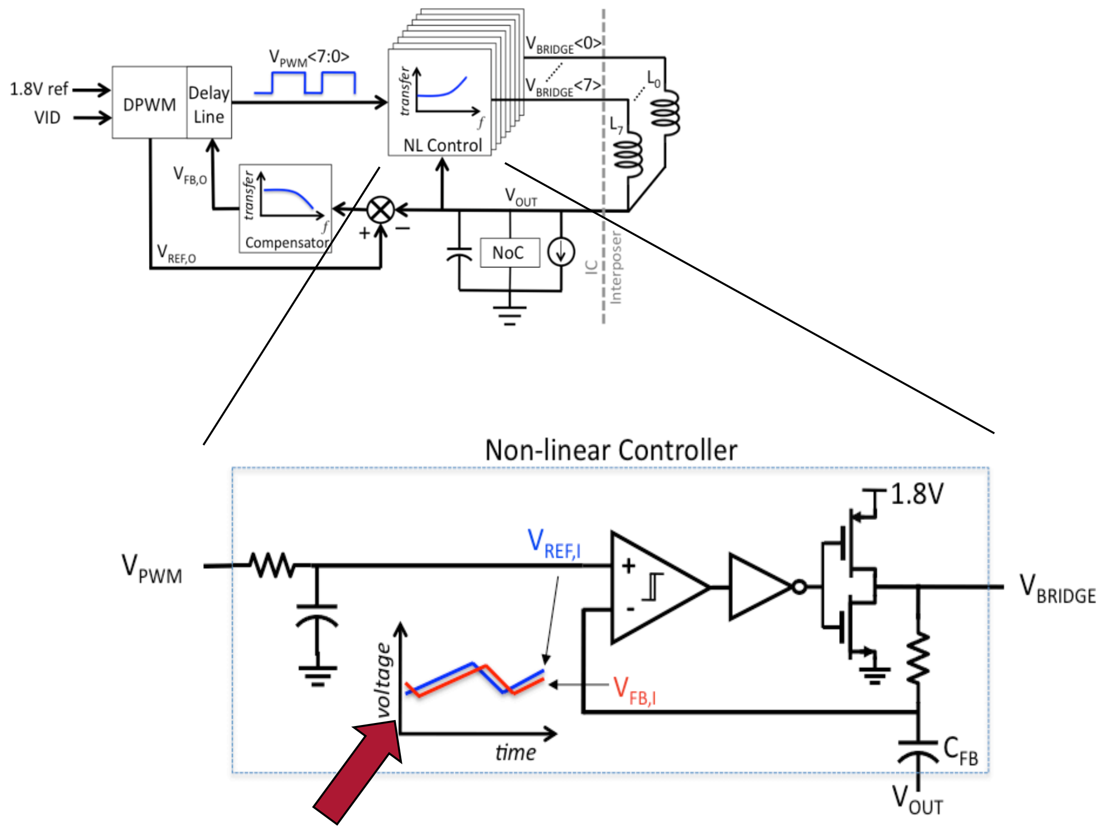
Cayuga SoC Test Chip: Controller





- Two control loops, a slow voltage-mode outer loop that provides low-frequency regulation and a fast inner loop that responds to high-frequency load transients.
- Digital pulse-width modulator (DPWM) receives a voltage identifier code (VID) – resolution of 250 ps as determined by on-chip clock reference.
- The compensator for the outer feed back loop is a low-pass filter with programmable pole frequency, chosen 10 to 16 times Nfs

Cayuga SoC Test Chip: Controller



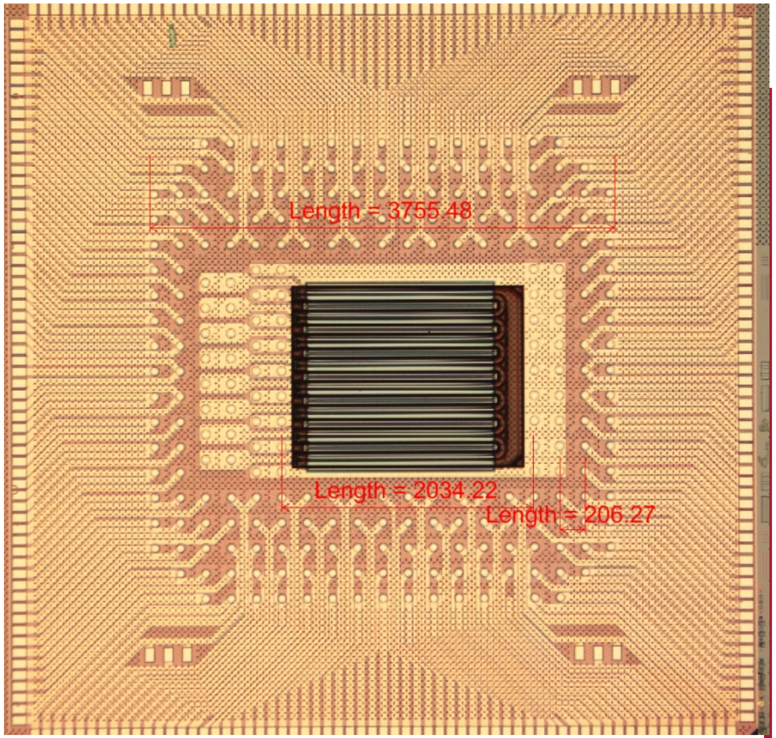
Steady-state amplitude of 150 mV

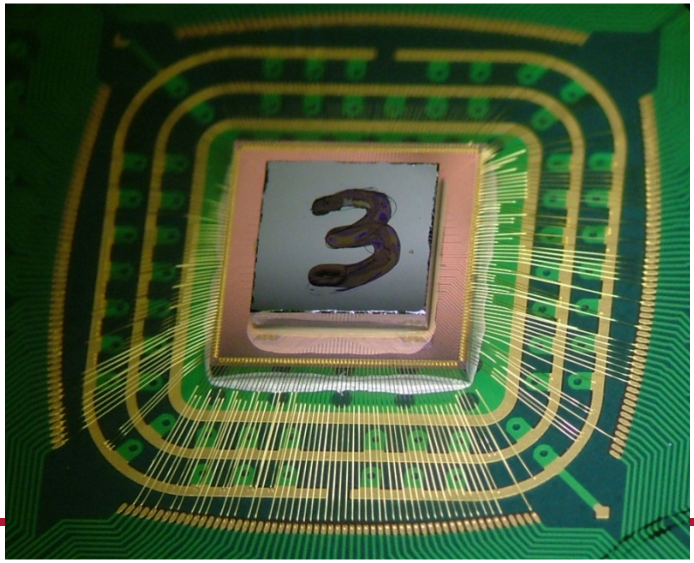
- V_{PWM} drives an RC filter to generate the inner reference voltage, $V_{REF,I}$, while the bridge output voltage for each phase, V_{BRIDGE}, drives another RC filter to generate the inner feedback voltage, $V_{FB,I}$
- In steady state, $V_{FB,I}$ will slew behind $V_{REF,I}$ and the resultant evaluation of the comparator causes V_{BRIDGE} to closely track V_{PWM}.

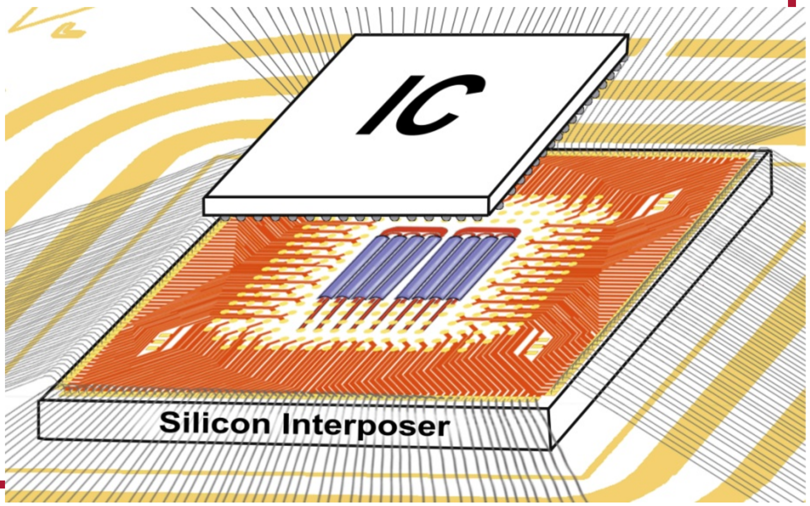
- In the event of a large load current transient, the error in the output voltage, V_{OUT}, will couple across C_{FB} onto $V_{FB,I}$ and the comparator will react immediately to reduce overshoot in V_{OUT}.

Interposer Design

- C4 connection to IC, bond wire connection to BGA package (2.5D)
- Quick/cheap method to demonstrate integrated power chip-stack
- Thru-Silicon-Vias (TSV) in future interposer design (will be compatible with C4 package)

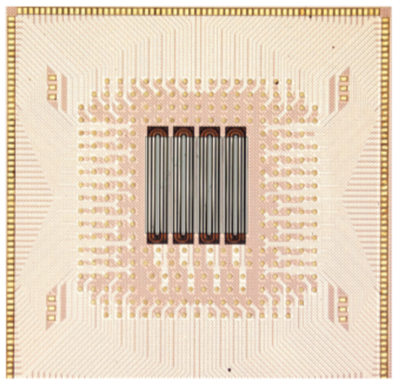


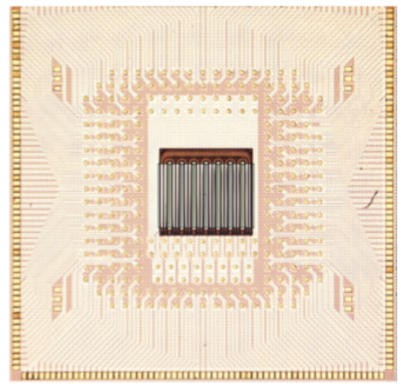




Inductor topologies considered

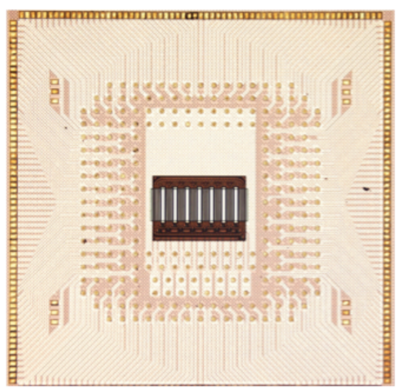
- Case 1. Four uncoupled two-turn inductors

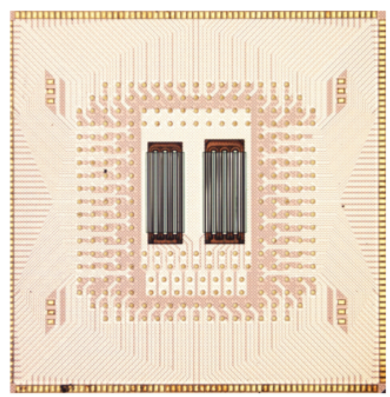




- Case 3. Eight two-turn coupled inductors

- Case 2. Eight single-turn coupled inductors

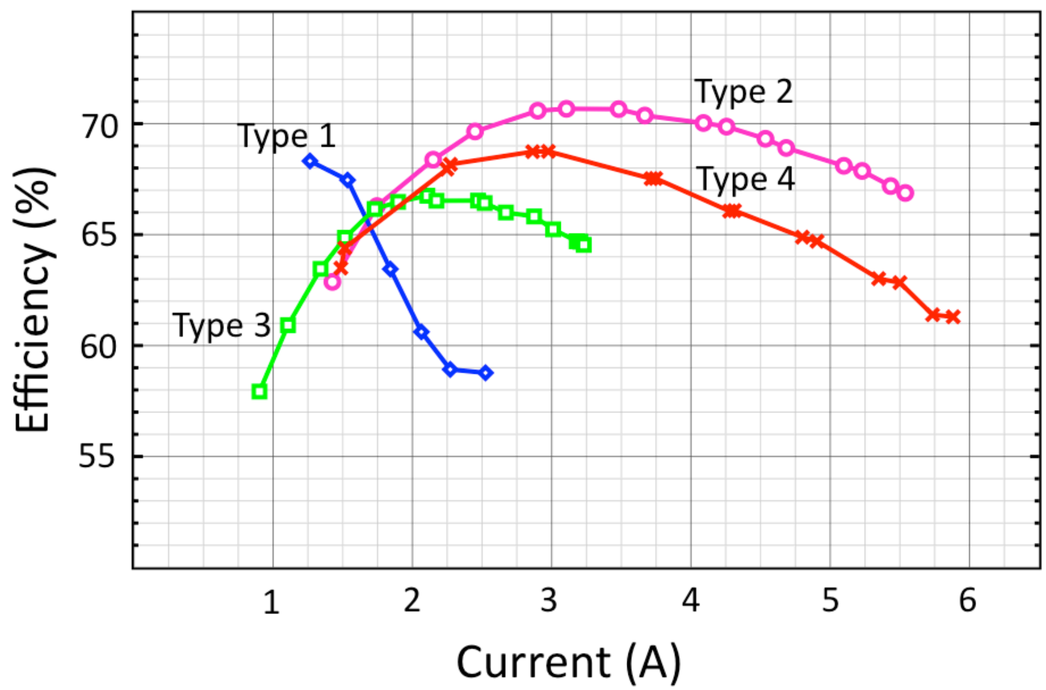




- Case 4. Two sets of four single-turn coupled inductors

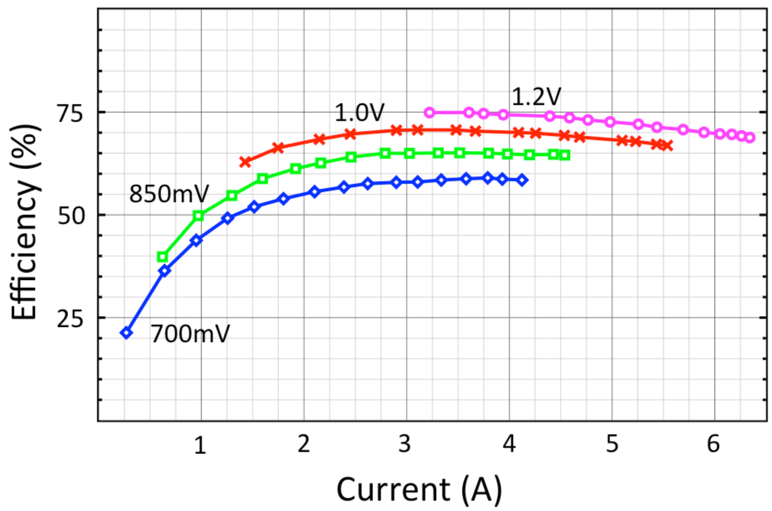
Converter efficiency

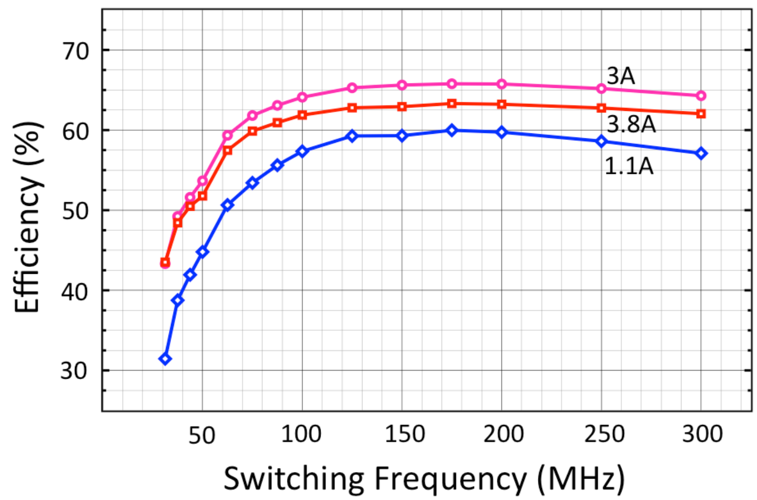
- Efficiency as a function of load current at 100 MHz switching frequency
- Type 2 design clearly the most efficient.
- Type 1 clearly falls off rapidly with current; problem of no coupling and saturating magnetization.



Chip Stack Results

- Efficiency given as function of load current, switching frequency, and output voltage.
- Initial results with peak efficiency (conversion ratio of 0.61, frequency of 75 MHz) of ~74% at FEOL current density of 10A/mm^2 and interposer current density of ~1A/mm^2

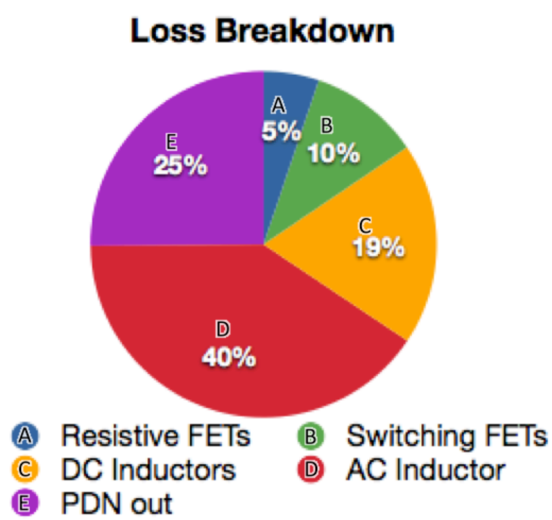


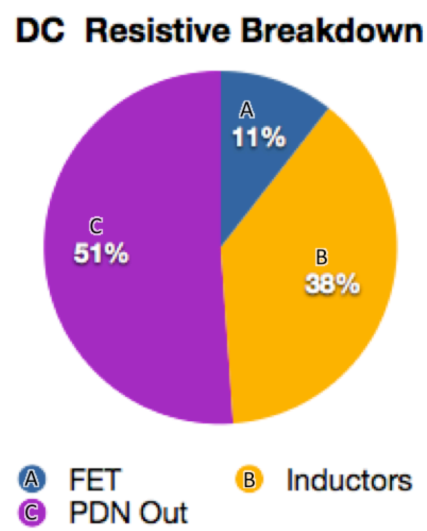


Losses in converter

- Inductors are primary source of loss. At peak efficiency, inductor DC and AC losses contribute approximately 19% and 40% of the total power loss, respectively, while switching and conduction of the bridge FETs contribute 25%.
- Addition of laminated magnetic core will reduce losses, suppressing eddy currents and domain wall motion

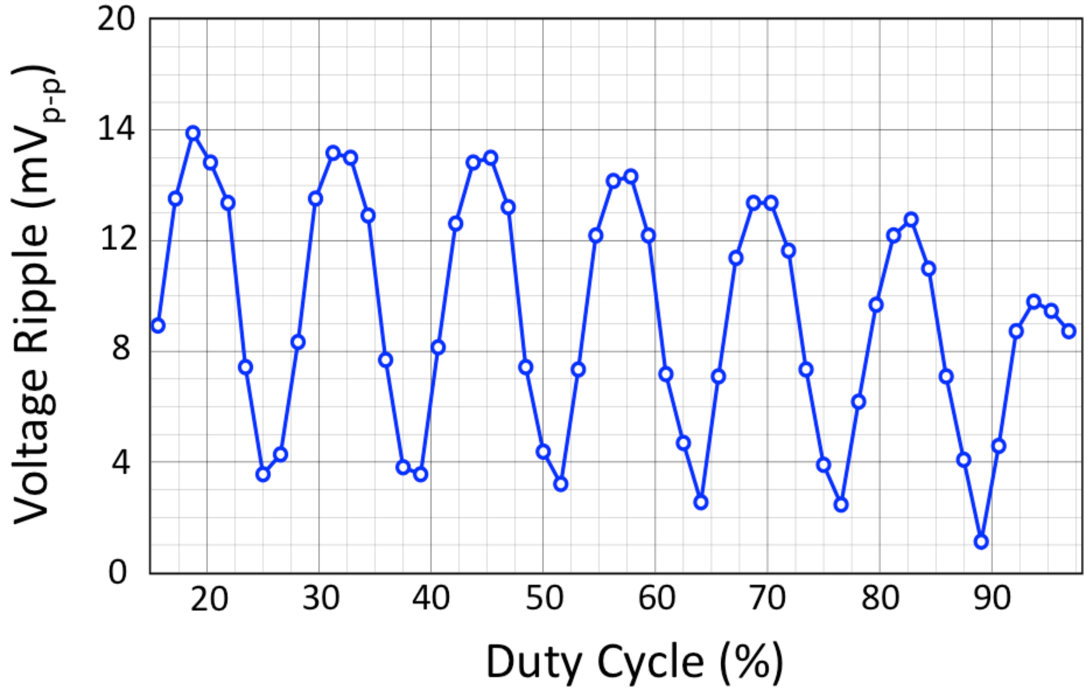
1 V output voltage, 3A output current





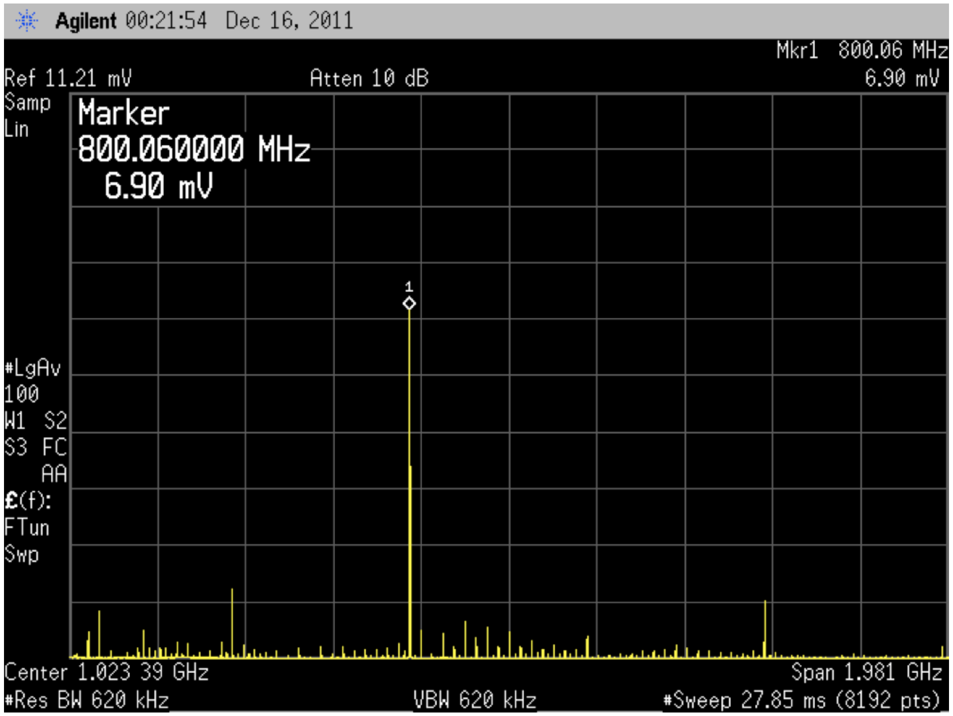
Voltage ripple

- Output voltage ripple as a function of duty cycle at 100 MHz switching frequency
- Peak voltage ripple is 14 mV peak-to-peak
- Reaches minimum at mod(D,1/8)=0 when inductor current ripple nearly identically cancels.
- This will improve with reduced inductor losses.



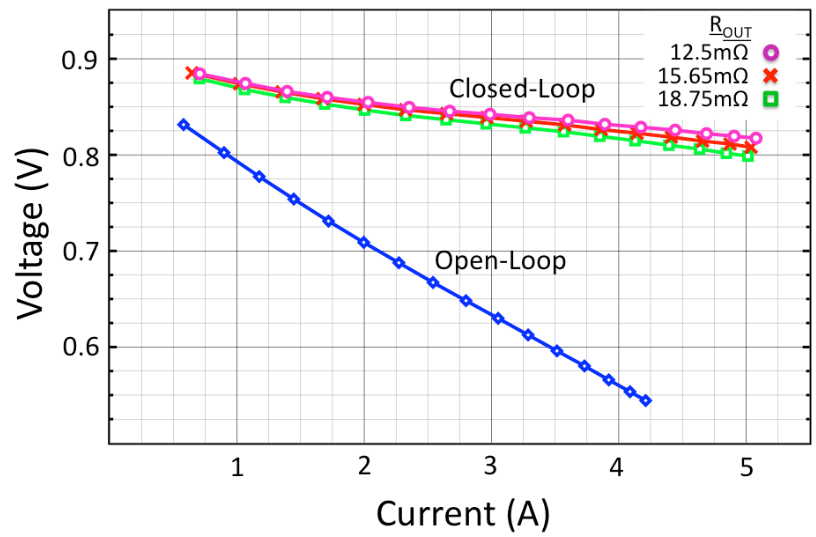
Supply noise spectrum

- Dominant tone in the output voltage is at 800 MHz at 100 MHz switching frequency.
- Limited spectral content in other harmonics indicated that current through inductors well balanced.



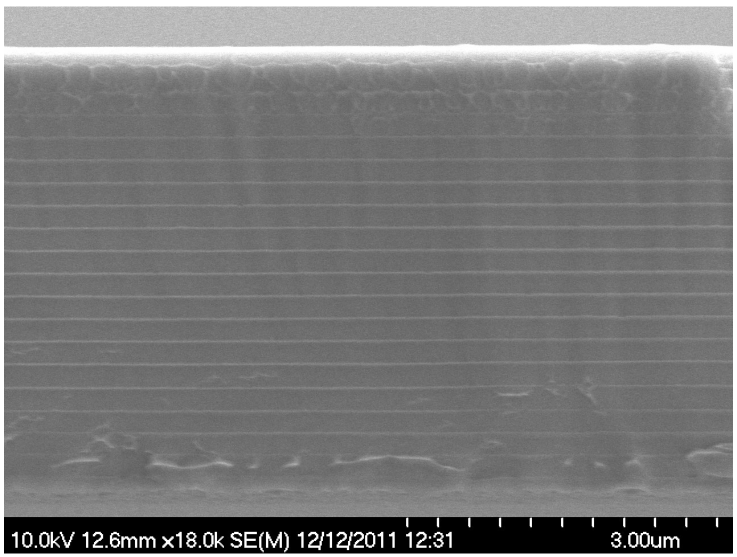
Voltage-mode feedback controller

- Large impedance of input PDN makes the load current response poor.
- However, we can confirm the load-line regulation capability of outer control loop for various gain settings for the error amplifier.

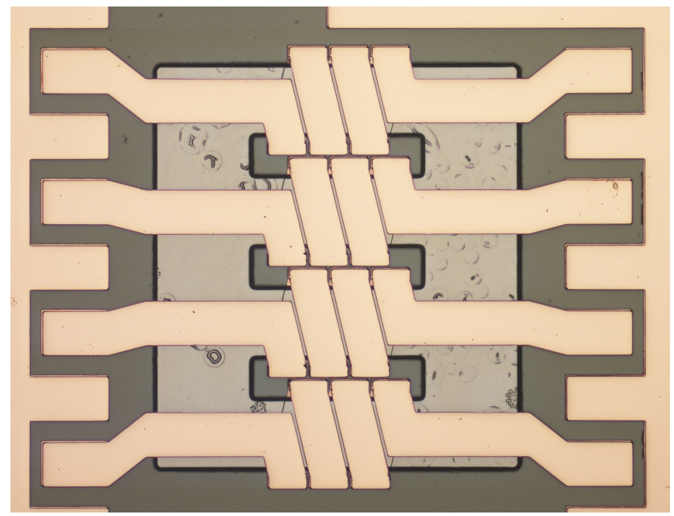


Toroidal inductor designs

- Laminated cores to reduce eddy current losses.
- Only one magnetic layer deposition necessary, simplifying fabrication
- Easy to couple inductors

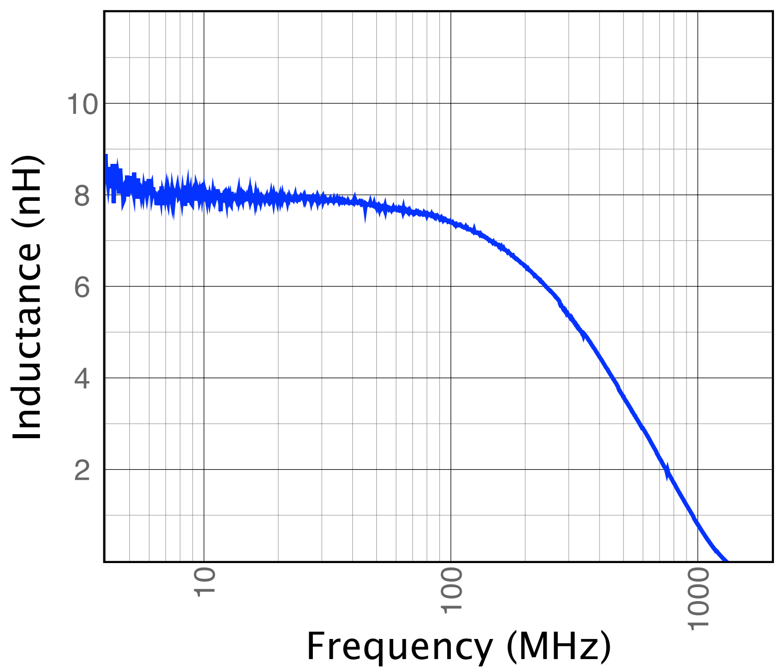


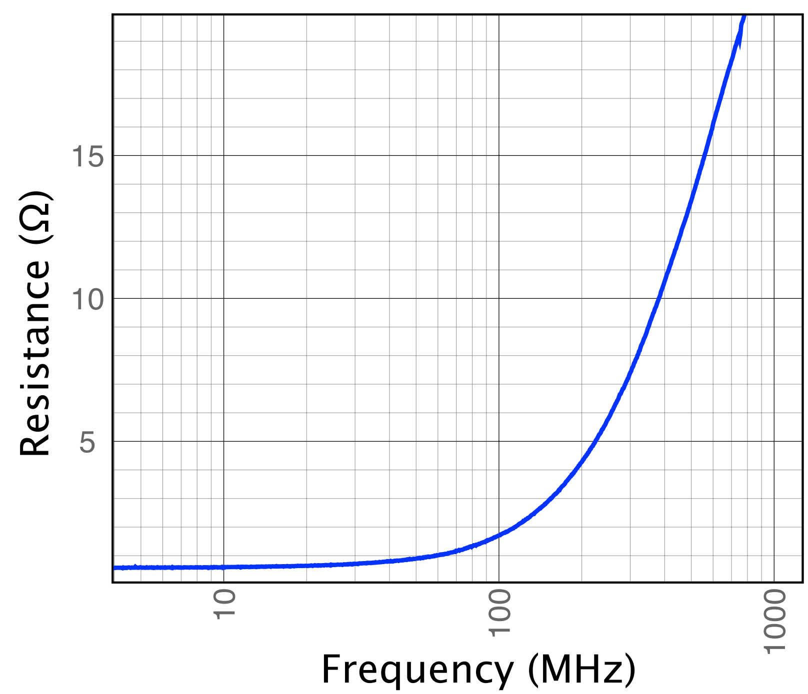
Cross-sectional SEM image of laminated core: 2nm Ta/180nm $Co_{91.5}Zr_{4.0}Ta_{4.5}$/2nm SiO_2 × 20



Toroidal inductor designs

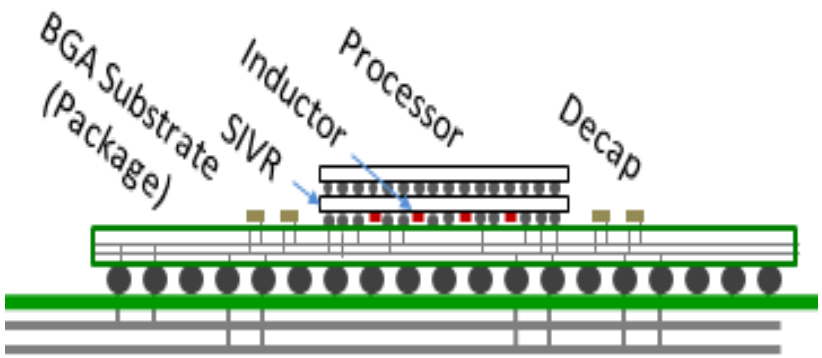
- Second lot of inductor prototypes are being tested
  - Greater than 10× higher "corner frequency" over yoke-based inductors
  - 65X increase in inductance; Inductance density of ~85nH/mm^2, expect this to double
  - DCR ~ 0.4 Ω caused by VIA contact resistance, expect this to fall by >4×
  - Q~4 @100MHz
  - Third lot in progress…





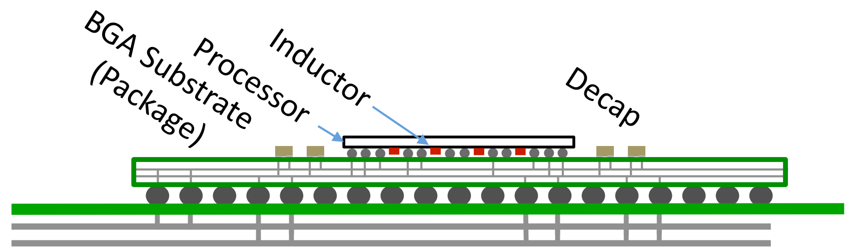
3D Chip Stacking

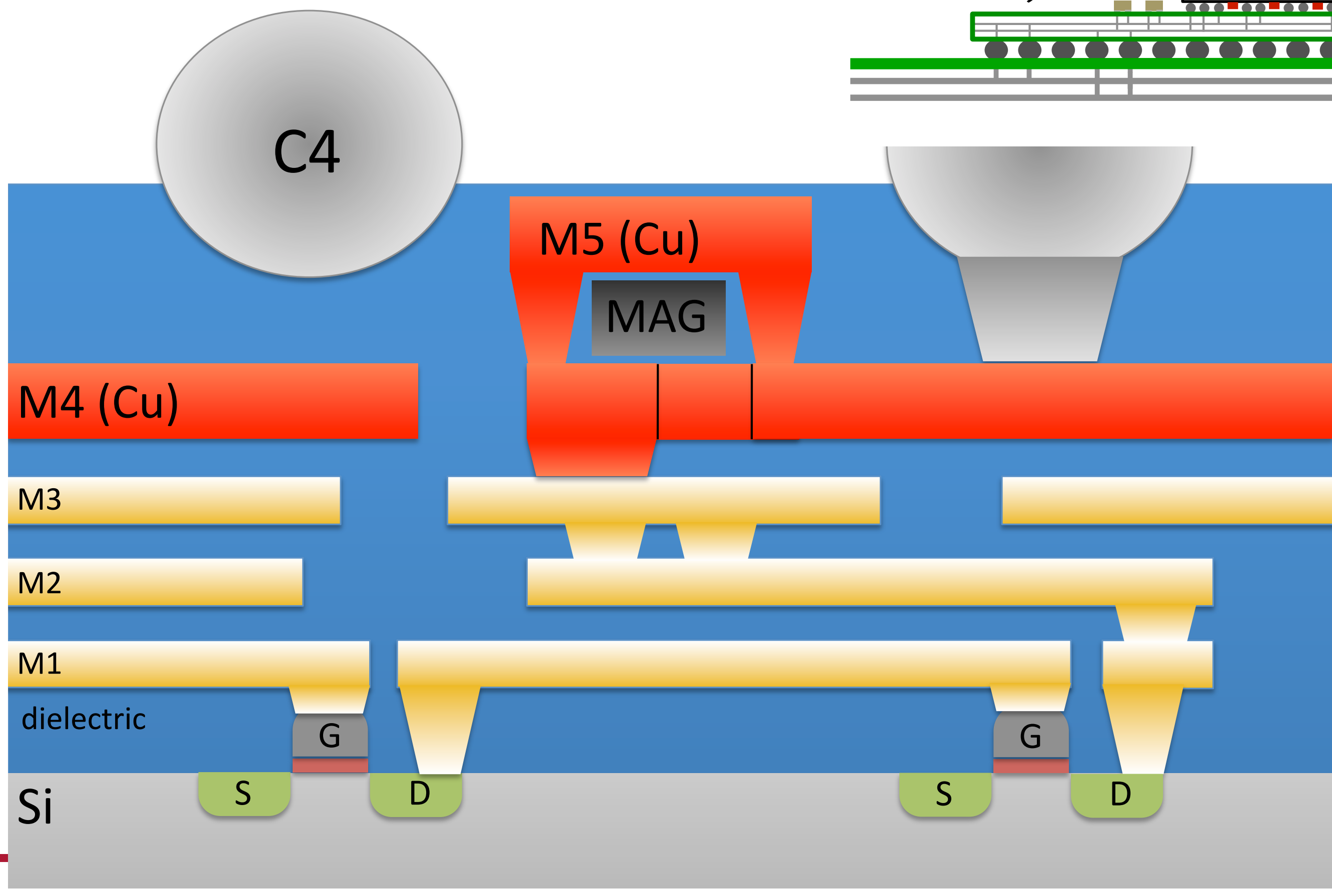
- Increased power density from custom fabricated power inductors
  - Inductors can be fabricated on a low-cost interposer and integrated with the IC via chip-stacking
  - Decap and power switches can be included on interposer design
  - Allows “one-way” current flow improving efficiency
  - Better transient performance due to lower impedance of input supply.
  - Step on the way to monolithic integration?



Monolithic integration

- **Monolithic Integrated Voltage Regulator** may ultimately be the best solution.





Conclusions

- Paradigm shift occurring in how power needs to be distributed to high performance processors which will require new approaches to magnetics, converter design, and packaging.
- Have demonstrated significant progress toward 3D power distribution using a silicon interposer, including the first prototype. (ISSCC, 2012)
- Future work is focused on a full-chip stack and expanded integration in the interposer.

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- **DOE**
- **SRC through Focus Center Research Program**
- **DARPA through PERFECT and DAHI programs**