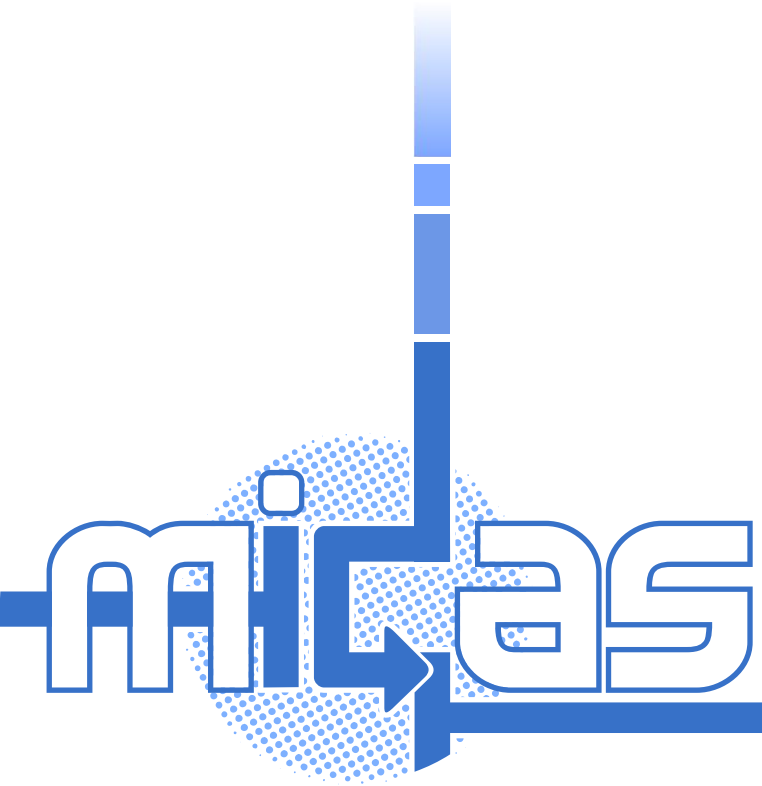
Fully Integrated SC DC-DC: Bulk CMOS Oriented Design

Hans Meyvaert
Prof. Michiel Steyaert

17 Nov 2012



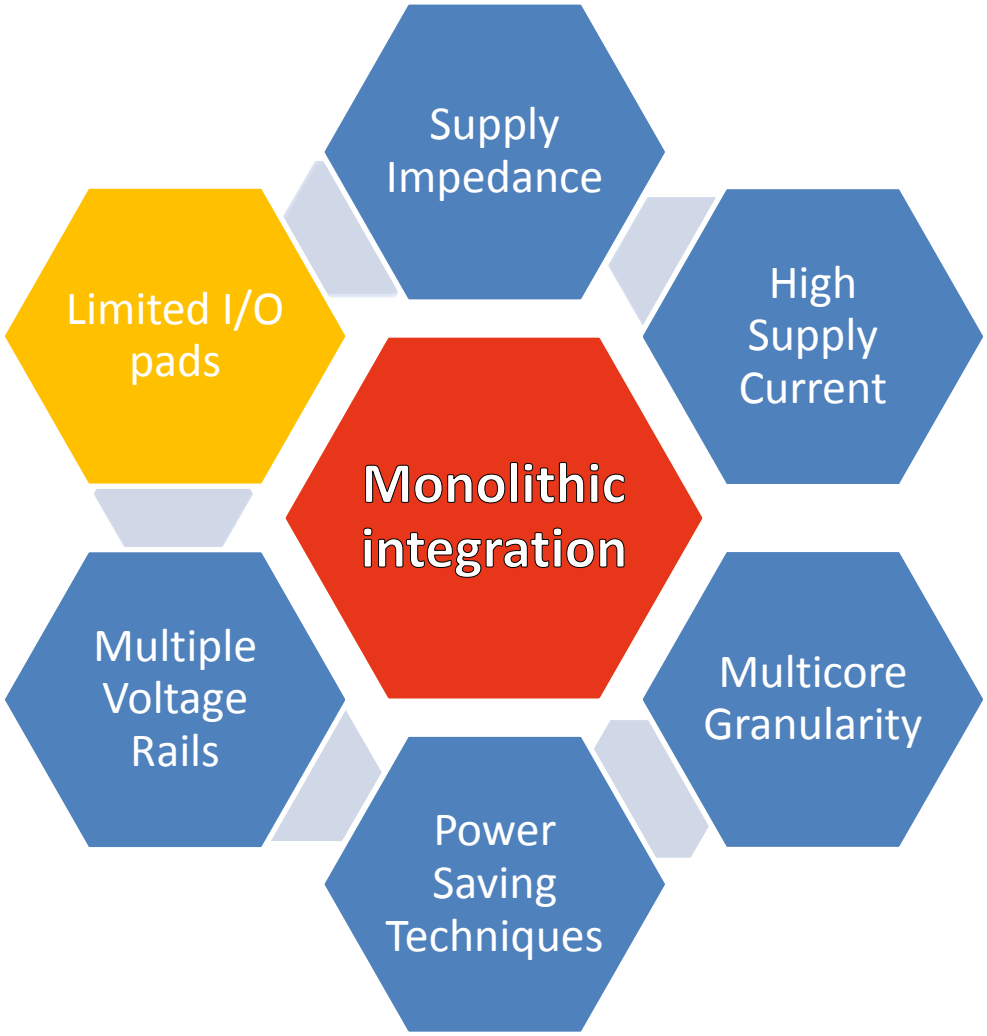
KATHOLIEKE UNIVERSITEIT
LEUVEN

Outline

- Towards monolithic integration
- CMOS as technology vehicle
- Techniques for CMOS DC-DC
- Conclusions

TOWARDS MONOLITHIC INTEGRATION

Driving aspects



CMOS AS TECHNOLOGY VEHICLE

Why CMOS?

- When there are other superior technologies such as GaN and GaAs
  - Superior parameters
  - But more expensive

- It depends on the specific requirements
- There is no single technology that can replace all others

Why CMOS?

- CMOS offers compact coexistence of power supply and load
  - Compatibility
  - Size

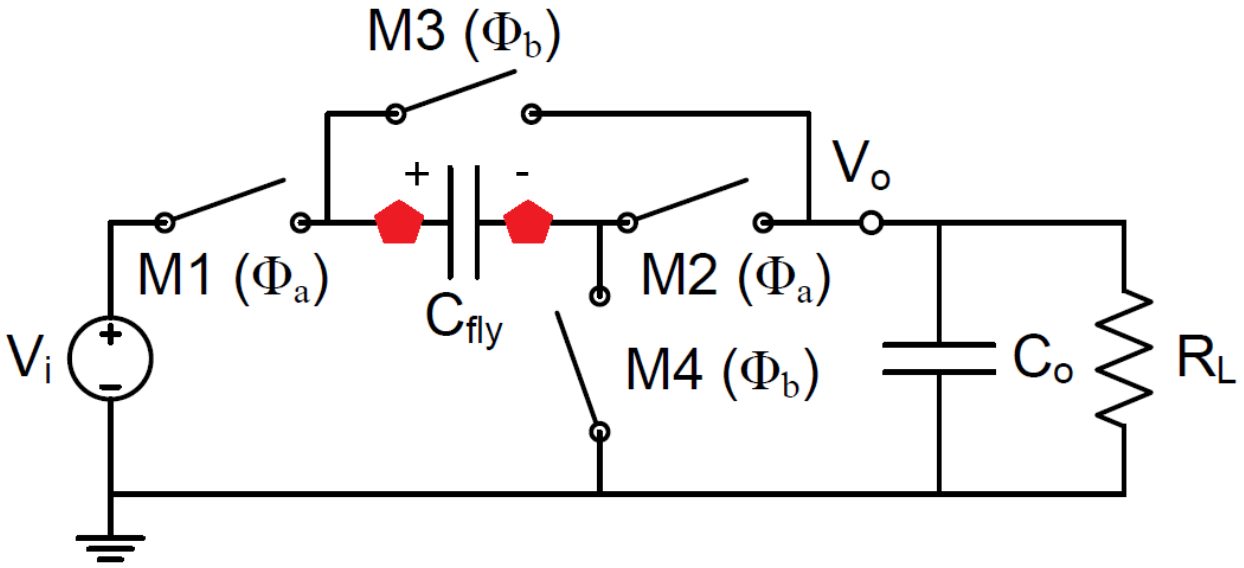
  } → Required for true granularisation
  - Cost
  - It's already available
- CMOS also offers parasitics …

In this case it is not a matter of being the best in class, but to be (more than) sufficient by coping for parasitics and having the benefit of low cost.

TECHNIQUES FOR CMOS DC-DC

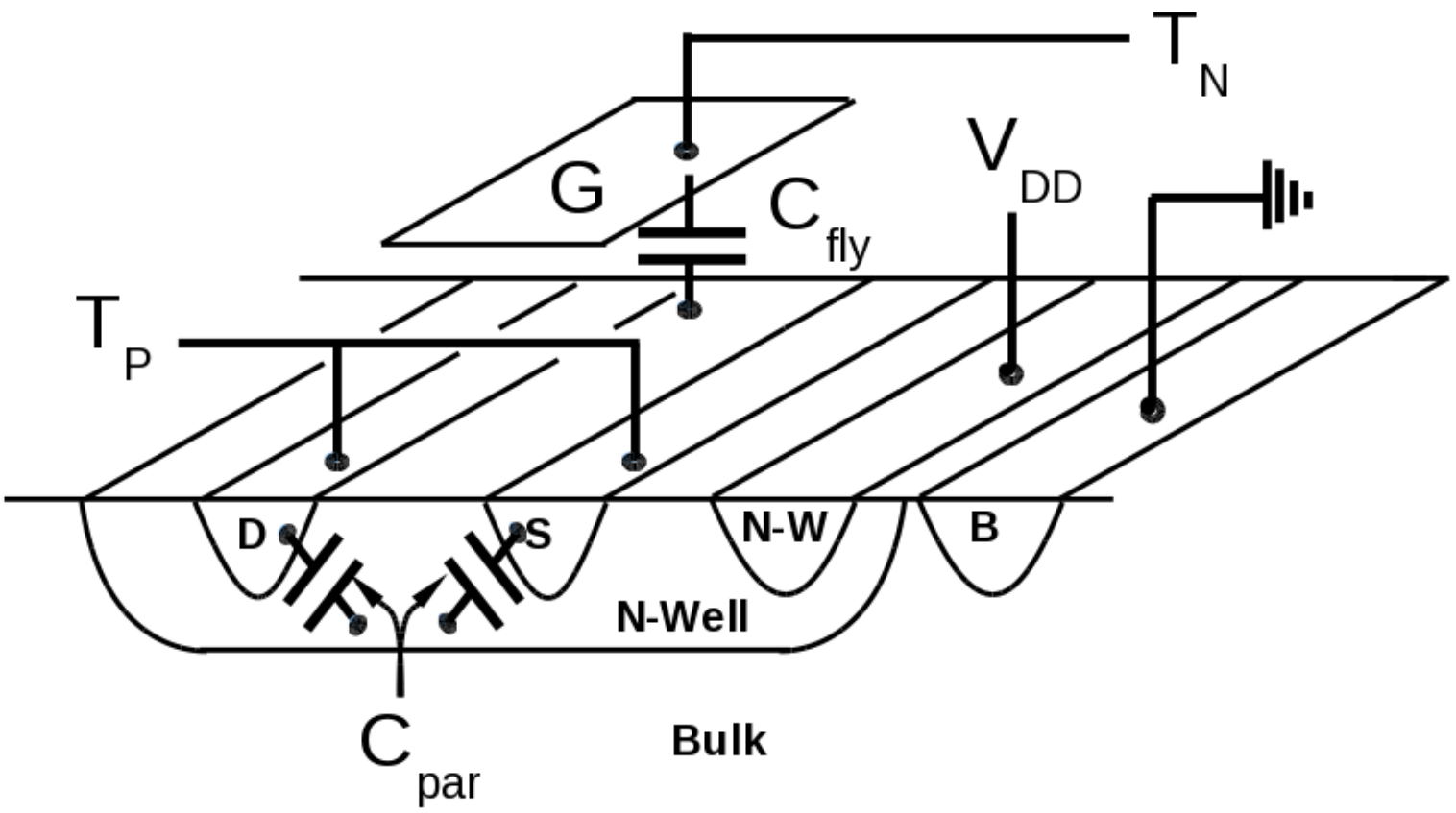
Bottom Plate Parasitic

- Concerns parasitic coupling of flying capacitor
  - 2 possible locations in a 2/1 step-down



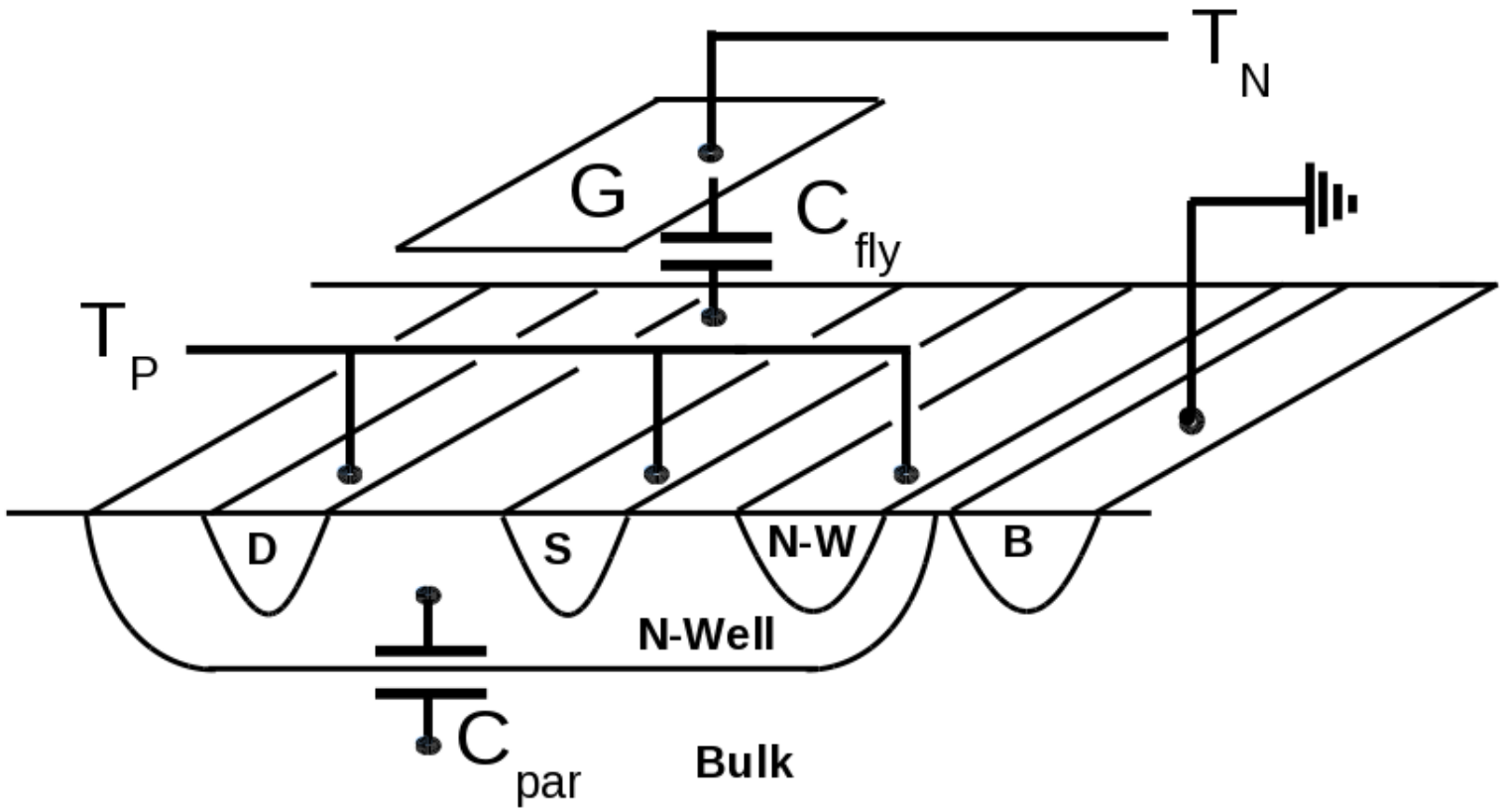
Parasitic Capacitor

- Typical bottom plate parasitic in CMOS



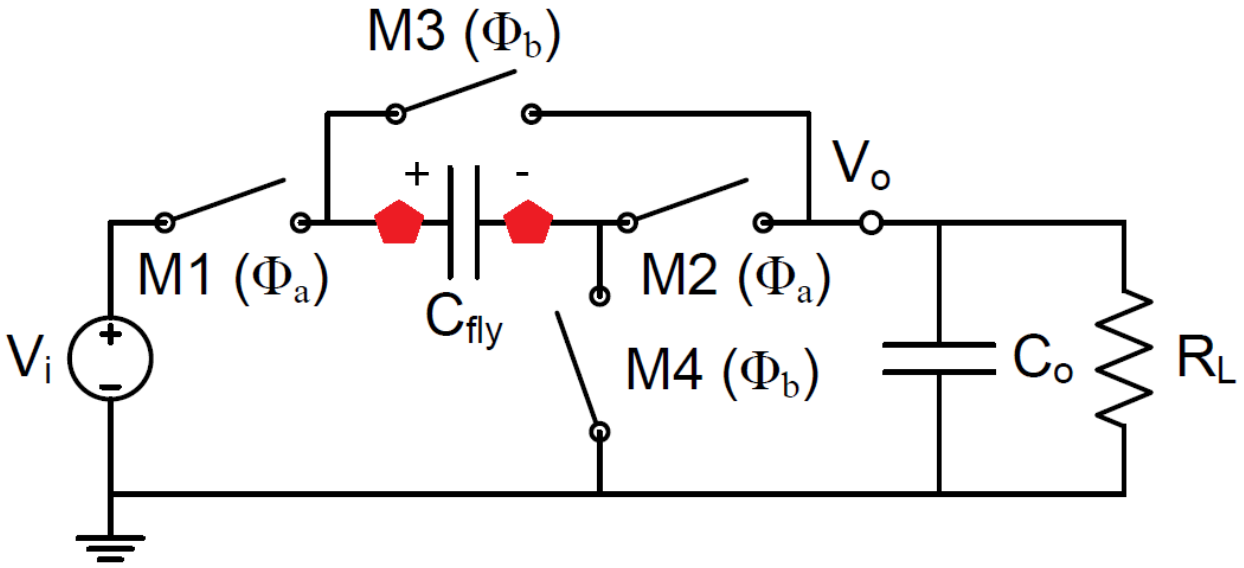
Flying Well

- Reduces C_{par} from >5% to 1.3% in this case



Intrinsic Charge Recycling

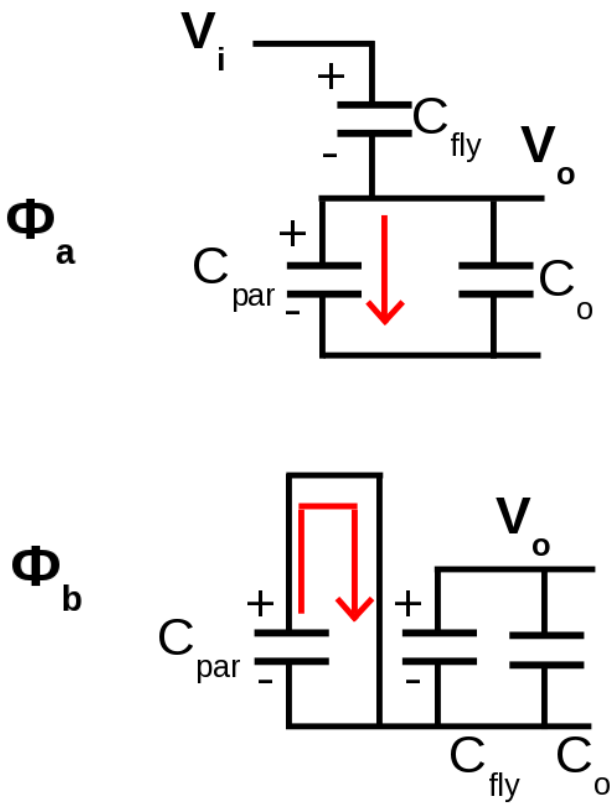
- Concerns parasitic coupling of flying capacitor
  - 2 possible locations in a 2/1 step-down



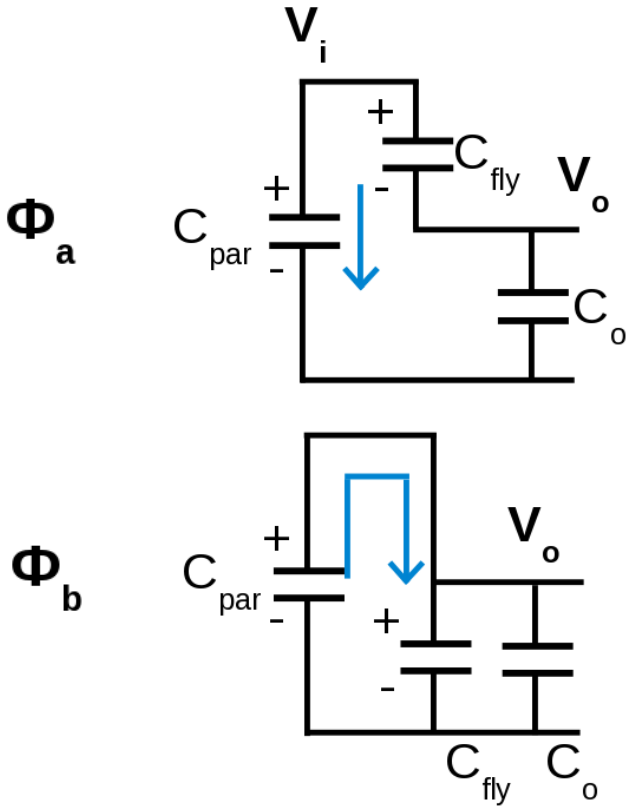
Intrinsic Charge Recycling

*An **output** perspective*

Without Recycling



With Recycling

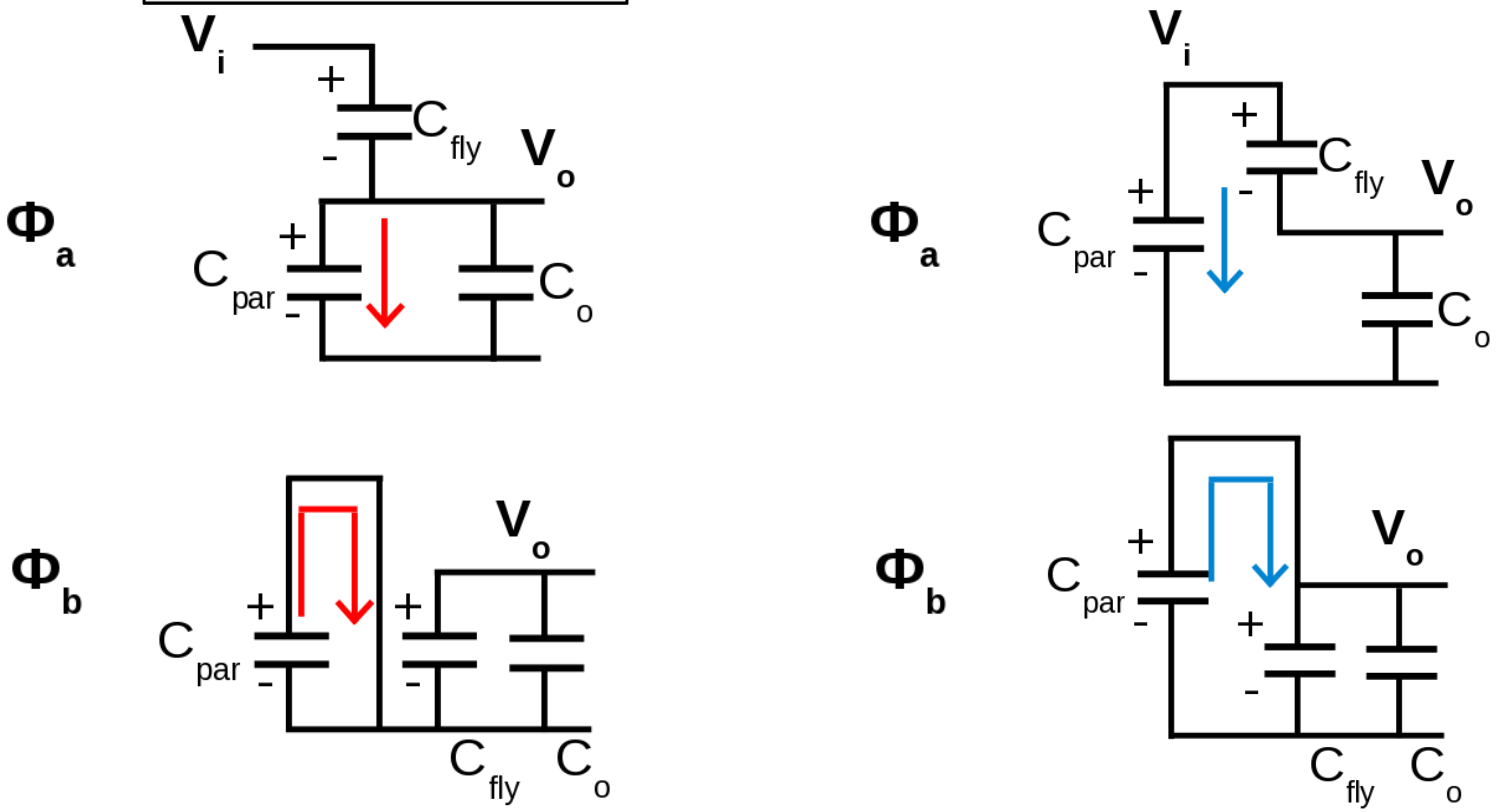


Intrinsic Charge Recycling

$$E_{O,C_{par},REG} = C_{par}(\gamma V_{o,id})^2$$

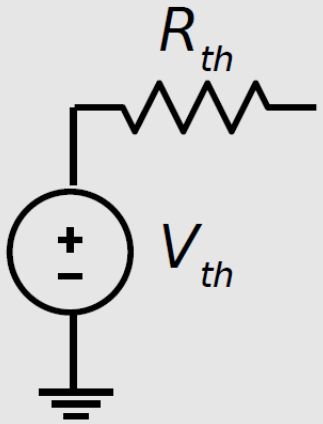
***tput** perspective*

With Recycling



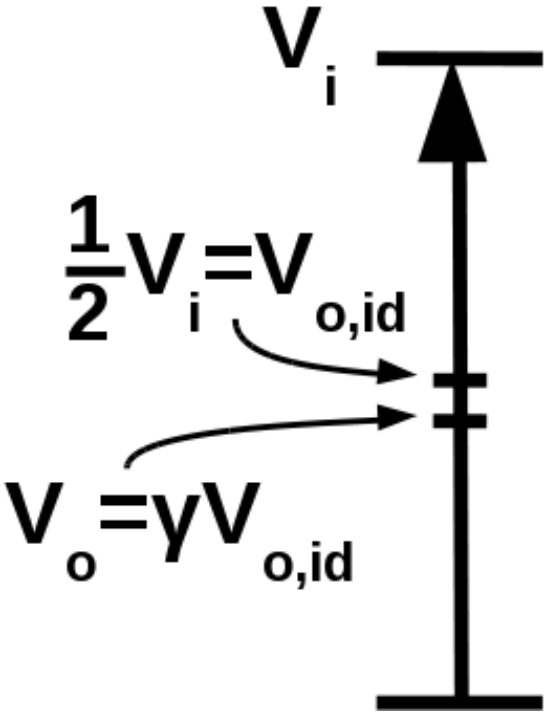
Intermezzo: $V_{o,id}$, V_o and γ

Thevenin Model



$$V_{th} = \frac{1}{2} V_i = V_{o,id}$$

$$R_{th} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad [5]$$



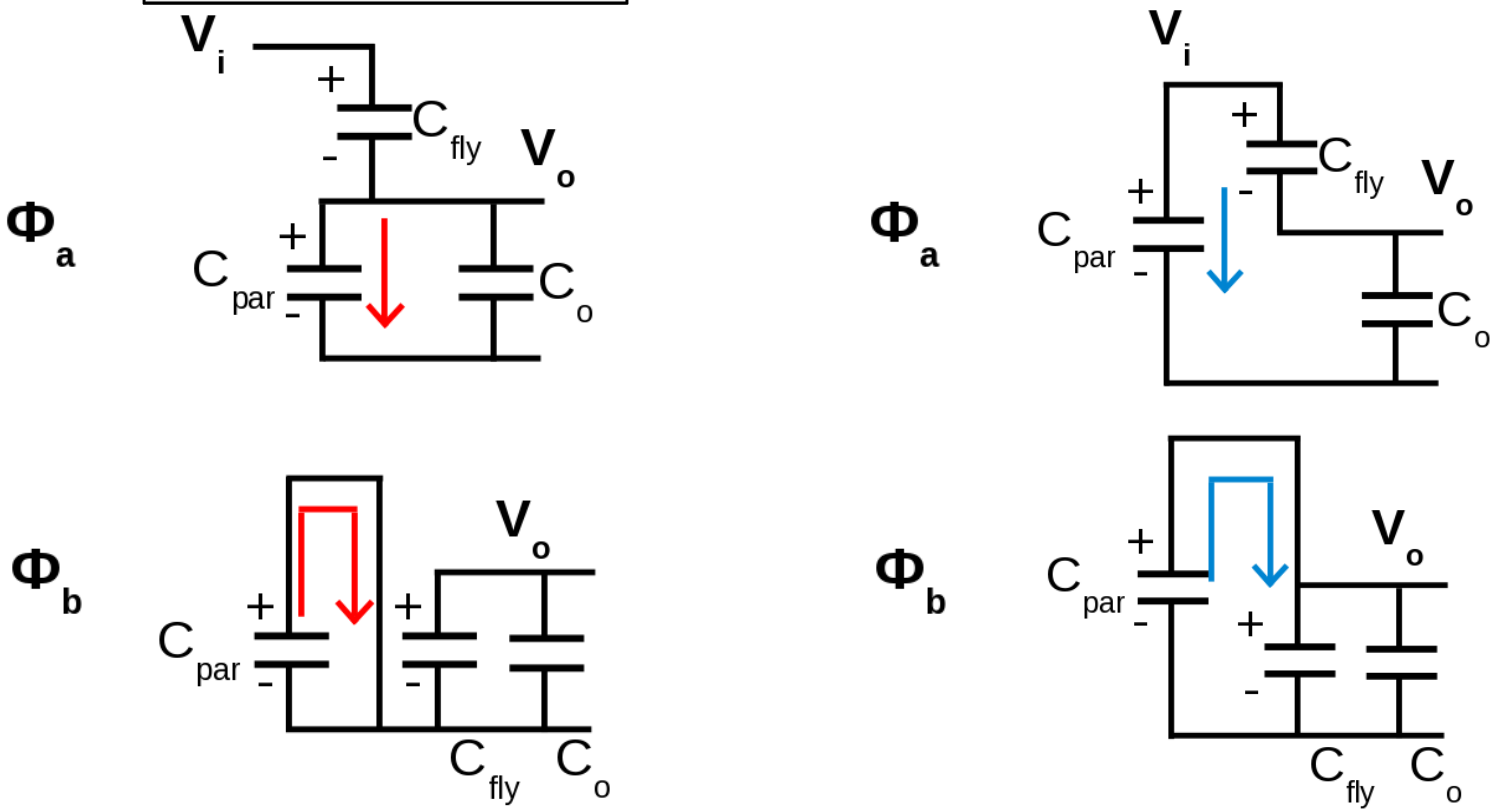
Voltage drop over R_{th} due to voltage divider formed by R_{th} and a R_L . This ratio equals γ.

Intrinsic Charge Recycling

$$E_{O,C_{par},REG} = C_{par}(\gamma V_{o,id})^2$$

***tput** persp*

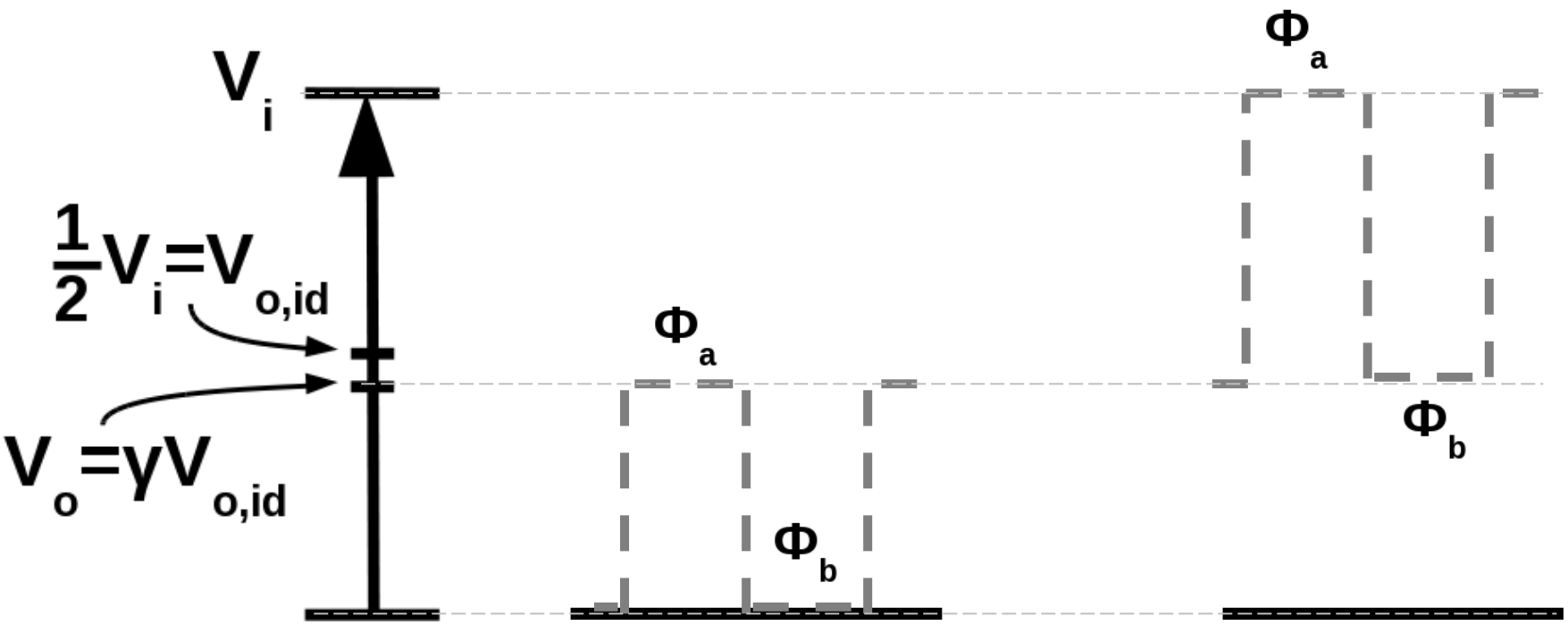
$$E_{O,Cpar,ICR} = C_{par}V_{o,id}{}^2(\gamma^2 - 2\gamma)$$



Intrinsic Charge Recycling

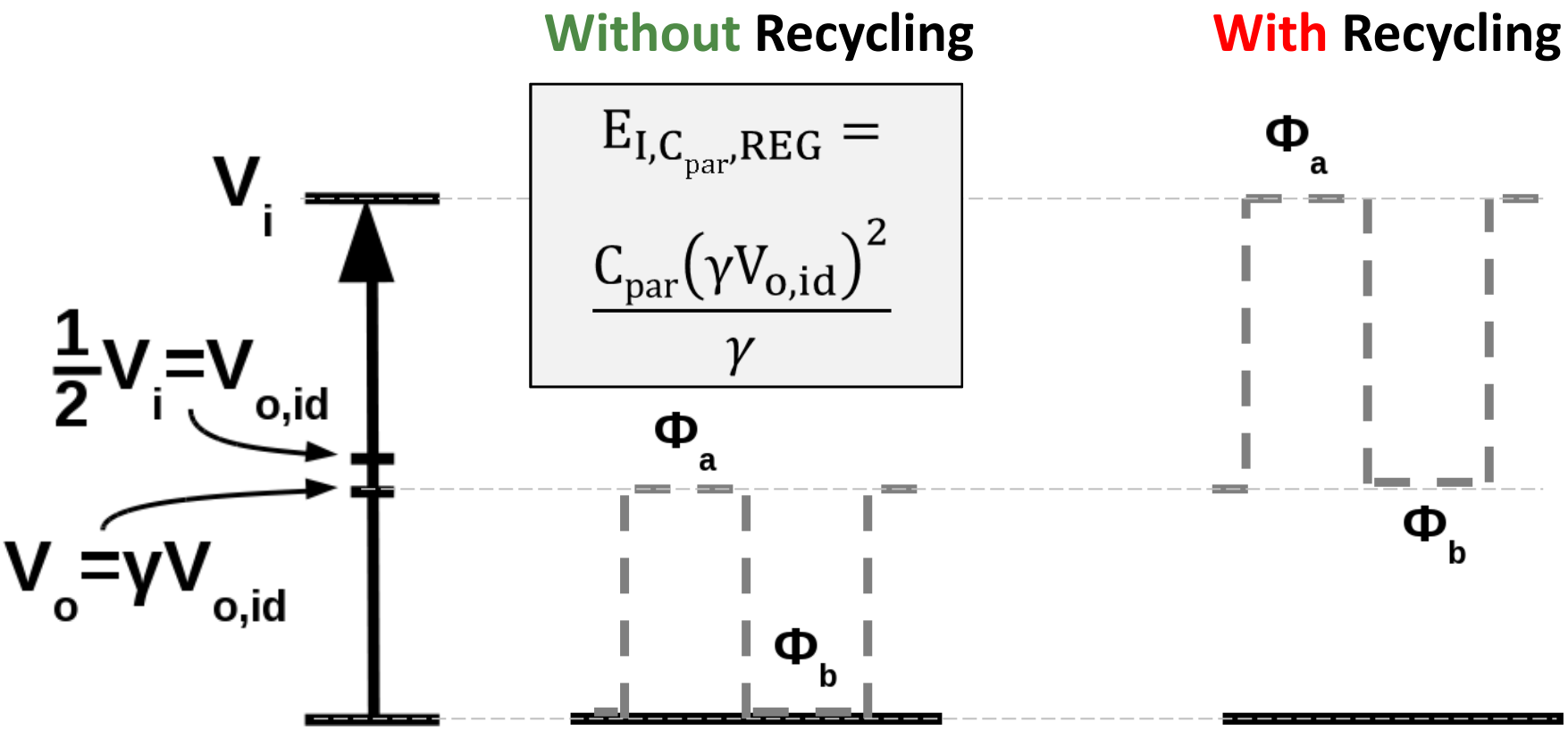
*An **input** perspective*

Without Recycling **With Recycling**



Intrinsic Charge Recycling

*An **input** perspective*

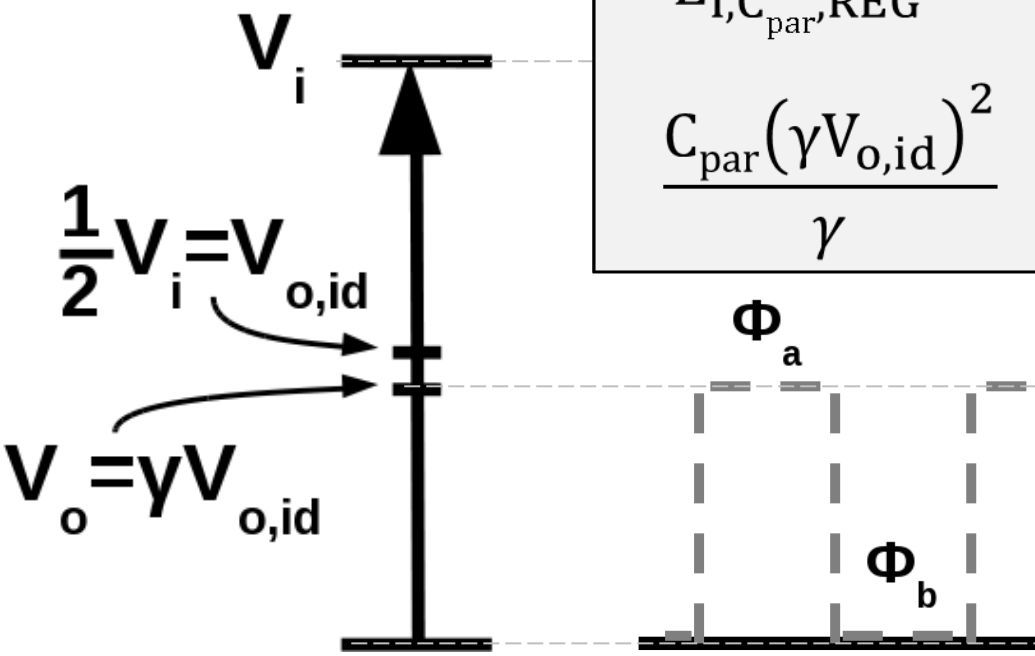


Intrinsic Charge Recycling

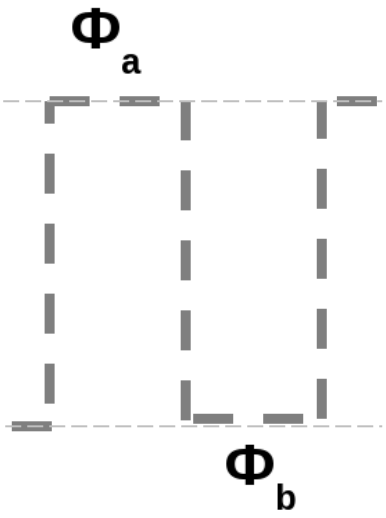
*An **input** perspective*

Without Recycling

$$E_{I,C_{par},REG} = \frac{C_{par}(\gamma V_{o,id})^2}{\gamma}$$



With Recycling



$$E_{I,C_{par},ICR} = C_{par} V_{o,id}{}^2 (4 - 2\gamma)$$

Intrinsic Charge Recycling

*The **combined** perspective*

➡ **Trade-off: $\Delta E_{out} - \Delta E_{in} \geq 0$**

$$\left(-E_{O,Cpar,ICR} + E_{O,Cpar,REG}\right) - \left(E_{I,Cpar,ICR} - E_{I,Cpar,REG}\right)$$

$$= \cdots$$

$$= C_{par} {V_{o,id}}^2 (5\gamma - 4)$$

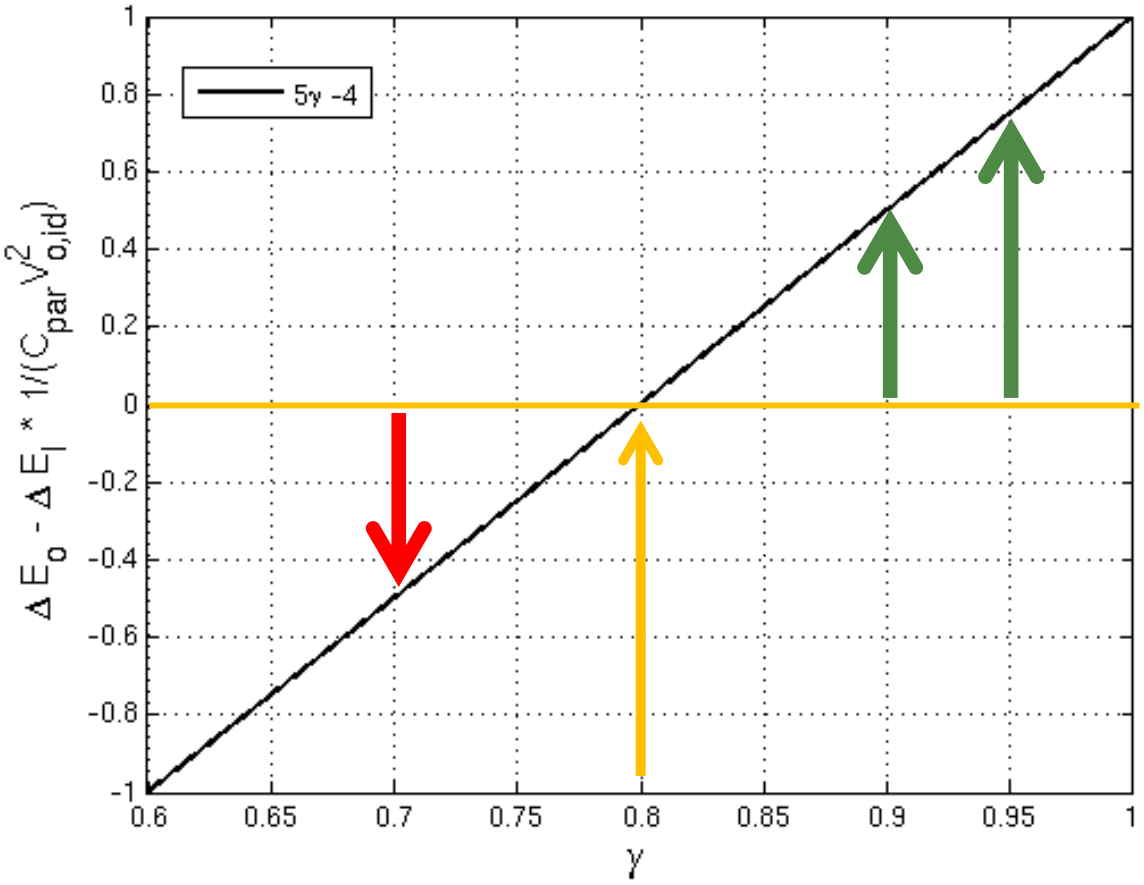
The trade-off is only function of γ!

⟶ **Any capacitor type**

⟶ **Any V_i**

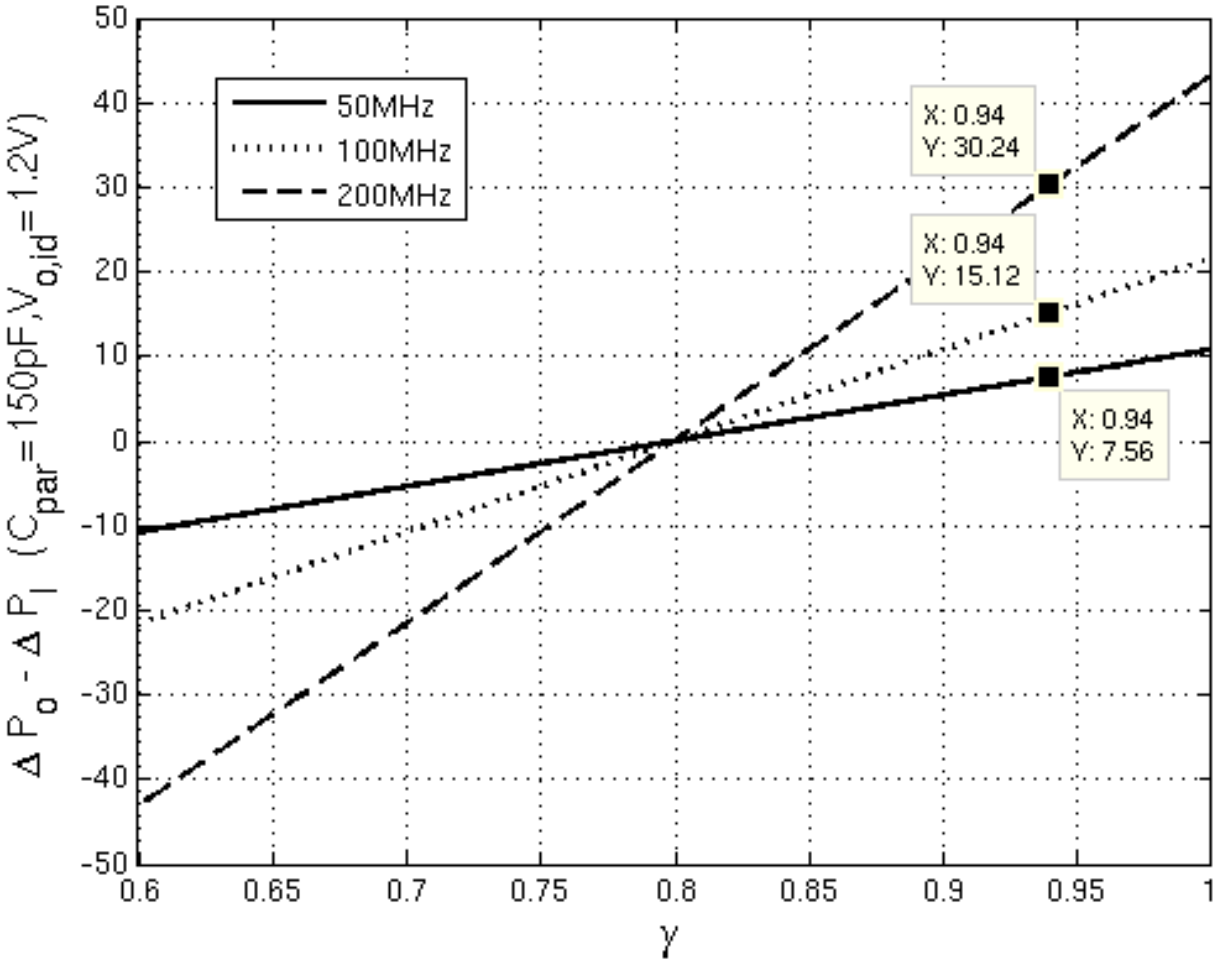
Intrinsic Charge Recycling

*The **combined** perspective*



Intrinsic Charge Recycling

*The **combined** perspective*



Intrinsic Charge Recycling

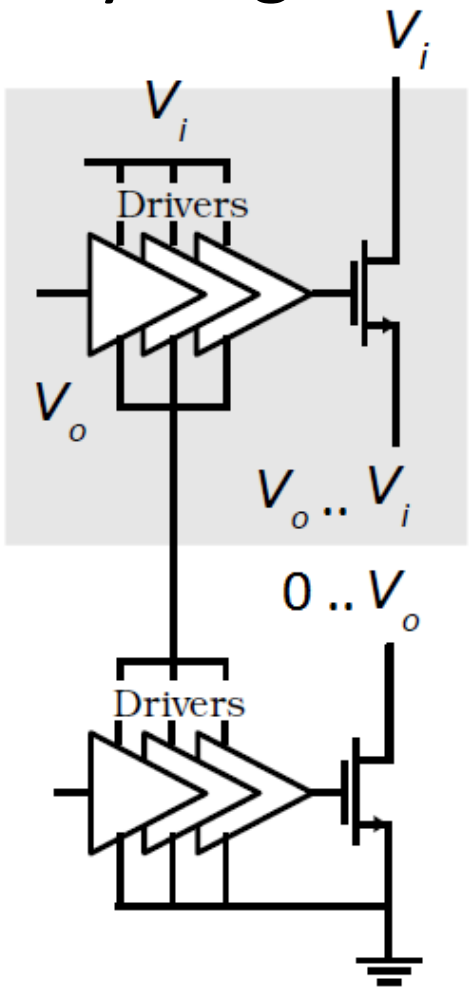
- Summary

✓ f_{sw} constant → $P_o \uparrow$

✓ P_o constant → $f_{sw} \downarrow$

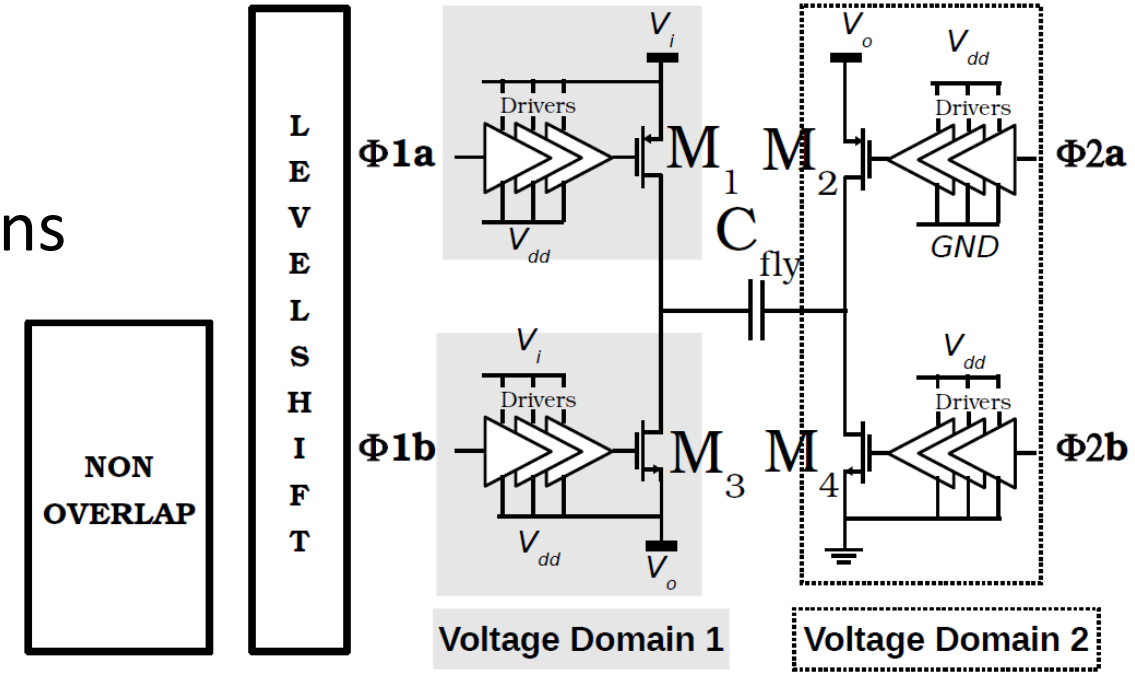
Charge Recycling

- Other forms of charge recycling
  - Voltage domain recycling by serial voltage domains



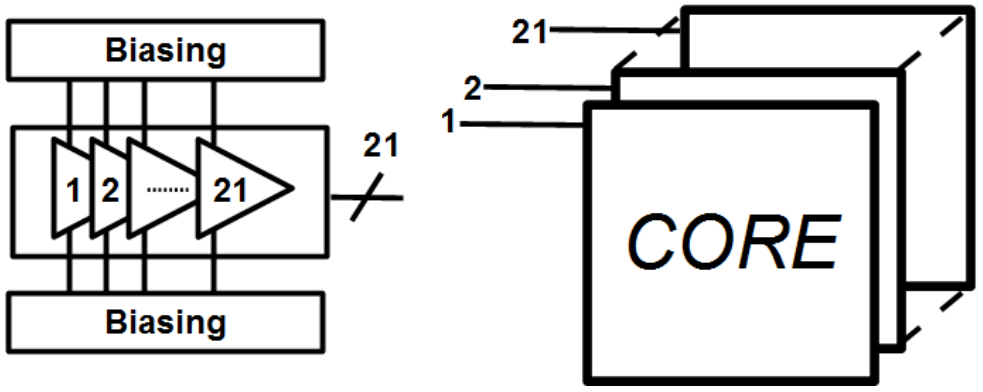
System Architecture

- Converter core
  - Non overlap generation
  - Level shifting
  - Buffering
  - 2 voltage domains
    - ground..V_o
    - V_o..V_i
  - 1 C_{fly}: P-moscap
  - 4 switches



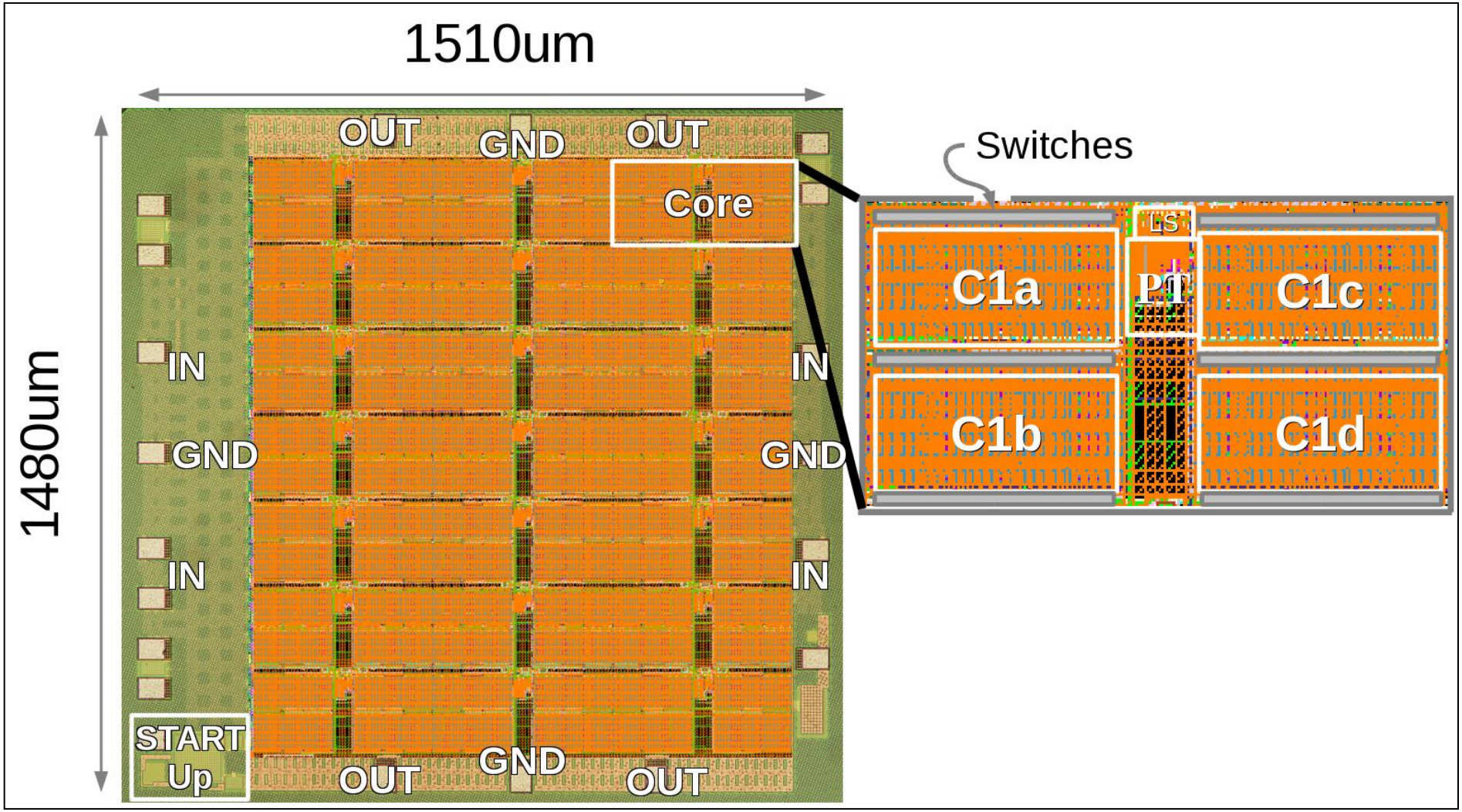
System Architecture

- On-chip 21 tap VCO
- 21 converter cores spread out of phase
- $C_{fly,total}$: 12 nF
- $W_{switch,total}$: 11.5 cm



- Integrated linear regulator for start-up

Chip microphotograph + layout



Measurements

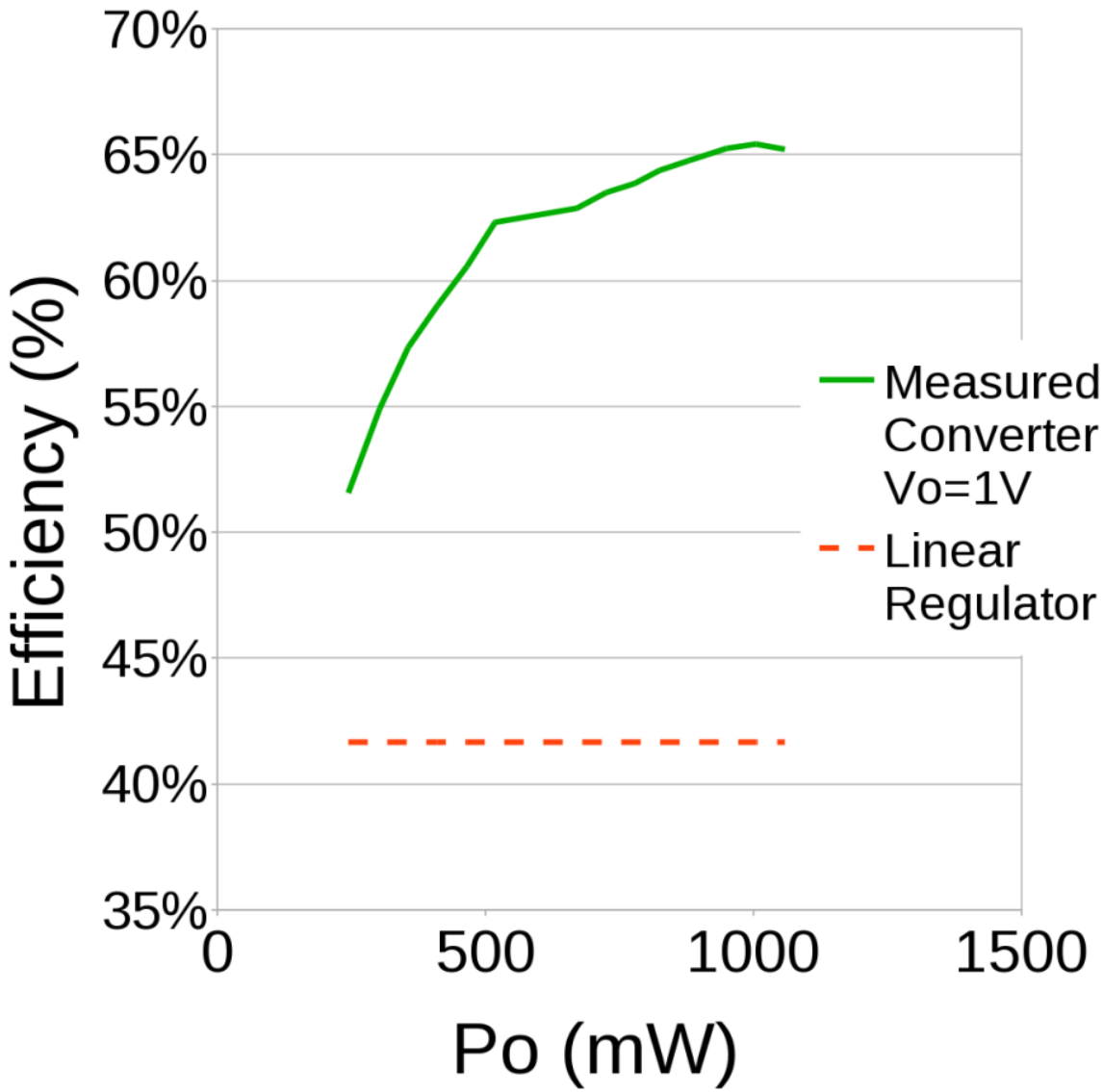
- Closed loop
- V_{in}: 2.4V
- V_{out}: 1V
- P_o range: 250-1050mW

- Peak efficiency:

  65% at 1W

- Battery lifetime extension (EEF [3]):

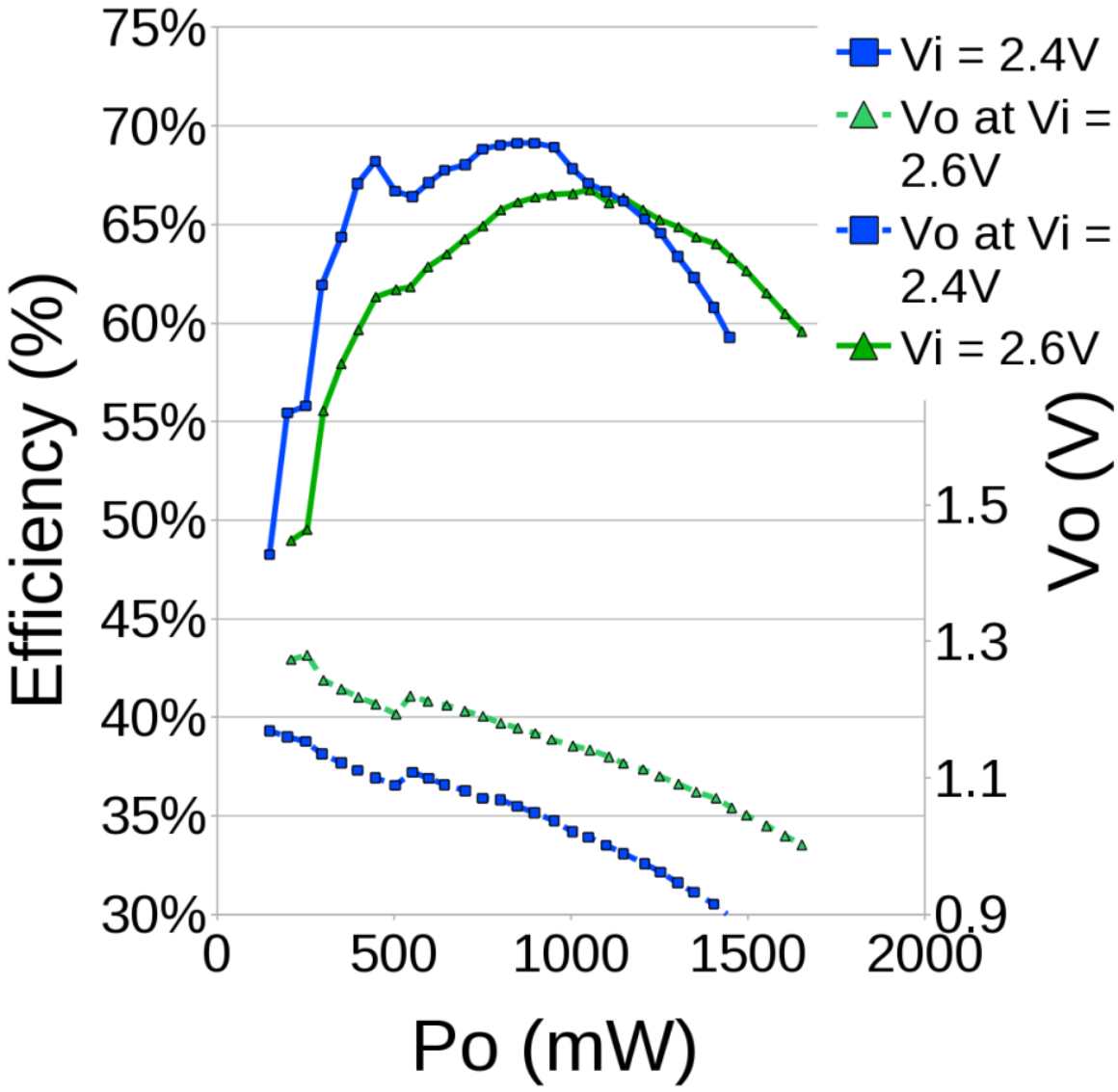
  +36%



Measurements

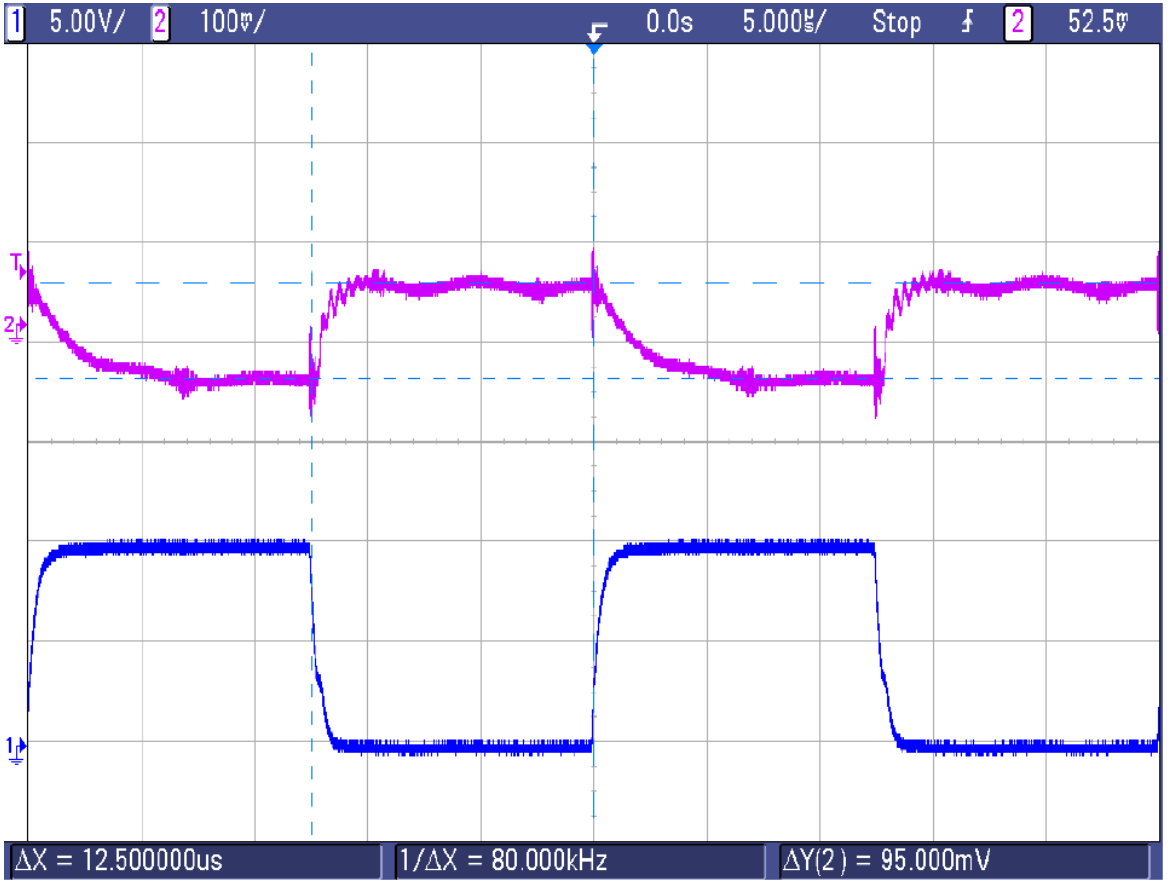
- Open loop

- Maximum P_{out}: 1.65W
- Maximum η: 69%



Measurements

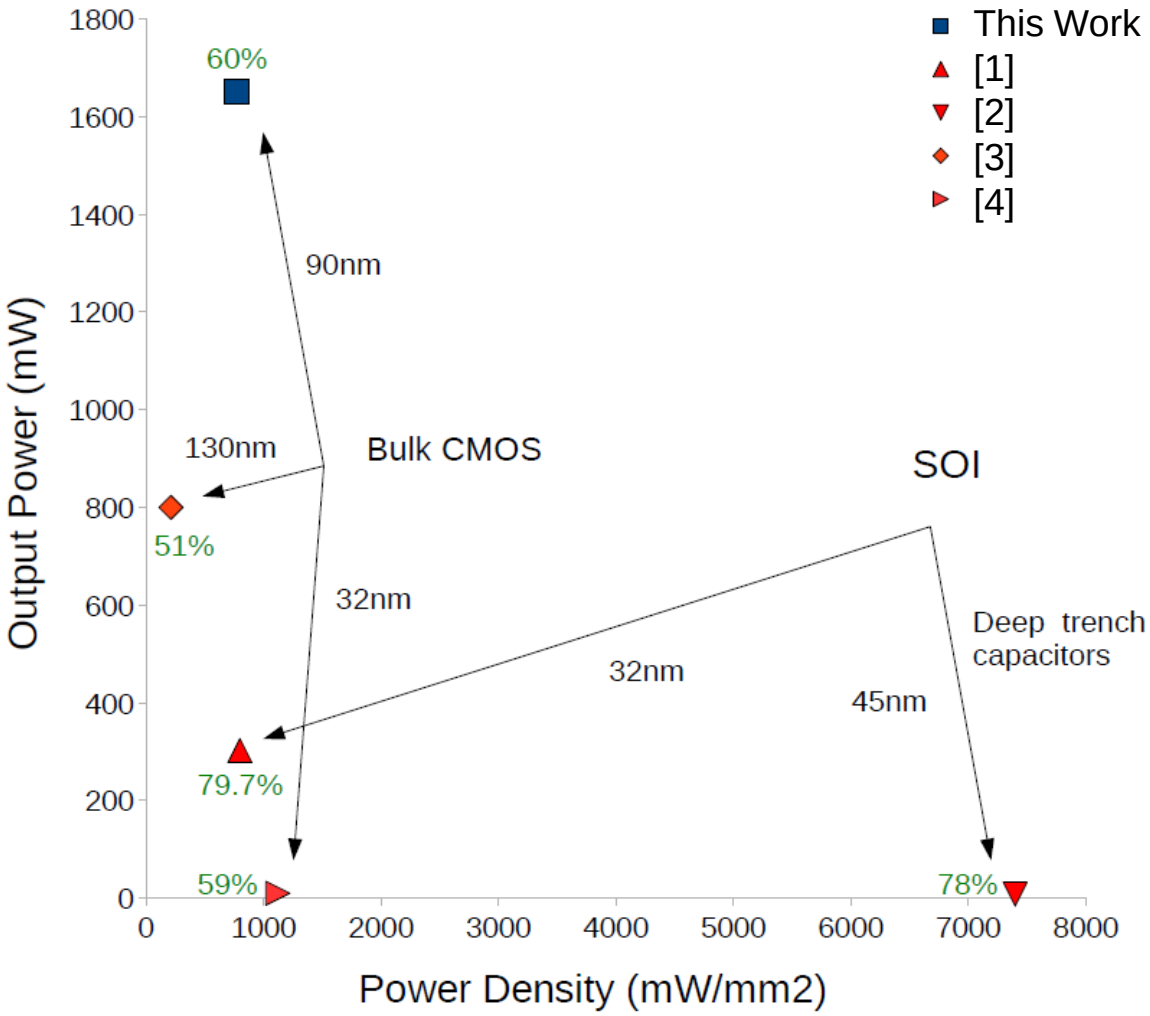
- Open loop load regulation
  - -0.175 Ω



Comparison with state of the art

	[1]	[2]	[3]	[4]	This work
Tech node	32nm	45nm	130nm	32nm	**90nm**
Type	capacitive	capacitive	inductive	capacitive	capacitive
Control	closed external	external f_{sw}	SCOOT	discrete step loop	closed external
Power density	0.86W/mm²	7.4W/mm²	0.21W/mm²	1.12W/mm²	0.77W/mm²
$P_{out,max}$	0.33W	8.88mW	0.8W	10.6mW	**1.65W**
η_{max}	85%	90%	58%	64%	69%
Tech option	SOI	SOI, deep trench caps	Bulk CMOS	Bulk CMOS, metal gate	Bulk CMOS
# interleaving	32	1	4	32	21

Comparison with state of the art



CONCLUSIONS

Conclusions

- Cheap and power dense integrated DC-DC converters facilitate on-chip power management
- The passives are the bottleneck!
  - ≈ 90% of die area
- Bulk CMOS is potential vehicle for PowerSoC
  - Flying Well
  - Intrinsic Charge Recycling
  - Multiphase Interleaving
  - Voltage Domain Stacking
- Application domain
  - High performance: solving I/O problem
  - Low performance: implementing energy saving techniques

Acknowledgement

- **NXP**
  - Henk Jan Bergveld
  - Gerard Villar Pique
  - Patrick Smeets
  - Leo Warmerdam
- **Micas Colleages**
  - Dr. Tom Van Breussegem (ICsense.com)
  - Dr. Mike Wens (MinDCet.com)
  - Piet Callemeyn
  - Aki Sarafianos

References

[1] H-P. Le, et al., “A 32nm Fully Integrated Reconfigurable Switched-Capacitor DC-DC converter Delivering 0.55W/mm2 at 81% Efficiency,” ISSCC Dig. Tech. Papers, pp. 210-211, Feb., 2010

[2] L. Chang, et al., “A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm2,” IEEE Symp. VLSI Circuits, pp. 55-56, Jun., 2010

[3] M. Wens and M. Steyaert, “A Fully-Integrated CMOS 800mW 4-Phase Semi-Constant On/Off-time Step-Down Converter,” IEEE Trans. Power Electronics, vol.26, no. 2, pp.326-333, Feb., 2011

[4] D. Somasekhar, et al., “Multi-Phase 1 GHz Voltage Doubler Charge Pump in 32 nm Logic Process,” IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 751- 758, Apr., 2010

[5] M. D. Seeman and S. R. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 841–851, 2008.

QUESTIONS?

- Thank you!