Era of Intelligent Power Delivery

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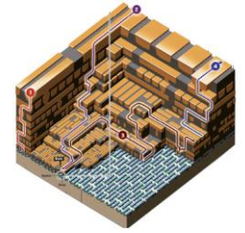
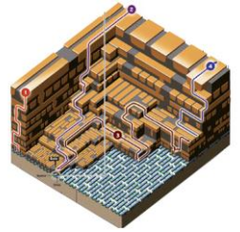


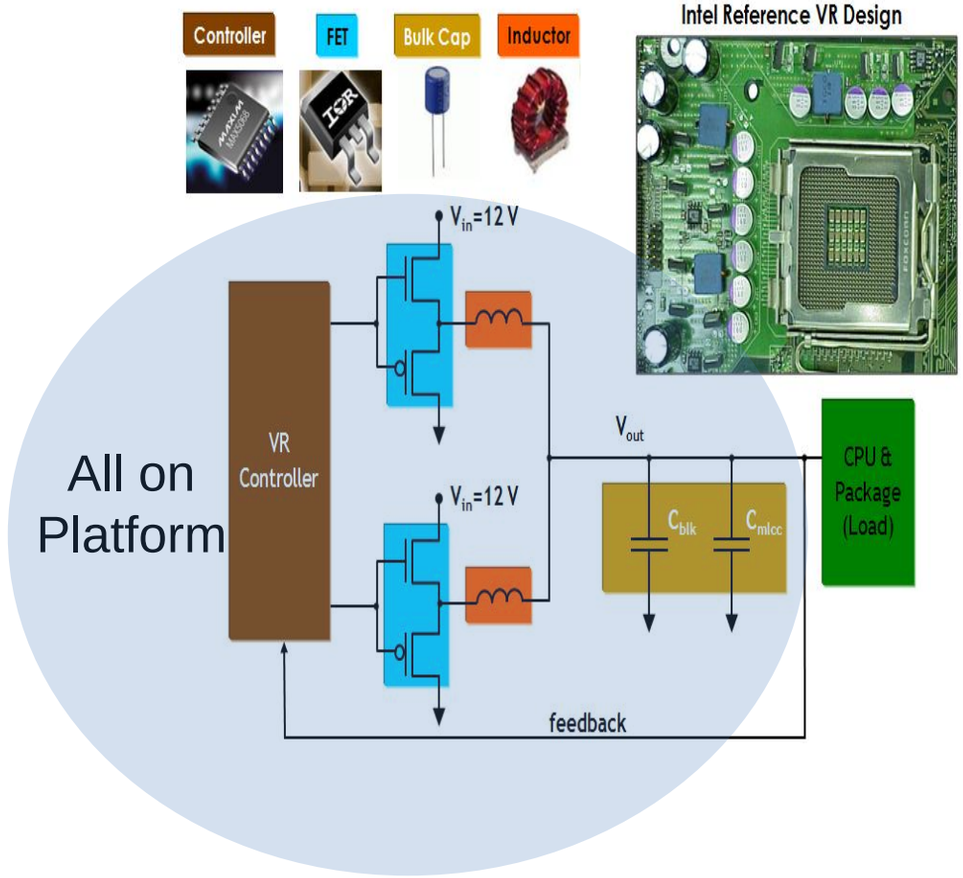
Outline

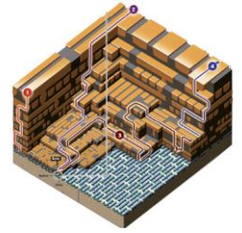
- Power Delivery Today
- Current Trends Challenging Power Delivery
- Opportunities
- Summary



Power Delivery Today

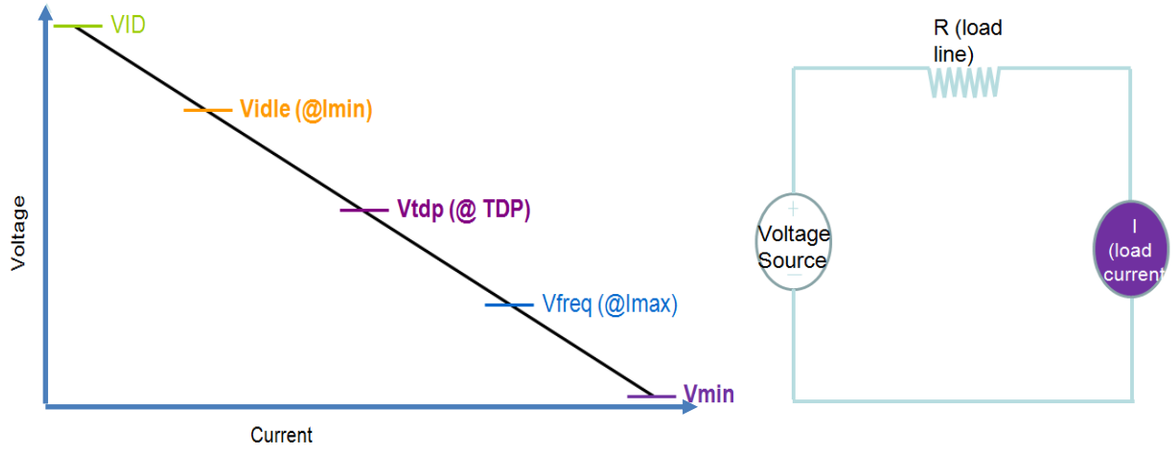
- **"Big Iron Solutions"**
  - Platform level VR power delivery
    - VR on motherboard with switching FETs, inductors to reduce ripple and capacitors to control droop, low resistance path to socket and minimal communication with load die
  - Metal Interconnect layers
    - Top level metal layers dedicated to power
    - Dedicated power and ground tracks on every metal layer
  - On-die device decap
    - Decap placement opportunistic/focused budgeting in I/O
  - Capacitors
    - Several arrays of capacitors on the motherboard and package

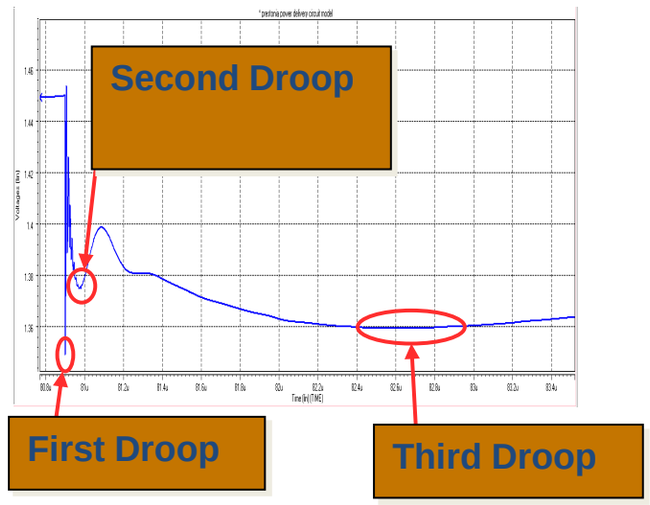


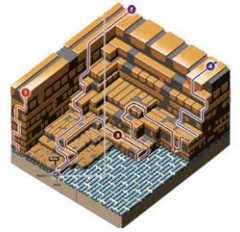


Power Delivery Today

- **Mitigation of non-ideal power delivery**
  - Load Line
    - Outcome of power delivery impedance
    - Triple operating voltage constraints
      - Idle (Imin) conditions: Top of loadline
      - Power Virus (Imax) conditions: Bottom of loadline
      - TDP conditions: somewhere along loadline
    - Active Voltage Positioning (AVP) to minimize power impact on load
      - Associated with 3rd droop
    - System exposed to “Excess” first droop
  - Droop mitigation mechanisms
    - AFS
    - DAF





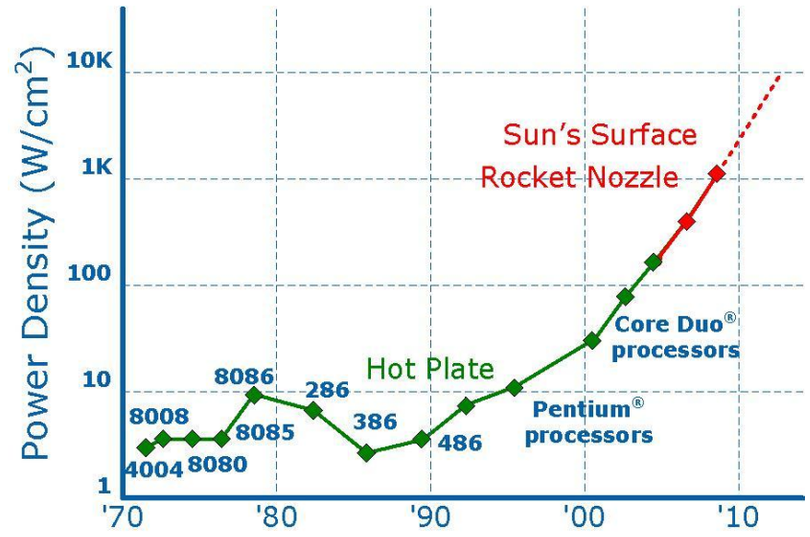


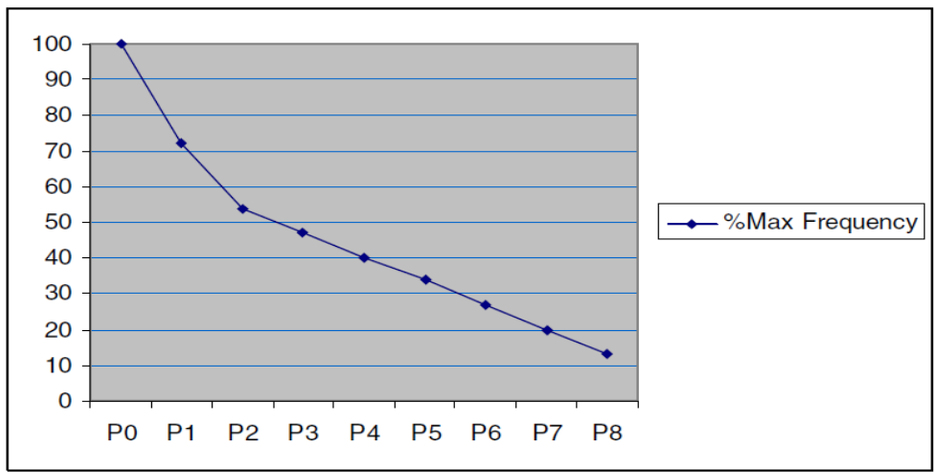
Power Delivery Today

- **Hit Power Wall**
  - Increasing performance while operating within Power limits
- **Response to power wall**

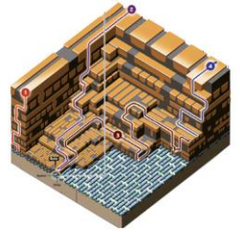
  Dynamic power = a.f* C *V²* f
  - Decreased Cdyn, lowered V and slowed chip down
  - Used clock-gating to reduce AF
  - Focused on Pipelined optimizations so all circuits run at ideal V/F – balanced pipeline

  Note: *continued lowering of V without improving power delivery can negate gains*
- **P (Performance)-states**
  - P-states enabled CPU cores to move along the V/F curve for optimizing power efficency



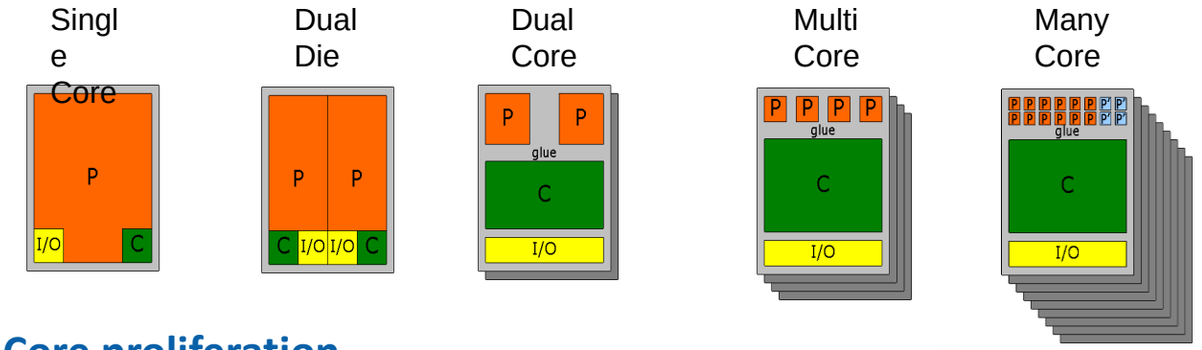


P-state CPU frequencies

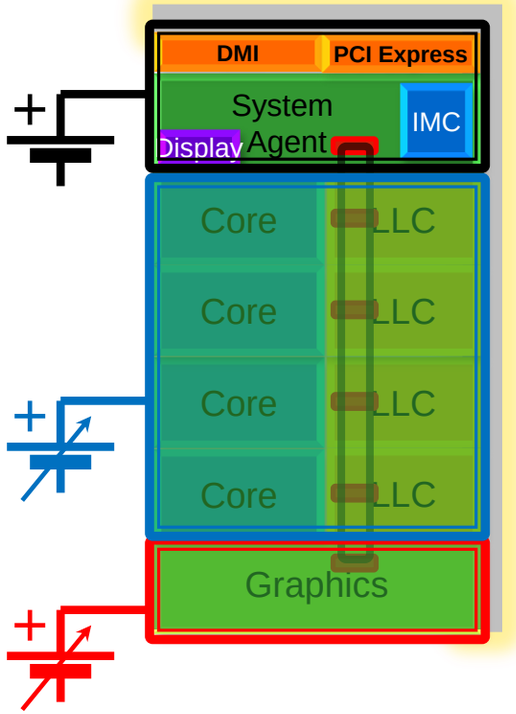


Power Delivery Today

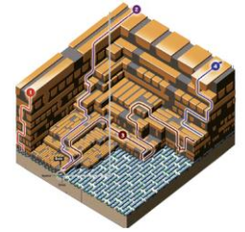
- **Response to power wall**
  - TM1/TM2
    - Thermal solutions driving initial challenges
  - Multiple cores
  - Multiple voltage domains
  - Die level Power gates which enabled dynamic ON/OFF



Core proliferation

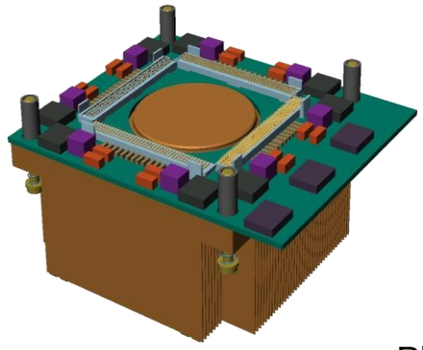


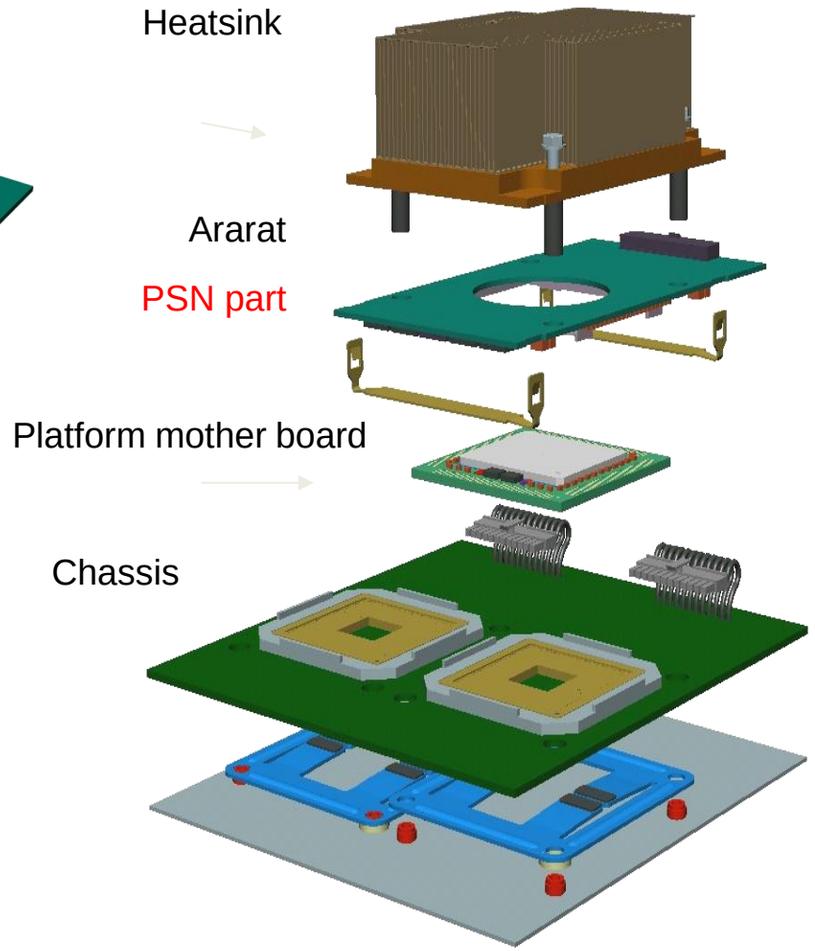
Power-gating on Intel's SandyBridge processor

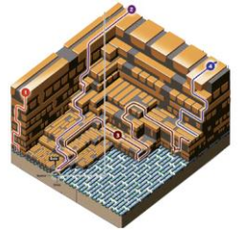


Power Delivery Today

- **Local VRs, more VRs and per core pair VID**
  - Availability of Ararat on Poulson
    - Enables power and performance optimization in light of increased variation
  - ***Ref: New Itanium for 32nm and Beyond (MPR report March 2011)***

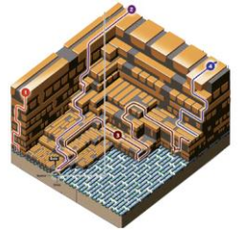






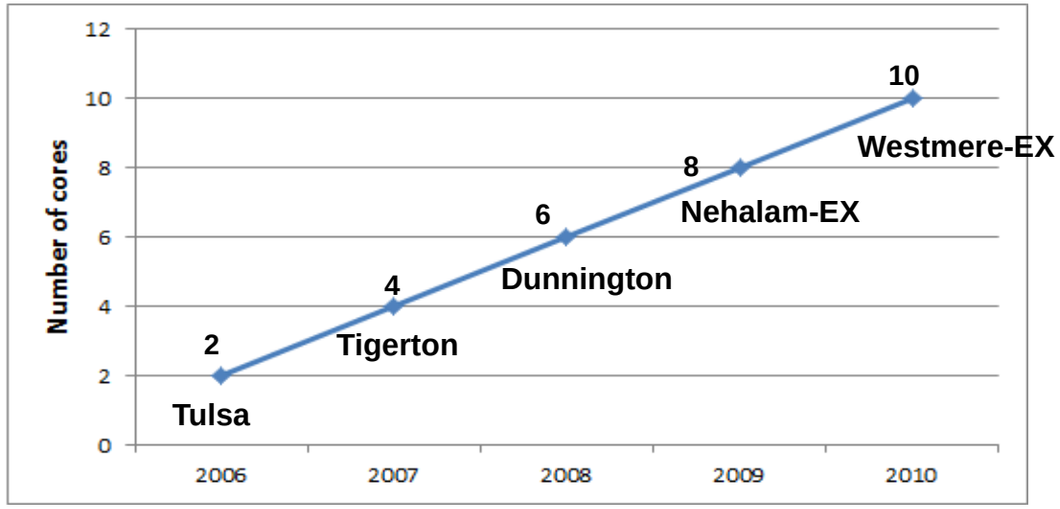
Current Trends Challenging Power Delivery

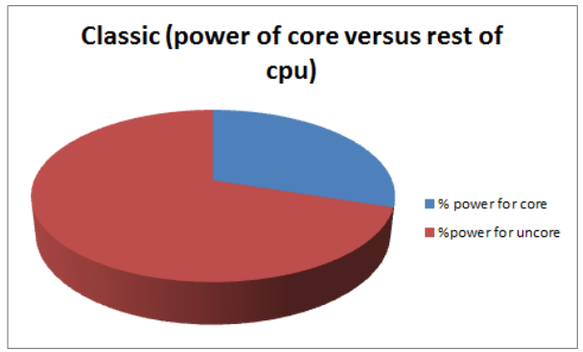
- **Some technology trends**
  - Transistor density ↑
  - Current density ↑
  - Iccmax ↑
  - Iccstep ↑
  - Vmin ↓
  - Vmax ↓
  - Bump pitch scaling : slow
  - Die size ↑
  - Metal stack↑
  - Interconnect wire width ↓

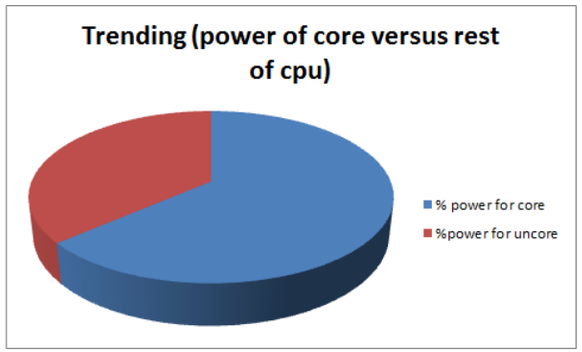


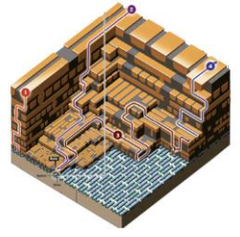
Current Trends Challenging Power Delivery

- **Increasing core count for microprocessors at power limited scaling**
  - Maximizing throughput under power budget ➔ increasing number of cores
  - Close to Vmin operation for Power efficiency
    - Increased sensitivity to droop
  - % of chip power reserved for cores increasing



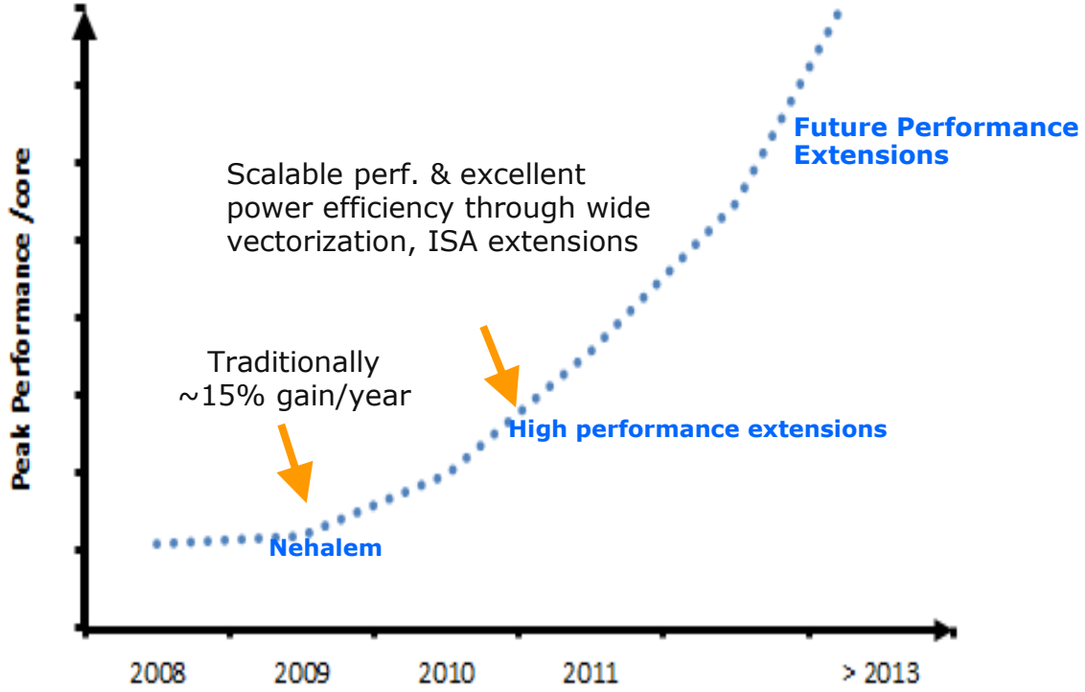


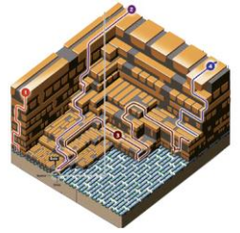




Current Trends Challenging Power Delivery

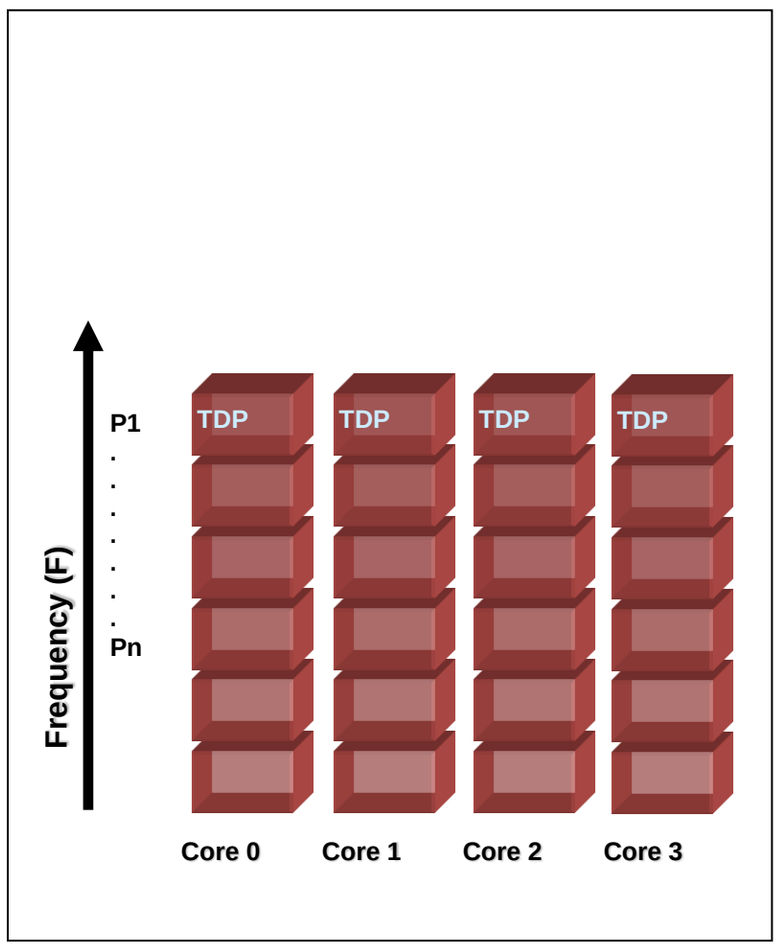
- **New core vectorized instructions for performance improvement:**
  - Suitable for floating point-intensive calculations in multimedia, scientific and financial applications (integer operations expected in later extensions)
  - Increases parallelism and throughput in floating point SIMD calculations
  - Reduces register load due to the non-destructive instructions

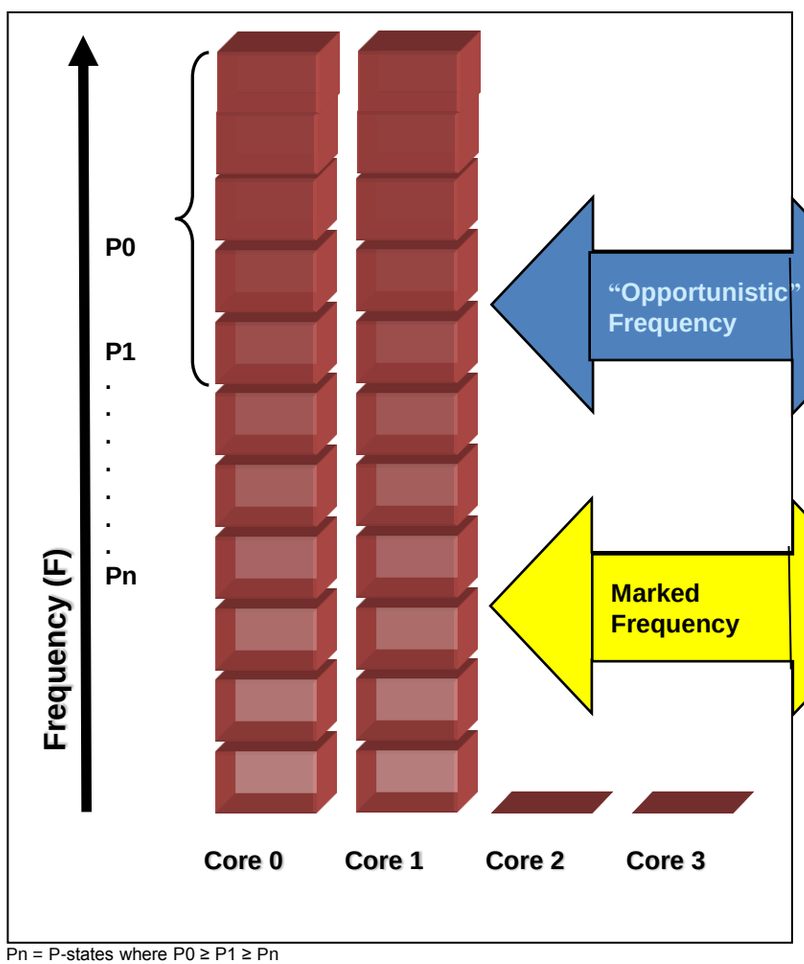




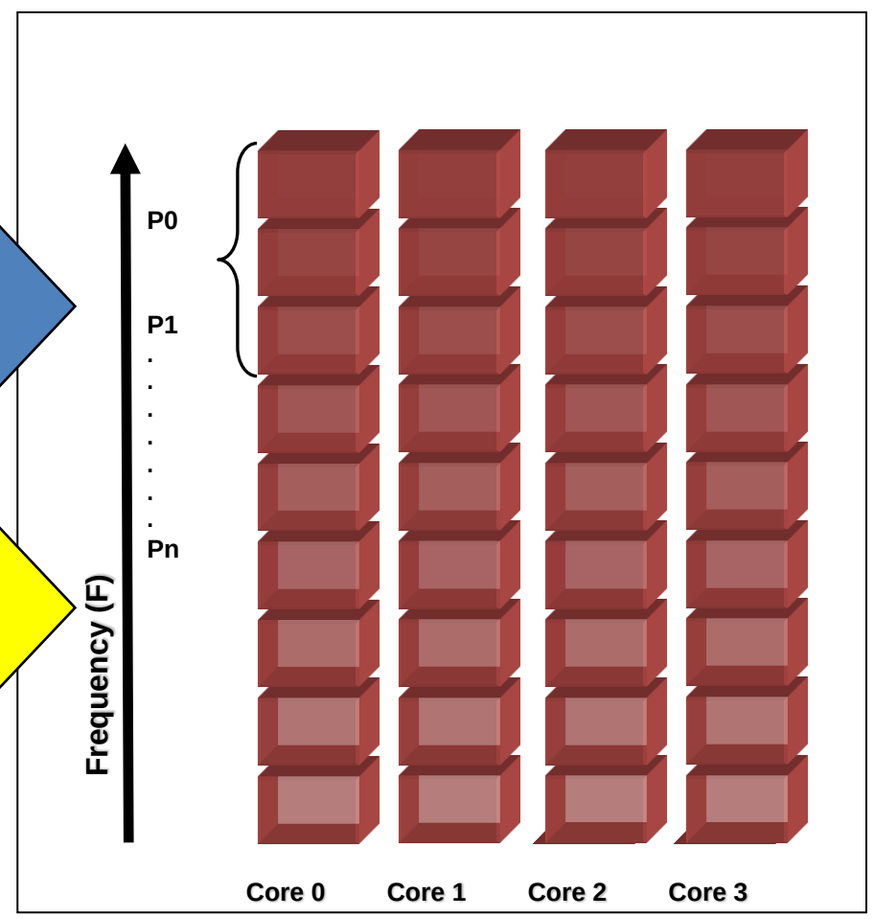
Current Trends Challenging Power Delivery

- Turbo 1.0 and Turbo 2.0 for opportunistic performance improvement





Pn = P-states where P0 ≥ P1 ≥ Pn



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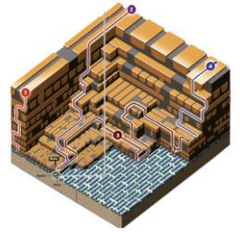
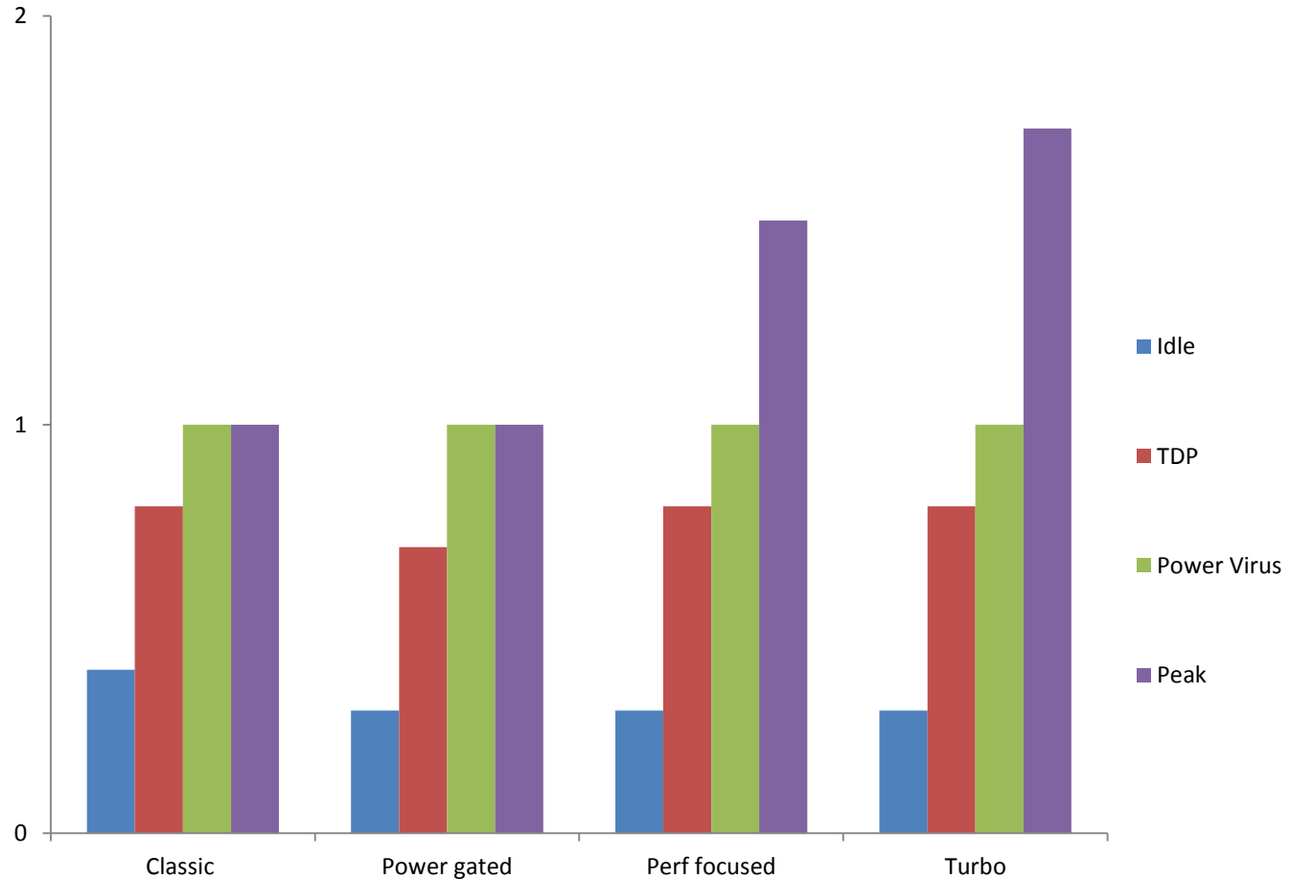
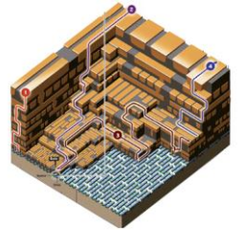


Current Trends Challenging Power Delivery

- **Dynamic range of core increasing due to**
  - Vectorized instructions
  - Turbo

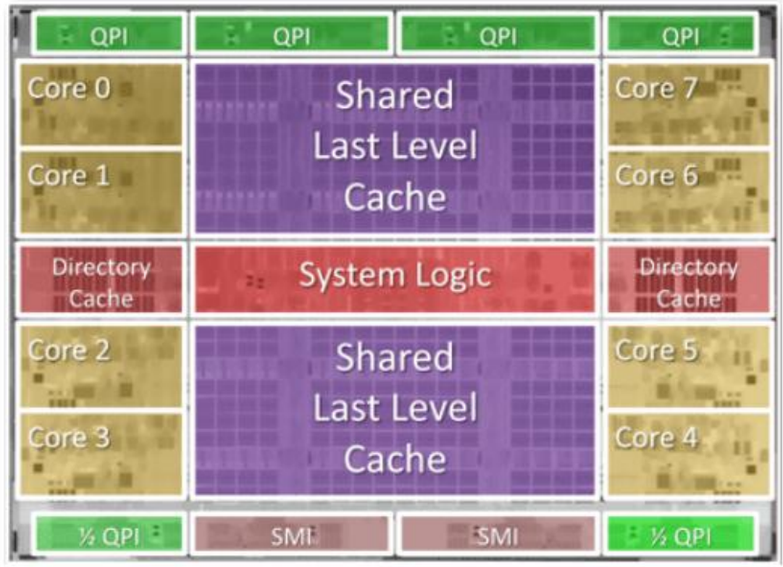
- **% of chip subject to dynamic swings increasing dramatically due to**
  - Vectorized instructions
  - Turbo
  - increased number of cores



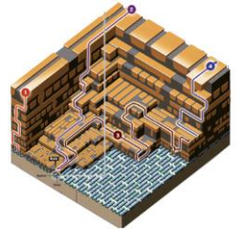


Current Trends Challenging Power Delivery

- **Voltage domain proliferation to minimize power consumption**
  - Dividing up power delivery resources to independently service each domain
  - Need for adequate decoupling for each domain
  - Leading to multiple clocking domains
  - Boundary latency issues
  - Requirement for increased circuitry
    - low power and variation-robust

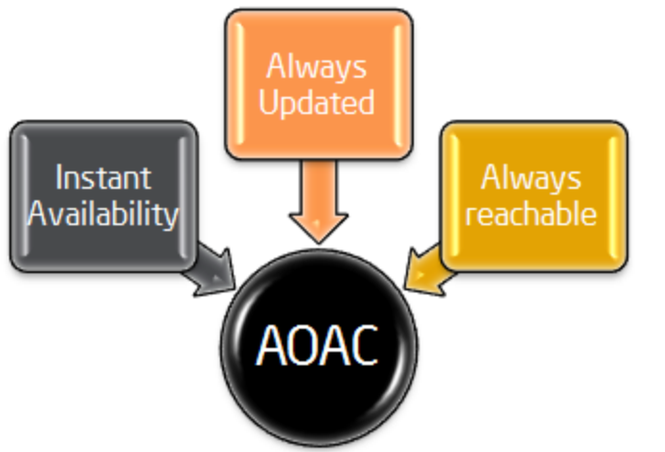


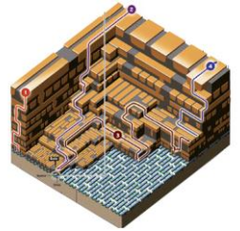
8 core Intel PSN IPF microprocessor with 10+ voltage domains



Current Trends Challenging Power Delivery

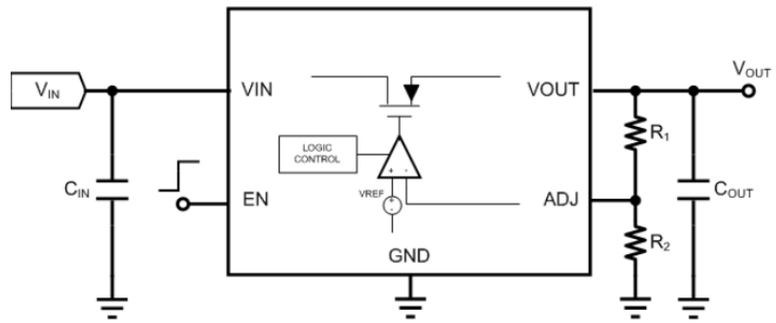
- **Improved User Experience**
  - Requirement for AOAC
  - Extended battery life on mobile devices
    - Low leakage critical
  - CPU cores needs to turn on and respond to changing workloads seamlessly



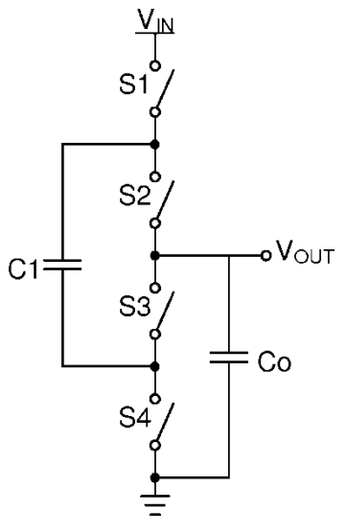


Opportunities

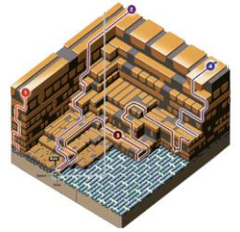
- **Develop fine-grained and efficient on-the-fly power delivery solutions**
  - Elimination of VR stages between source and point of consumption to improve response time and reduce losses
  - Increased integration of efficient low cost VR solutions to reduce droop
    - LDOs, SCVRs etc



Sample LDO

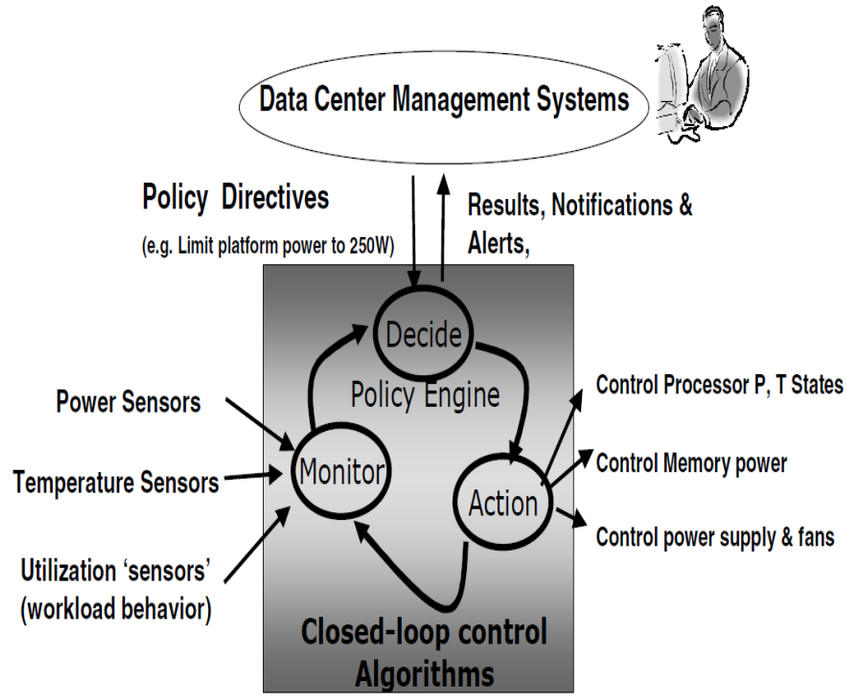


Sample SCVR

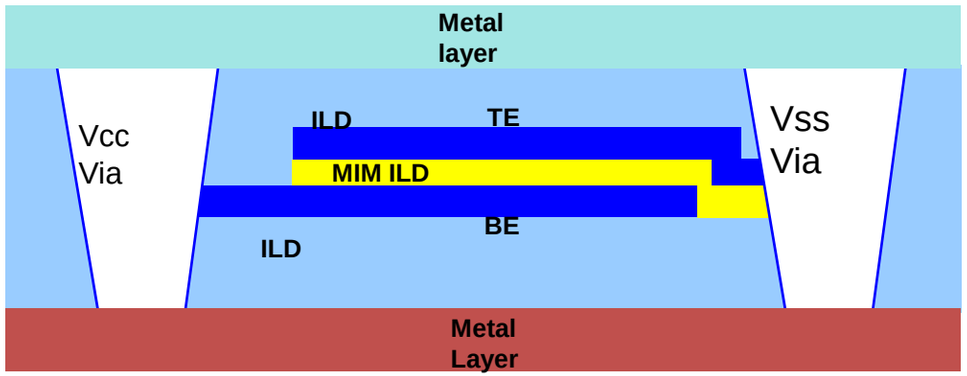


Opportunities

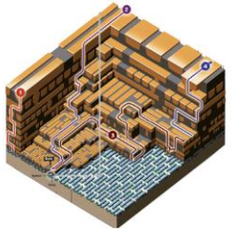
- **Develop fine-grained and efficient on-the-fly power delivery solutions**
  - Active and sophisticated control systems that respond rapidly to current demands
  - High density die decoupling solutions
  - Deliver smooth and high fidelity power with minimal noise as voltage domains are power up and down



Power Management architecture



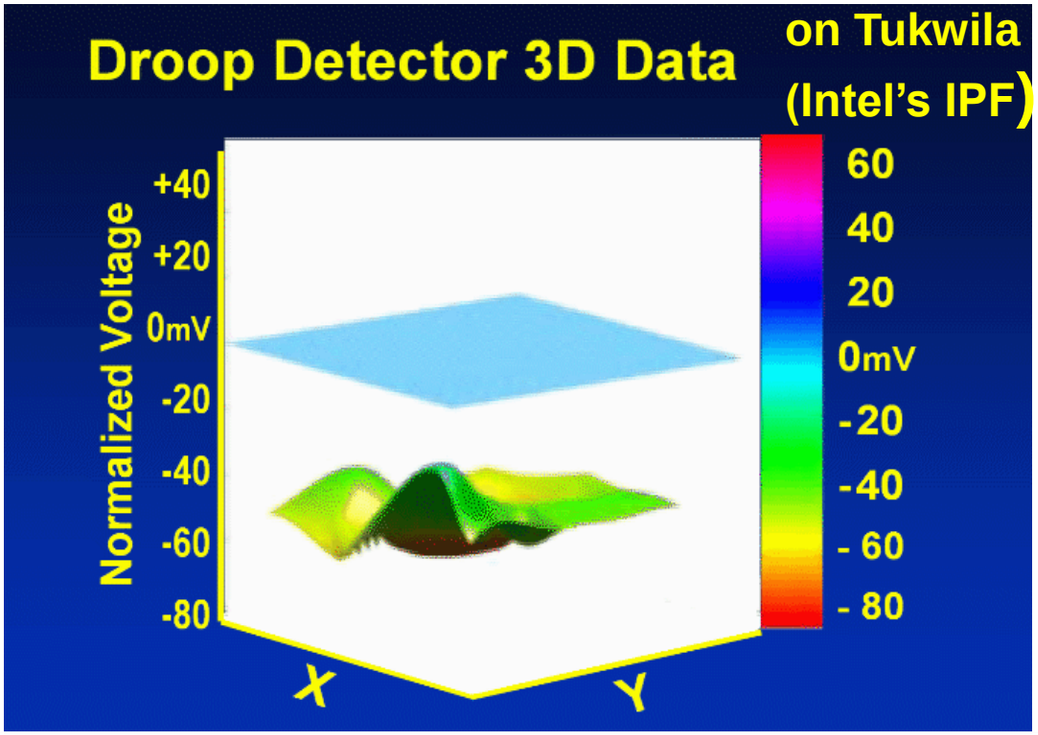
Sample Metal-Insulator-Metal cap

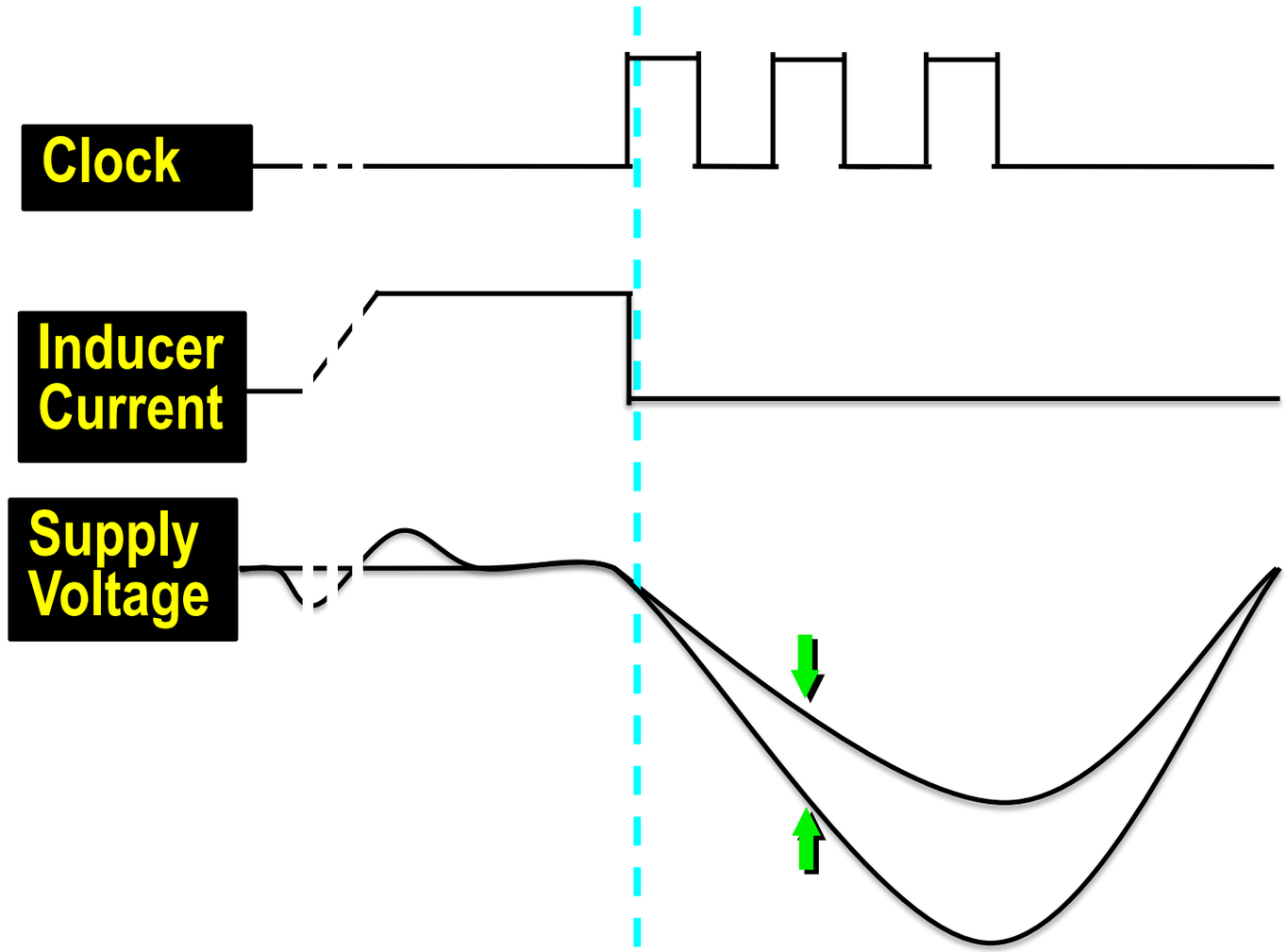


Opportunities

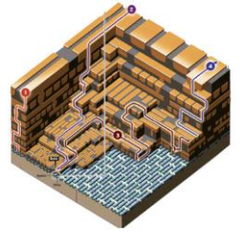
- **Droop monitors to track and understand impact of droop**
  - Droop detectors
  - Droop inducers

Ref: ITC-2009 " Voltage Transient Detection and Induction for Debug and Test"



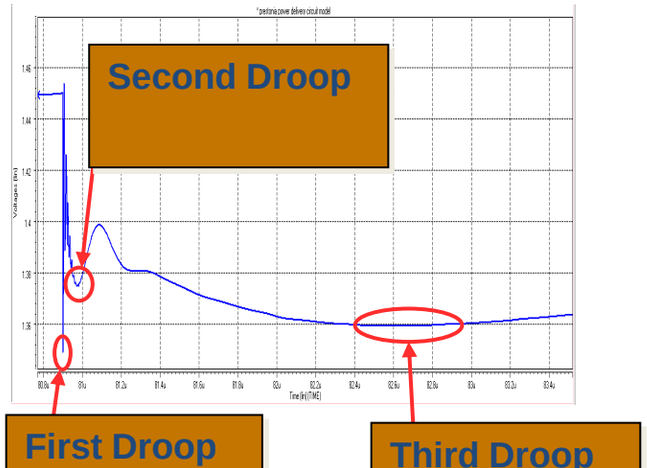


Droop inducers being used to mitigate droop on Tukwila (Intel's 65nm IPF)

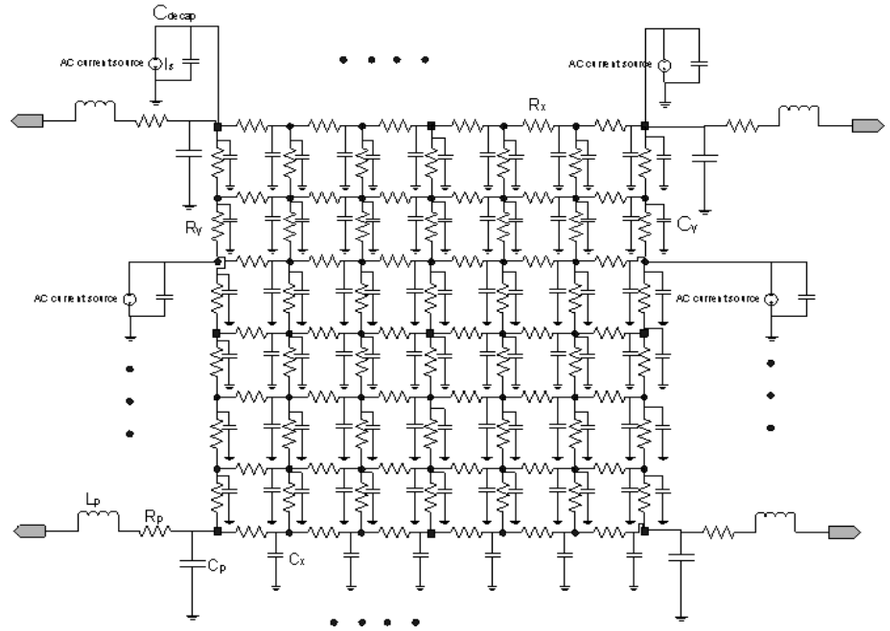


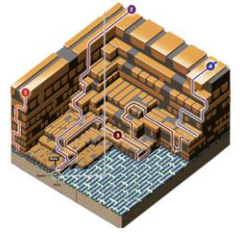
Opportunities

- **Enhanced architectural solutions to proactively control and reduce high frequency droops**
  - Instruction reordering
  - Instruction throttling



- **Simulation strategies to accurately predict behavior in pre-Si**
  - CAD tools to support capacity and efficiency
  - Emphasis on Package-die co-design/simulation

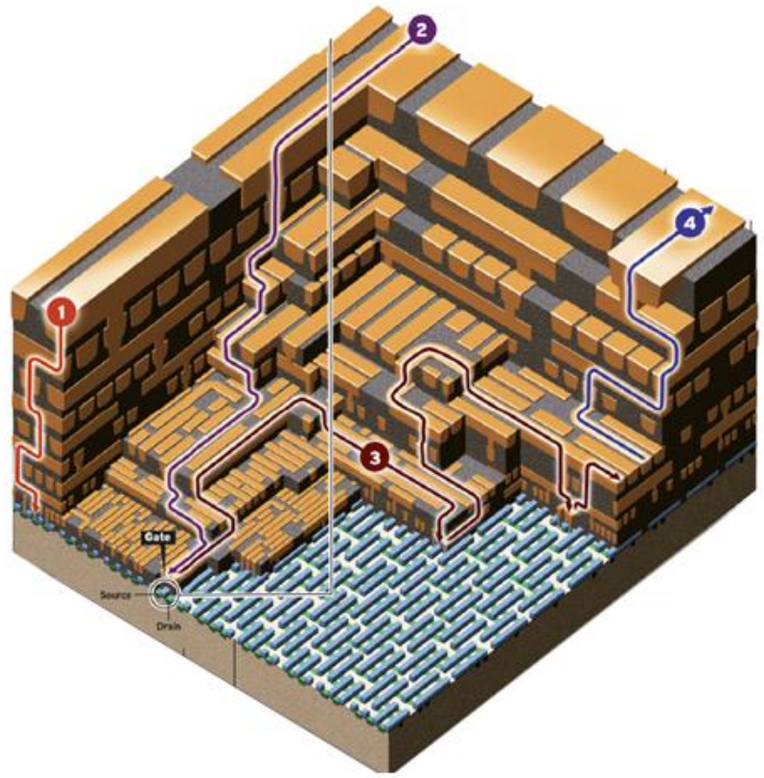




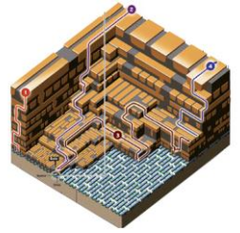
Summary

Entered era of bringing in intelligence to the power delivery system

- **Look at increased integration of VRs to seamlessly support active and changing current demands on the chip**
- **Power management ←→ power delivery solution interactions**
- **Solutions to understand and alleviate**
  - Impact of increased Cdyn range due to new instructions, higher performance cores, SIMD
- **Creation of testbenches & tools to project and understand impact of degraded power delivery in pre-Si**



Lots of opportunities ahead!



BACKUP