Soft Charging Switched Capacitor CMOS Power Converters - Increasing Efficiency and Power Density Using a Merged Two-Stage Architecture

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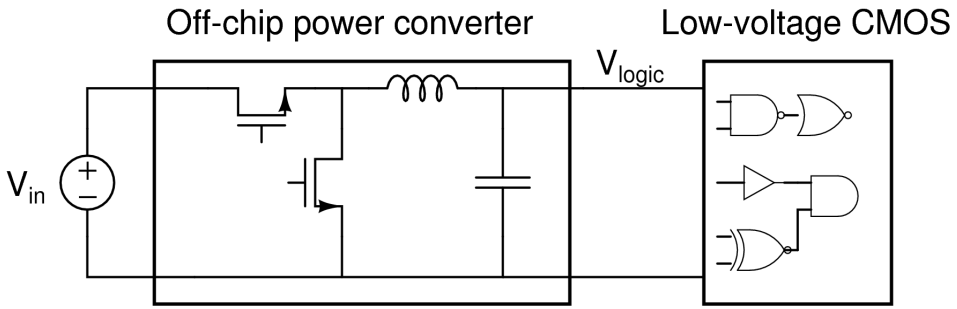
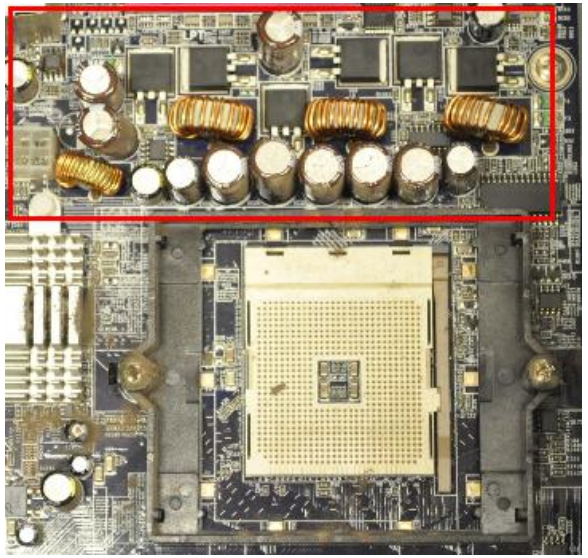
Acknowledgments

- Professor David Perreault (MIT)
- Ryan May (UIUC)
- Yutian Lei (UIUC)
- Interconnect Focus Center, a DARPA and SRC program

Introduction

- Energy processing electronics
  - No Moore's law
  - Often dominate electronics size, weight



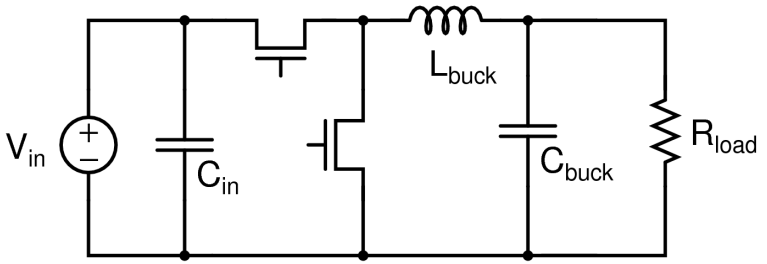


- Switches rated to block full input voltage
  - Low switching frequency, low control bandwidth
  - Large passive components

Can we achieve high voltage blocking capability and high switching frequency?

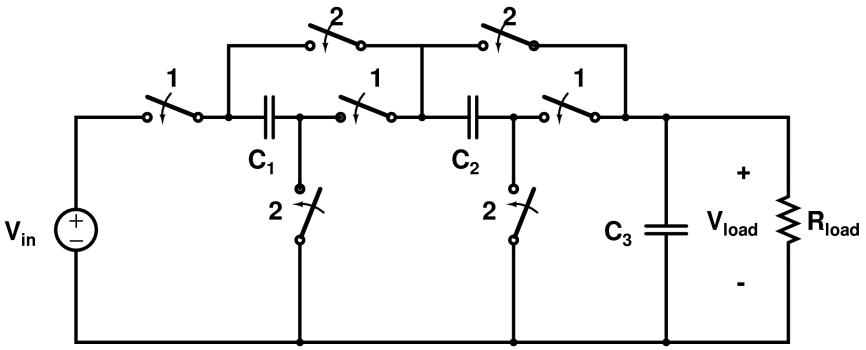
Converter topologies

- Inductor based
  - Excellent regulation
  - Difficult to integrate on die
    - Desire small inductors
    - Require high switching frequency
  - Large step-down at high frequency is challenging



$$E_{inductor} = \tfrac{1}{2} LI^2$$

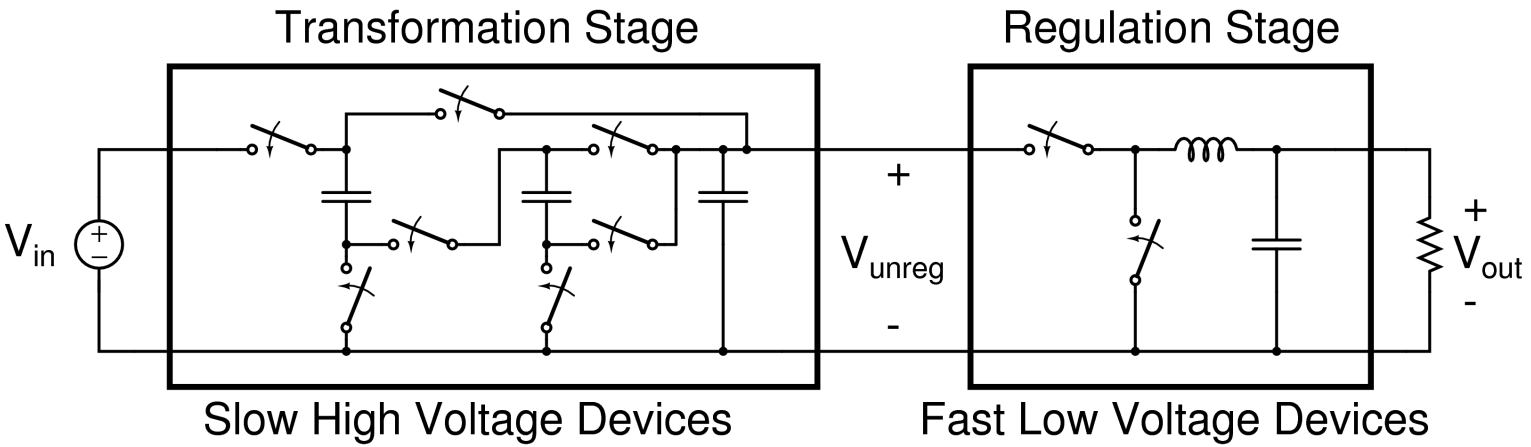
- Capacitor based
  - High power density
  - High efficiency
  - High on-chip capacitance available
  - Large step-down possible at high frequencies
  - Poor regulation
  - Poor energy utilization



$$E_{capacitor} = \tfrac{1}{2} CV^2$$

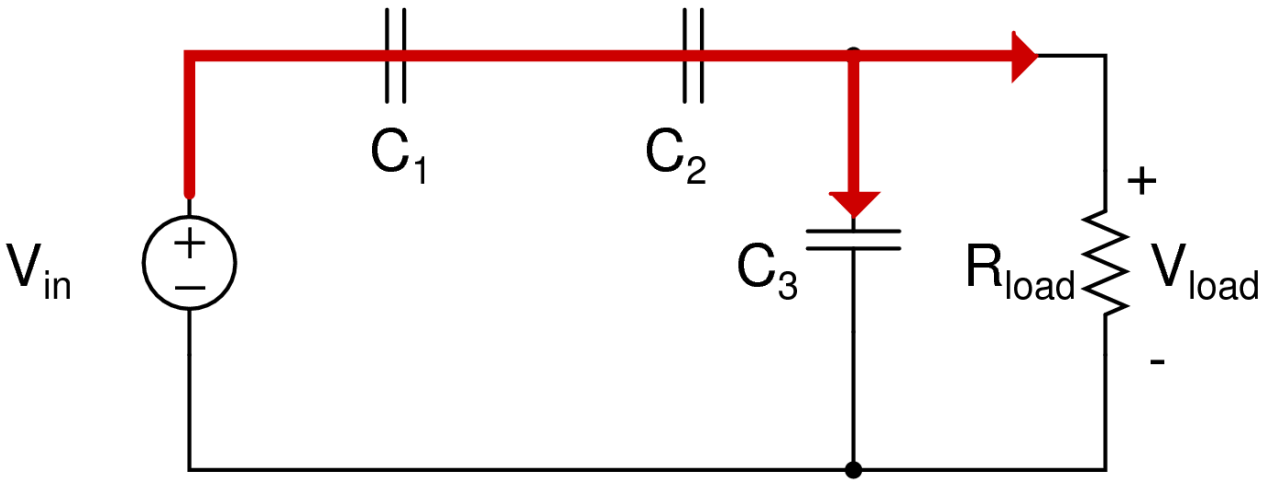
Can we combine the benefits of each converter topology?

Two-stage Converter

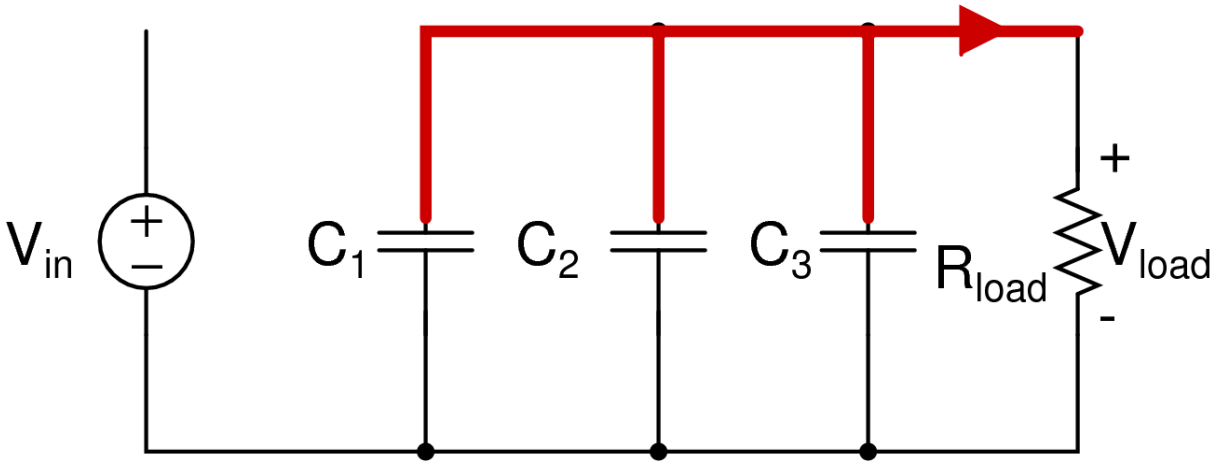


- Switched-capacitor transformation stage
  - Step down to low voltage at fixed conversion ratio
  - High efficiency at specified conversion ratio
- Magnetic fast regulation stage
  - High frequency regulation with low-voltage buck converter, small inductor
  - Provides high bandwidth regulation and additional step-down

Series Parallel SC Converter Example

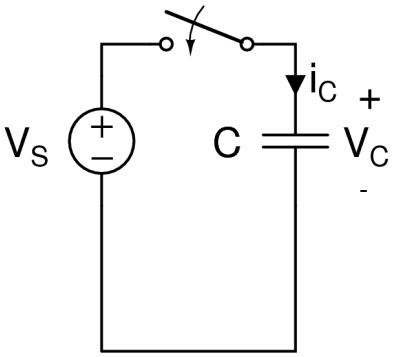


$V_{load} = V_{in}/3$



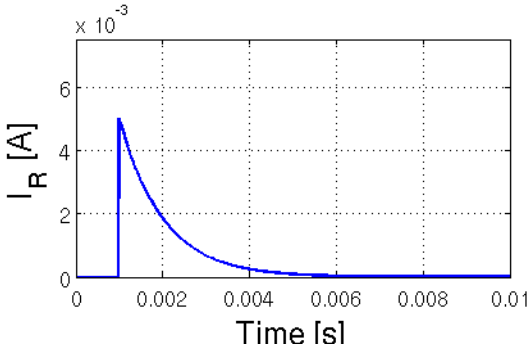
Limitations of Switched Capacitor Converter

- Switched capacitor stage limitations
  - Poor energy utilization in switched-capacitor stage



$$V_C(t<0) = V_S - \Delta V$$

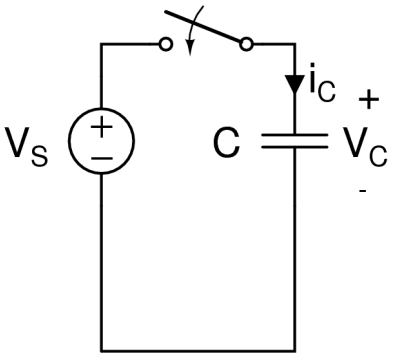
$$E_{diss} = \frac{1}{2}C(\Delta V)^2$$



- To minimize loss, must keep capacitor voltage ripple small
  - Use big capacitors
  - Operate at high switching frequency

M.D. Seeman and S.R. Sanders “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” IEEE Transanctions on Power Electronics, March 2008.

Soft Charging Operation



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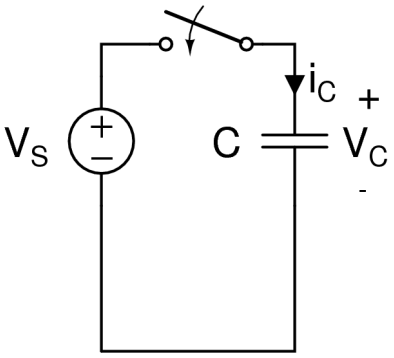

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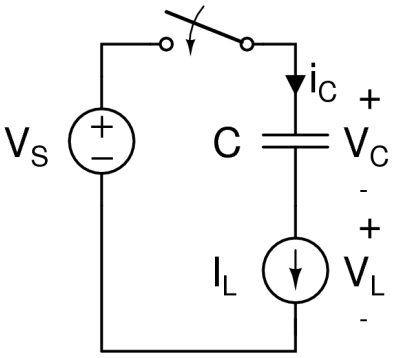
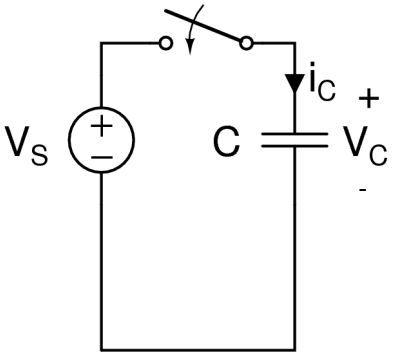


$$E_{diss} = \frac{1}{2}C(\Delta V)^2$$

- Controlled charging current

Soft Charging Operation



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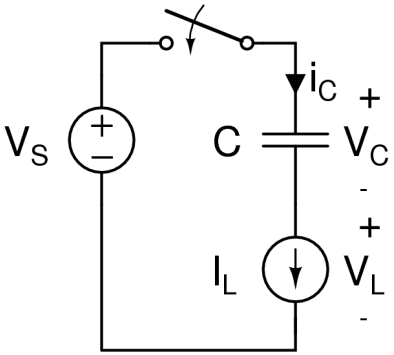

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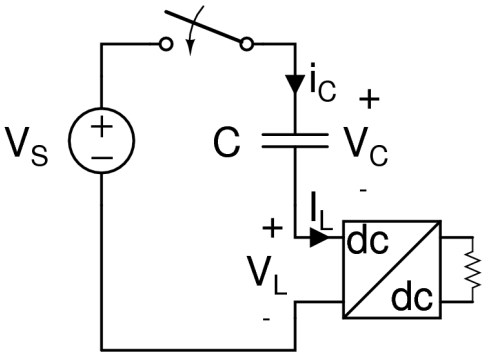
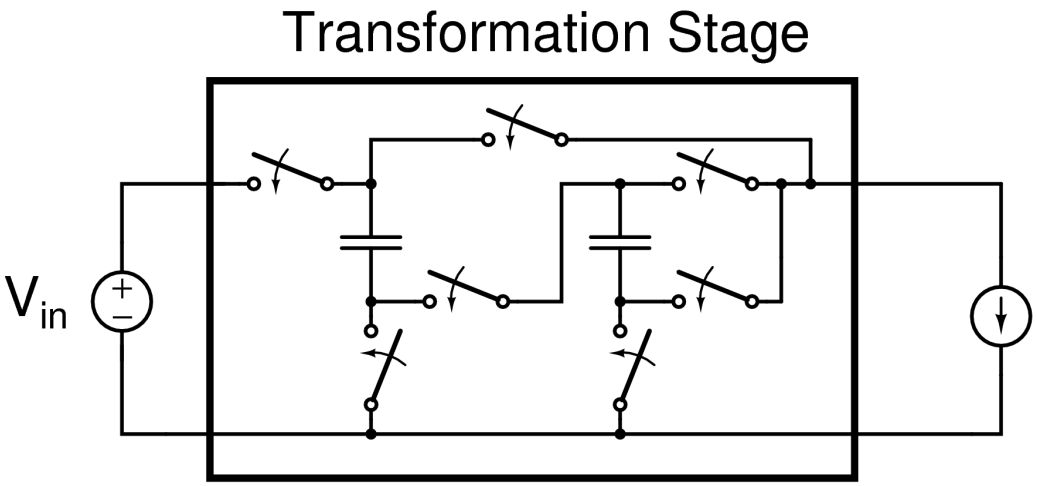


$$E_{dc-dc} = \frac{1}{2}C(\Delta V)^2$$

- Controlled charging current
- Recover energy that is normally dissipated

Soft-charging Two-stage Converter



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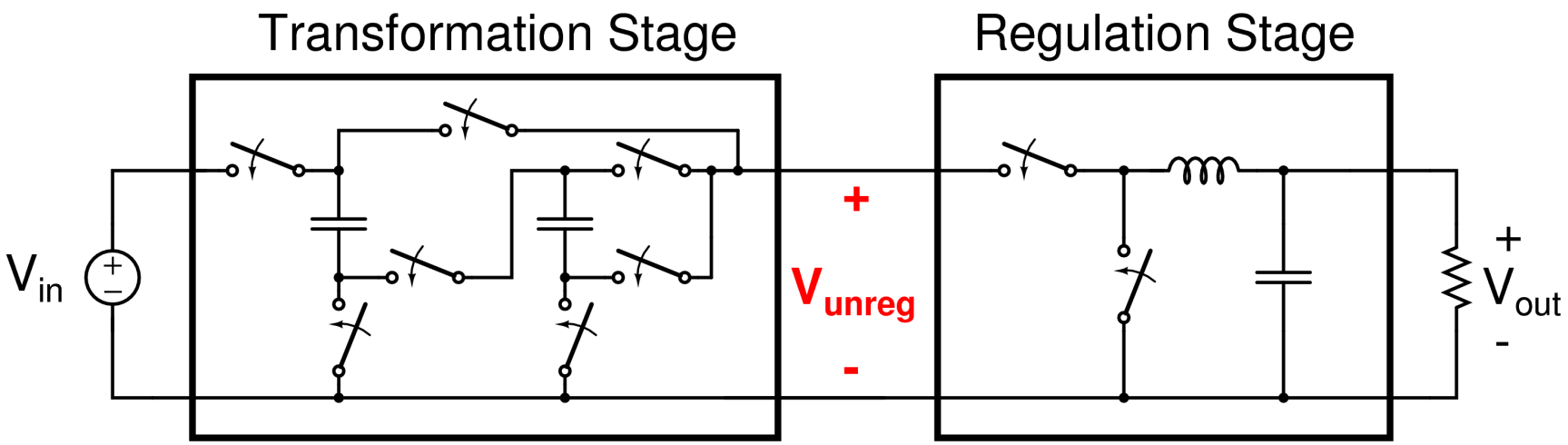
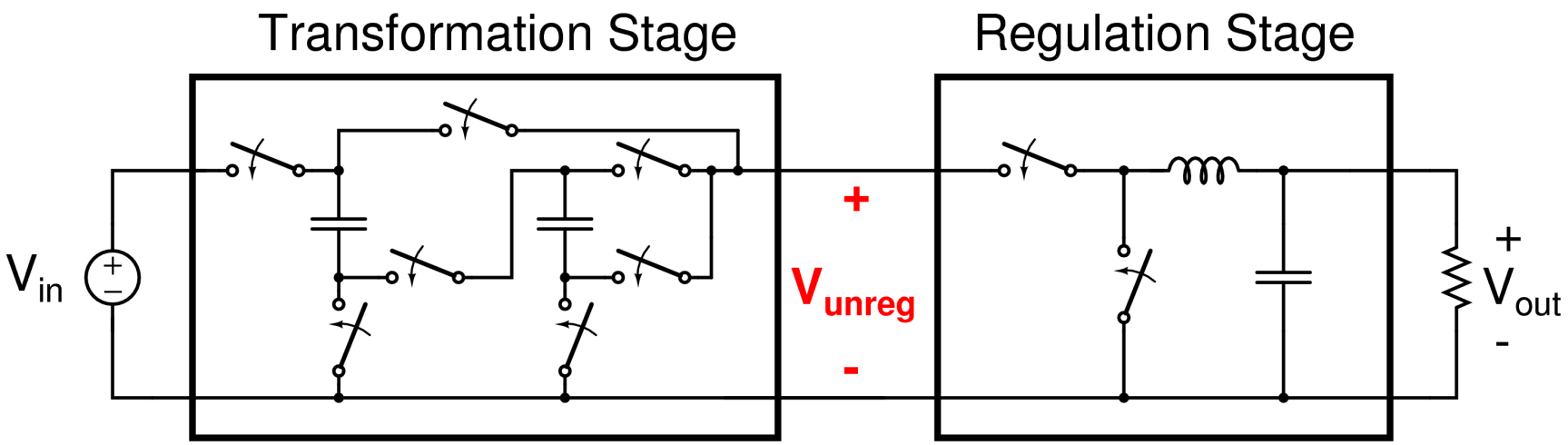


Soft-charging Two-stage Converter



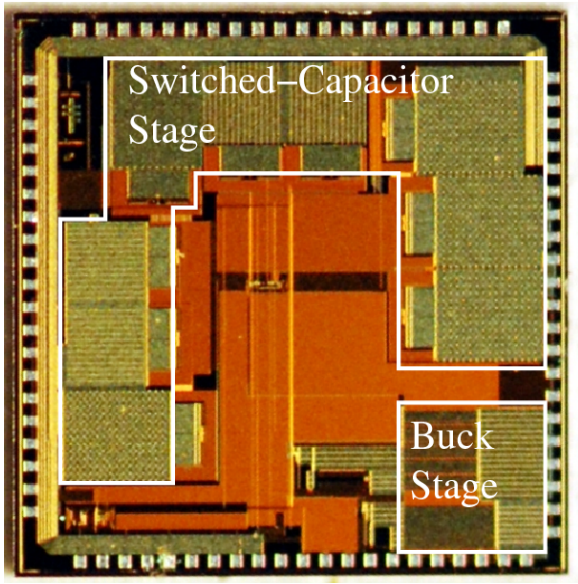
- Charge/discharge capacitors via regulation stage
  - Recover energy otherwise lost (soft charging)
  - Enable large ripple voltage on capacitors
  - Requires new control methods

R.C.N. Pilawa-Podgurski, D.M. Giuliano, and D.J. Perreault "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," IEEE Power Electronics Specialists Conference, 2008

Fully Integrated 180 nm CMOS Converter

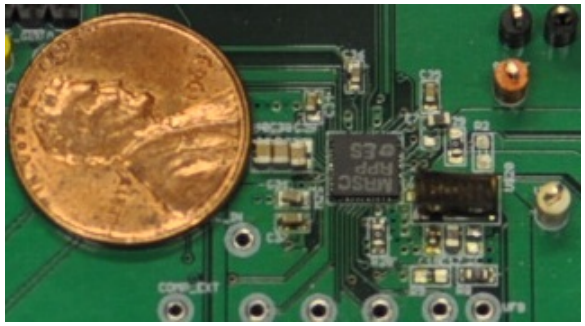
ILLINOIS

- Transformation stage: 5 V thick gate oxide devices, 22 uF off-chip capacitors. F_{sw} = 2-200 kHz
- Regulation stage: 2 V devices, off-chip inductor and output capacitor. F_{sw} = 10 MHz
- All power devices, control and startup circuitry on-chip



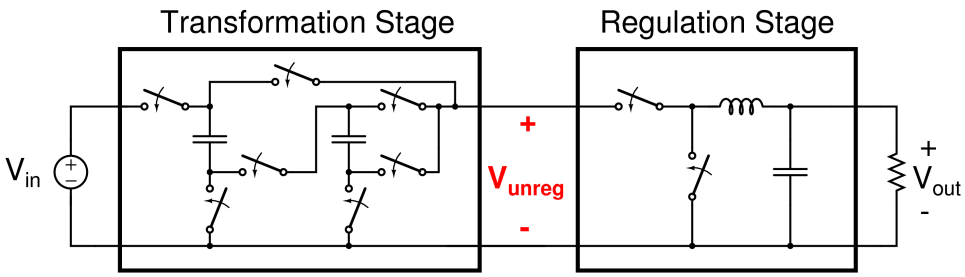
CONVERTER SPECIFICATIONS

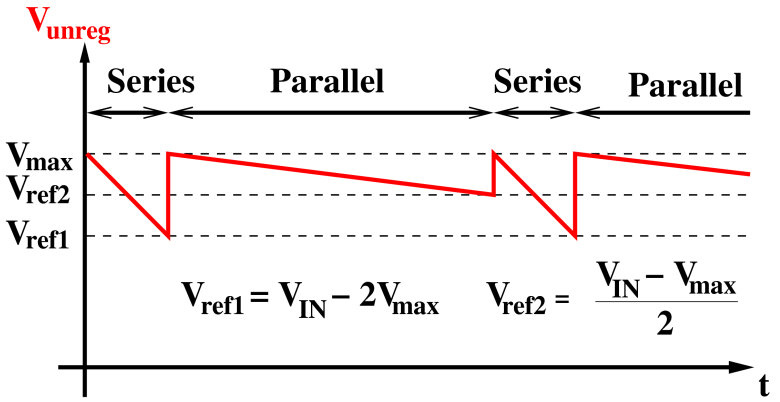
Input Voltage Range	4.5-5 V
Output Voltage Range	1-1.3 V
Output Power Range	0.3-0.8 W
SC Switching Frequency	2-100 kHz (load dependent)
Buck Switching Frequency	10 MHz
Peak Efficiency	81%

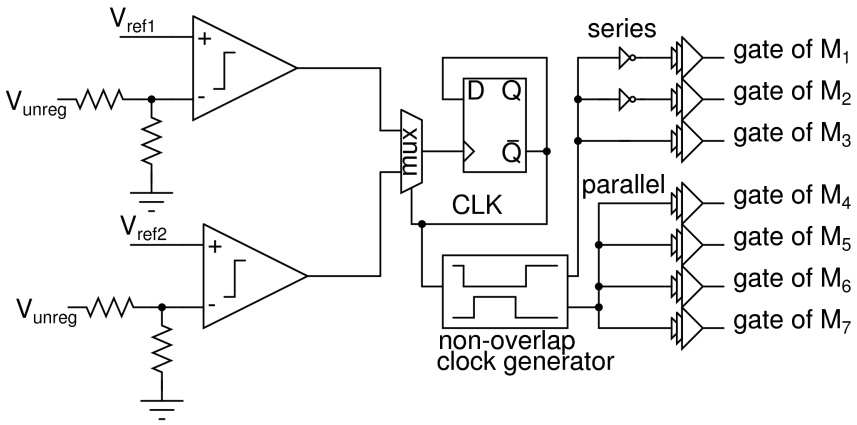


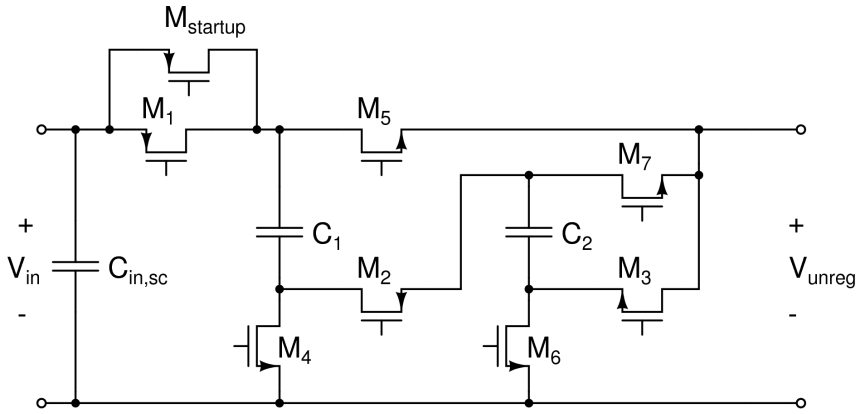
R.C.N. Pilawa-Podgurski, D.J. Perreault, "Merged Two-Stage Power Converter with Soft Charging Switched-Capacitor Stage in 180 nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 47, No 7, pp. 1557-1567, 2012

Transformation Stage Control Implementation

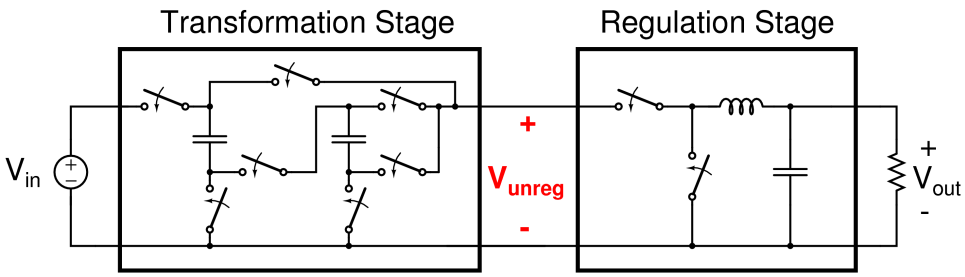


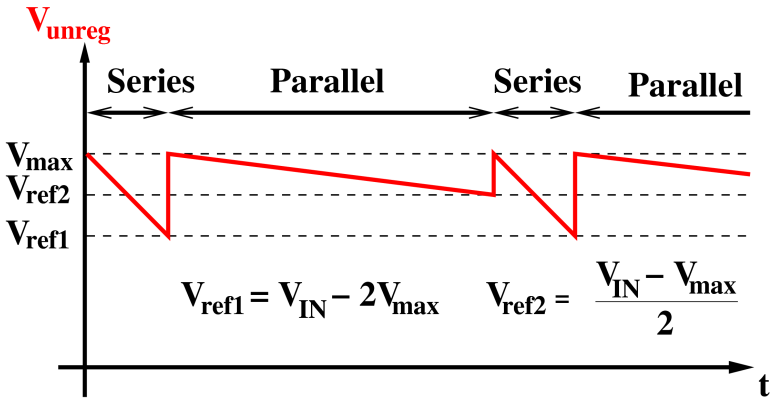


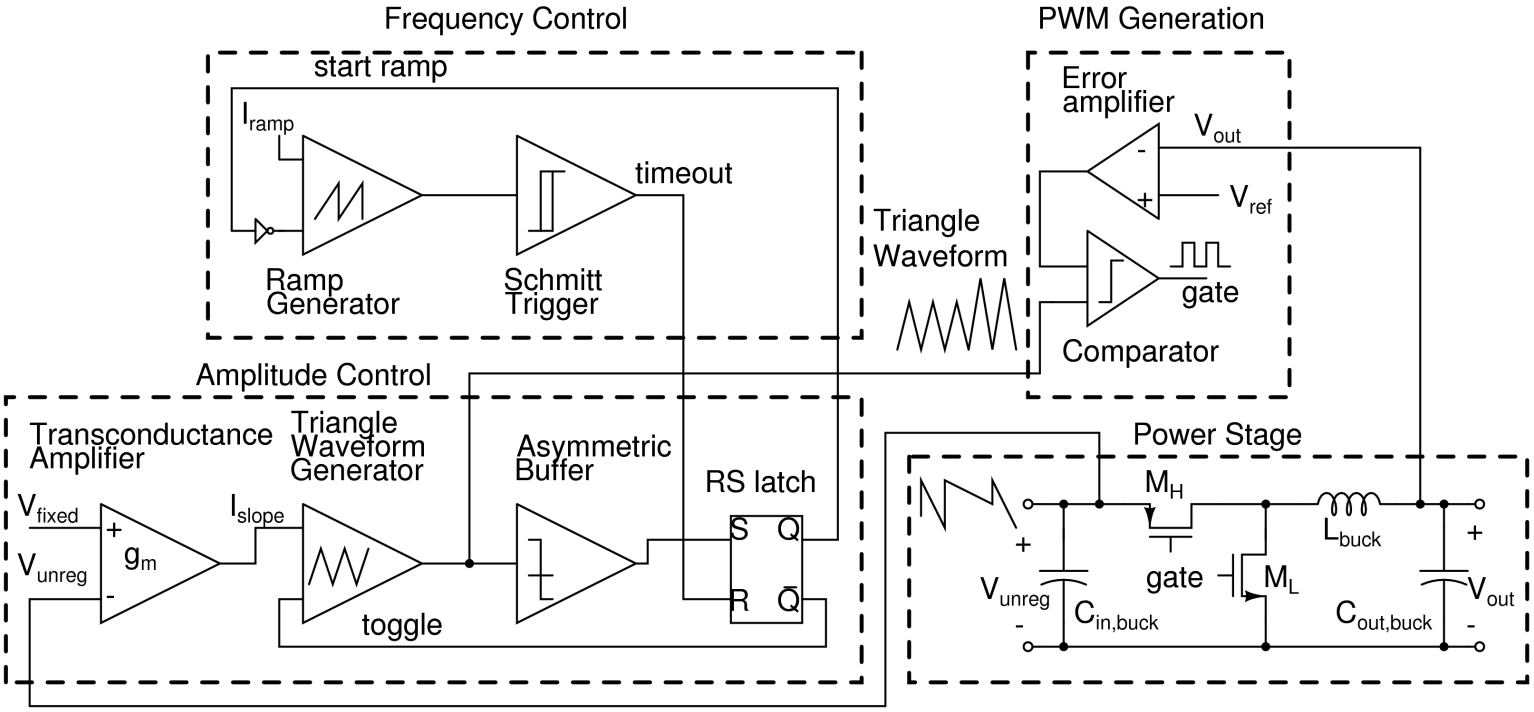




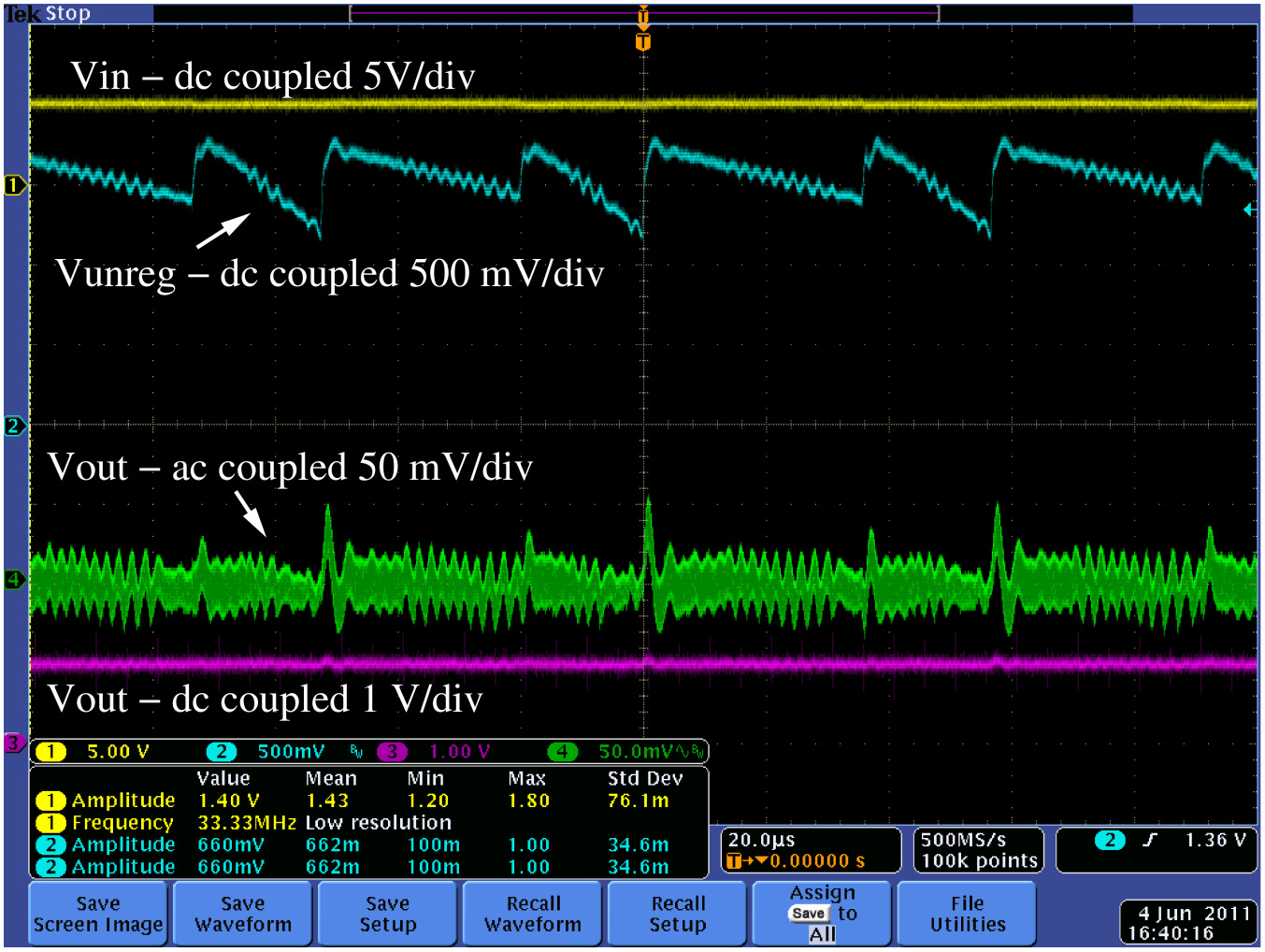
Regulation Stage Control Implementation





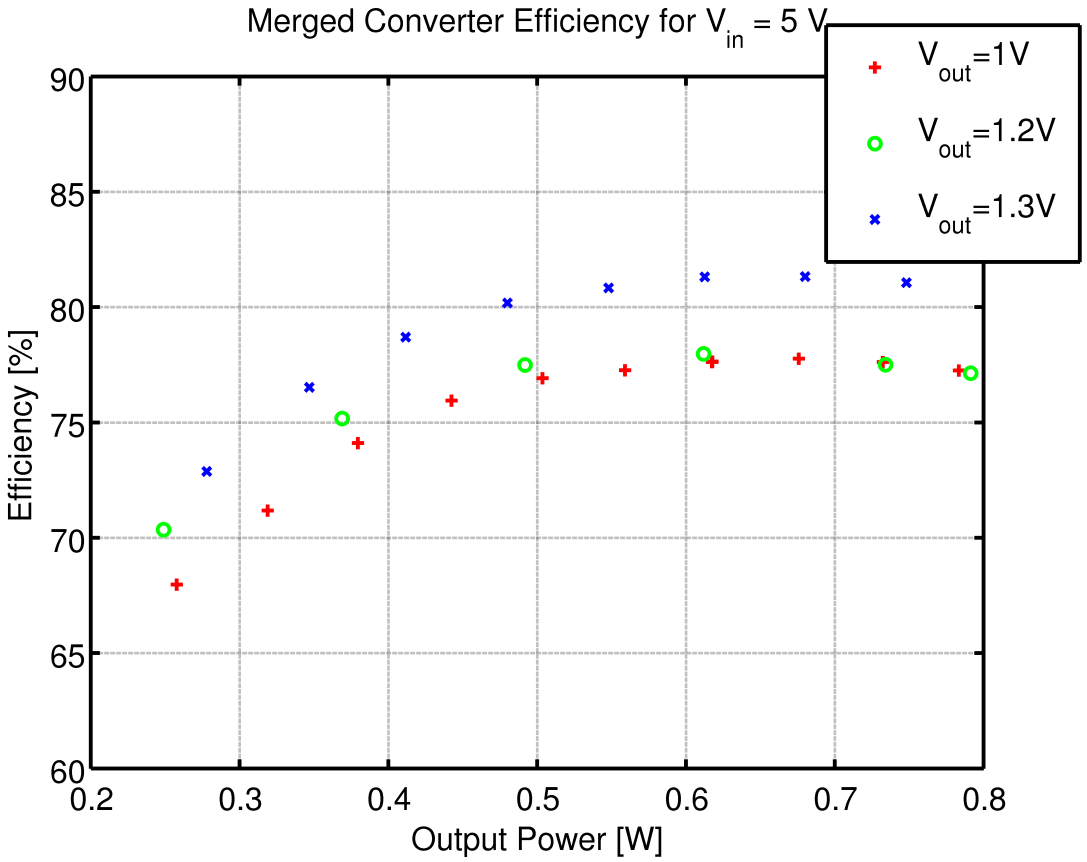


Experimental Waveforms



Feedforward control keeps V_{out} steady despite large ripple on V_{unreg}

Two-stage converter performance



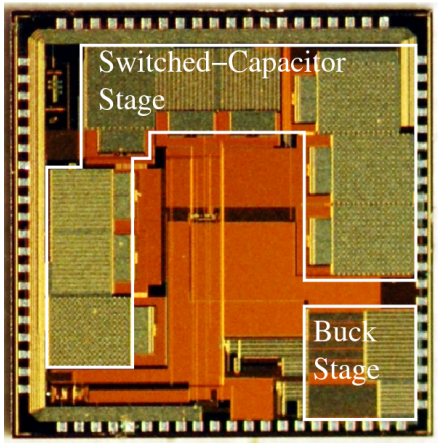


TABLE II
ESTIMATED CONVERTER LOSS BREAKDOWN AT P_{out}=0.8 W

Bond-wire conduction loss	60 mW
Transistor gating loss	45 mW
On-die metallization conduction loss	40 mW
Transistor conduction loss	11 mW
Inductor loss	5 mW
Control losses	2 mW

Efficiency is limited by packaging parasitics

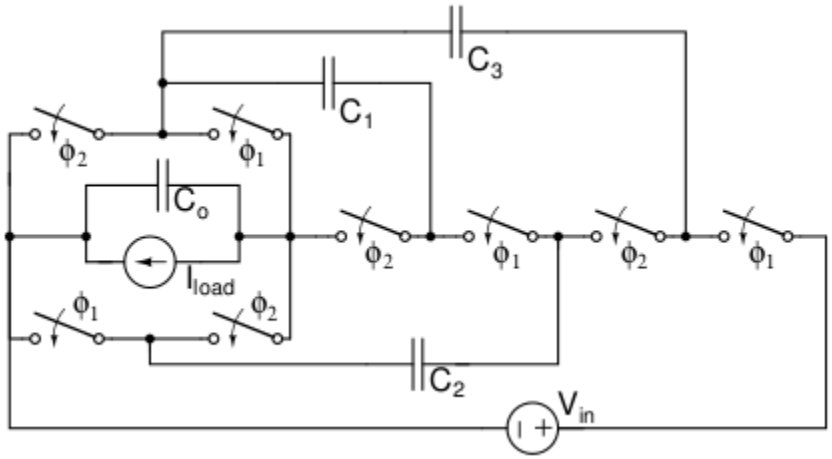
Improving Performance

ILLINOIS

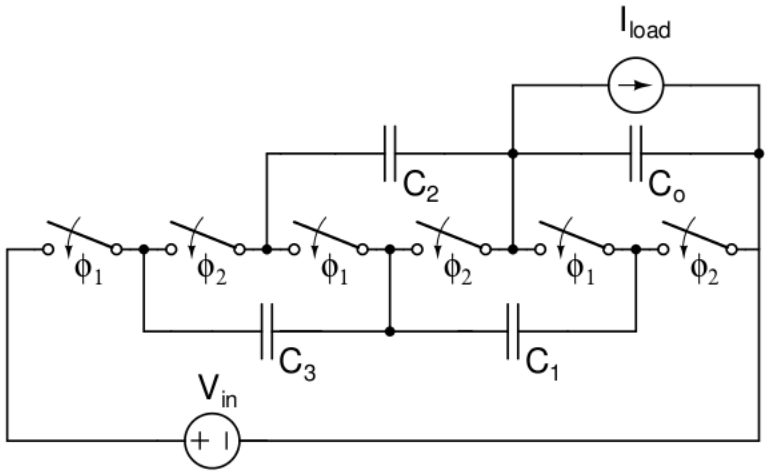
- Better packaging
  - Industry solutions exist
- Series Parallel SC topology is not optimum
  - Lower switch stress in Dickson topology
- Advanced control
  - Predictive control
  - Current-mode control of regulation stage
- More advanced CMOS process

Extensions

- Demonstrated soft charging operation in series-parallel SC converter
- Can soft-charging techniques be used for other SC topologies?
  - Dickson topology – yes, with modifications
  - Ladder topology – no
- Can determine suitability using charge flow vectors
  - Ongoing work



Dickson topology



Ladder topology

Conclusions

- Two-stage power converter architecture
  - Make use of CMOS device characteristics
  - Separate transformation and regulation functions
  - Achieve large voltage step down and high bandwidth control
- Soft charging operation
  - Recover energy in regulation stage
  - Enable large voltage ripple on capacitors
    - Smaller size, higher efficiency
  - Requires new control implementations
- Experimental prototype
  - Achieve good performance
  - Efficiency in prototype is limited by packaging parasitics
- Exploring additional SC topologies for soft charging operation