The 3D Silicon Leader

High Density Silicon based Capacitors for Power Electronics System Integration

Powersoc ,November 2012

Catherine Bunel

Outline

- Introduction
- 3D Silicon Capacitor density roadmap
- A new worldwide record of capacitor density
- High voltage capacitors
- Examples of applications
- Conclusion

Introduction

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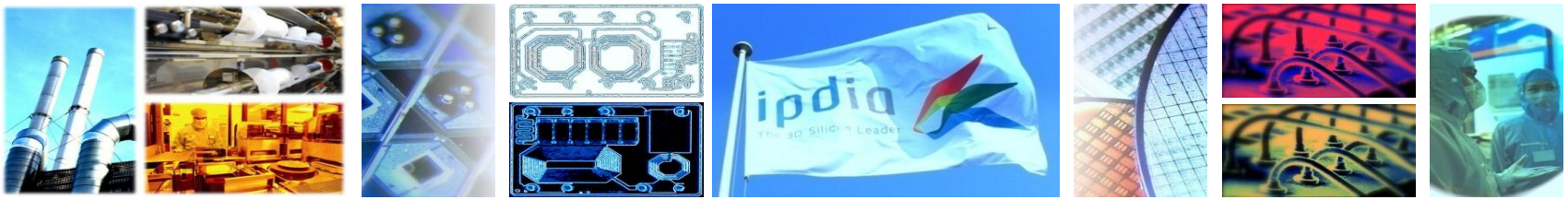
Who are we?

- Independent Company located in Caen, Normandy, France
- Dedicated to manufacturing of leading edge Integrated Passive Devices
- 20 M$ revenues, 100 people and operating own Silicon wafer fab
- Strong R&D team and collaborations with leading research institutes



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What do we do?

High performance, **high stability** and **high reliability** silicon passive components to customers in communication, harsh environment, industrial, lighting, and medical markets.








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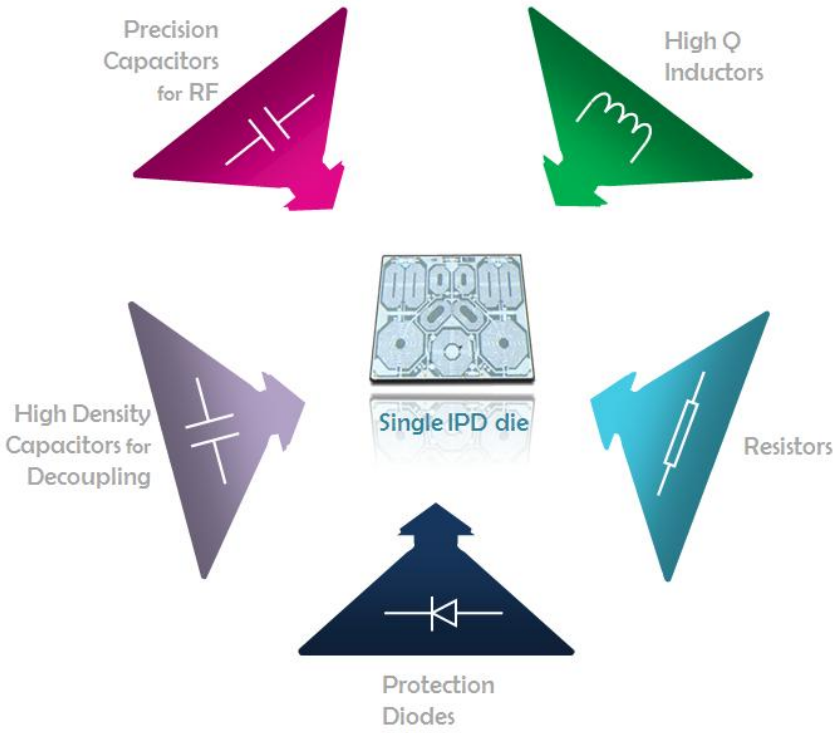
PICS-IPD, a Unique Technology

Passive **I**ntegration **C**onnecting **S**ubstrate



Up to 100's of passive components can be integrated

Value proposition is:

- Size
- Cost
- Performance

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IPDIA value proposition: Technology that enables

- **Miniaturization of application**
  - Module: High density integration
  - High PCB area saving (e.g. > 40%)
  - Silicon die with embedded passives as replacement of external SMD components
  - Compatible with standard wire bonding or reflow assembly according to scenarios

- **Reduced Cost**
  - BOM level
  - Simpler manufacturing with module
  - Simpler application with less components to place

- **Enhanced Performance**
  - Very high stability vs temperature, -55°C to +210(*)°C operating range
  - High stability vs voltage, time…
  - High reliability (no cracking & very low failure rate<2ppm)
  - Efficient decoupling with low ESR/ESL by full integration on silicon
  - Lower battery life time with very low leakage current
  - PCB influence cancelled

- **Greater Flexibility**
  - One configurable IPD allowing a set of output voltages

(*): limited by the active part, up to 250°C is possible with our passive integration

3D CAPACITOR DENSITY ROADMAP

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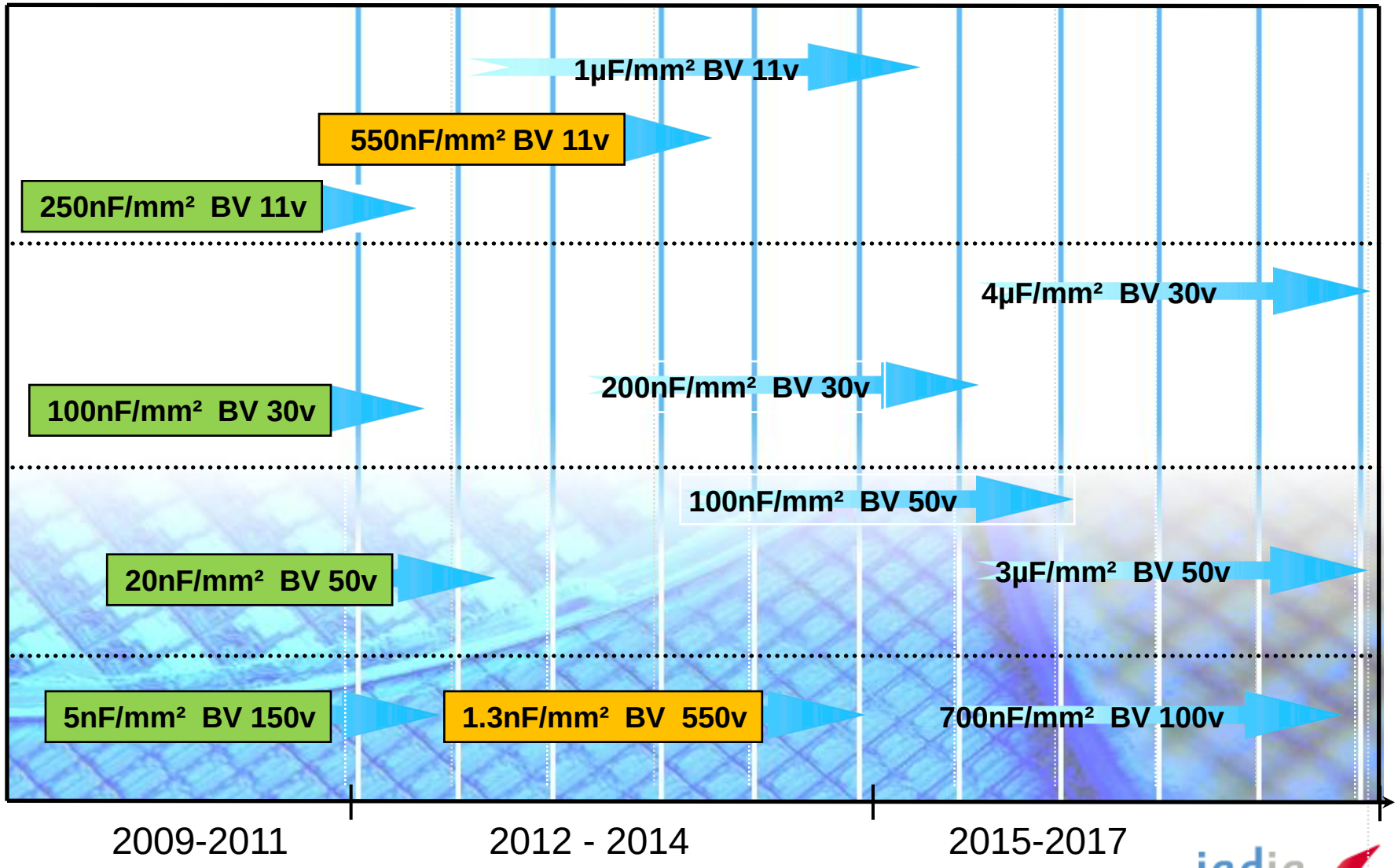
3D Capacitor Density Roadmap



Company confidentia

Production

Demonstrated

PICS4=550nF/mm²
A NEW WORLDWIDE RECORD

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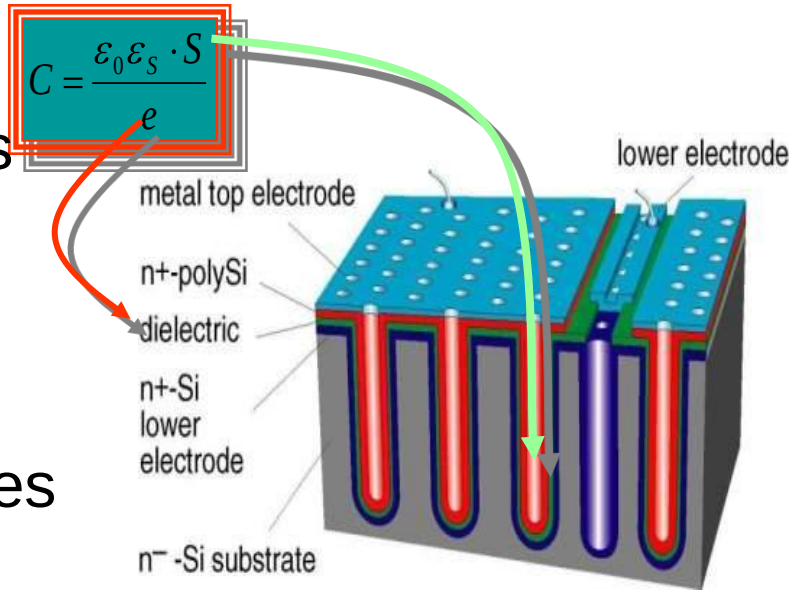
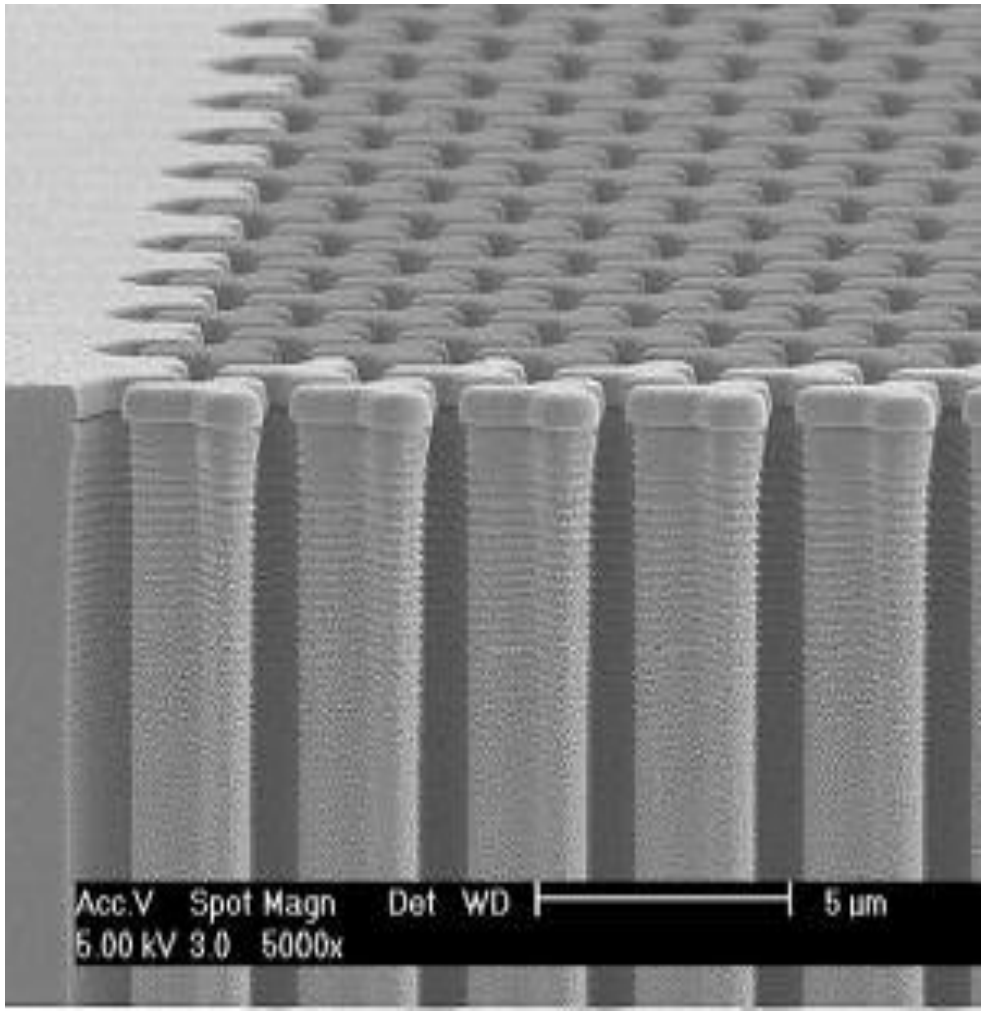
Key features for highly integrated Capacitors

- Increase the effective capacitor surface by etching 3D structures with high aspect ratio.



- Suitable high k material with appropriate deposition techniques
  - High permittivity
  - High breakdown voltage > 10V
  - Low leakage current <1nA/µF
  - Excellent temperature and voltage linearity < 100ppm/°K & < 100ppm/V
  - Failure in Time < 1

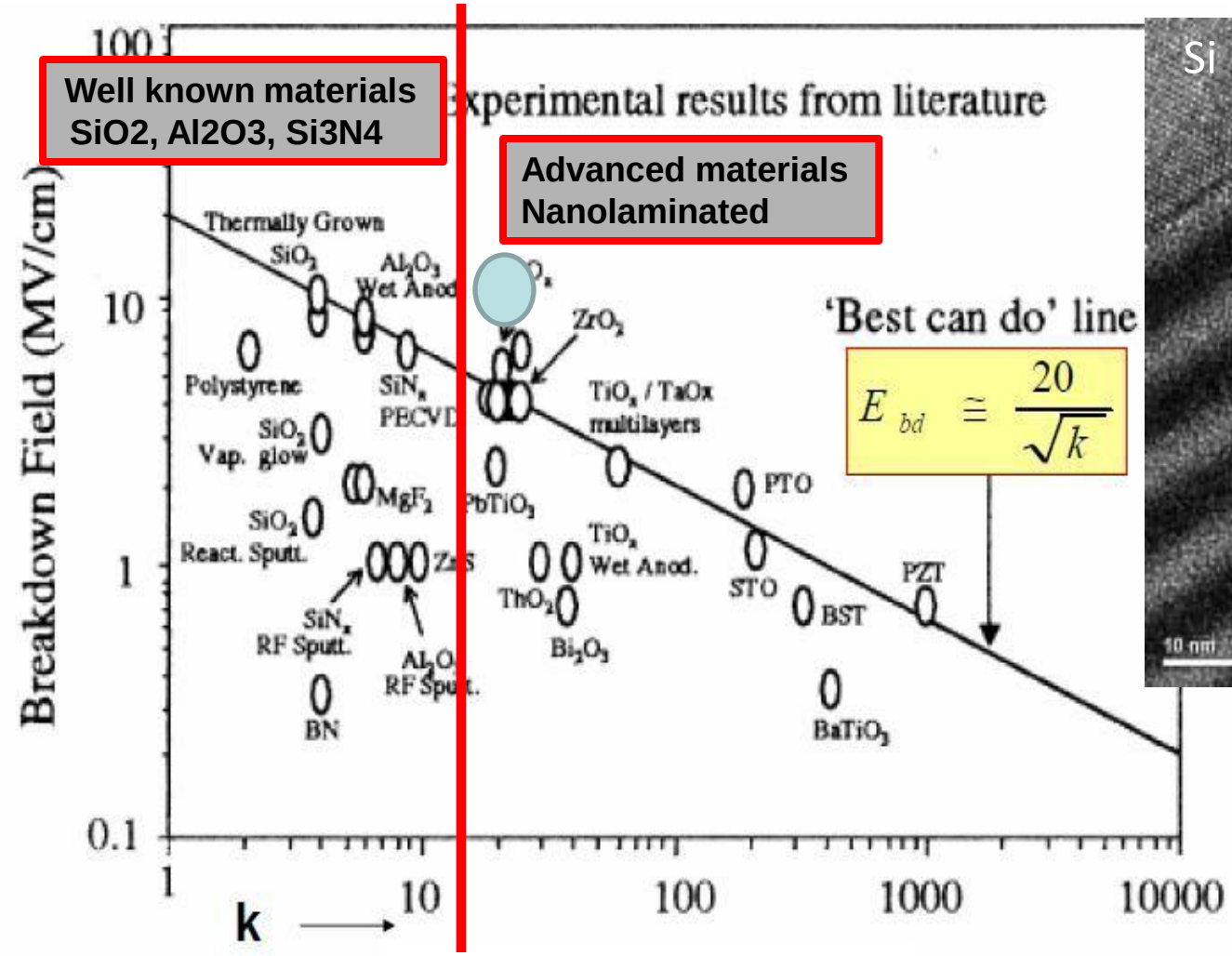
Key features for highly integrated capacitors :The deep Silicon etching

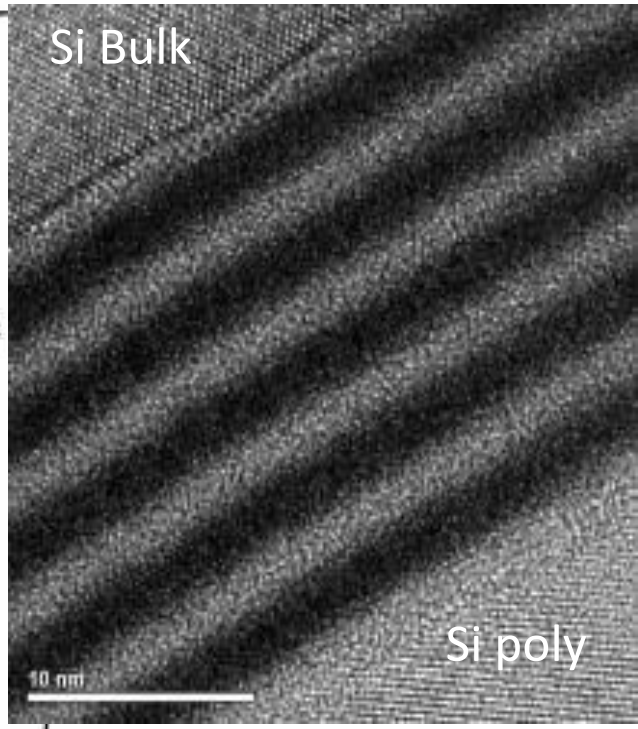


Tripod shape

with Aspect Ratio up to 60

Key features for highly integrated capacitors : The dielectric

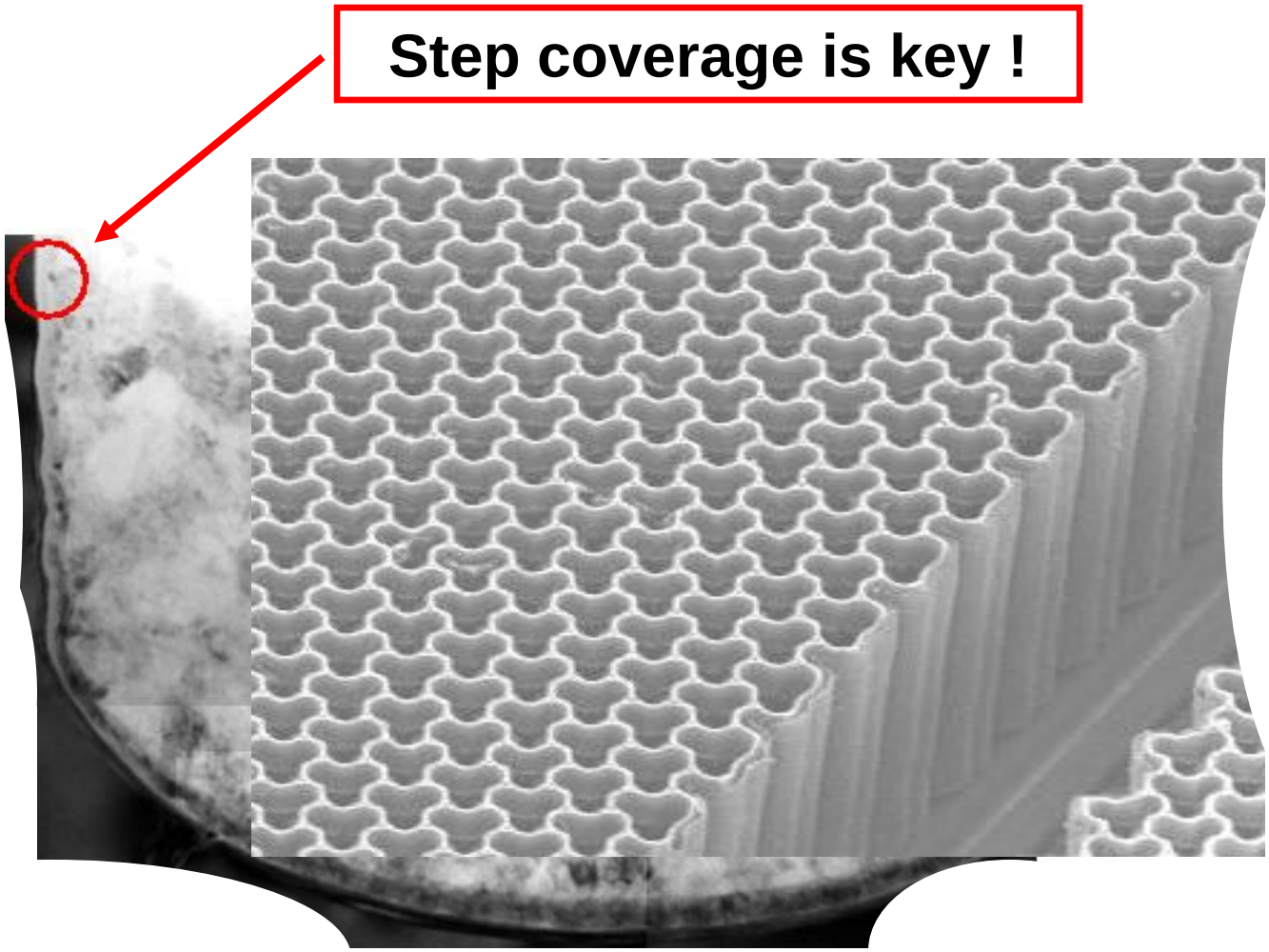




Relative permittivity as a function of Breakdown field

From "Proposed Universal Relationship Between Dielectric Breakdown and Dielectric Constant" – McPherson et Al

Key features for highly integrated capacitors : The dielectric deposition



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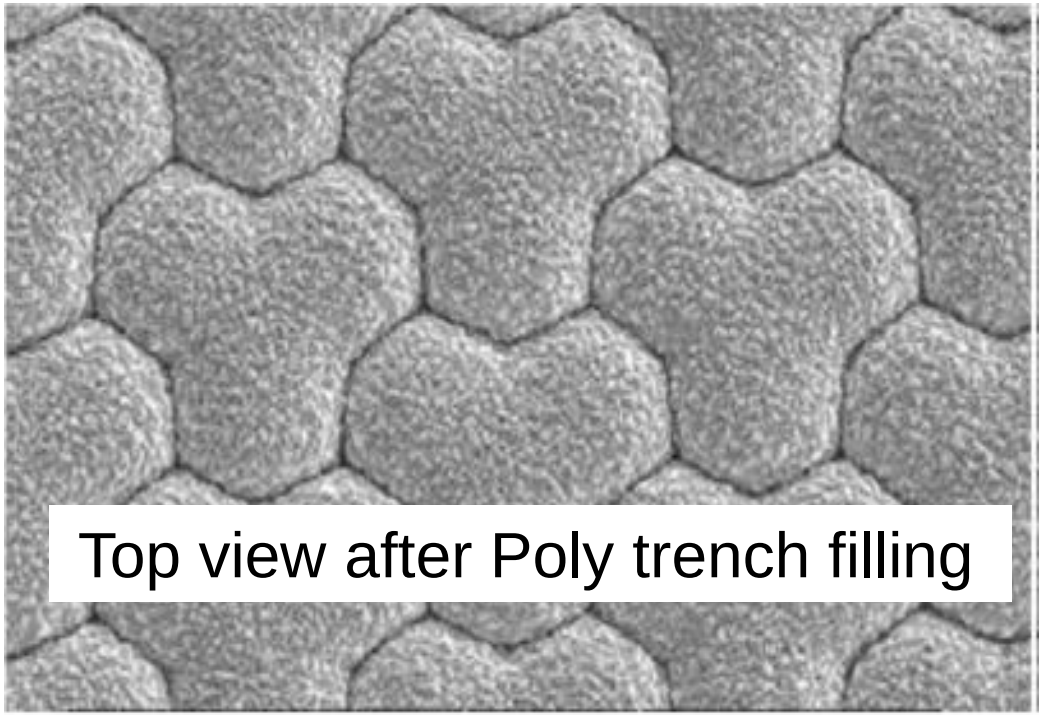
Key features for highly integrated capacitors :

The trenches filling and the thermal budget seen by the 3D structures

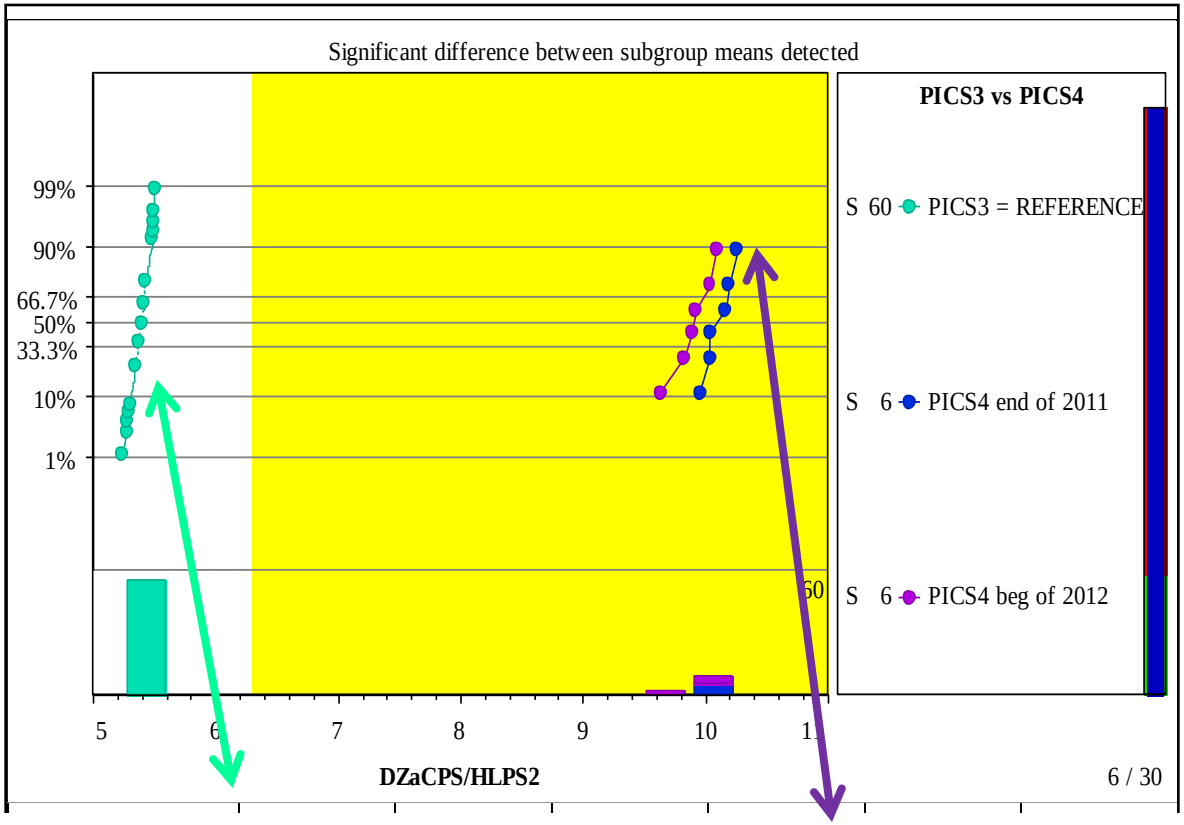


PICS4 characterization

- Batches were characterized at PCM level (Process Control Modules)
- Investigated parameters are those corresponding to leakage through the dielectric, capacitance density and also breakdown voltage for both 2D and 3D capacitors
- Results were obtained from Keithley (raw PCM results).
- Two sets of measurements

PICS4 characterization

2D capacitor densities of the PICS4 wafers compared to a PICS3 reference batch :

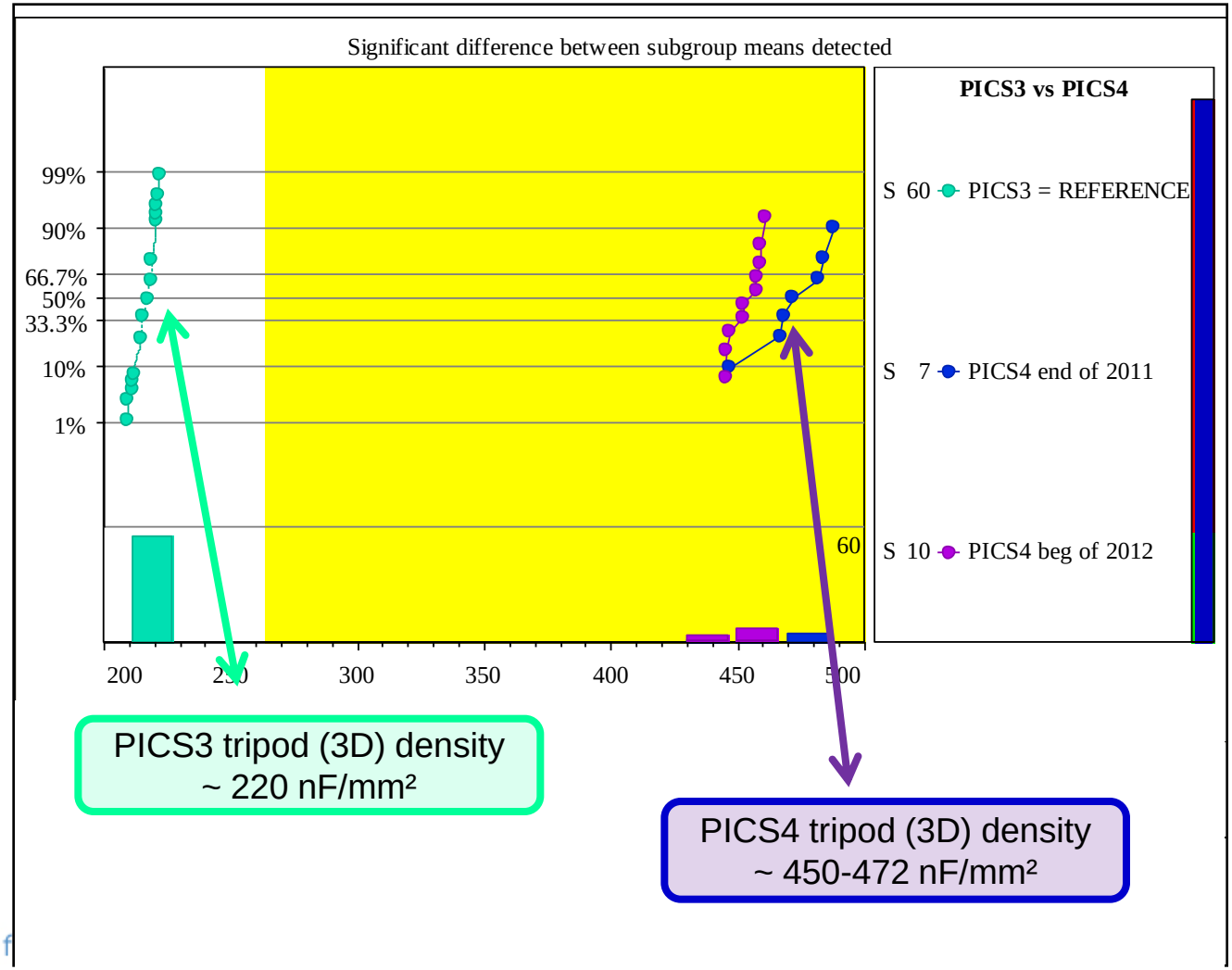


PICS3 planar (2D) density
~ 5.4 nF/mm²

PICS4 planar (2D) density
~ 10.0 nF/mm²

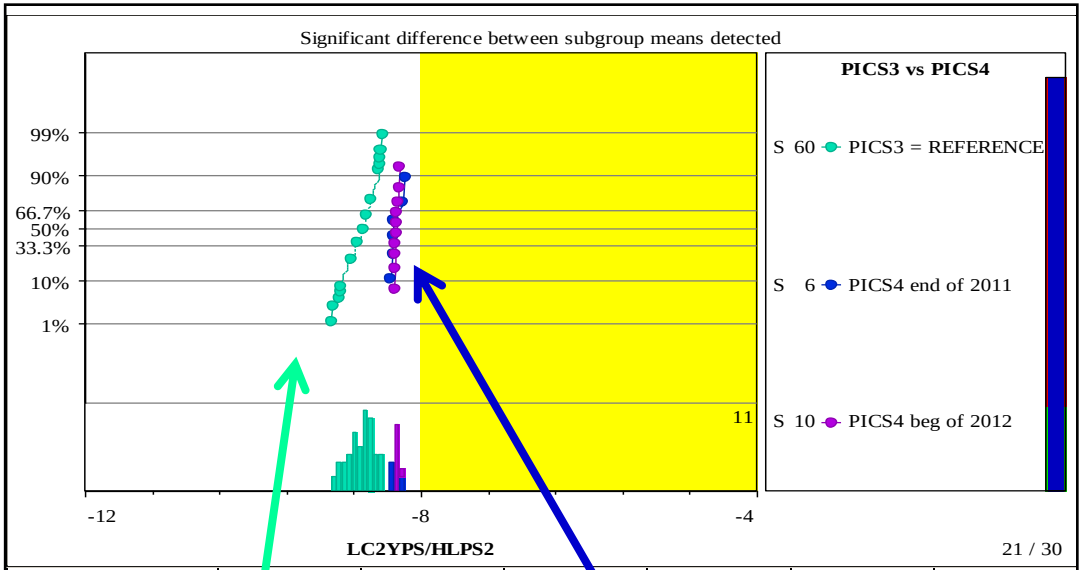
PICS4 characterization

3D capacitor densities of the PICS4 wafers compared to a PICS3 reference batch :



PICS4 characterization

3D capacitor leakage of the PICS4 wafers compared to a PICS3 reference batch :



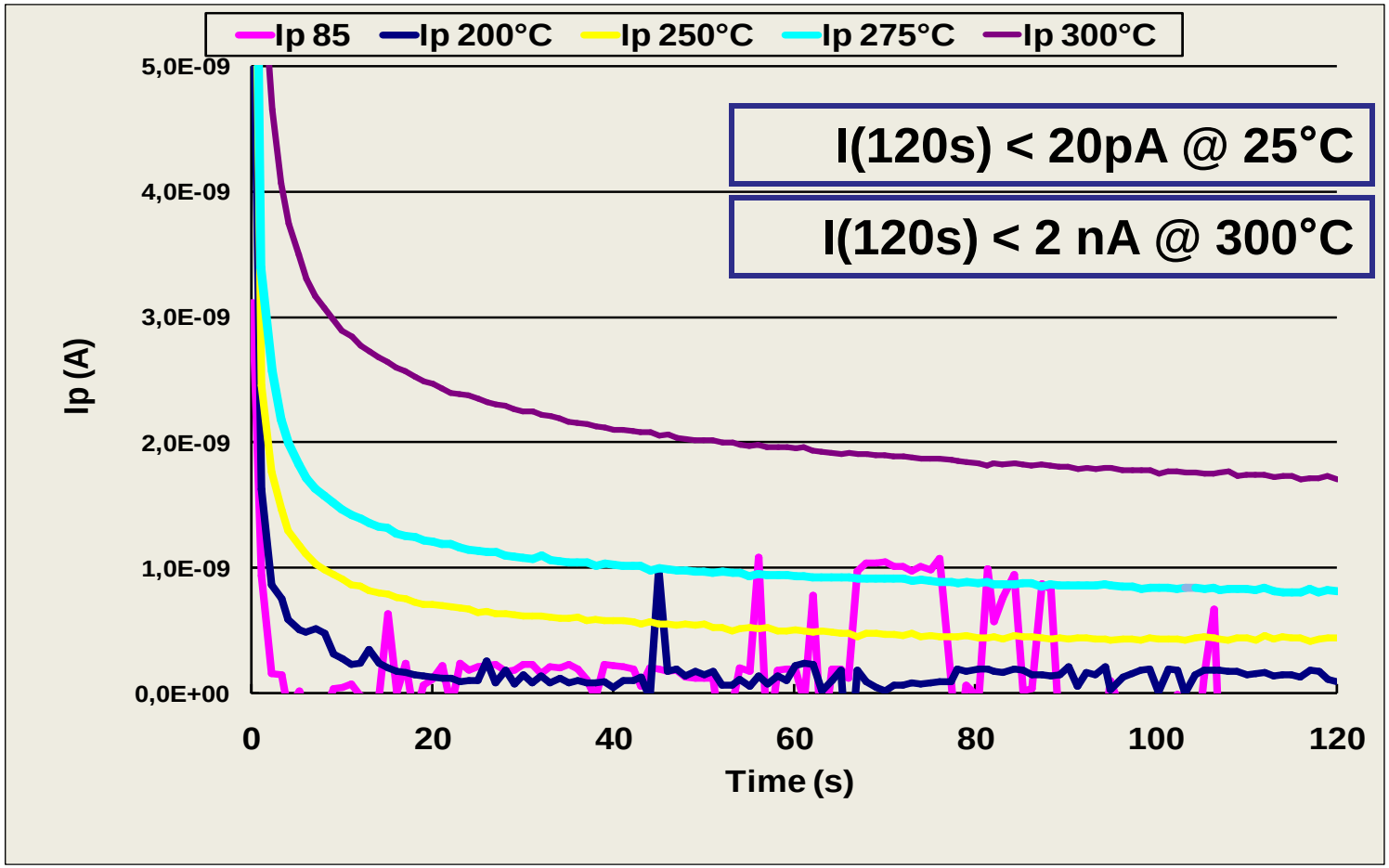
Group	Count	Mean	Std dev	Min	Max	Q2
PICS3 = REFERENCE	60	-8.713	0.154	-9.069	-8.466	-8.689
PICS4 end of 2011	6	-8.295	0.070	-8.359	-8.192	-8.332
PICS4 beg of 2012	10	-8.290	0.022	-8.315	-8.254	-8.290

PICS3 tripod (3D) leakage ~ -8.7 logA

PICS4 tripod (3D) leakage ~ -8.3 logA

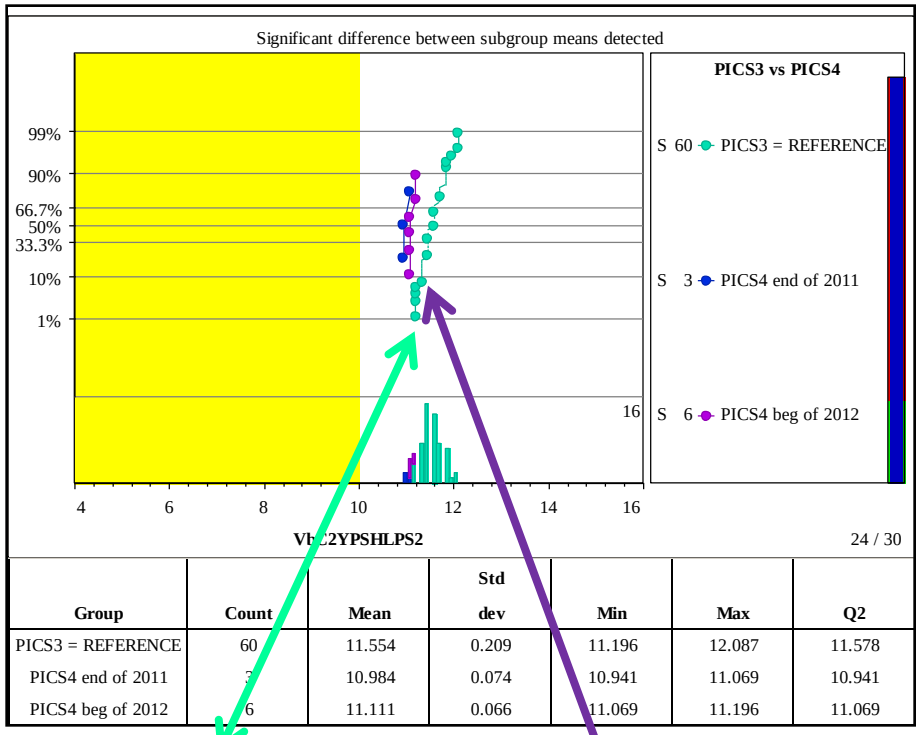
DC leakage current at high Temperature

C= 100nF (Amps @ 3V)



PICS4 characterization

3D (CAPY) capacitor V_{BD} of the PICS4 wafers compared to a PICS3 reference batch :



Group	Count	Mean	Std dev	Min	Max	Q2
PICS3 = REFERENCE	60	11.554	0.209	11.196	12.087	11.578
PICS4 end of 2011	3	10.984	0.074	10.941	11.069	10.941
PICS4 beg of 2012	6	11.111	0.066	11.069	11.196	11.069

PICS3 tripod (3D)
VBD ~ 11.6 V

PICS4 tripod (3D)
VBD ~ 11V

PICS4 characterization

- Capacitance density calculation at PCM level is impacted by the area required to connect to the electrodes.

- As a consequence, PCM densities are lower than the density measured on the products.
- The real capacitance densities are the following :

  - 2D = 11.40nF/mm² in PICS4 (6.15nF/mm² in PICS3 on the ref batch)
  - 3D = 542.44nF/mm² in PICS4 (243.96nF/mm² in PICS3 on the ref batch)

PICS
High Voltage

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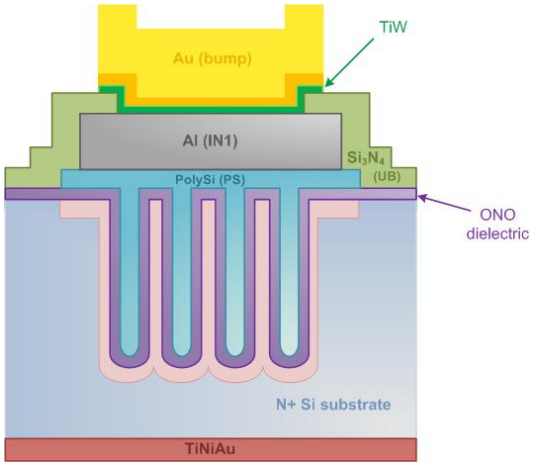
PICS High Voltage

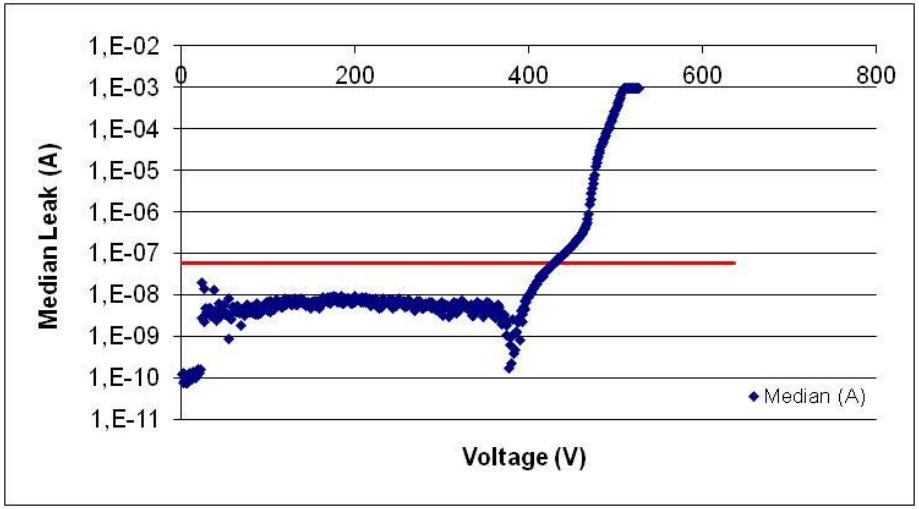
Larger pores to introduce a thicker dielectric

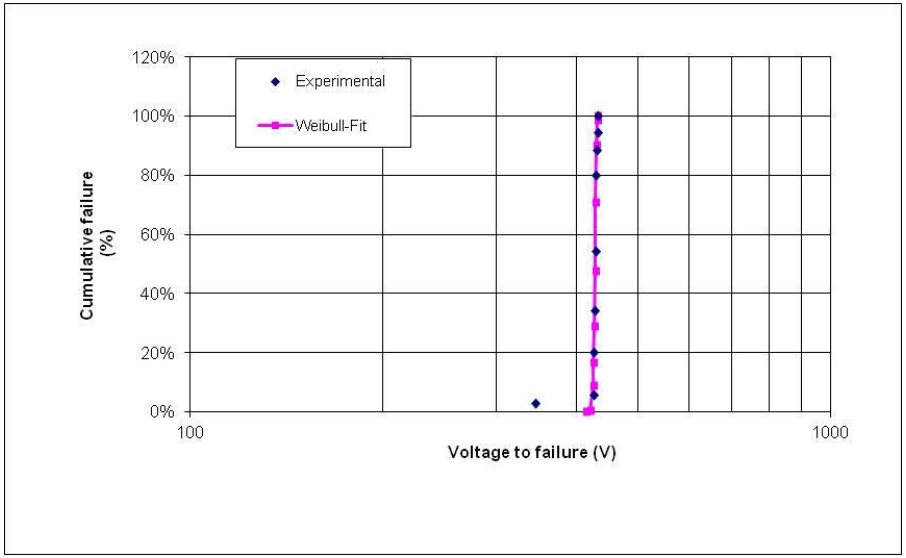
Deeper pores to keep high capacitance density

C=1.35nF/mm^2



Vuse = 421 V (0.1% cumulative failure) at room temperature





Examples of application

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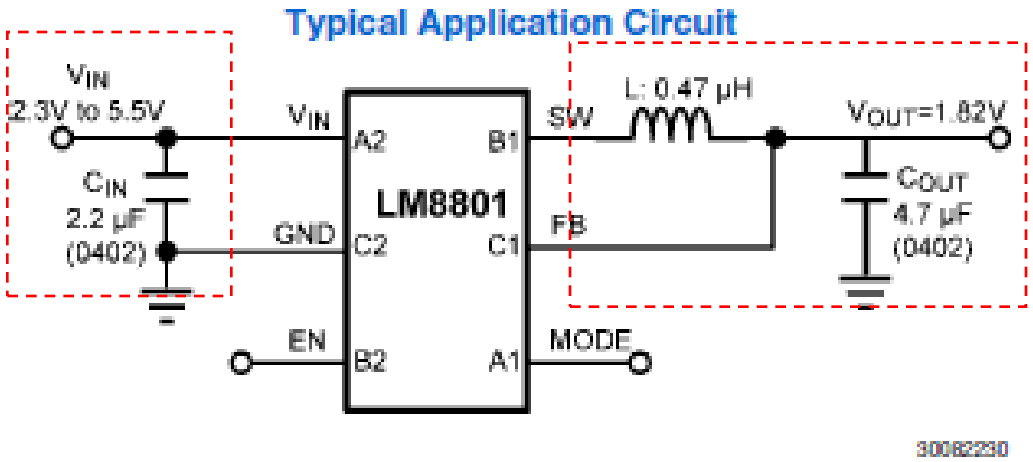
DCDC converter
LM8801 overview*

* Courtesy NationalSemi. see application brochure for details



Inductor

- •Current rating steady = 600mA
- •Current rating max ~ 900mA
- •ESR <=100mOhm
- •L >= 300nH

Capacitors

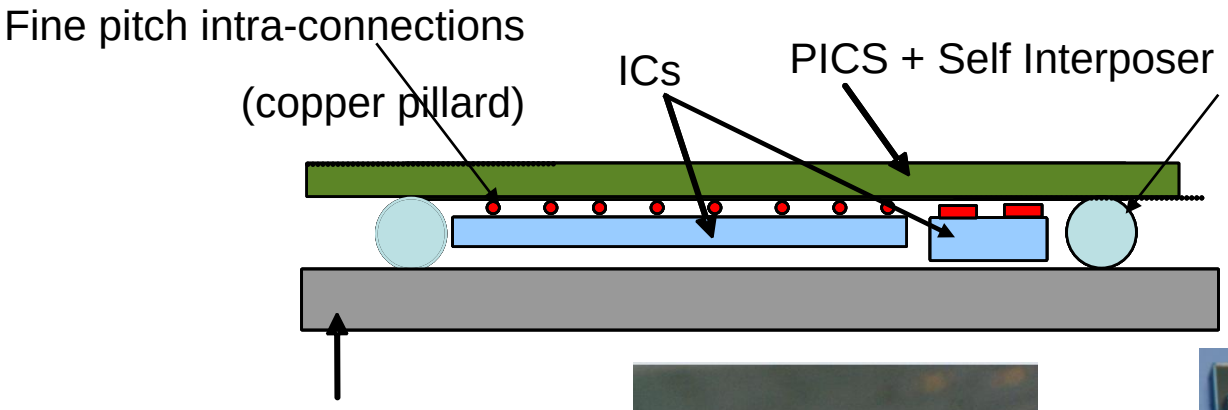
- • ESR <=100mOhm
- • Cout = 4.7µF
- • Cin = 2.2µF
- • Absolute Max rating = 6.3V
- • Typ rating = 3.6V

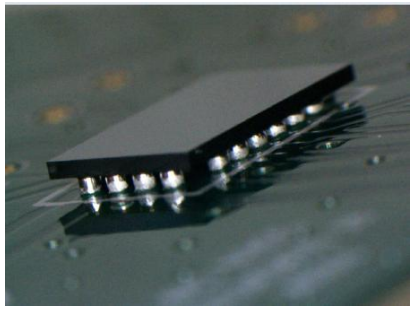
Small footprint : min 4.8 x 4.8 mm

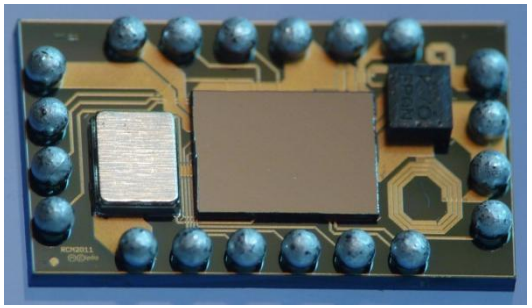
Ultra low profile : 0.35

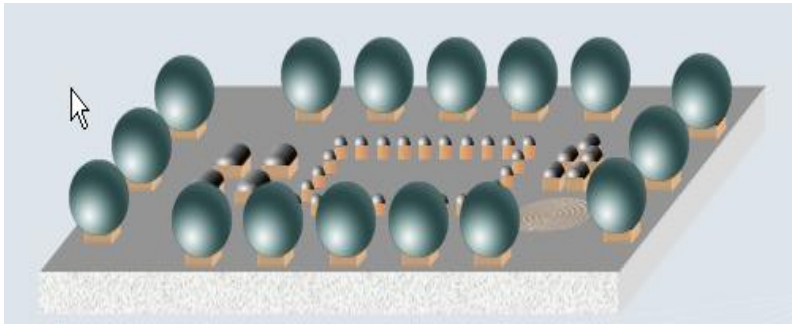
Several assembly options : WLCSP or FlipChip

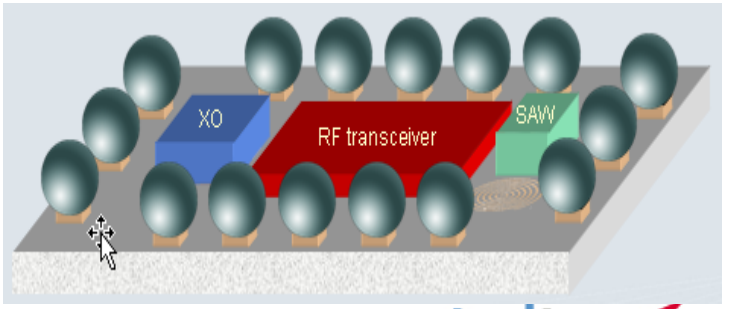
Integration capabilities with PICS











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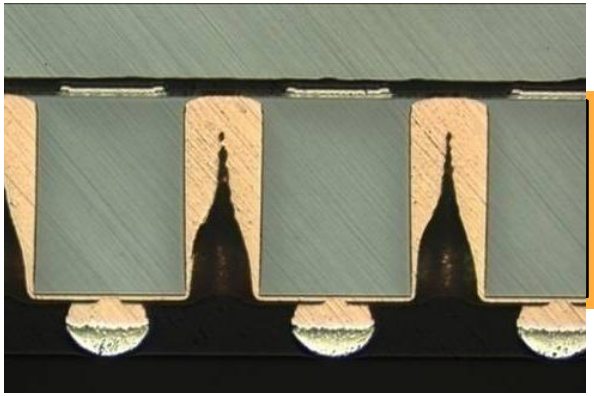
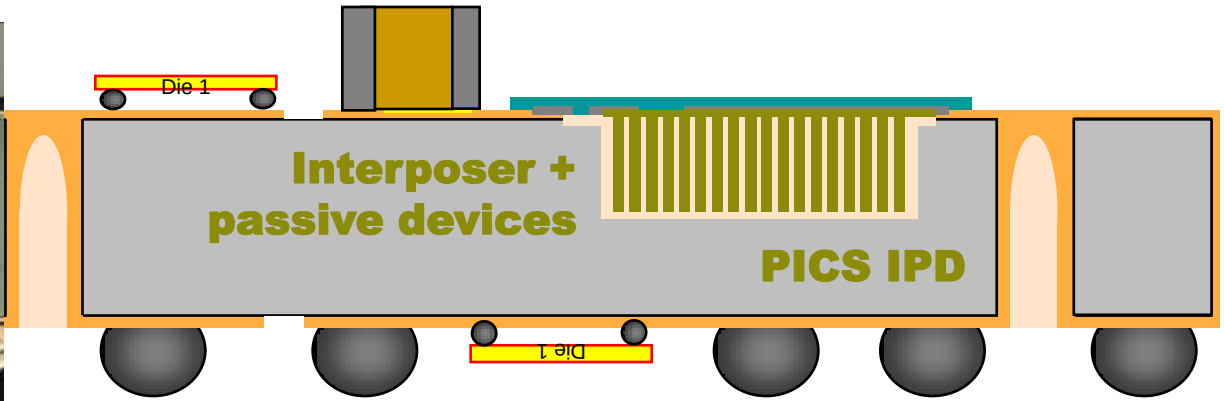
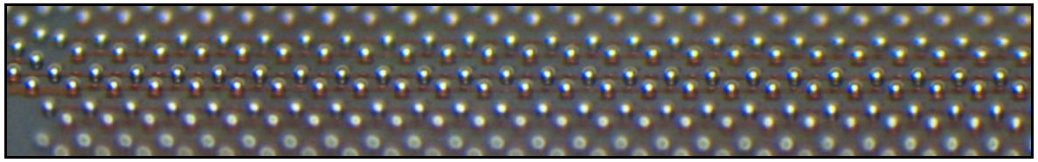
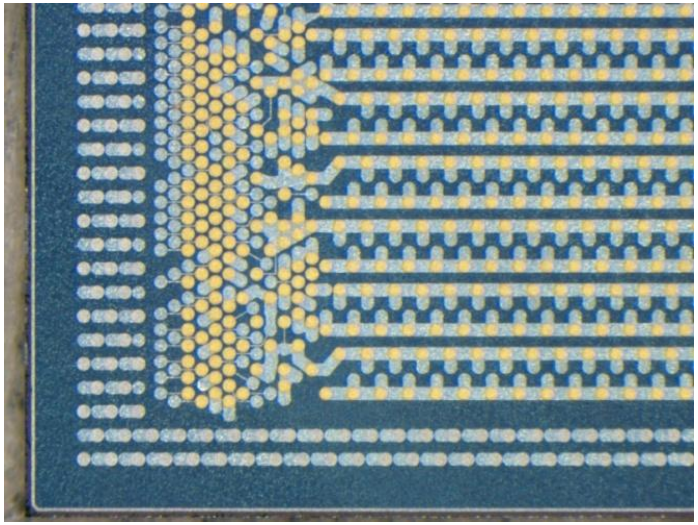
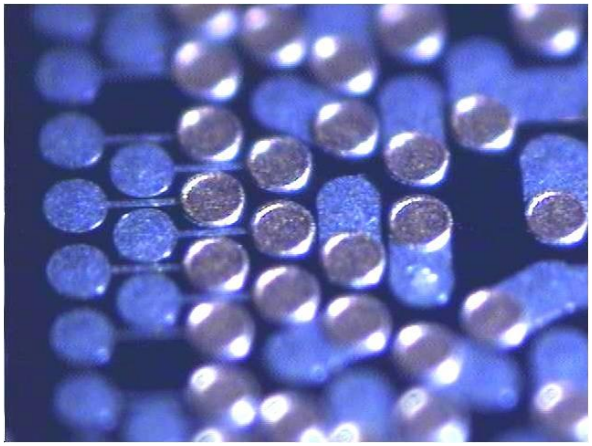
Through Silicon Vias

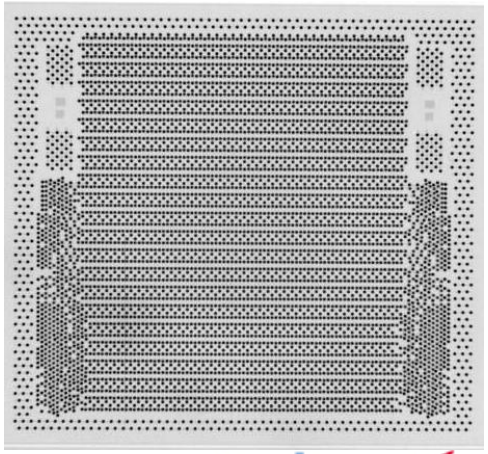












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Conclusion

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Conclusion

IPDIA 3D Silicon Capacitor is offering many advantages :

- ✓ High capability of integration, low profile
- ✓ Very high stability with an outstanding behaviour at 250°C
- ✓ Extremely low failure rate .No burn-in test .
- ✓ Ultra Low leakage .
- ✓ High quality manufacturing process
- ✓ High flexibility

Coming soon : higher integration in the power system management thanks to higher Capacitor density !

www.ipdia.com