Integration of Power-Supply Capacitors with Ultrahigh Density on Silicon Using Particulate Electrodes

POWERSOC 2012

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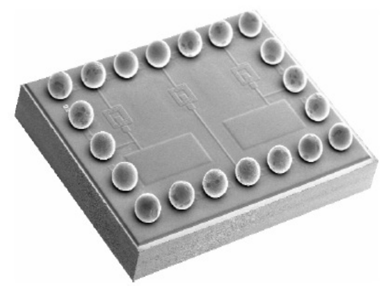
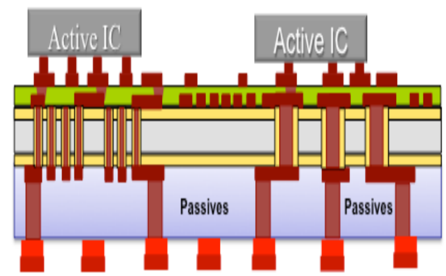
Outline

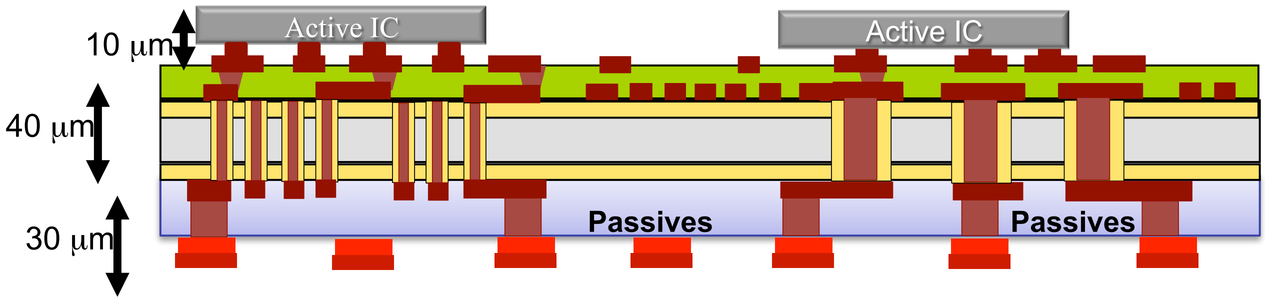
- Component integration using 3D IPAC Concept
- 3D IPAC goals
- Applications
  - VRM and decoupling
    - Thinfilm decoupling capacitors
  - Power convertor
    - High-density capacitors

Passives Trend

Discretes	Array of Discretes	Silicon and Glass IPDs	3D IPAC
			
500 microns (0402)	500 microns (0402)	400-500 microns	40 microns
Thick Devices 500-800 microns	Thick Devices 500-800 microns	200-800 microns	40-100 microns

Courtesy: Kemet, Fraunhofer IZM

What is 3D IPAC Concept and Why?



1. Ultra-thin Glass Core ~ 30 μm

2. Low Loss

3. Fine-pitch and coarse-pitch through-package vias

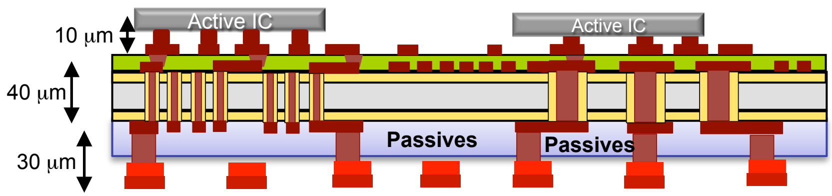
4. Passive components on both sides of glass.
    - RF capacitors, inductors
    - Power supply capacitors and inductors
    - Decoupling Capacitors
    - Precision components

5. Active components for power, digital, RF and Analog

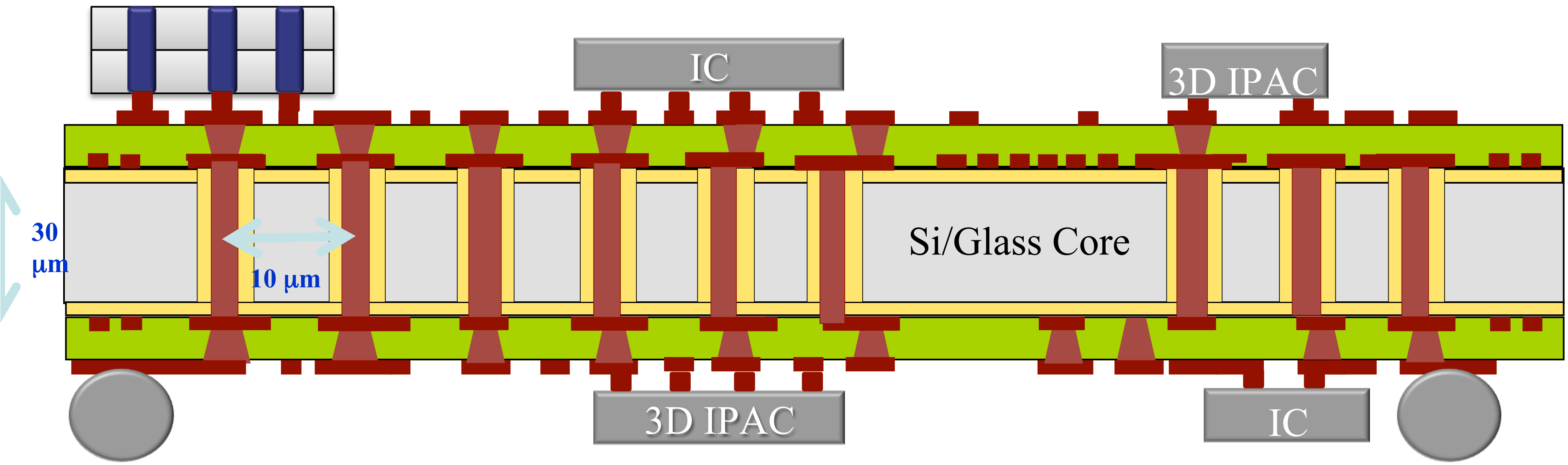
6. Interconnections

3D IPAC is a functional module

3D IPAC on Interposer



3D IC



Thin 3D IPAC Capacitor

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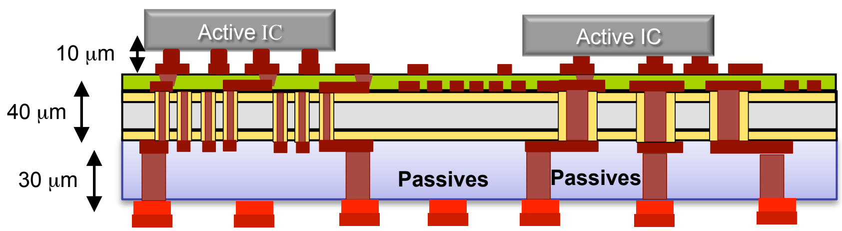
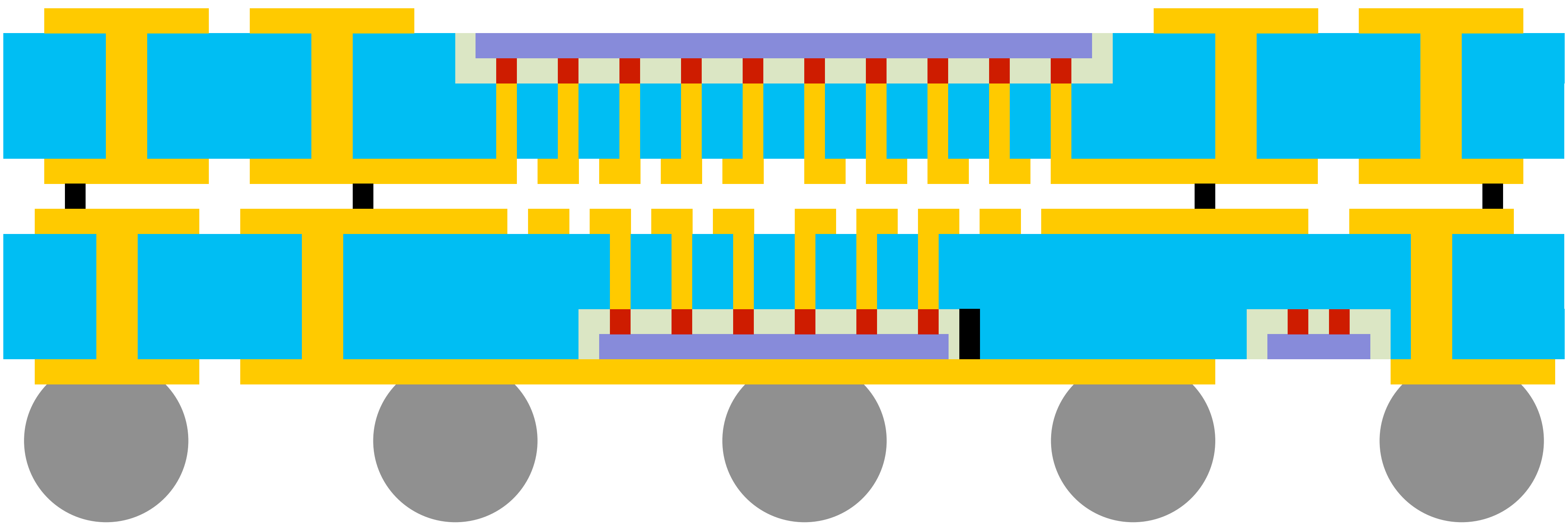
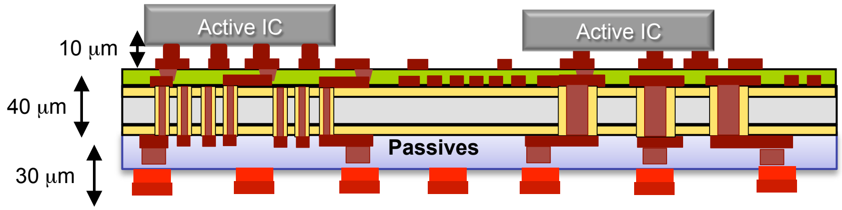
3D IPAC in the 3D POP





3D IPAC on PWB



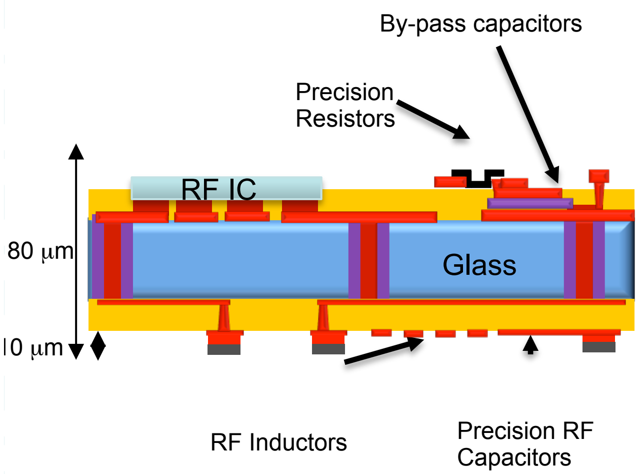
PWB

Goals of 3D IPAC

- Miniaturization:
  - 5X reduction in thickness
- Cost:
  - 2—5X reduction in cost
- Performance:
  - Higher bandwidth at lower power compared to today's systems
- Functionality:
  - Double-side component integration for heterogeneous functions in an ultrathin module

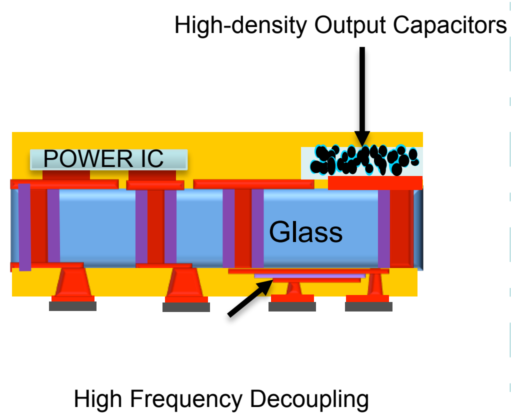
3D IPAC – Applications

RF MODULE



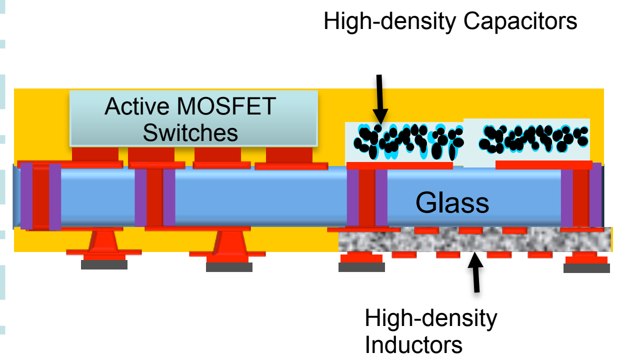
- RF ICs
- High Q and Precision Components:
  - Capacitors
  - Resistors
  - Inductors

PDN Module



- Voltage regulator module
- VRM output capacitors
- Decoupling capacitors

Power Convertor Module



- Power switches
- High-density capacitor
- High-density inductor

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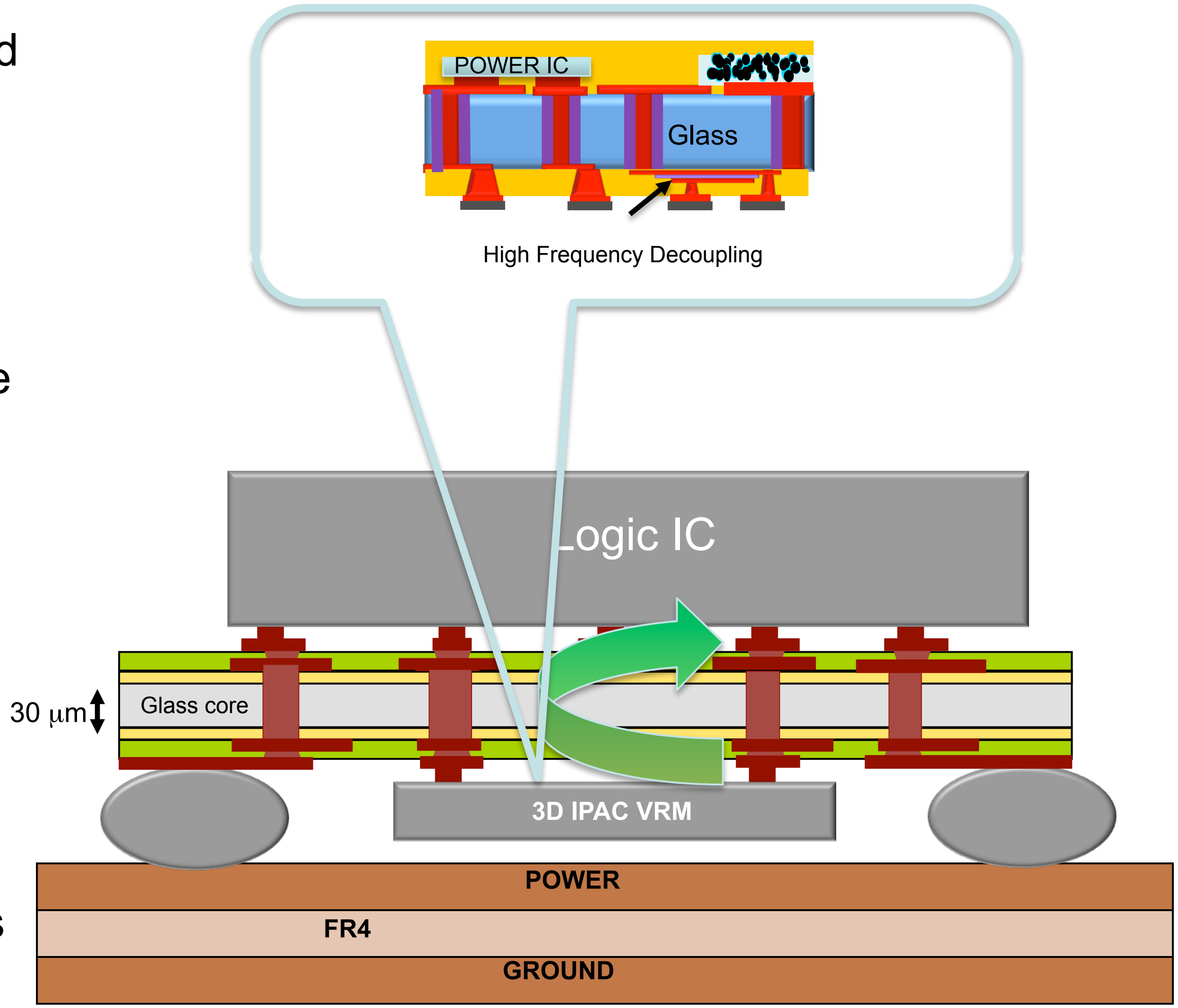
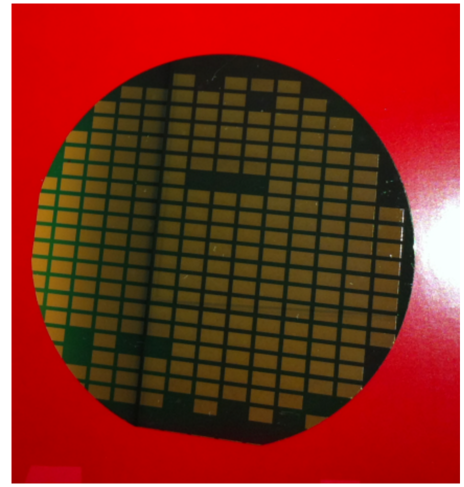
3D IPAC – PDN Module

- Improved power integrity for 3D ICs and packages with thinner packages
- VRM and decoupling functions in the interposer, close to the package
- Reduces the number of decoupling capacitors
- Thin power ICs (ex. MOSFET switches)
- High-density inductors
- High-density capacitors



Sputtered BST Thinfilm Capacitors

- Thinfilms (100-300 nm):
  - Thinner films (Barium Strontium Titanate);
  - Faster crystallization;
  - Higher capacitance density of 14 nF/mm^2

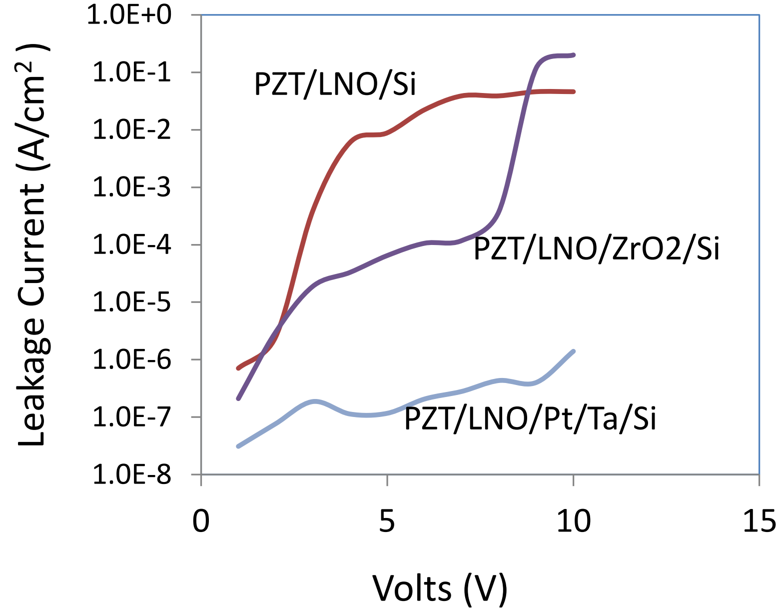


Key Result BST on Si/SiN/Ta/Ni	
BST sputtering	Ar/O_2 (60% O_2); 100 W; 2.5 hrs
Annealing conditions	750 C, 30 min in N2
Capacitance density	9 – 11 nF/mm2
Higher yield with large area electrodes	220 nF achieved on 0.28 cm2
Leakage current of the order	μA/cm^2 achieved up to 3 V (4 nF/mm^2)
Yield	85% (30/35 devices yielded)

Solgel PZT –Thinfilm Capacitors

2.5 μF/cm2 (1 V)

1 μF/cm2 (10 V)



1.2 x 2.5mm^2:	100-110 nF, loss 0.1-0.3	Yield 51% (56/110)
2.9 x 2.5mm^2:	225 nF, loss 0.4-1.2	yield 14% (8/57)

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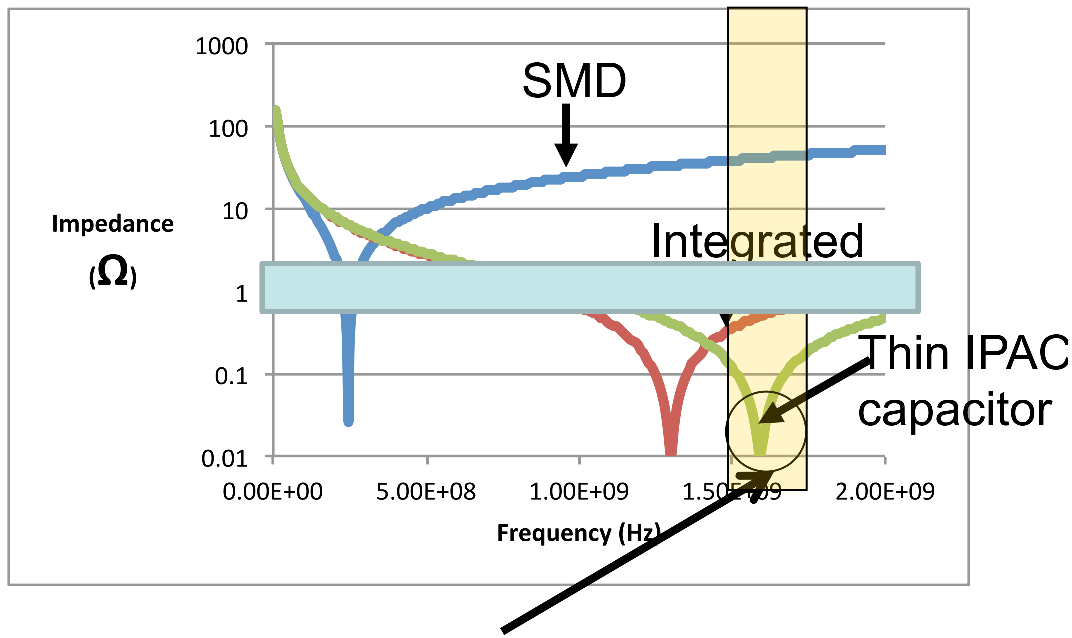
3D IPAC-Based PDN

- Three decoupling capacitor integration scenarios were modeled
  - SMD on board shows highest parasitics and lowest performance;
    - Requires excessive on-chip decoupling
  - ThinFilm integration in today's packages can achieve higher frequency stability, but has limited manufacturability
  - IPAC micro-assembled close to IC shows best performance because of thin interposer and short bump parasitics;

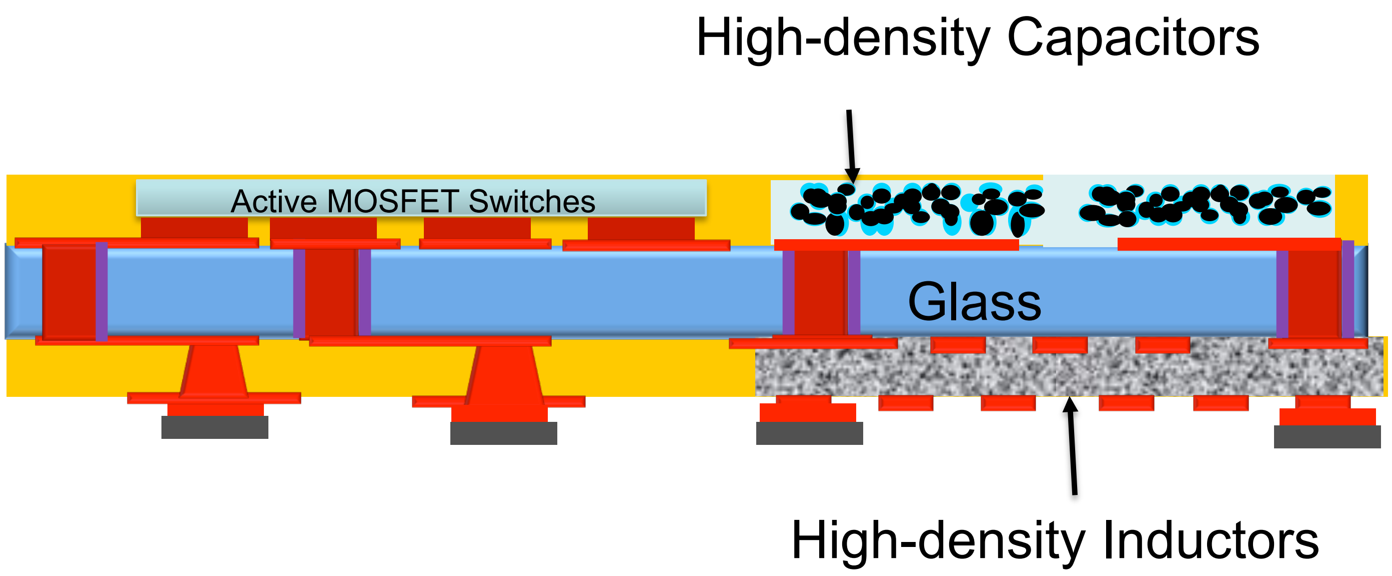


5X improvement in frequency performance with the proposed 3D IPAC strategy

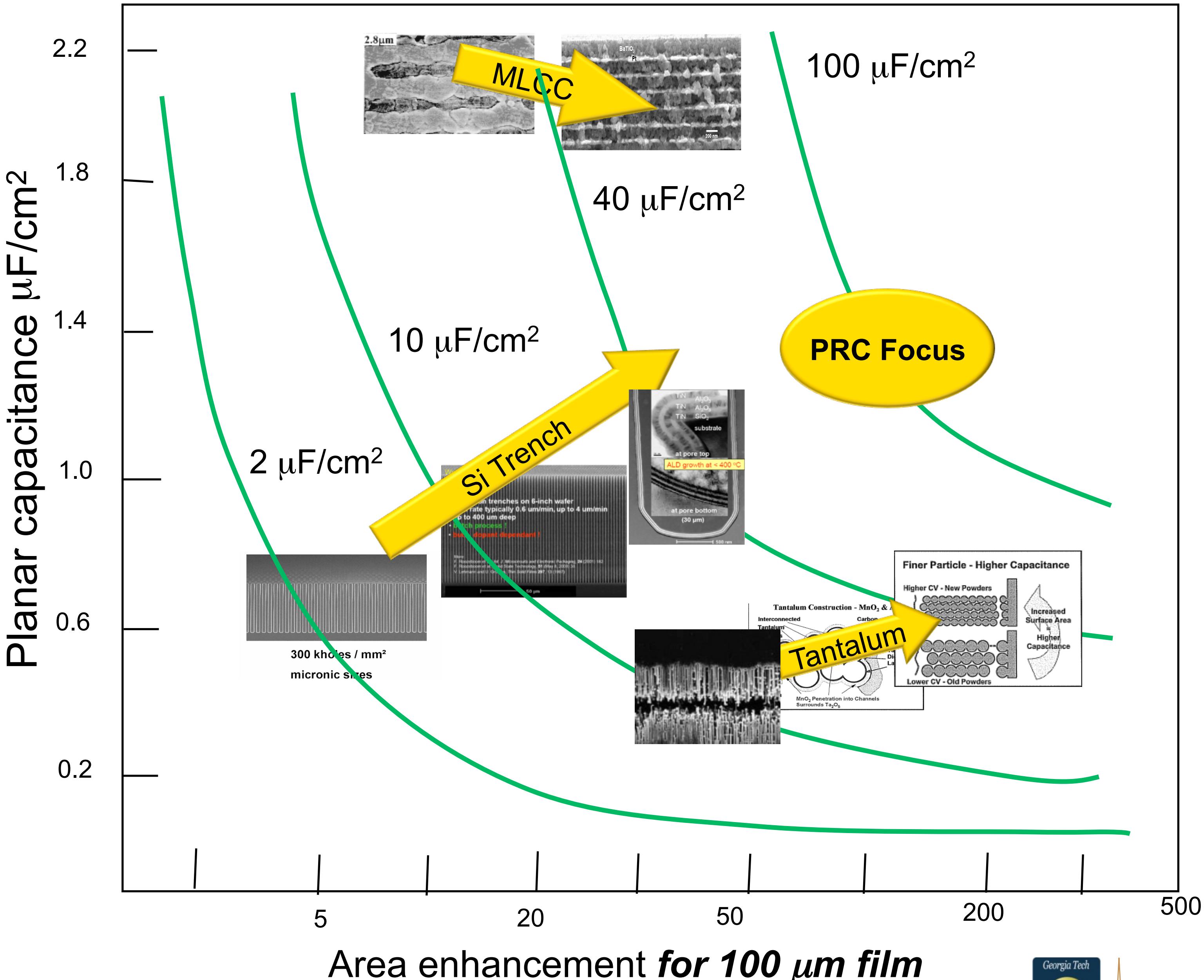
3D IPAC – Power Converter Module

Power Module:

- Switching regulator or charge-pump based
- Thin power ICs
- High-density inductors
- High-density capacitors

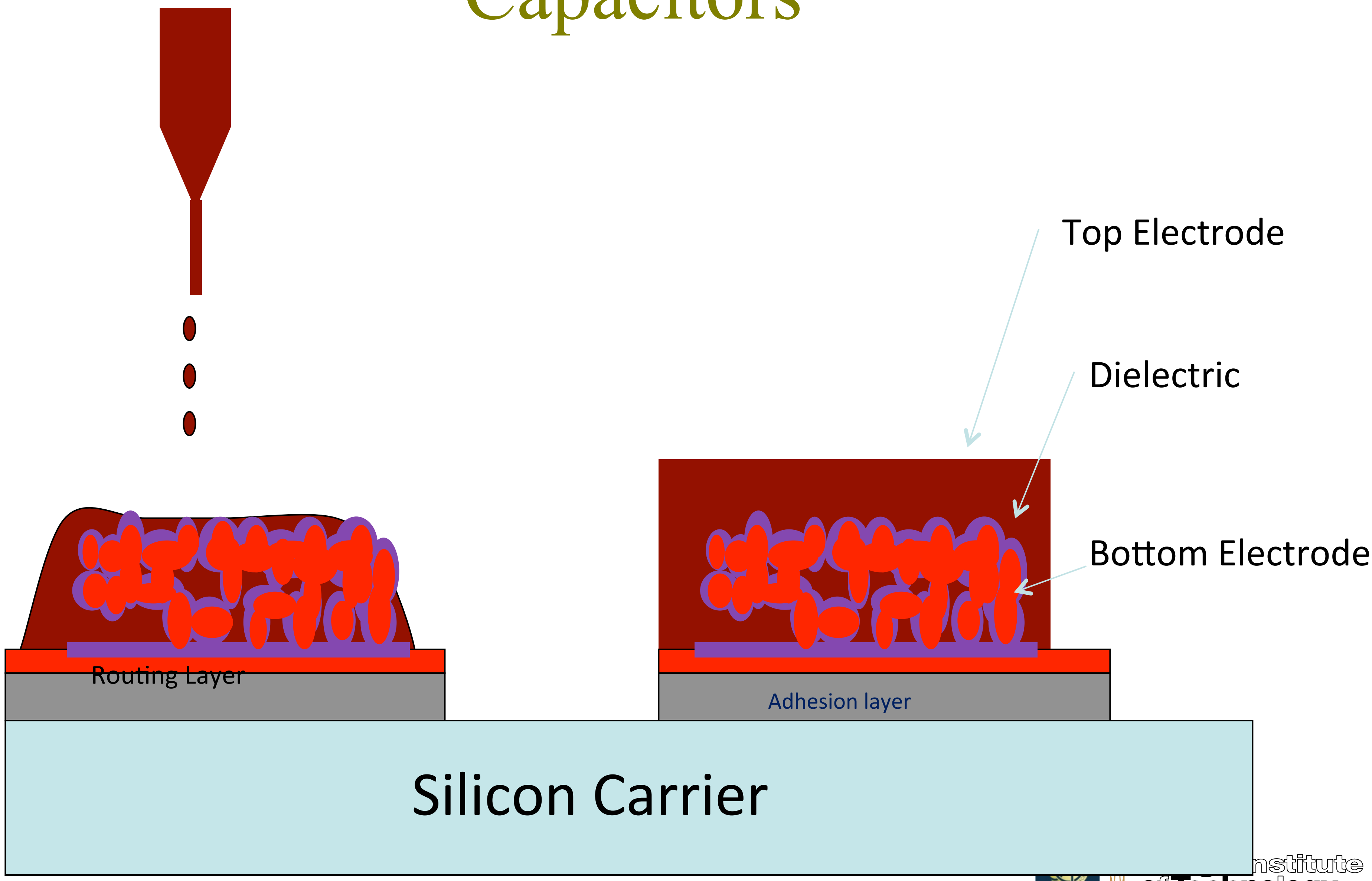


High-Density Capacitors



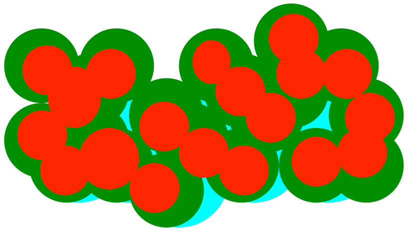
Planar capacitance µF/cm2
2.2
1.8
1.4
1.0
0.6
0.2
5
20
50
200
500
Area enhancement for 100 µm film
100 µF/cm2
40 µF/cm2
10 µF/cm2
2 µF/cm2
MLCC
Si Trench
Tantalum
PRC Focus
300 kholes / mm²
micronic sizes
Finer Particle - Higher Capacitance
Higher CV - New Powders
Increased Surface Area
Higher Capacitance
Lower CV - Old Powders
at pore top
ALD growth at < 400 °C
at pore bottom
substrate

Process flow for High-Density Capacitors



Porous Electrode with Highest Surface Area Efficiency

Silicon Trench vs. Copper Particulate Electrode



Silicon Compatible

100 X enhancement in area

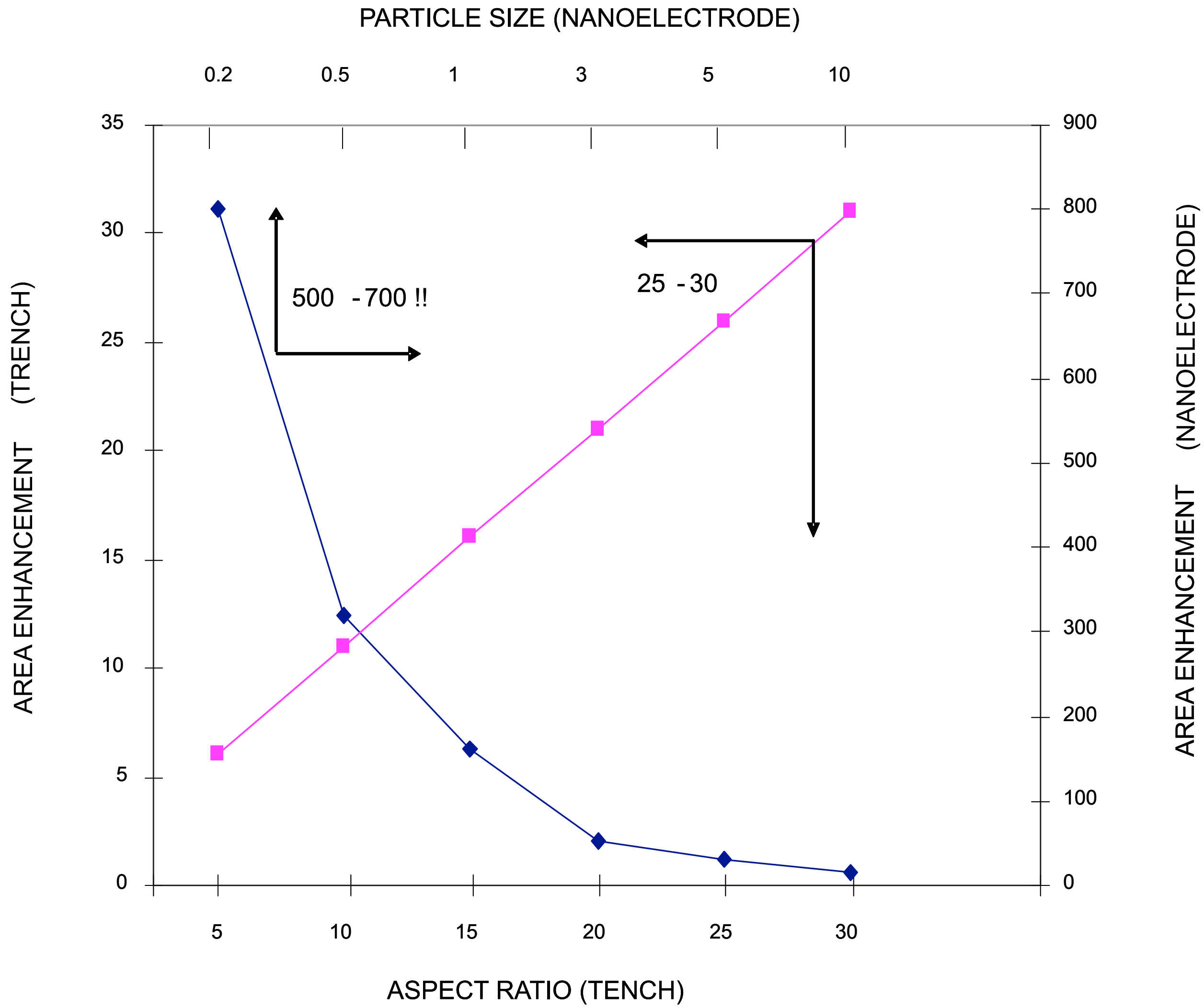
Expensive silicon micromachining tools

Silicon Compatible

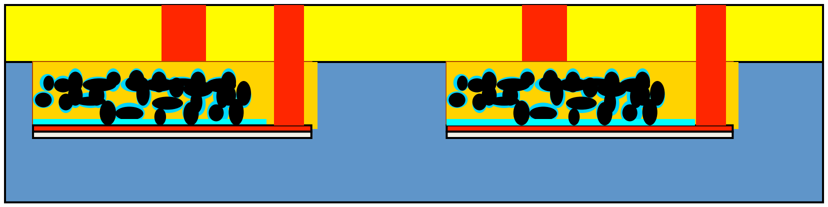
Potential for >2000 X enhancement in surface area from BET measurements (100 μm)

Low-cost paste processing

Area Enhancement: Nanoelectrodes Vs Trenches

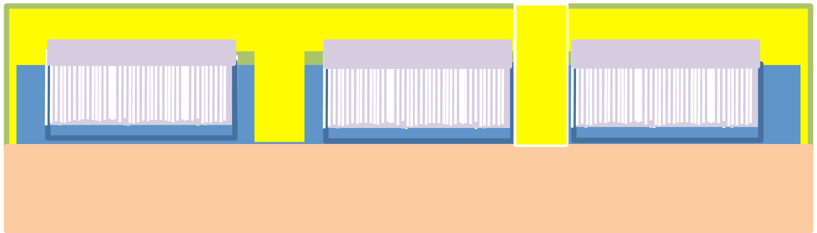


PRC's Background High-Density Capacitor Research

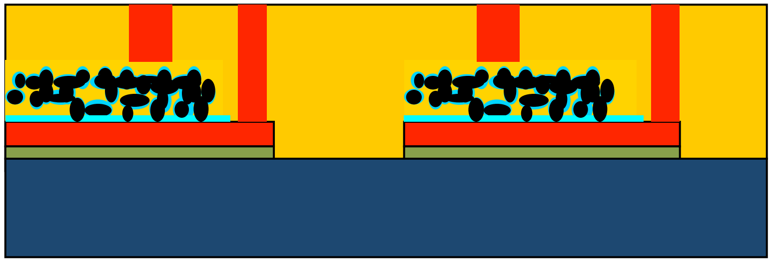


High surface area electrodes on silicon trench;

US 8,084,841 B2



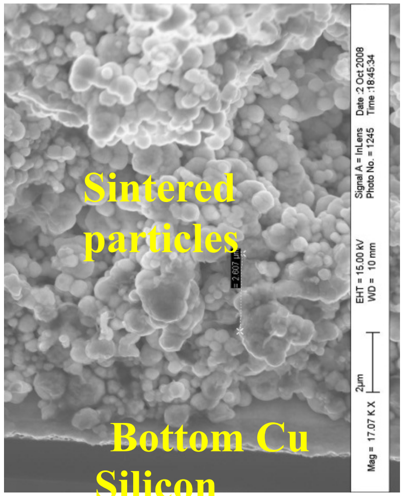
High surface area electrodes on organic substrate with etched foil

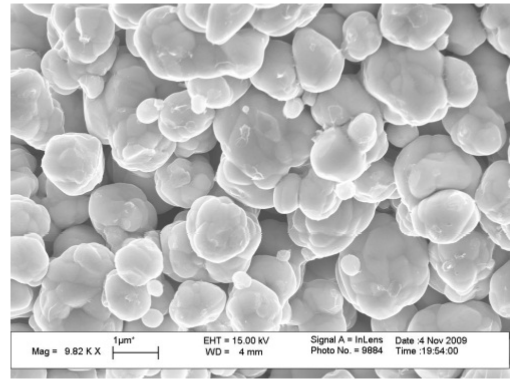


High surface area electrodes on organic substrate with sintered particles

US 8,174,017

Nanoelectrodes on Si





Step 1:

- Copper powder
- Dispersant (Phosphate ester)
- Binder: Propylene carbonate

Step 2:

- Printing on Silicon

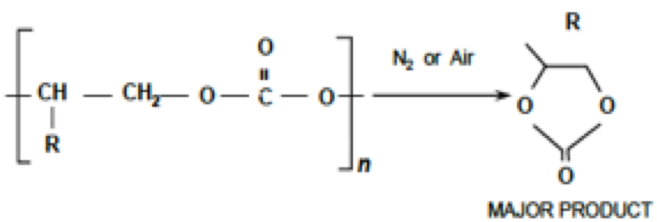
Step 3

- Sintering – 400° C – 600° C

- Copper particle size : 1-2 µm
- High surface area enhancement due to open pores
- 30-40X surface area enhancement for 25 µm film

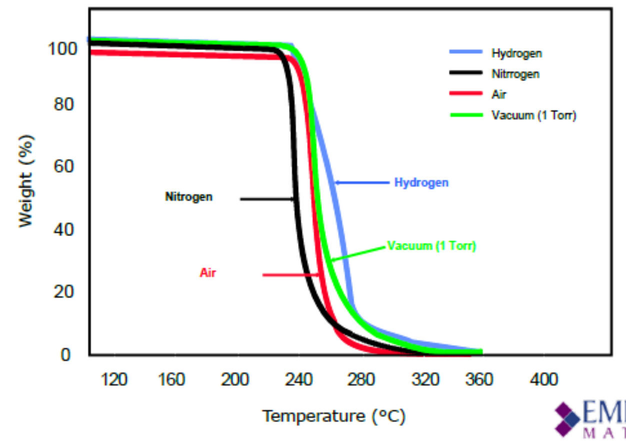
Porous electrode with Sacrificial Polymers

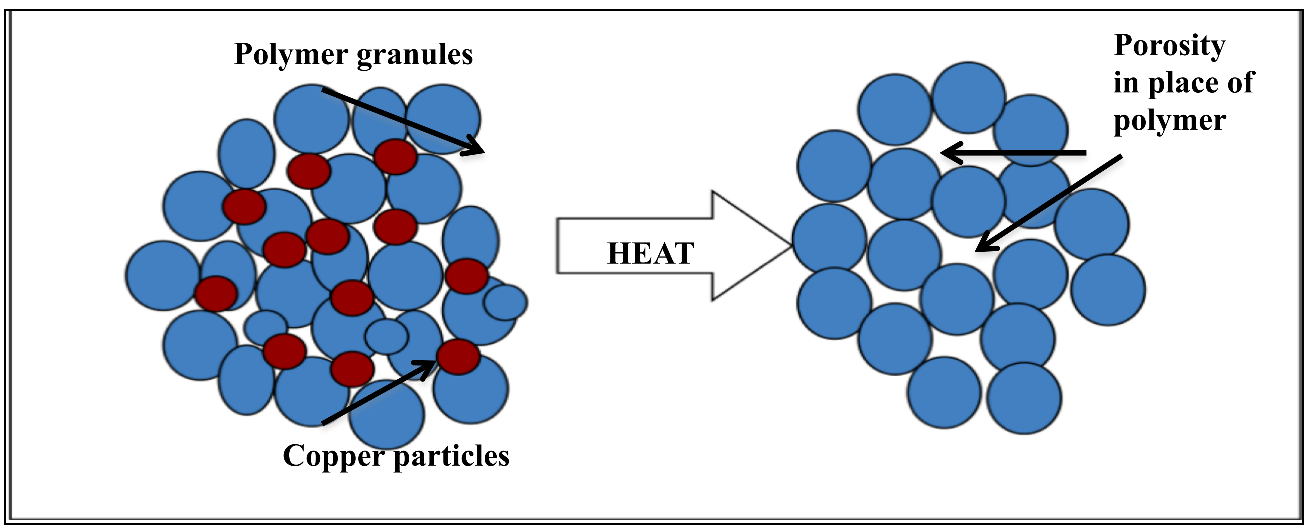
•Using a sacrificial polymer (polypropylene carbonate) that would decompose easily at sintering temperatures in reducing atmosphere



Volatile by-product

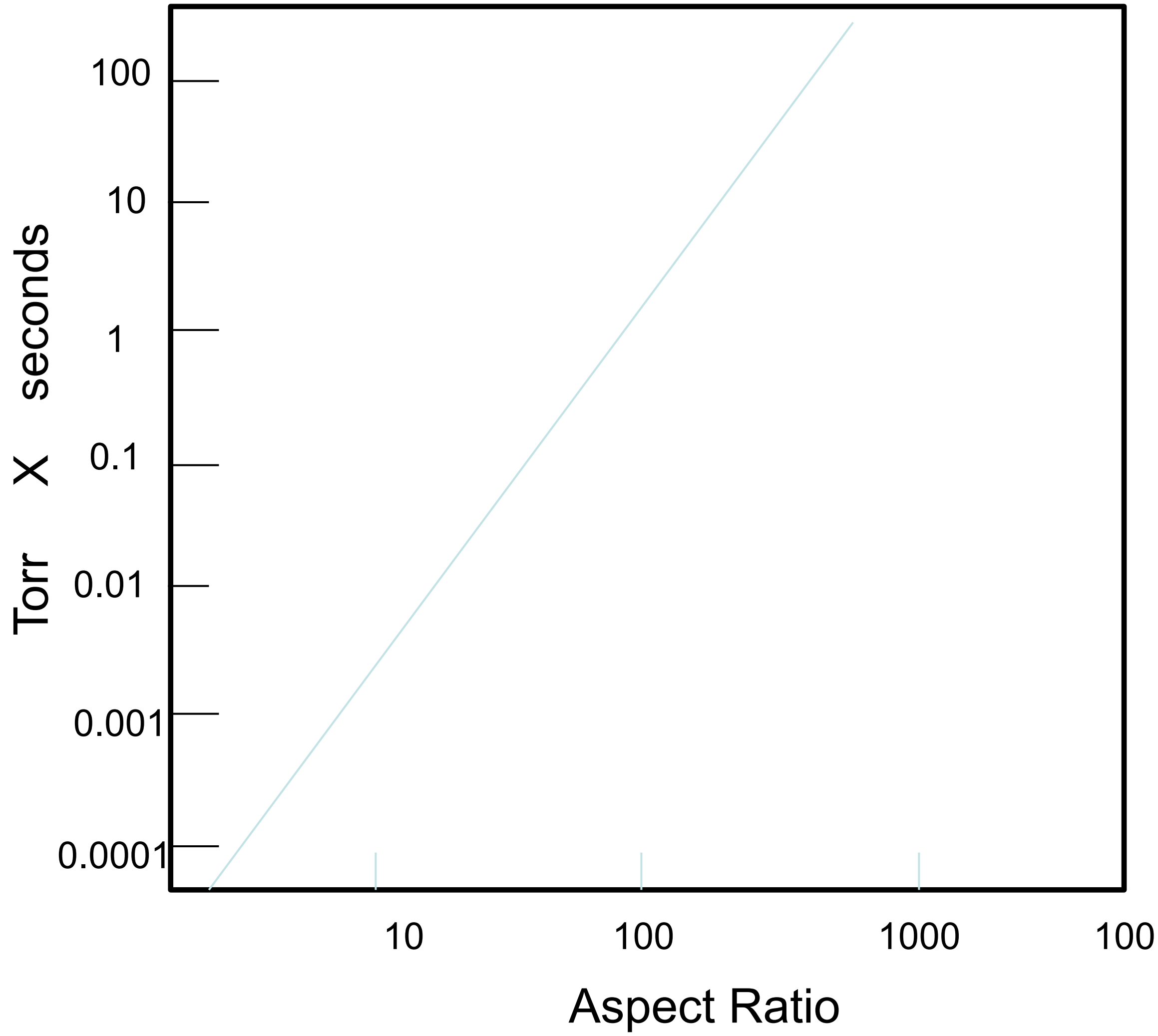
Polypropylene carbonate





ALD Conformality Studies

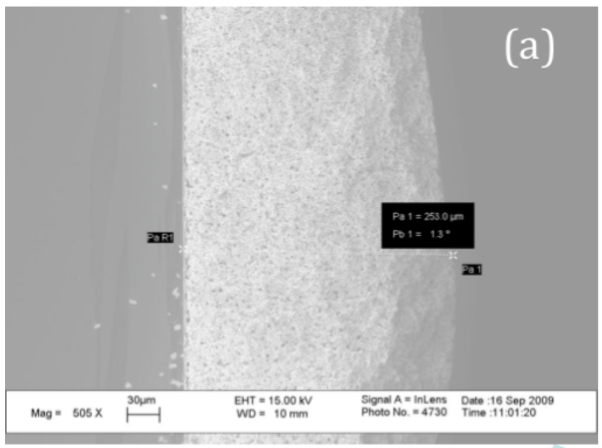
- Increase diffusion time of the ALD vapor
- For aspect ratio of 1000
  - 1 torr: 100 seconds
  - 0.2 torr: 500 seconds
  - Larger than ALD pumpdown time;
  - ALD time can start becoming larger;
- For aspect ratio of 10:
  - Micro to milli seconds;
  - Very small fraction of ALD pumpdown time;
  - no affect on ALD process time;

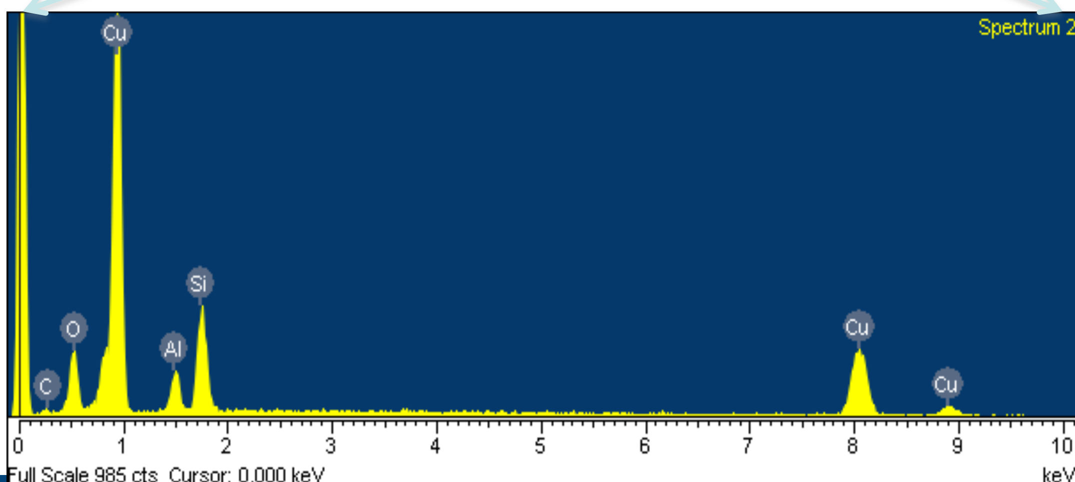


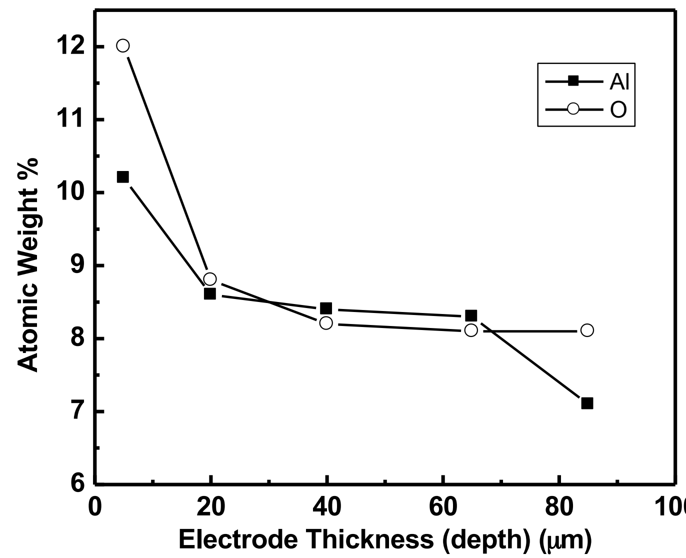
Based on modeling by:
Gordon, Haussman and Kim (Harvard); Shephard (IBM)

Conformality Studies using EDS

EDS Scan at the bottom of 200 um thick electrode



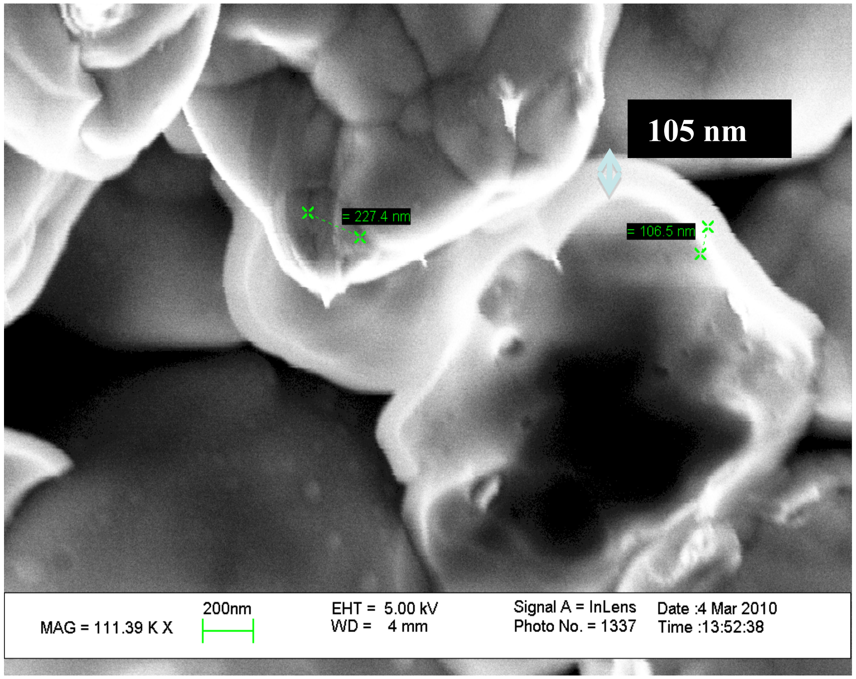




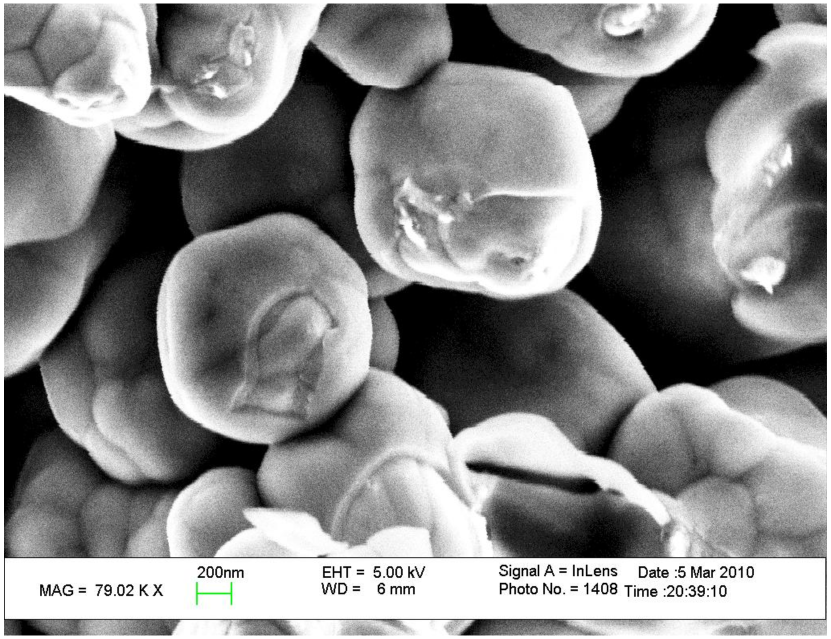
ALD conformality as a function of electrode depth

Conformal Dielectric on Porous Electrodes

- 700 cycles of ALD alumina (~ 100 nm)
- FESEM showed 105 nm thick Alumina film on copper particle necks



Cross-section of sintered bottom electrode showing ALD alumina layer



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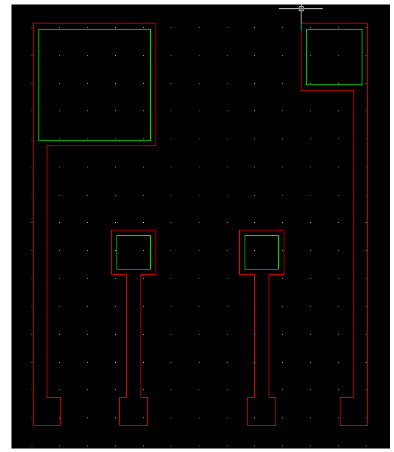
Conformal Top Electrode

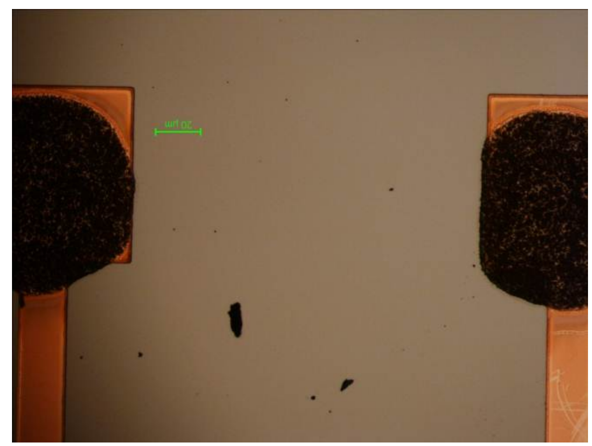
<u>Key Challenge</u>: To access the high surface area by using a conformal top electrode

<u>Approach</u> : Use of a liquid conducting polymer– polyethylene dioxythiophene (PEDT)

<u>Polymerization</u>: EDT+ oxidizer+ inhibitor – 1:25 (in-situ)



- Conductivity ~ 100 S/cm
- Fluid nature with low viscosity for easy infiltration of particulate electrode
- Low temperature processability (50^{o} C)
- Self-healing characteristics

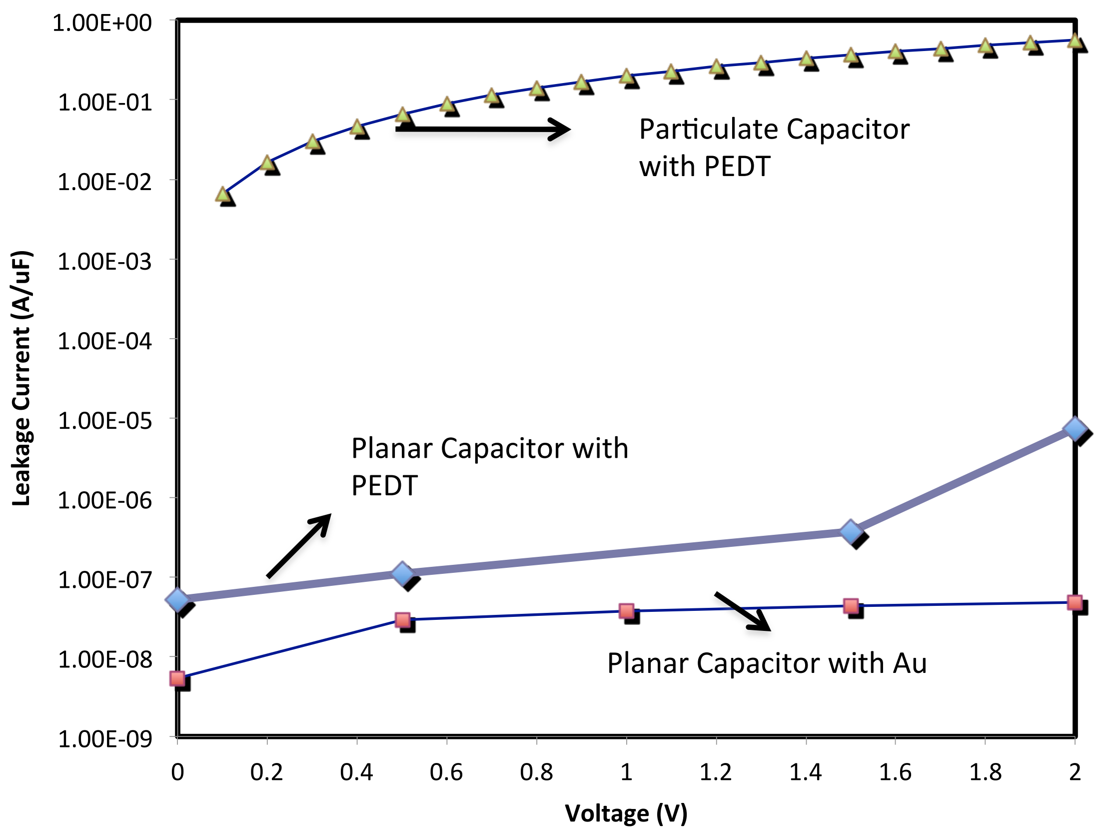


Demonstration of Nanoelectrode Capacitors

Device Thickness	Area Enhancement	Capacitance Density
Planar (0.6mm x 0.6mm)	--	0.12μF/cm²
<5 μm	10X	1.1 μF/cm²
10 μm	25 X	3.9 μF/cm²
25 μm	150-200X	30 μF/cm²
>75 μm	400-500X	55-60 μF/cm²

Nanoelectrode Capacitors : Leakage Current

I-V plot of planar and particulate electrode capacitor



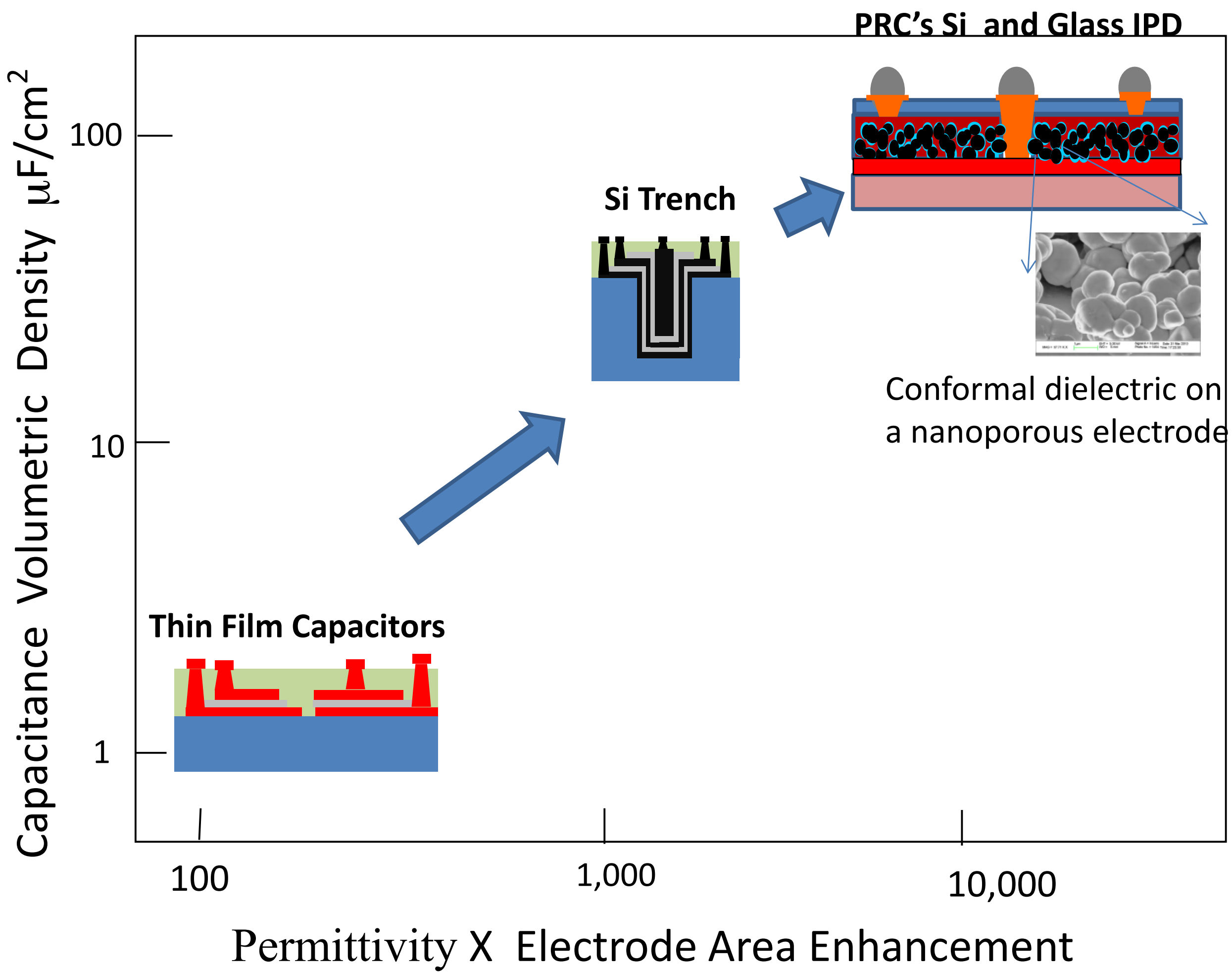
Particulate electrodes using PEDT show very high leakage as compared to planar capacitors.

Two possible reasons identified:

(I)PEDT/ Al_2O_3 interaction

(II) Inherent Defects in Al_2O_3 film

GT PRC: HDCAP Vs State-of-the-Art



Conclusions

- 3D IPAC shown as a compelling new technology for active and passive component integration in ultrathin functional modules

  - Better miniaturization
  - Lower cost
  - Higher performance

- Novel silicon or glass-compatible high-density capacitor technologies investigated to meet 3D IPAC goals