Silicon, GaAs and GaN Technologies for Monolithic DC-DC Power Converter ICs

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- David Anderson – Texas Instruments
- Peter Wright – Tri-Quint

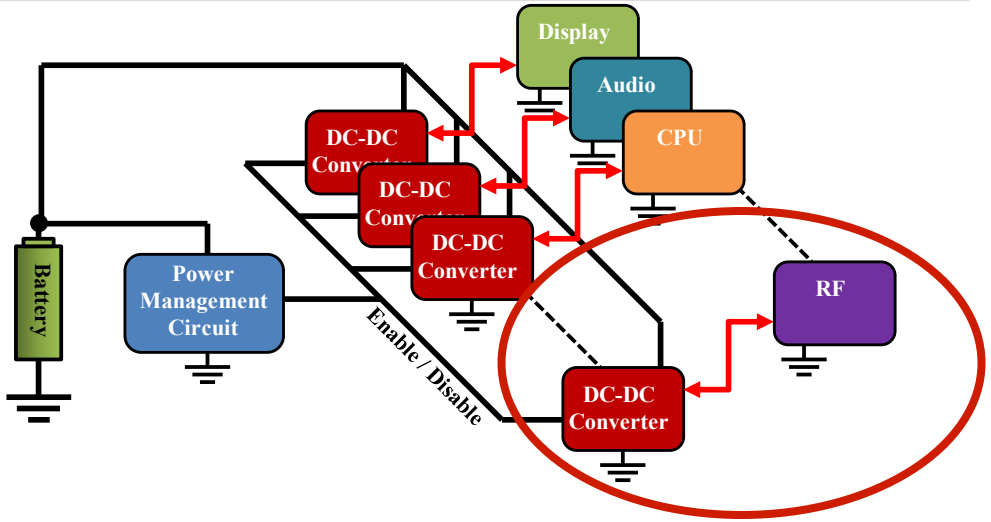
Outline

- Device FOM
- Power Converter ICs
  - Si
  - GaAs
- GaN Integration
- Summary

Power Supplies For Portable Electronics

System Trends

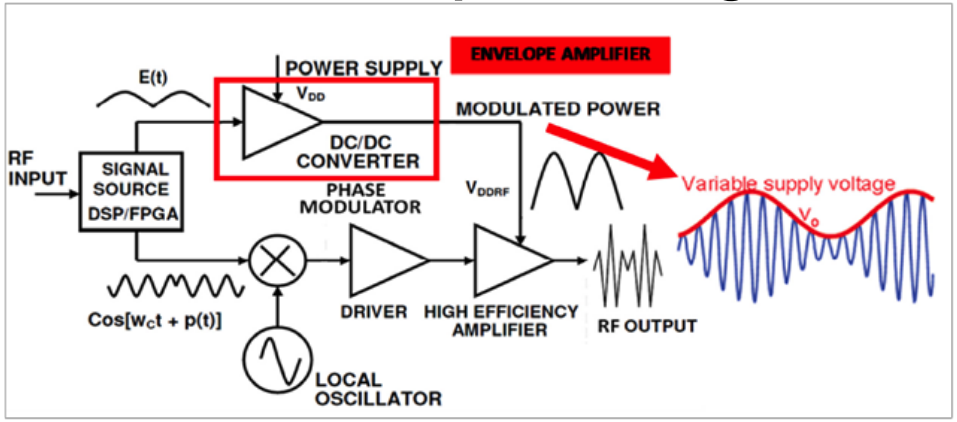
- Point of Load power conversion
- IC Voltage Scaling
- Slow Battery Capacity Increase
- Miniaturization



Power Electronics

- Low V – High I
- Higher Switching Frequency, Bandwidth
- Integration / System on Chip

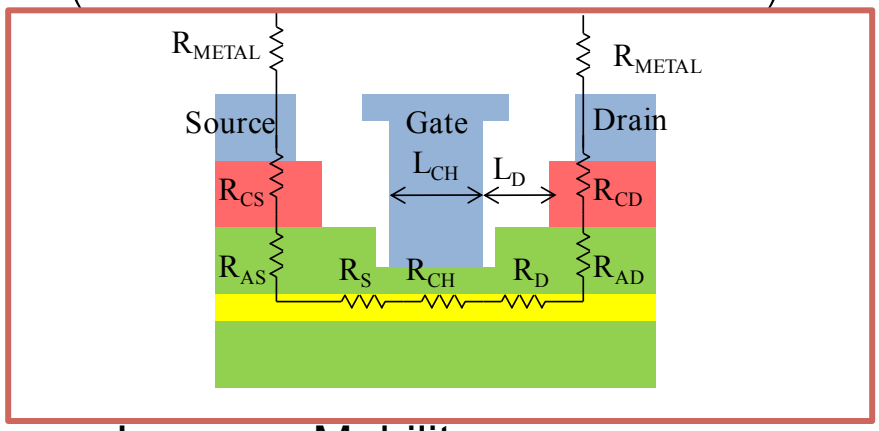
Envelope Tracking

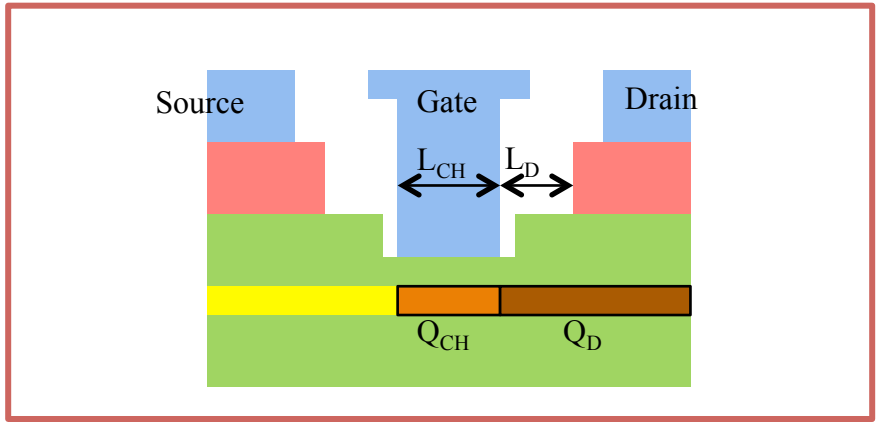


Power Switching Figure of Merit

$$FOM = R_{ON} \times Q_G$$

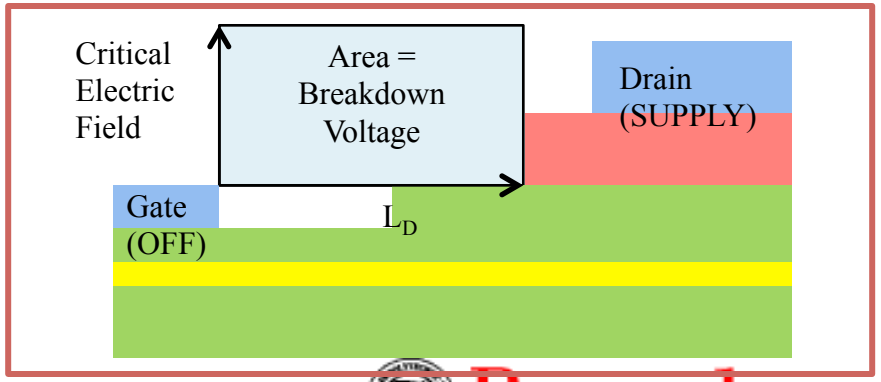
$$\left(R_{ON,SP} = \frac{L_{CH}}{\mu_{CH} Q_{CH}} + \frac{L_D}{\mu_D Q_D} + R_{EXT} \right) \times \left(Q_{G,SP} = L_{CH} Q_{CH} + L_D Q_D \right)$$



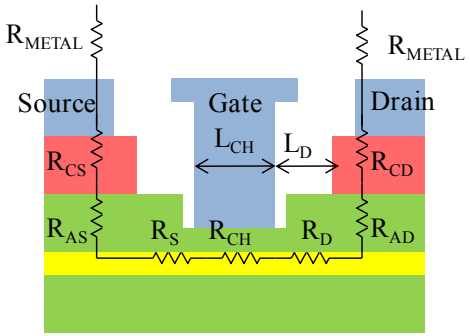
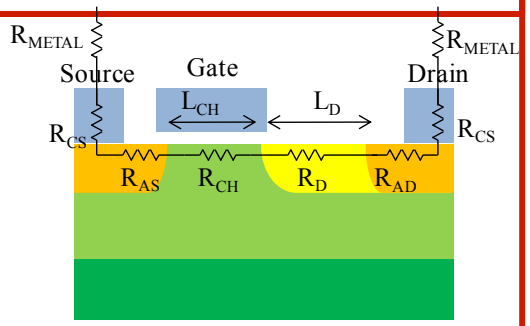


- Increase Mobility
- R_{EXT} : Interconnects
- Reduce Channel length
  - Scaling
- Reduce L_D
  - Compromises breakdown voltage
  - High Bandgap Materials

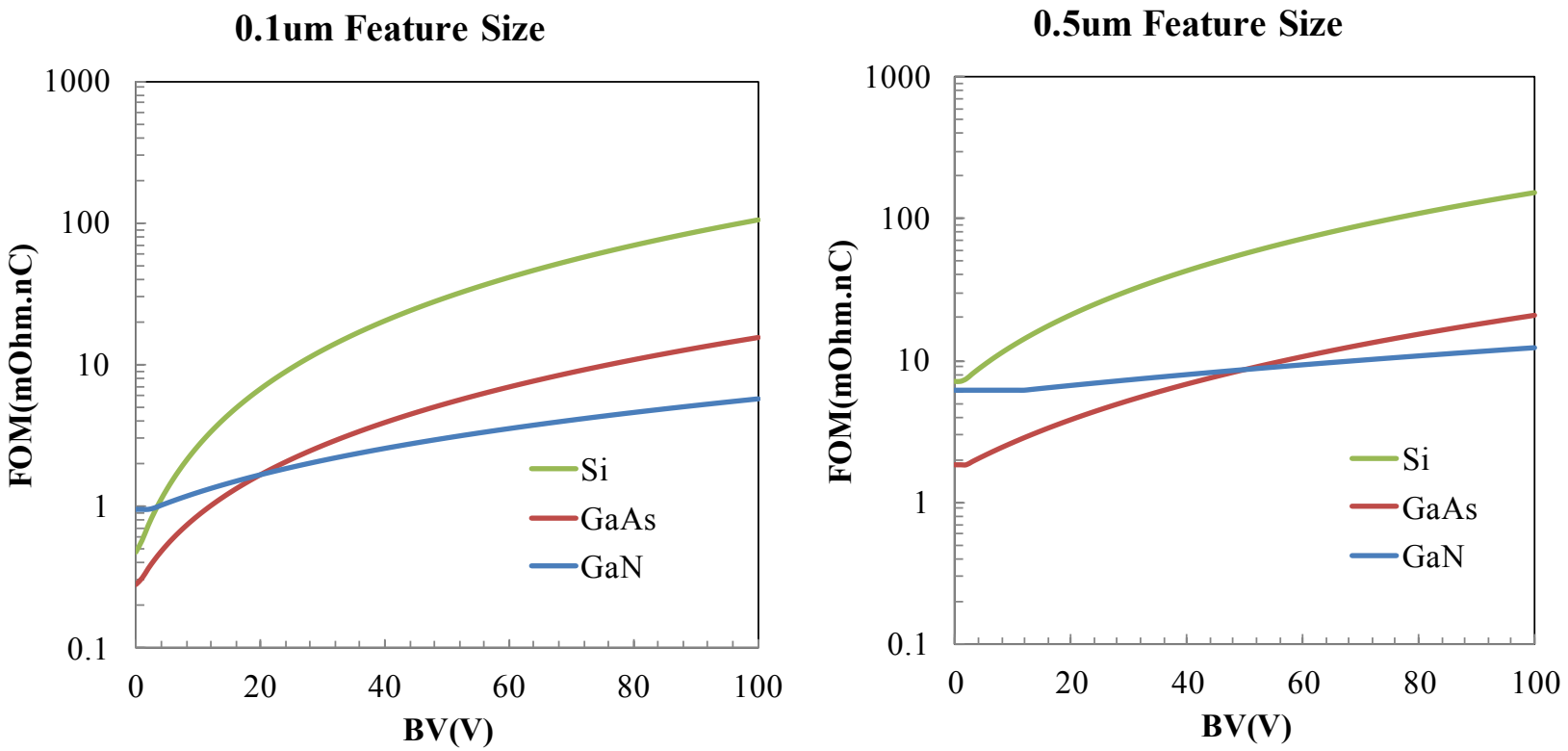
Ideal Drift Electric Field



Comparison of Device Technologies

Device	HEMT		LDD NMOS
Structure			
Technology	**AlGaAs/InGaAs/ AlGaAs**	**AlGaN / GaN**	**Silicon LDD NMOS**
μ_{CH} ($cm^2V^{-1}s^{-1}$)	~6000	~1800	~500
μ_D ($cm^2V^{-1}s^{-1}$)	~6000	~1800	~1200
$E_{C,Lat}$	~25V/μm	~150V/μm	~15V/μm
R_{Ext}	~0.2 Ω.mm	~0.2 Ω.mm	~0.1 Ω.mm
	• Highest Mobility • Intermediate Bandgap • Suited for (5-40V)	▪ Widest Bandgap but for low BV, it makes less impact for FOM ▪ Ideal for high voltages (>40V)	▪ Lower parasitics, more conducive to scaling ▪ Ideal for low voltages (<5V)

FOM Technology Comparison

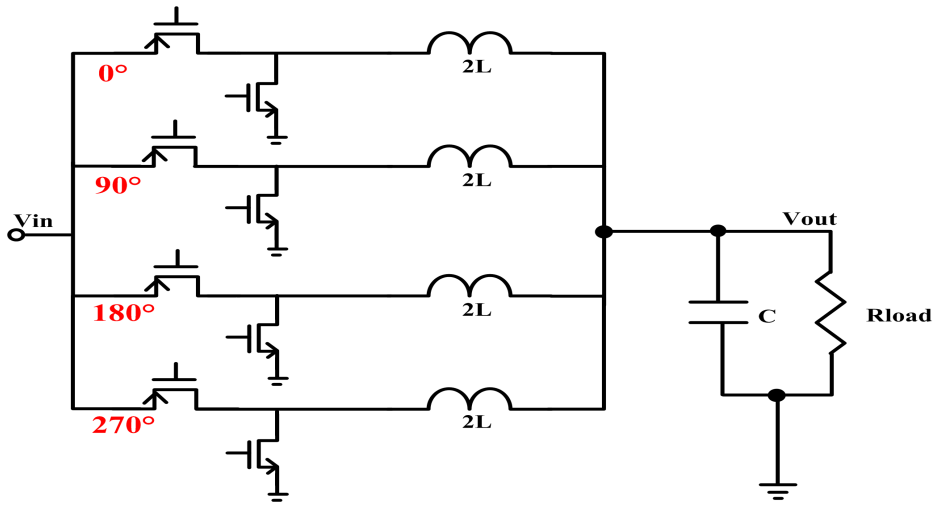


- To take advantage of Wide Bandap for low voltage devices, extremely small scaling rules are required
- GaAs has the best (smallest) FOM for <20V for 0.1μm feature size or above

V. Pala, H. Peng, P. Wright, M.M Hella and T.P Chow, "Integrated high-frequency power converters based on GaAs pHEMT : Technology Characterization and Design Examples," *IEEE Trans. Power Electron.* , vol. 27, no. 5, pp. 2644-2656, 2012.

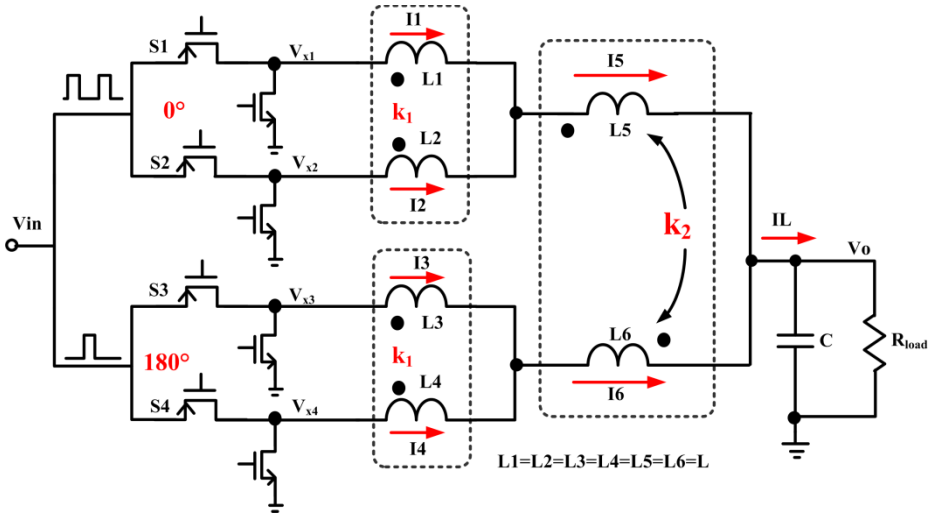
Phase Shedding/Segmentation

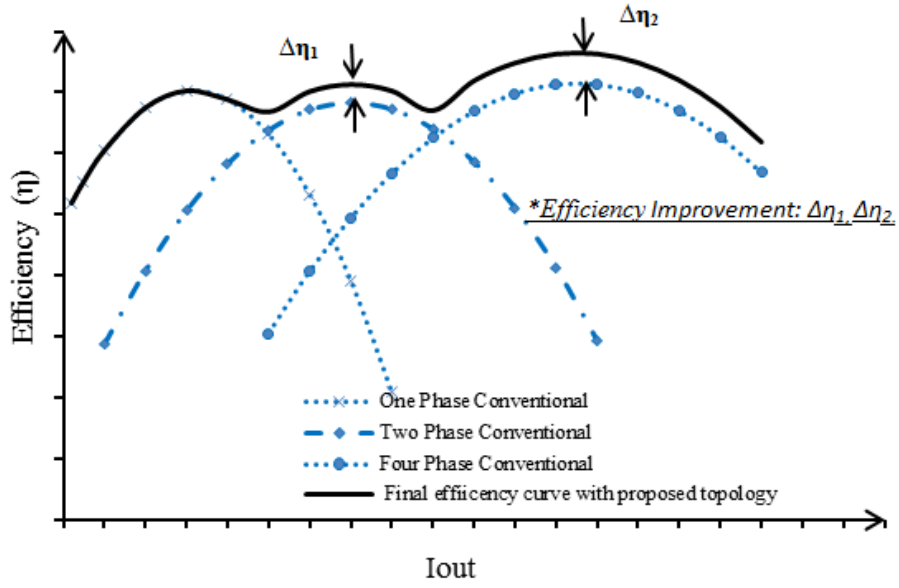
- Operation phases/ segments are switched ON/ OFF depending on different load conditions.
- Maintain constant efficiency at different loads.
  - Easy to extend the load current range by adding more phases.



- Drawbacks:
  - Require larger inductor value or variable switching frequency when reducing phases.
  - Output ripple may be large: large output cap is required.
  - Require digital control blocks: ADC, etc.

Inductor Coupling in Output Network

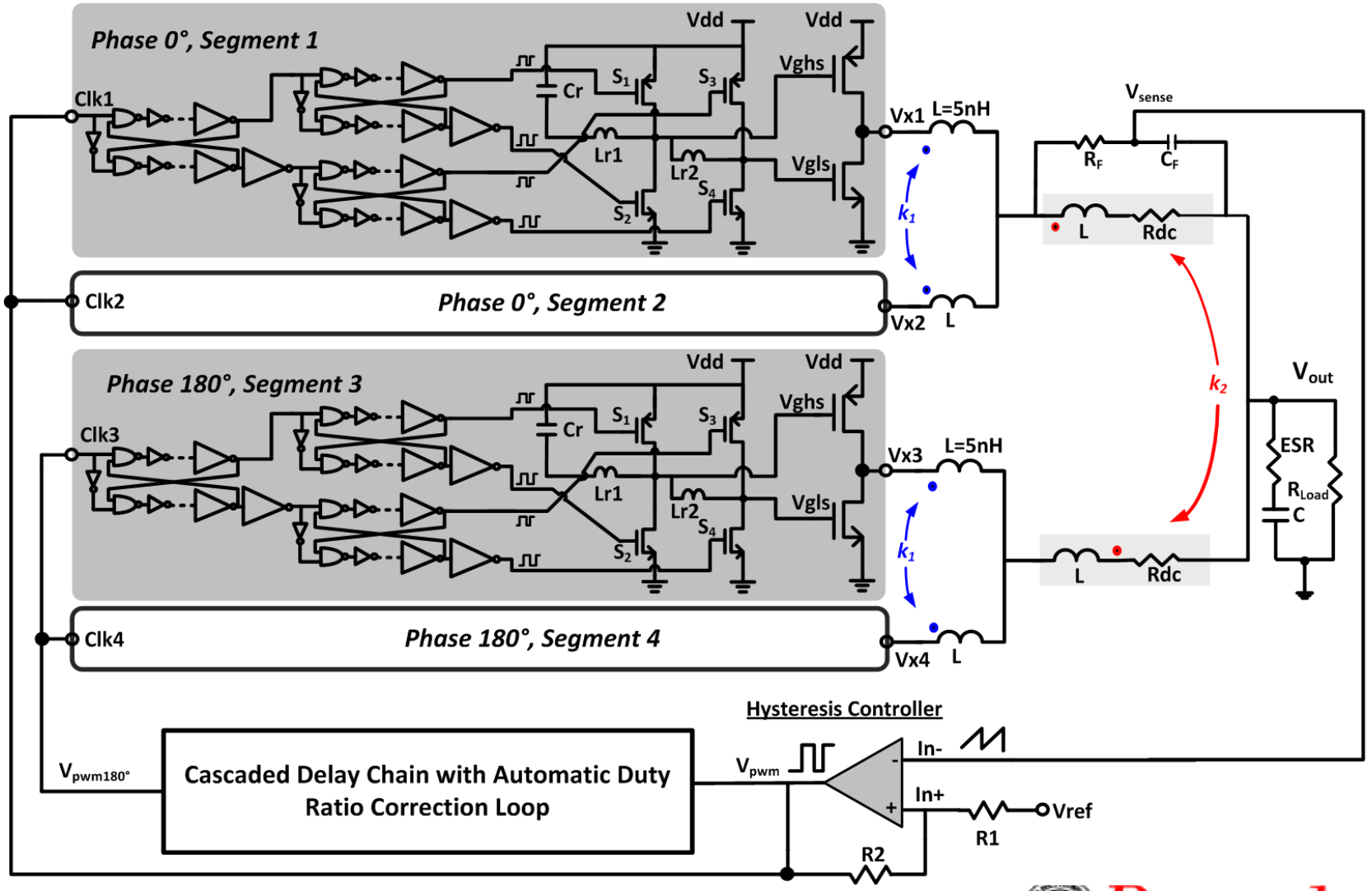




- Negative coupled inductors bring better efficiency at two-segment & four-segment operation:
  - Larger equivalent inductance.
  - Ripple cancellation.

You might want to add equations to prove this

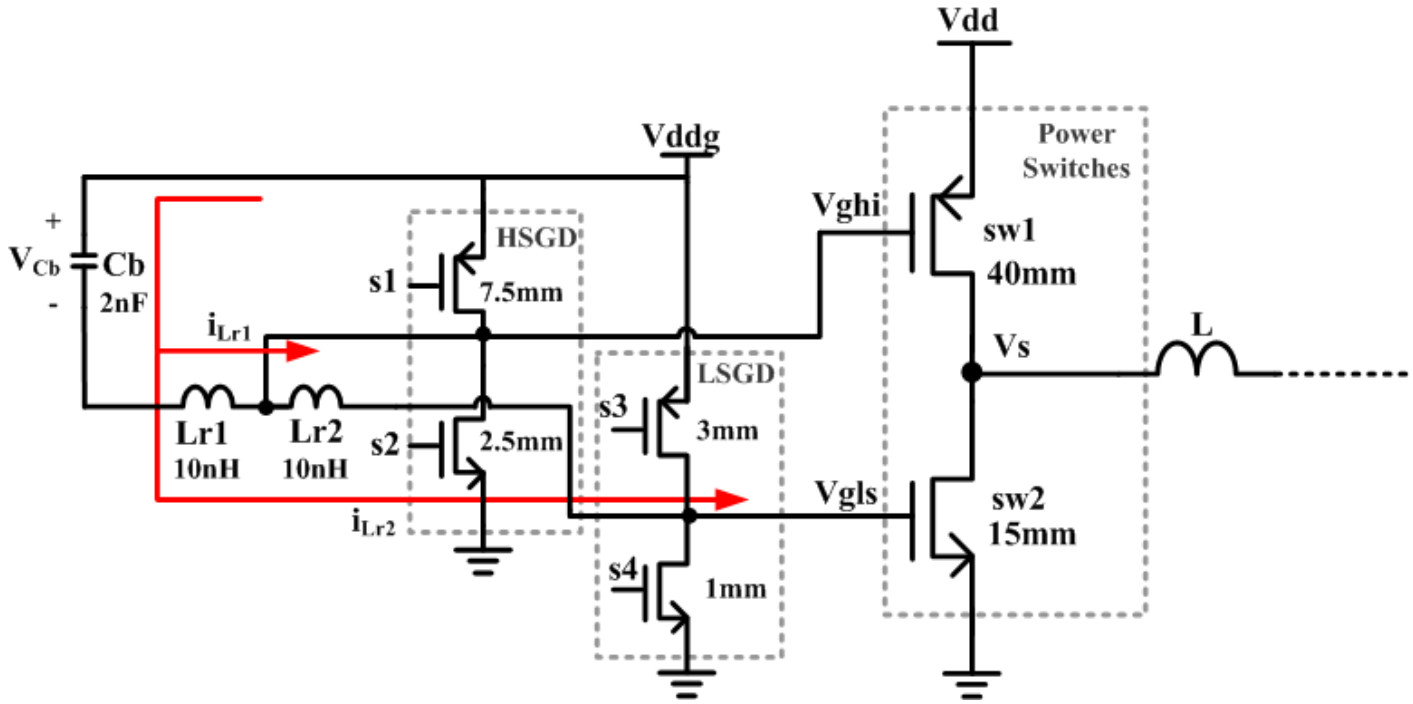
Circuit Implementation



Circuit Implementation

- HS and LS switches are sized at 5V-to-2.5V conversion ratio and 0.5 A load current.
  - PMOS: 40 mm, NMOS: 15 mm.
- Combined HS-LS resonant gate driver with partially shared inductance is adopted.
  - Energy distribution is changed and stored in resonant inductor.
  - Soft switching is realized by deliberated designed gate signals.

Resonant gate driver design

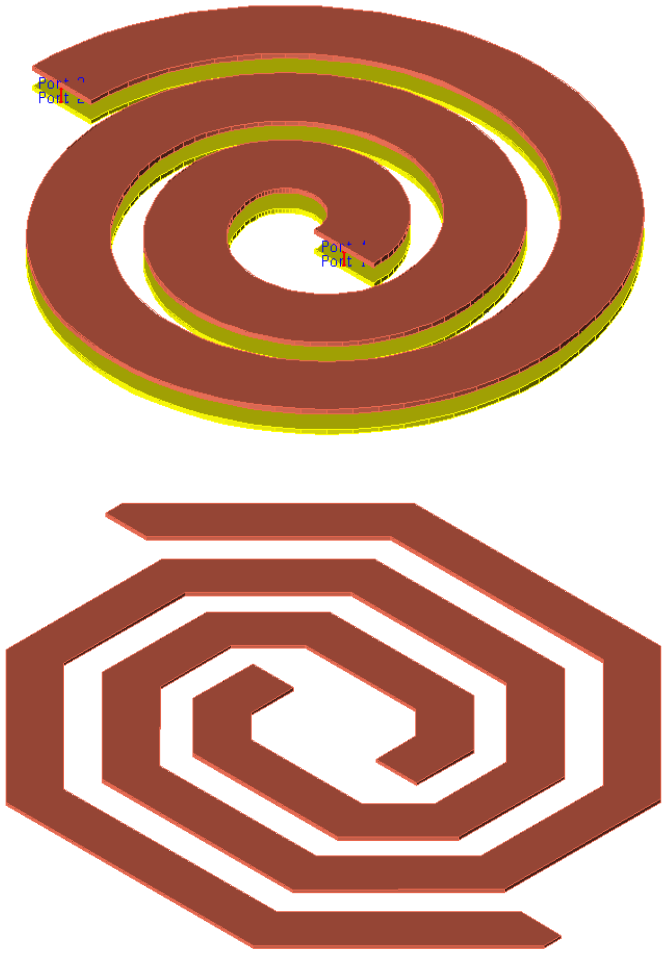


- Energy distribution is changed and stored in resonant inductor.
- Soft switching is realized by modifying the gate signals.
- Tradeoffs between gate driver loss and main switch's switching loss.

Coupled inductor design

- Coupled inductors are implemented on PC-Board.
- 1 oz, 20 µm thick copper layer.
- Min. 2.7 mil spacing between layers.

	Positive Coupled Ind.	Negative Coupled Ind.
Area (mm^2)	2.58 × 2.37	3.4 × 4.35
Width (µm)	300	300
Spacing (µm)	120	200
Turns	2.5	1.5
L (nH)	6.27	6.48
R_{dc} (mΩ)	32	32
k	0.799	0.397
Q @ 100MHz	37	45



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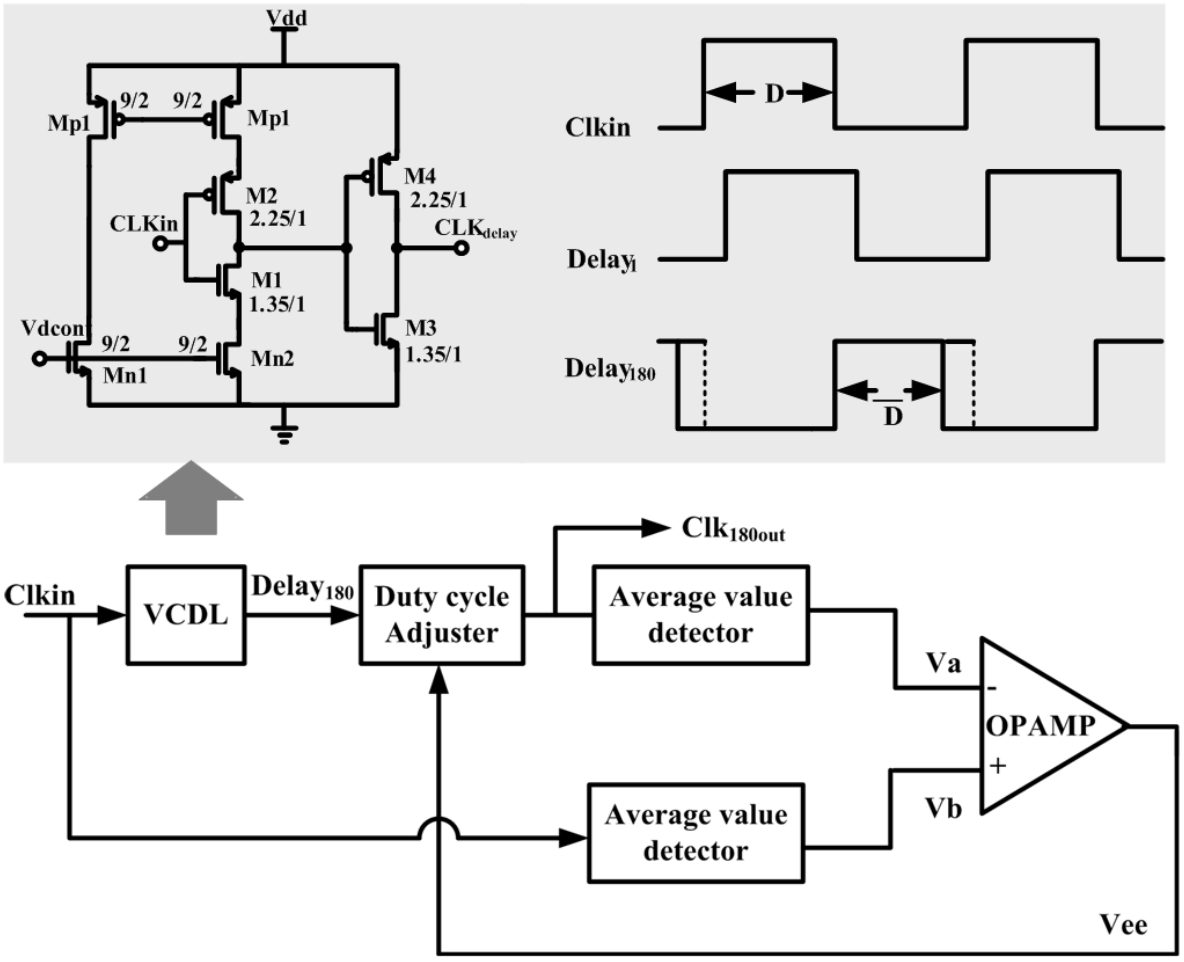
Feedback control loop

- Hysteresis controller for fast transient response and large close loop bandwidth.
- Synchronization between two phase operation:
  - 0.5T delayed signal produced from voltage controlled delay cells.
  - Unbalanced duty ratio will cause current sharing problem.
  - Automatic duty ratio corrector.

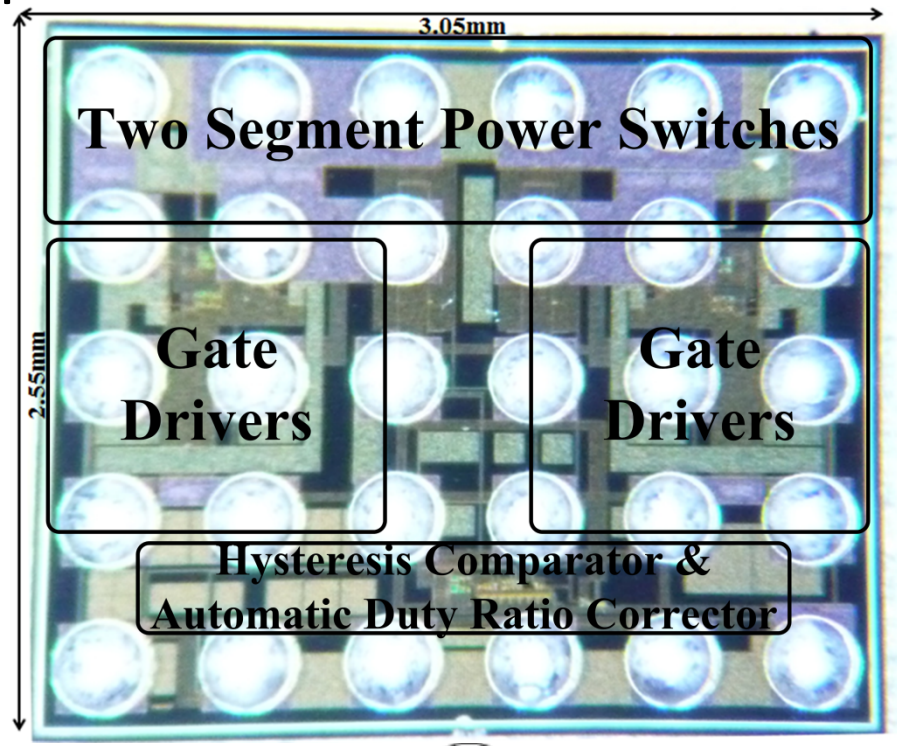
Feedback control loop



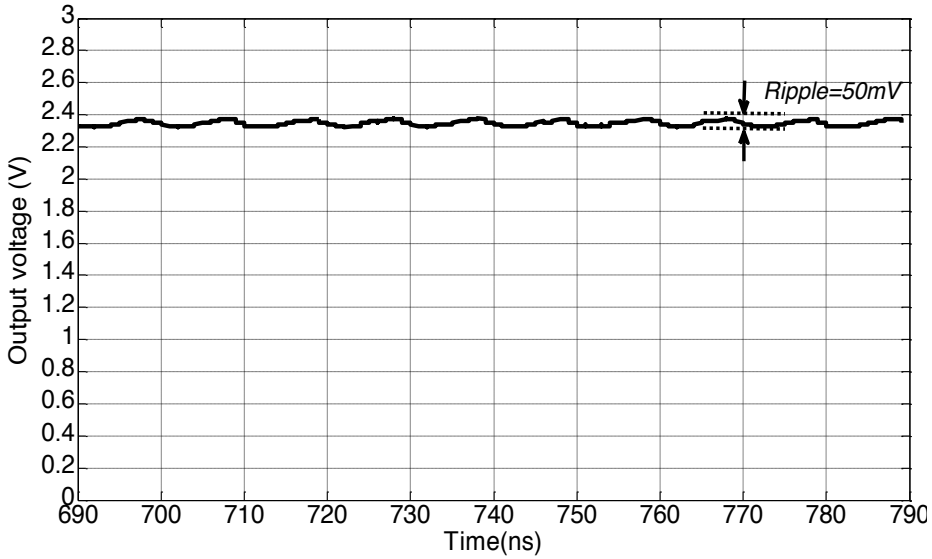
Eight cascaded delay cells, each producing 0.625 ns delayed signal with 1.7 V control voltage.

Measurement results

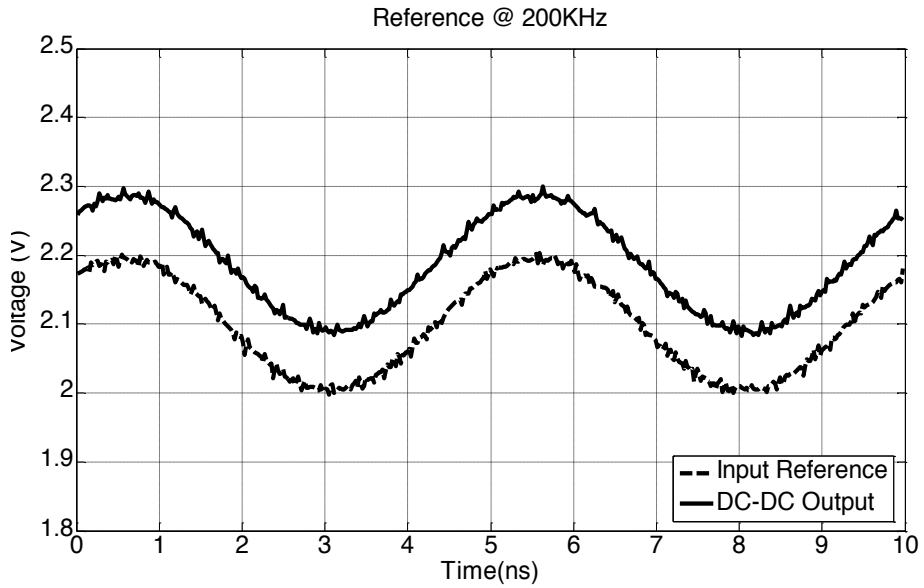
- Implemented in 0.5 µm CMOS technology with 6 Metal layers + 1 distribution layer
- Flip clip package. Vias footprint: 5 X 6
- 4 layer PCB.
- Load capacitor : 47 µF
- Feedback network:
  - R_f : 1KΩ, C_f : 2.7 pF



Measurement results

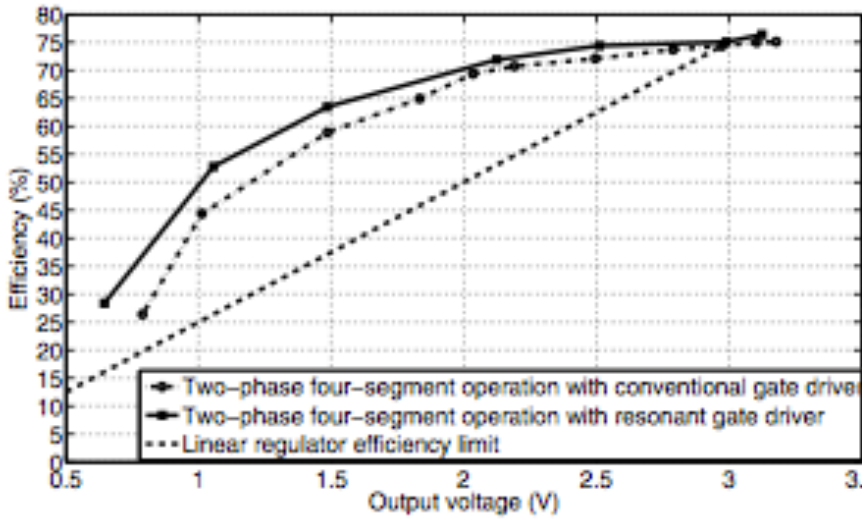


Output transient response with Vin=4 V, Vout= 2.3V. Voltage ripple is 50 mV.

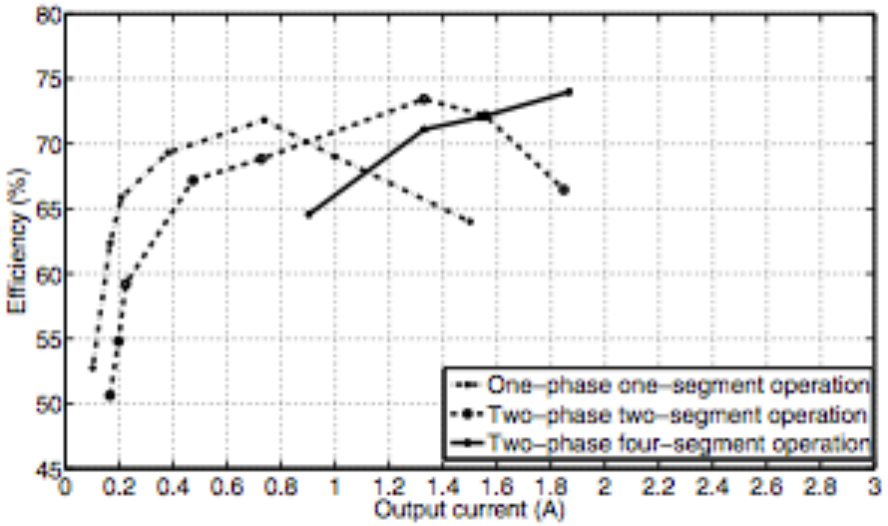


Tracking model results with sinusoidal reference signal.

Measurement results



Efficiency vs. output voltage at two-phase four-segment operation with resonant gate drivers



Phase shedding/segmentation results with Vin = 4 V, Vout= 2 V.

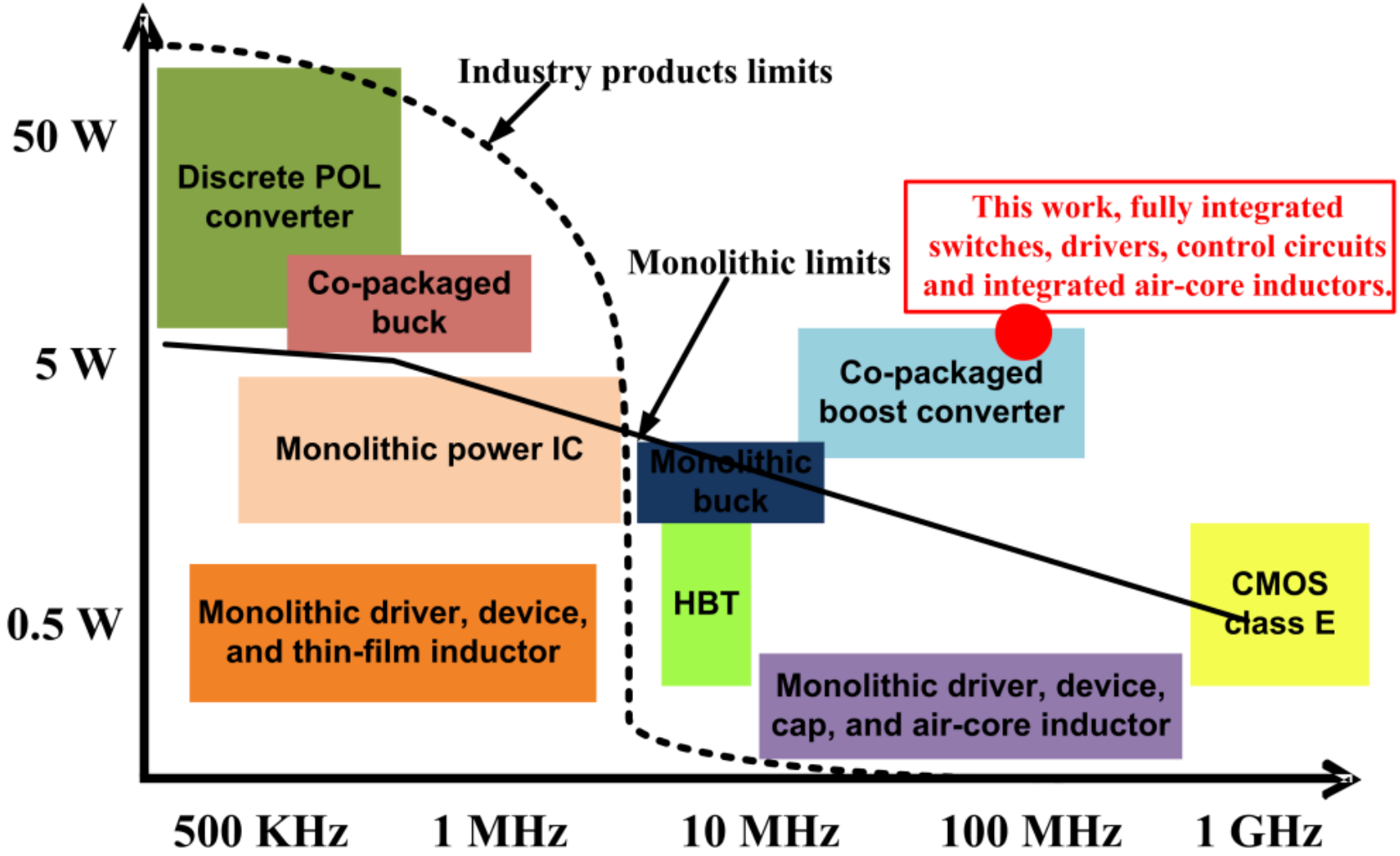
Results summary and comparison

Technology		0.5 µm CMOS, 5 V & 1.8 V devices
Switching frequency		100 MHz
Die area	CMOS die	7.78 mm^2
	Positive cou. ind.	6.61 mm^2
	Negative cou. ind.	15.3 mm^2
Supply voltage	Power stage	4 V
	Comparator	1.8 V
Num. of phases/ segments		2 / 4
Peak Output		3 V/1.86 A
Output voltage ripple		50 mV
Peak efficiency		77.4 %

Comparison with Prior Art

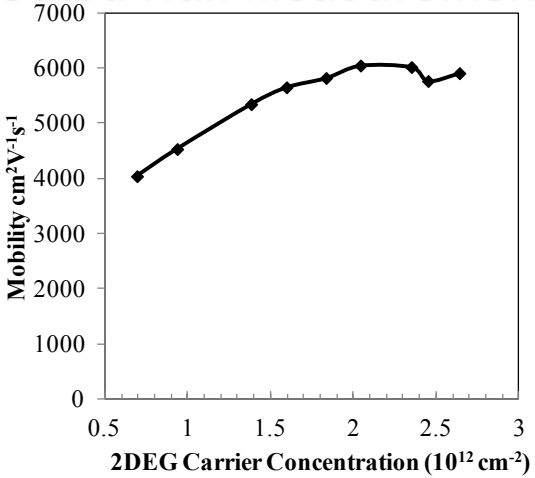
Ref	Tech.	# Phases	In/Out Voltage V/V	Output Current (A)	Sw. Freq. (MHz)	L (nH)	Peak Eff. (%)
Intel JSSCC'05	90 nm CMOS	4	1.2/0.9	0.3	233	6.8 SMT	82.5
RPI APEC'07	0.18 µm BiCMOS	2	1.8/0.9	0.5	200	2.14 On-die	64
ISSCC '08	0.25 µm BiCMOS	1	3.6/3.1	0.62	130	110 SMT	83
Trans. PE 2012	0.25 µm BiCMOS	1	3.6/2.2	0.33	200	51 SMT	77
ECCE'09	65nm CMOS	1	1.2/0.85	0.08	100	11 on-die	87.5
JSSCC'07	0.35µm CMOS	1	3.3/2.3	0.06	200	22 on-die	86
This work	0.18 µm CMOS	2	4/3	1.8	100	5 on-PCB	77.4

Comparison with Prior Art

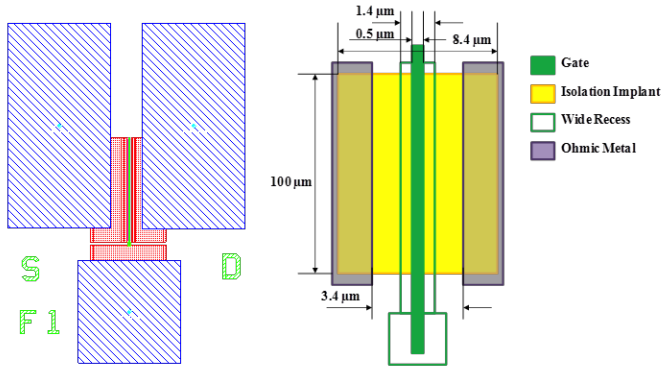


Intrinsic Device ON Resistance

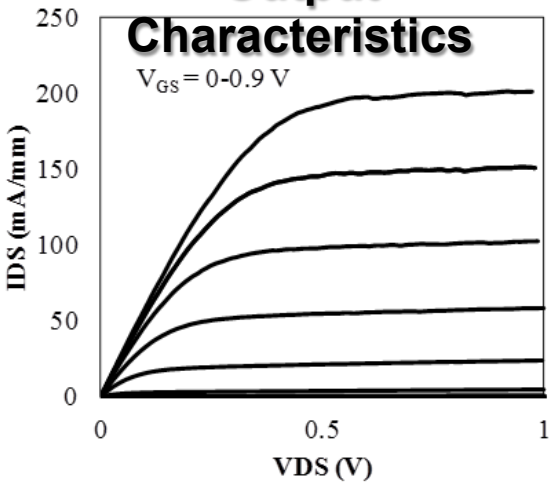
Gated Hall Measurements

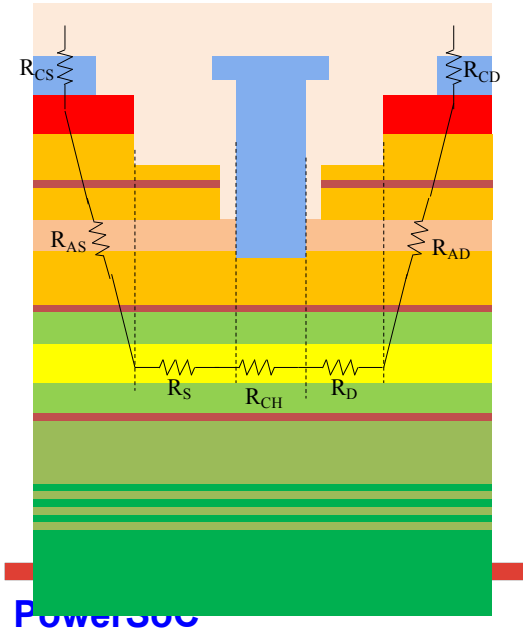


100µm pHEMT Layout

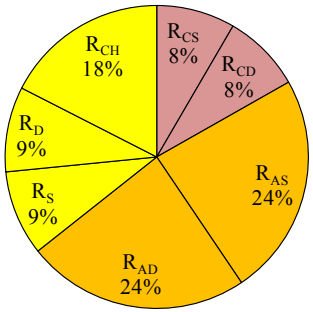


Output Characteristics





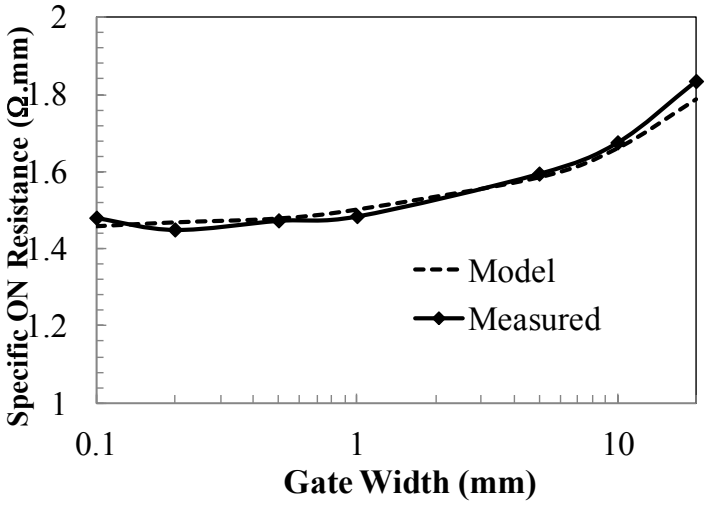
R_{CS}	0.12 Ω.mm
R_{CD}	0.12 Ω.mm
R_{AS}	0.34 Ω.mm
R_{AD}	0.34 Ω.mm
R_S	0.13 Ω.mm
R_D	0.13 Ω.mm
R_{CH}	0.25 Ω.mm



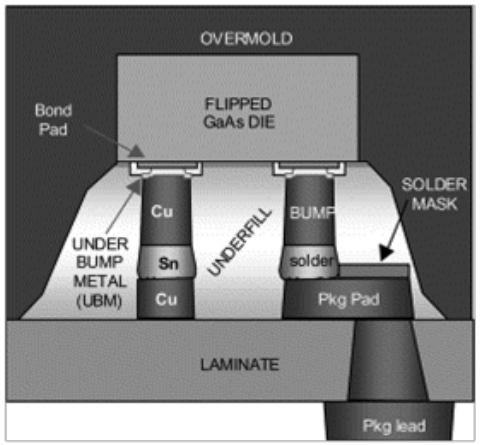
- Intrinsic Specific R_{ON} = 1.46 Ω.mm
- TLM Measurements show that 64% of the resistance is from contact and access Resistance

ON Resistance : Interconnect Metallization Scheme

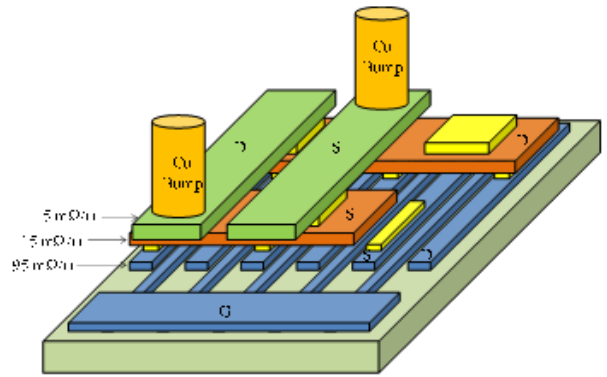
Unit Cell ON Resistance due to Metal Interconnects



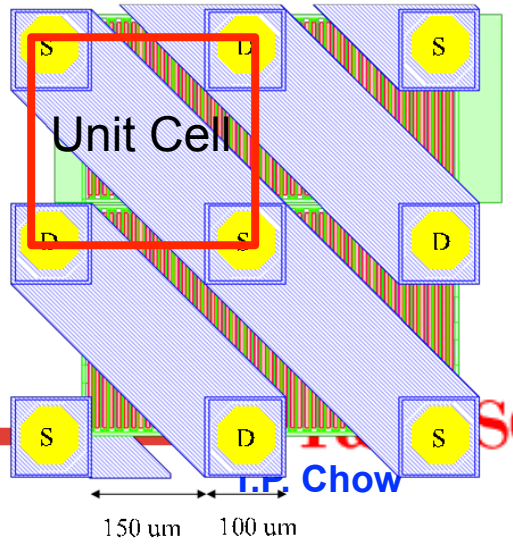
Flip Chip Bonding using Cu Bumps



Flip Chip Interconnect Scheme



Layout for Flip Chipped Device

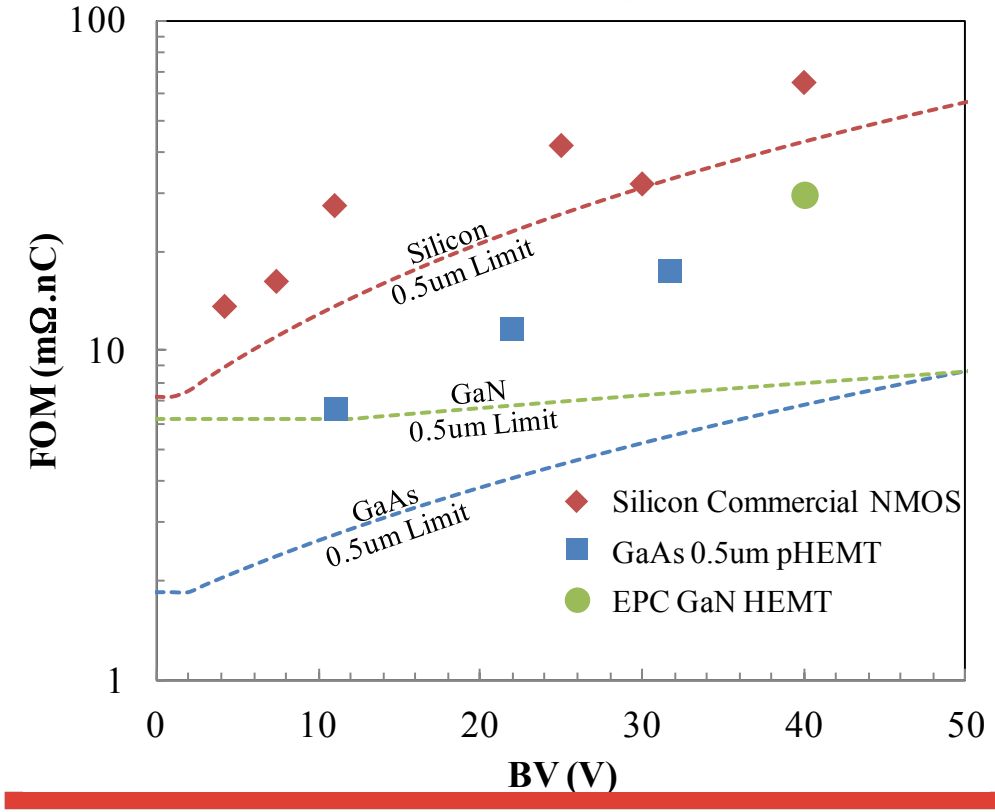


22 and 32V GaAs pHEMTs Figure of Merit

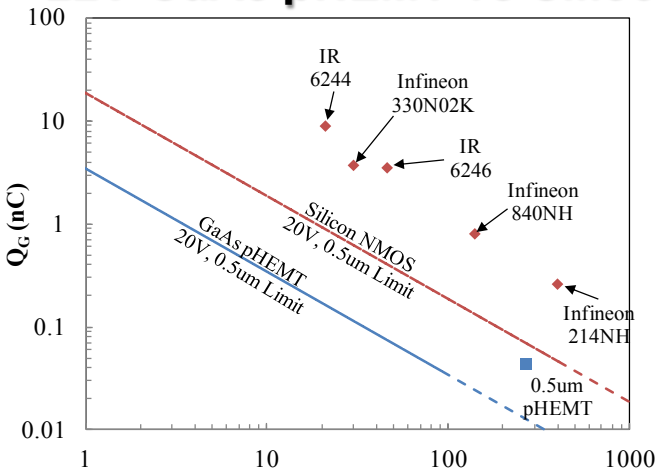
Characterization Results

BV	Gate Width	Current	R_{ON}	Q_G	FOM
22 V	5 mm	0.5 A	268 mΩ	44 pC	12 mΩ.nC
32 V	5 mm	0.5 A	303 mΩ	58 pC	18 mΩ.nC

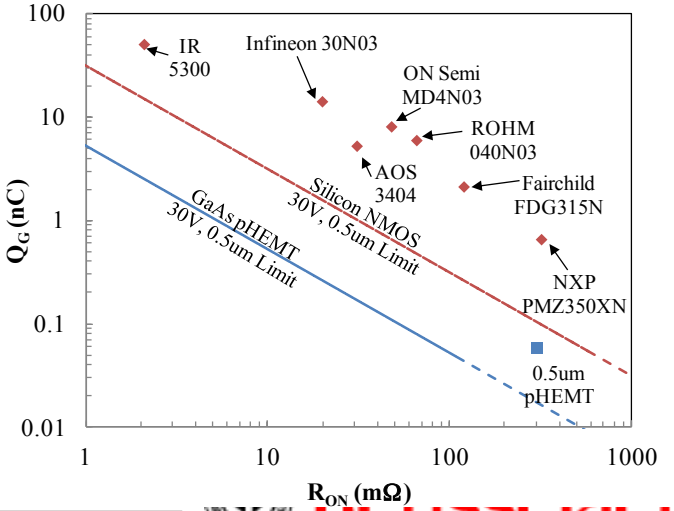
Breakdown Voltage vs FOM



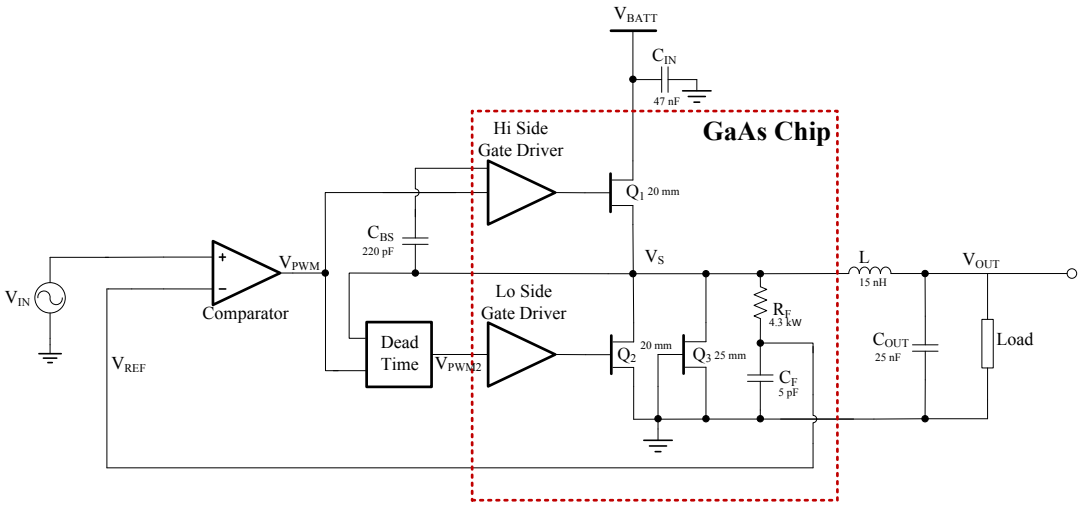
22V GaAs pHEMT vs Silicon



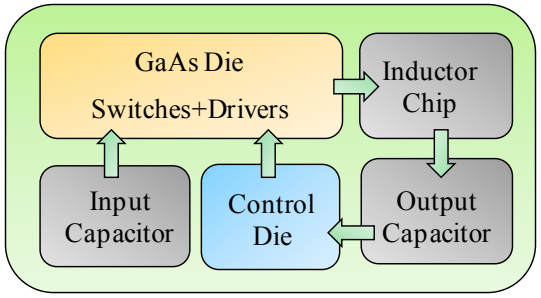
32V GaAs pHEMT vs Silicon

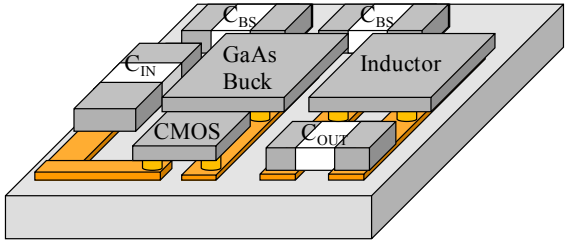


pHEMT DC-DC Converter : Output Stage Prototype

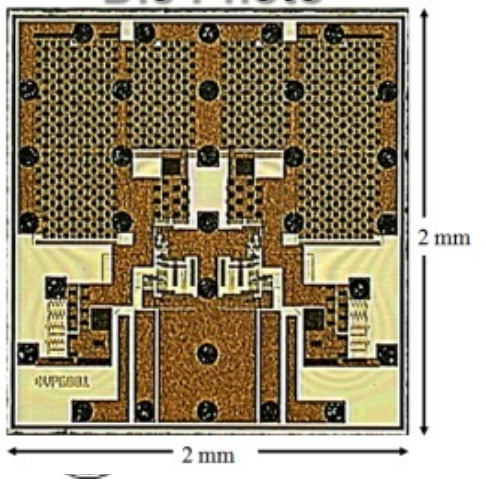


Converter Schematic





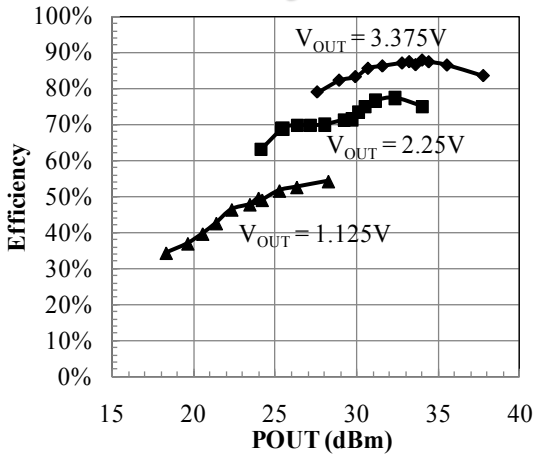
Die Photo



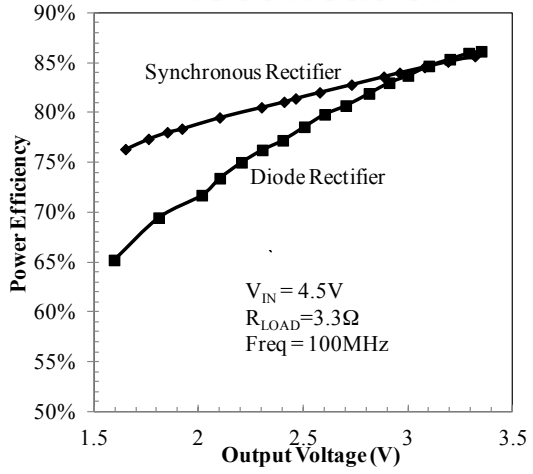
- Specifications
  - Target Application : Envelope Tracking in RF Amplifiers
  - Switching Frequency =100MHz
  - Buck Type, 4.2-11V in, 1.5-3.5V Out
  - Peak P_{OUT} = 6.6W
  - Target tracking bandwidth : 10MHz
  - pHEMT “Dummy CMOS” Controller

Converter Efficiency

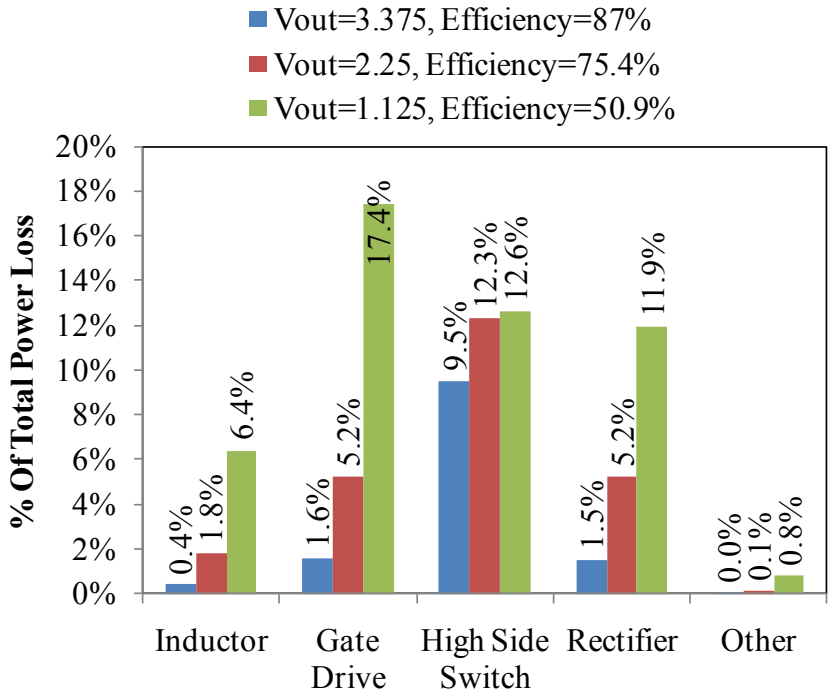
Efficiency vs Power



Effect of Synchronous Rectification

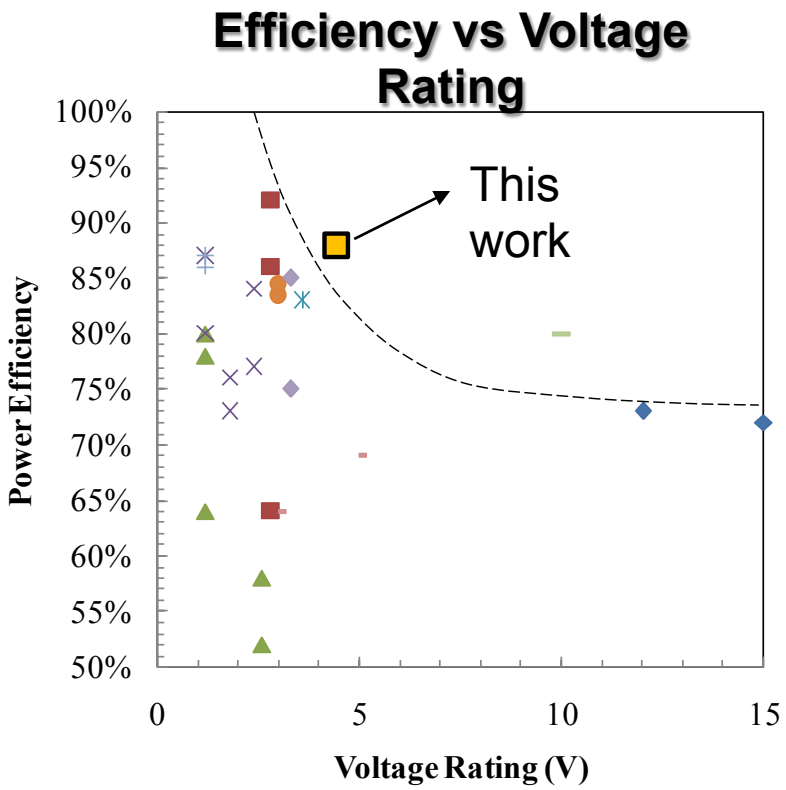


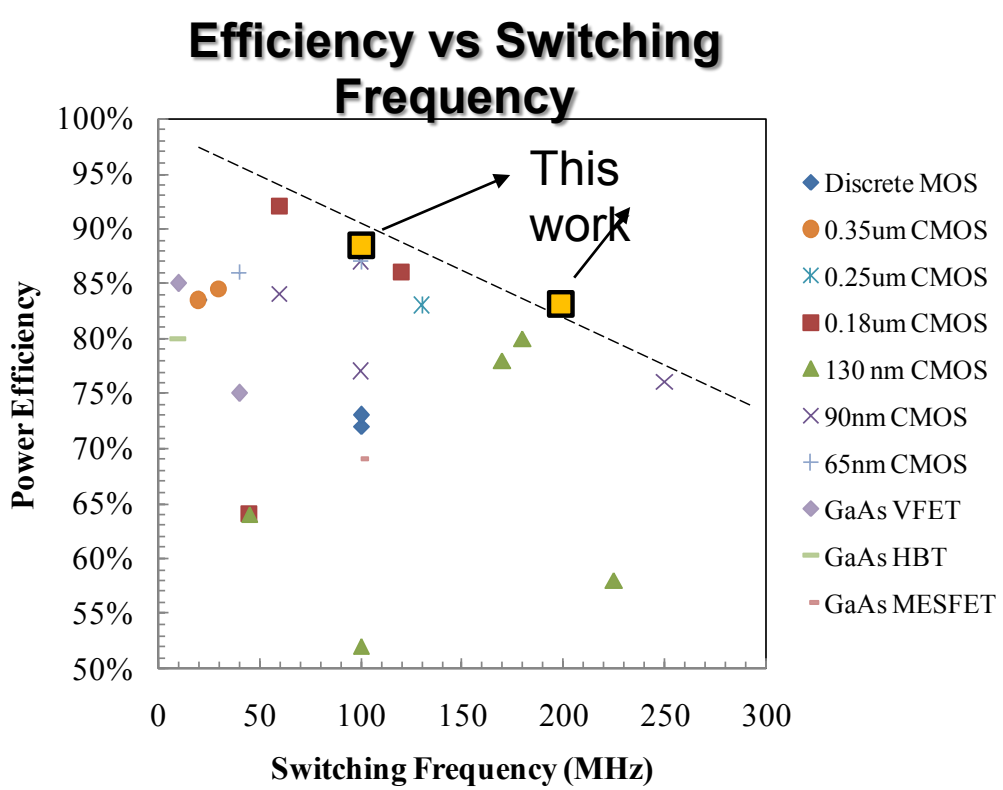
Power Loss Components



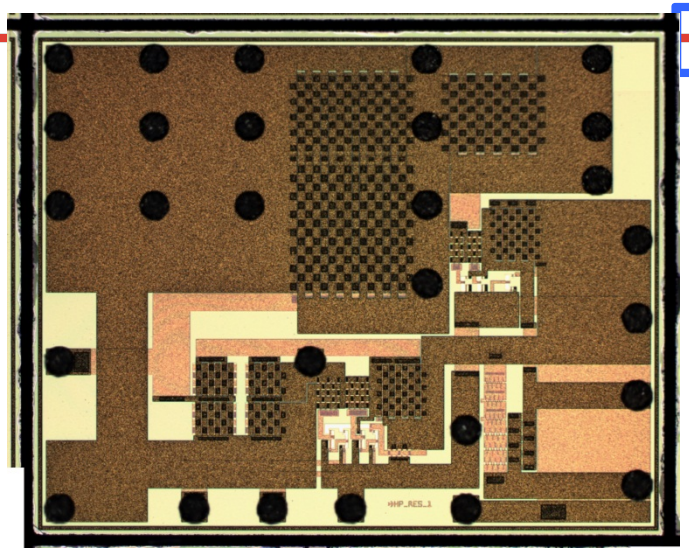
- At low power, the power losses are dominated by gate drive
- GaAs pHEMT drivers consume static power
- Can be improved by CMOS drivers

DC-DC Converter Performance

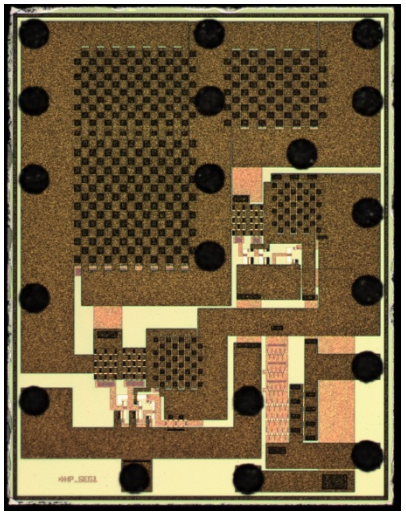




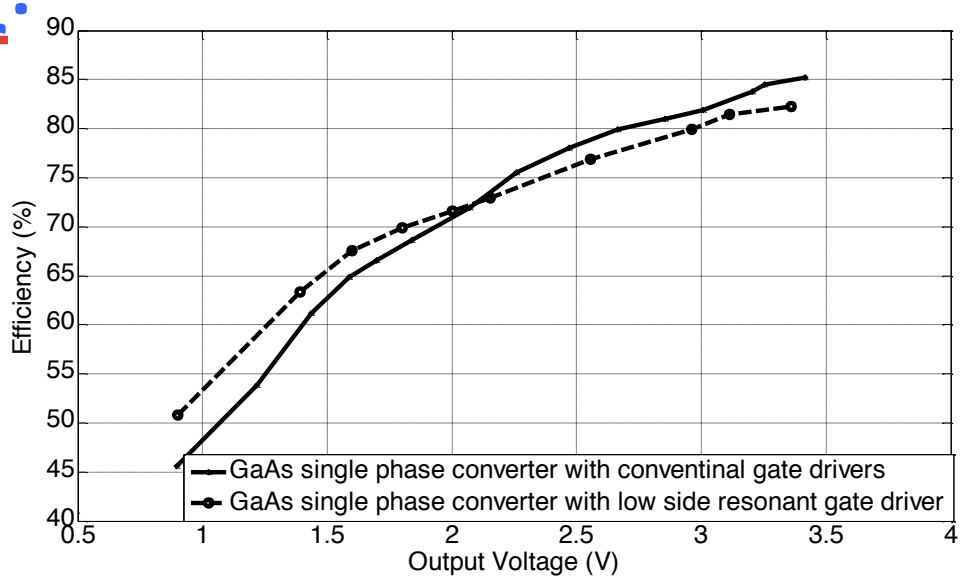
GaAs p-HEMT Resonant Gate Dr

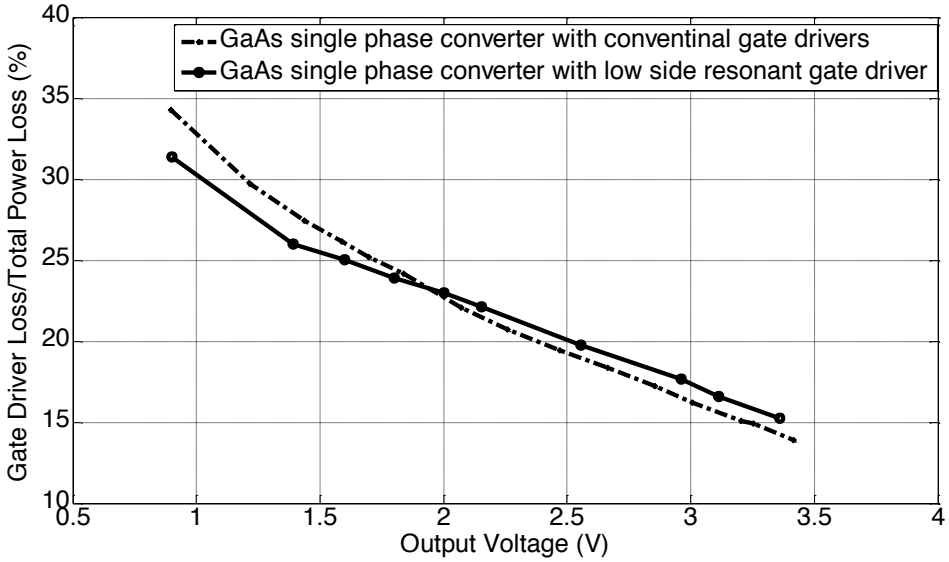


Single phase GaAs converter with low side resonant gate driver.



Single phase GaAs converter conventional gate driver.

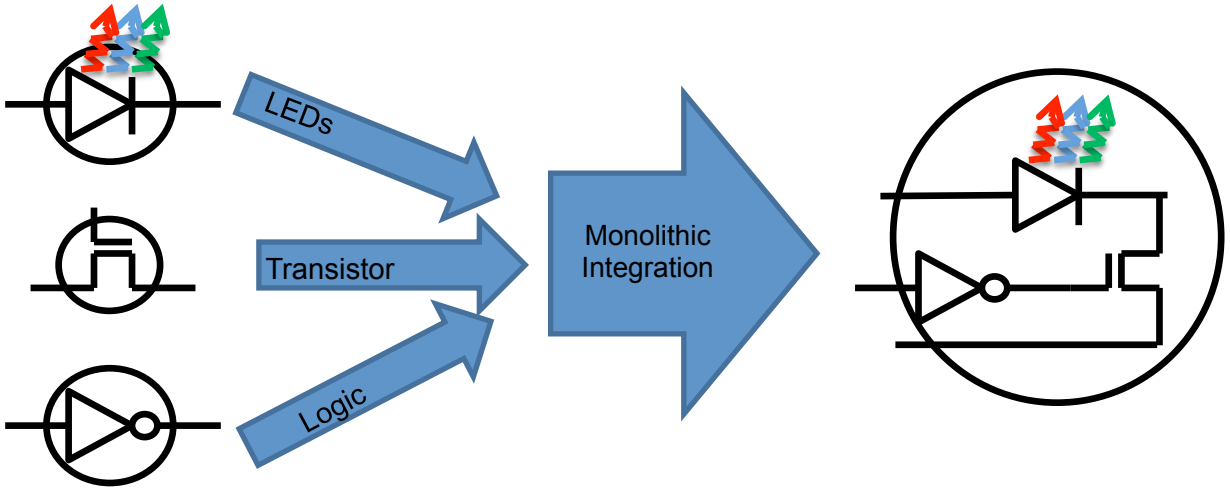




Monolithic Integration

SL-ERC Project S1.3.1:

- Start date: July, 2010
- Duration: Through June, 2018

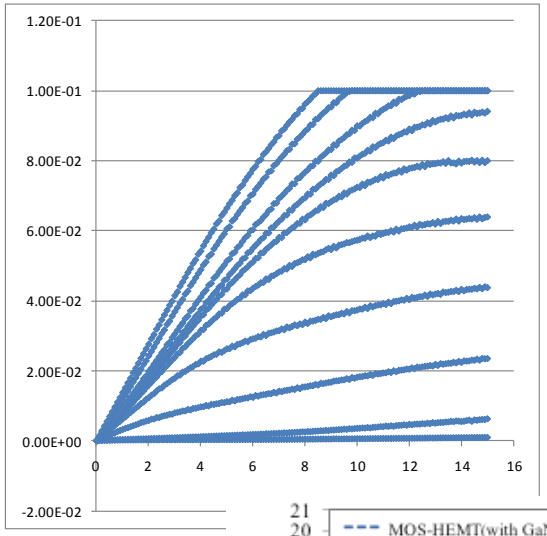


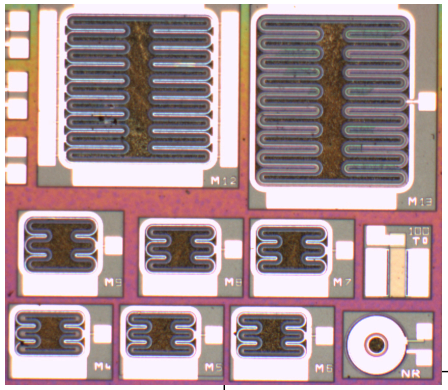
Objective:

- Develop a process to enable monolithic integration of LEDs, control logic and power transistors. This IC will have the full spectrum of smart lighting features for a wider variety of applications due to reduced package size and cost and improved reliability.

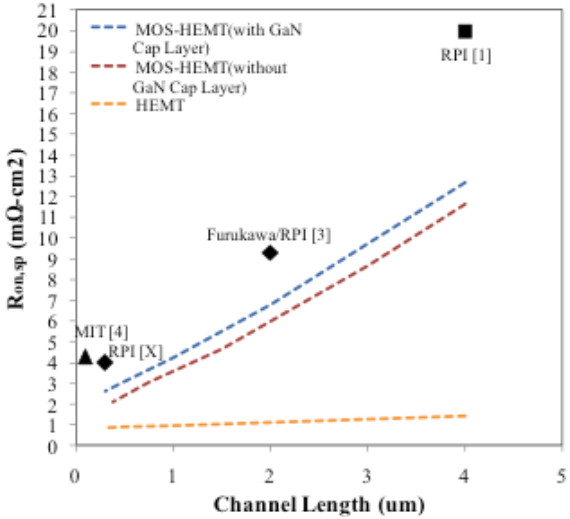
RPI MOS Channel-HEMT

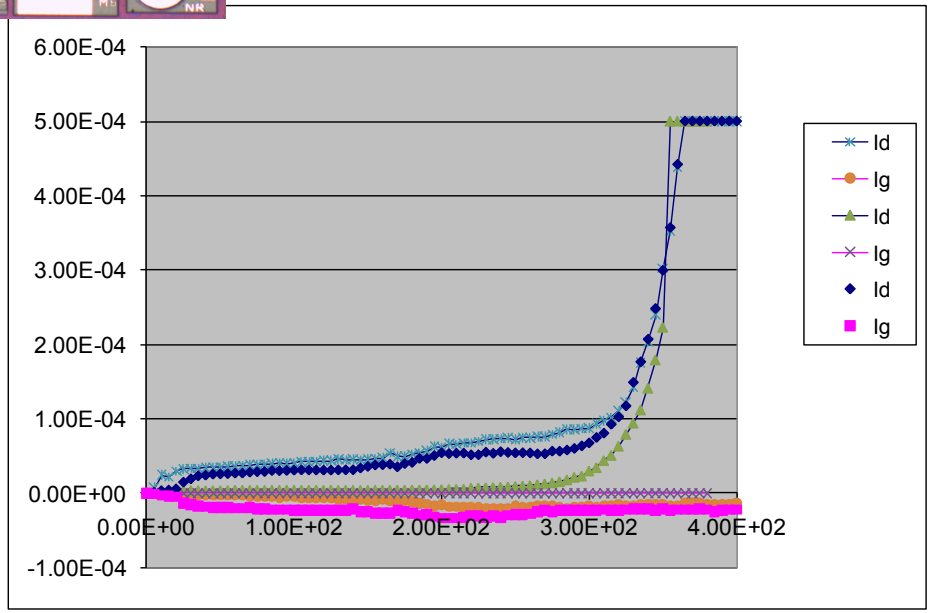
MOS Channel-HEMT on Si





- BV = 350V
- Ron,sp=4.0mOhm-cm2
- V_T=0.3V
- Lch=0.3 um
- Ldrift=8 um

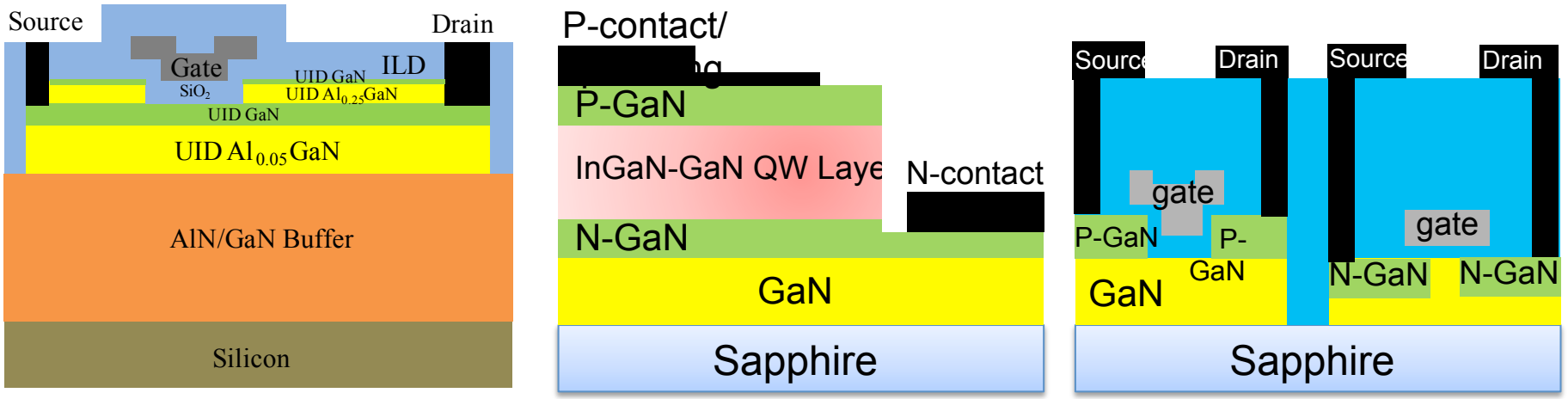




Z. Li and T.P. Chow, ISPSD 2012

Optoelectronic IC Integration

The ability to use Silicon as a substrate for LEDs will lead to a lower overall cost. To prepare for this paradigm shift, we have included research on GaN-MOS-HEMTs built on a Silicon substrate.

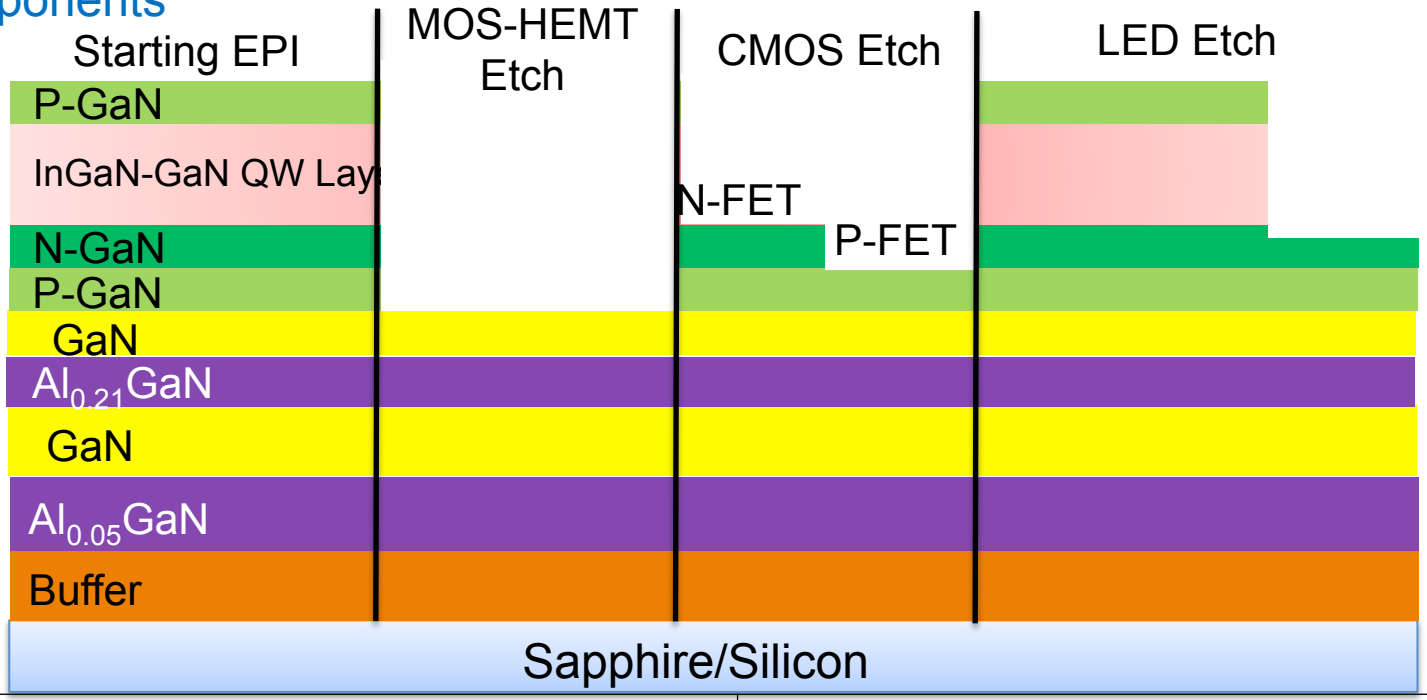


Left to Right: MOS-HEMT structure for GaN on Silicon, Current LED structure, Proposed GaN-CMOS structure.

GaN controls and power FETs will enable high frequency and high efficiency switching for data and power conversion applications

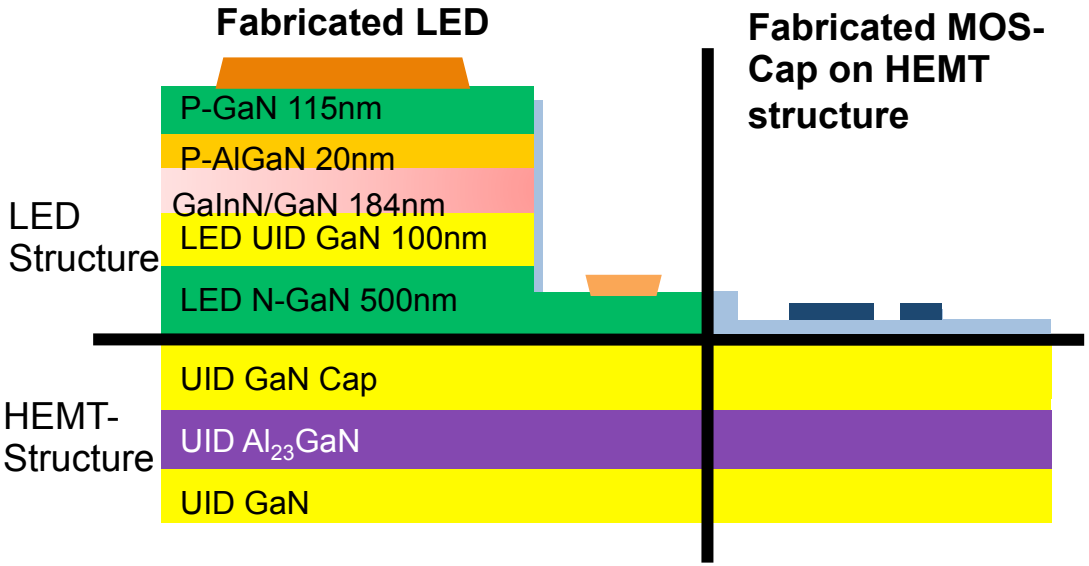
Integration Approaches

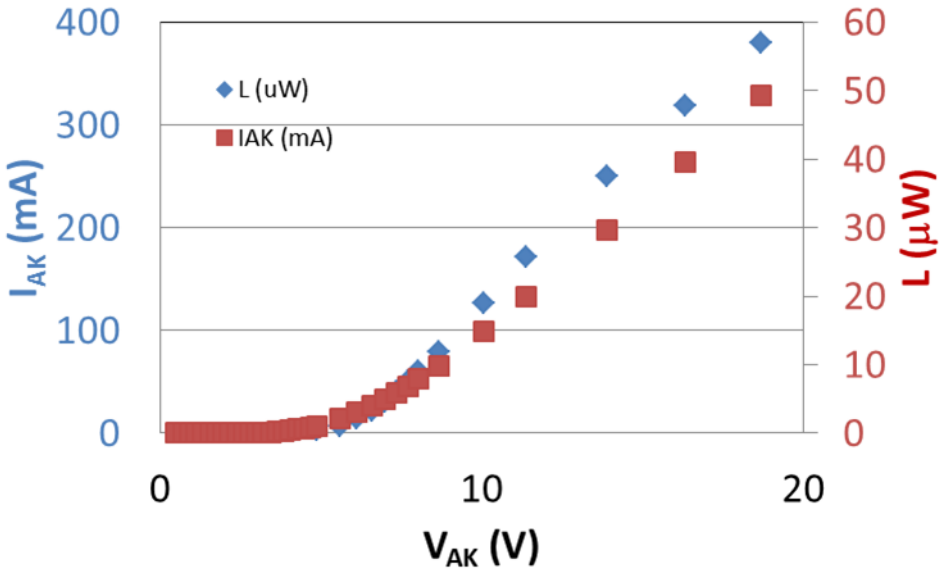
First: Grow wafers with necessary EPI layers, use subtractive etching to make components



Advantages	Risks
High temperature steps of layer growth complete before processing	Thermal budget of processing may be incompatible
	Highly non-planar, lithography obstacle
	Larger thermal path for cooling LEDs
	Need selective or high controlled etch to hit depth

Experimental Results





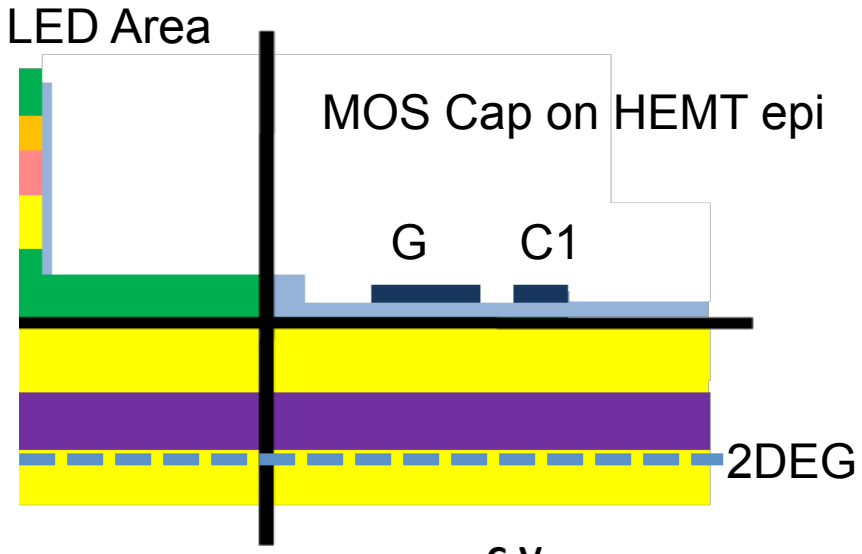
Monolithic Integration

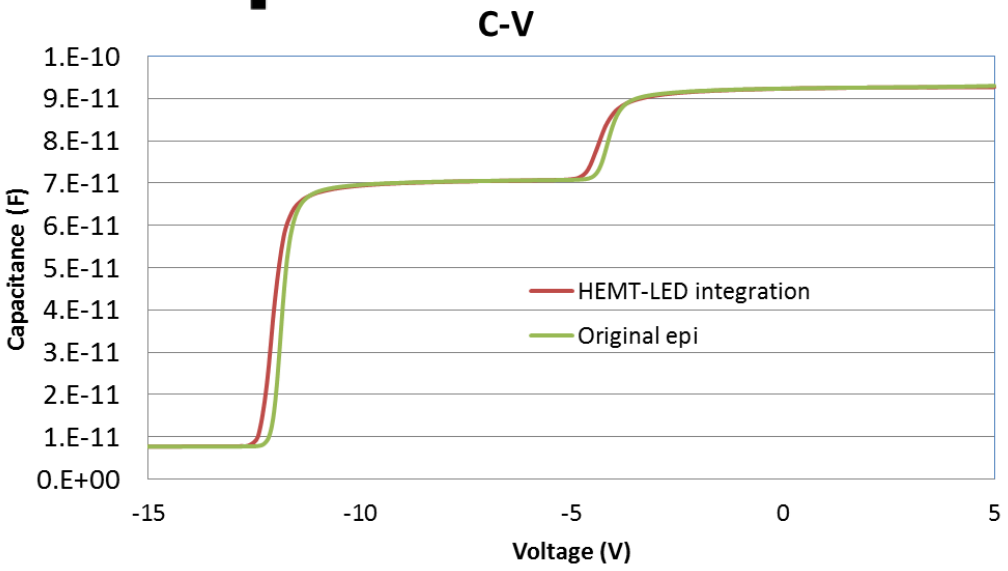
LED structure successfully grown on HEMT-structure

- Initial tests show functioning LEDs
- Evaluation of HEMT structure underway via MOS-capacitors

Collaboration with Wetzel (S1.2.2) gives flexibility to grow LEDs on HEMT structure without degrading 2DEG (2D electron gas)

Process compatibility





Monolithic Integration

- LED epi selectively etched to fabricate MOS capacitors on HEMT structure
- Etch depth controlled to prevent removal of GaN Cap (20nm thick despite ~800nm etch)
- CΔV yields charge required to deplete 2DEG
- Growth cycle of LED epi did not compromise concentration of 2D electron gas (2DEG)
  - 2DEG of Original epi: 3.2e12/ cm^2
  - 2DEG of HEMT/LED epi: 3.0e12/cm^2

References

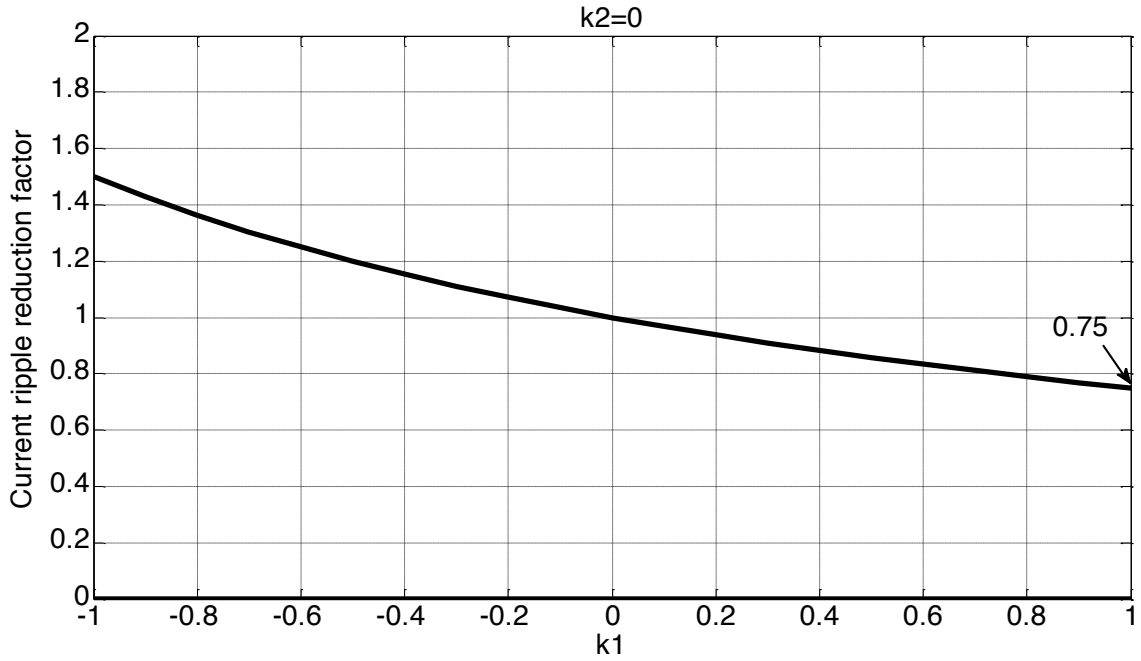
- H. Peng, and M. M. Hella, “100 MHz CMOS DC-DC Converter with Light Load Efficiency Enhancement,” under review, IEEE Trans. on circuits and systems.
- H. Peng, V. Pala, T.P Chow, and M. M. Hella, “100 MHz, 85% Efficient Integrated AlGaAs/GaAs Supply Modulator for RF Power Amplifier Modules,” accepted for presentation, APEC 2013, Long Beach, CA, March 2013.
- H. Peng, I. D-Anderson, and M. Hella, “A 100 MHz Two-Phase Four Segment DC-DC Converter with Light Load Efficiency Enhancement in 0.18 μm CMOS Technology, ” IEEE Custom Integrated Circuits Conference CICC, San Jose, CA, September 2012.
- H. Peng, V. Pala, P. Wright, T. P. Chow, and M. M. Hella, “High Efficiency, High Switching Speed, AlGaAs/GaAs P-HEMT DC-DC Converter for Integrated Power Amplifier Modules. J. Analog Integrated Circuits and Signal Processing. Volume 66 Issue 3, pp. 331-348, March 2011.
- H. Peng, V. Pala, T. P. Chow, and M. M. Hella, “A 150MHz, 84% efficiency, Two Phase Interleaved DC-DC Converter in AlGaAs/GaAs P-HEMT Technology for Integrated Power Amplifier Modules. IEEE Radio Frequency Integrated Circuits Symp. RFIC, Anaheim, CA, May 2010, pp. 259-262.
- H. Peng, T.P. Chow, and M. Hella,"A Highly Efficient Interleaved DC-DC Converter using Coupled Inductors in GaAs Technology", IEEE International Symposium on Circuits and Systems ISCAS, Taiwan, 24-27 May 2009, pp. 2037-2040.

Thank You!

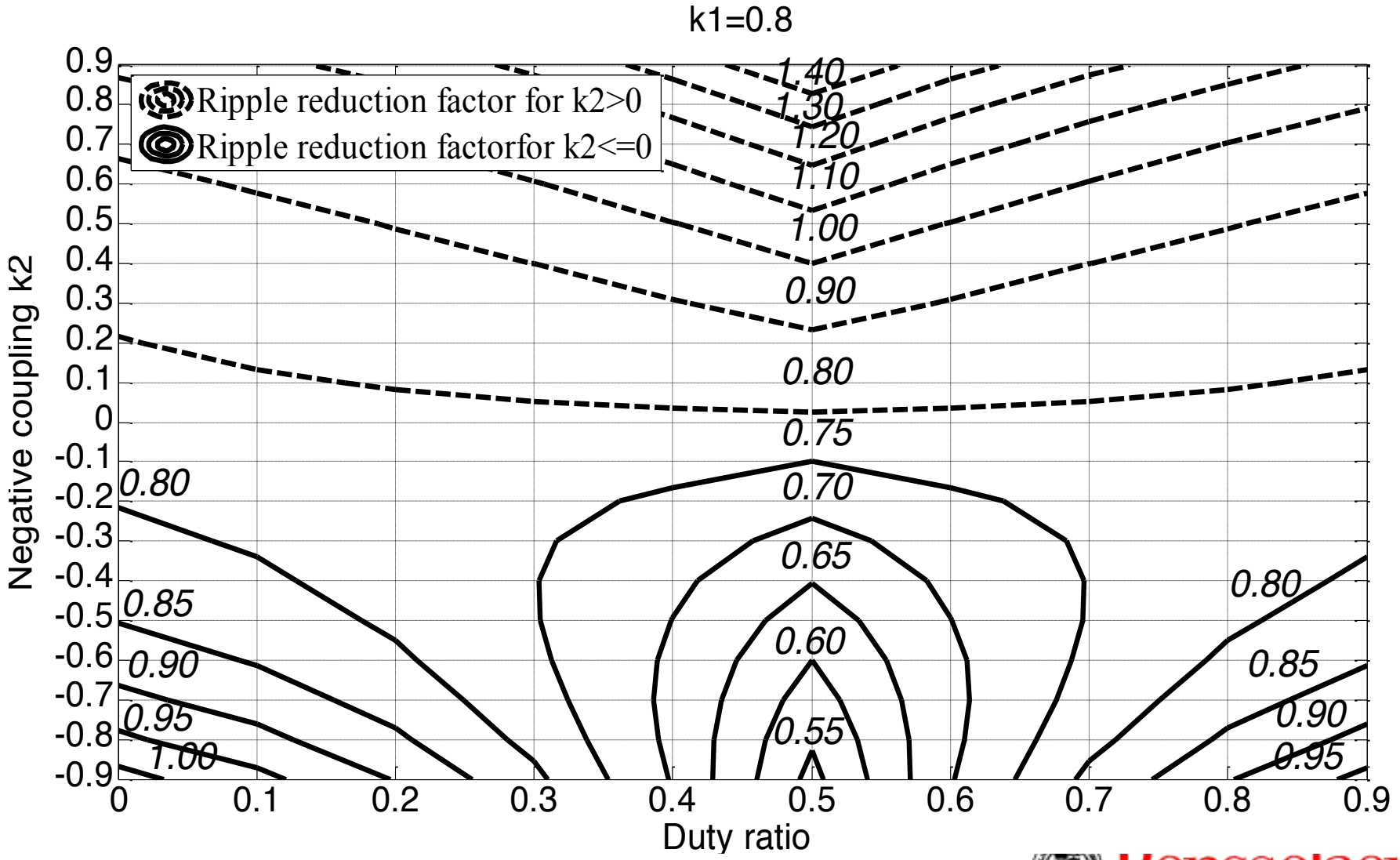
Any Question ?

Output Network

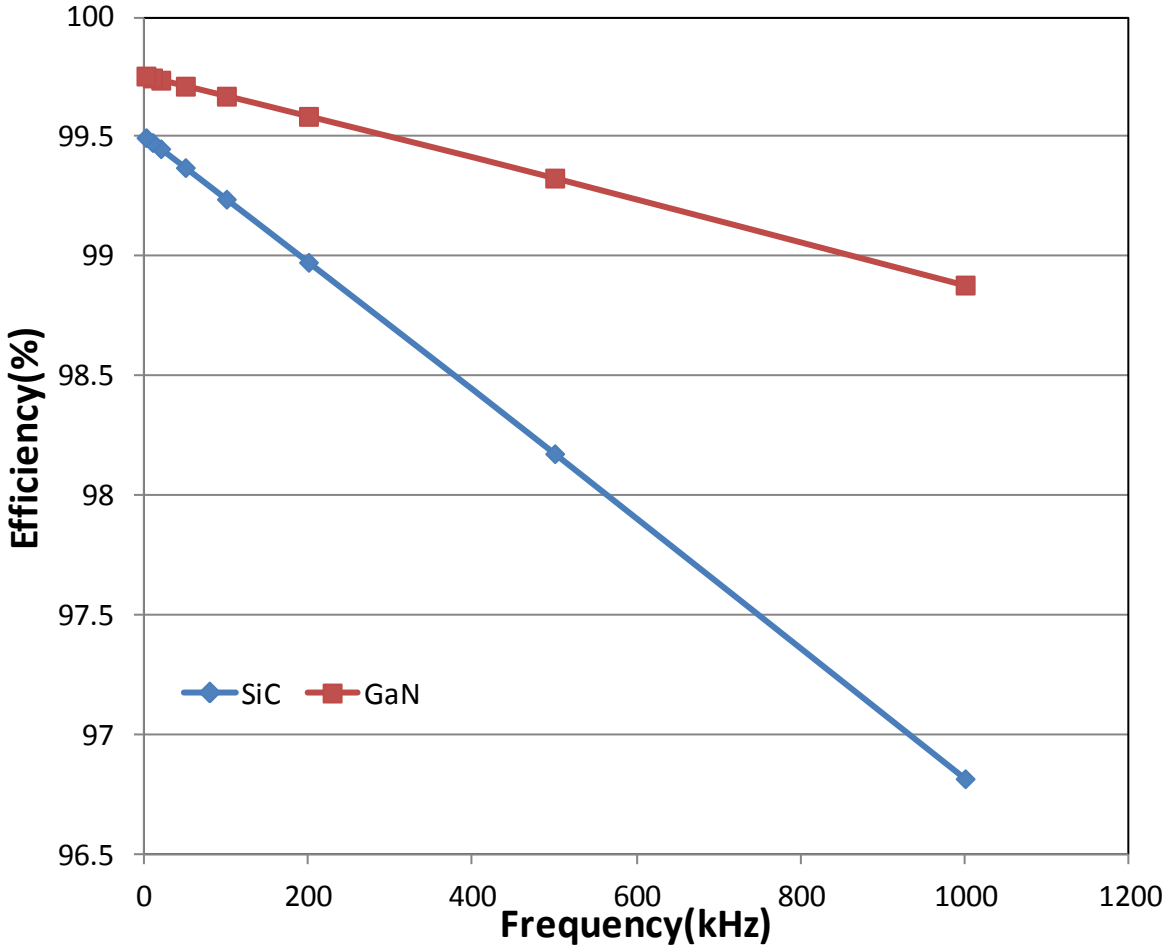
- Positive coupling (k1):
  - Larger k1 generates larger effective inductance.
- Negative coupling (k2):
  - Ripple reduction is correlated with duty ratio.



Effect of Coupling



Efficiency at Higher Freq.

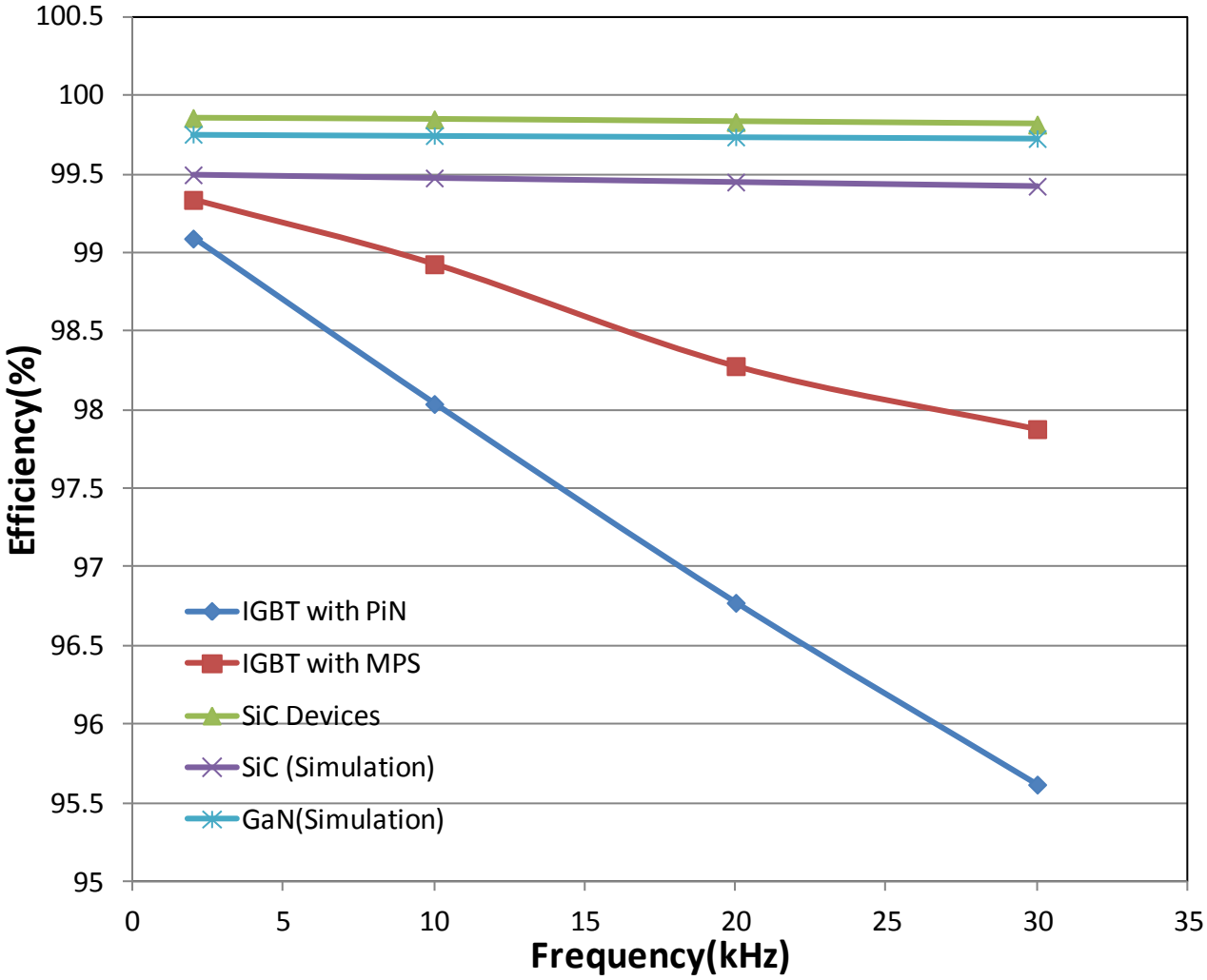


- Most of the losses coming from transistor.
- Diode and gate drive losses negligible.

Simulation

- SiC Simulation
  - Switching at 600V, 10A: Power ~6kW
  - Gate Drive: 0 to 20V
- GaN Simulation
  - Switching at 600V, 10A: Power ~6kW
  - Gate Drive: 0 to 5V (Gate turns on for Vg>5V)

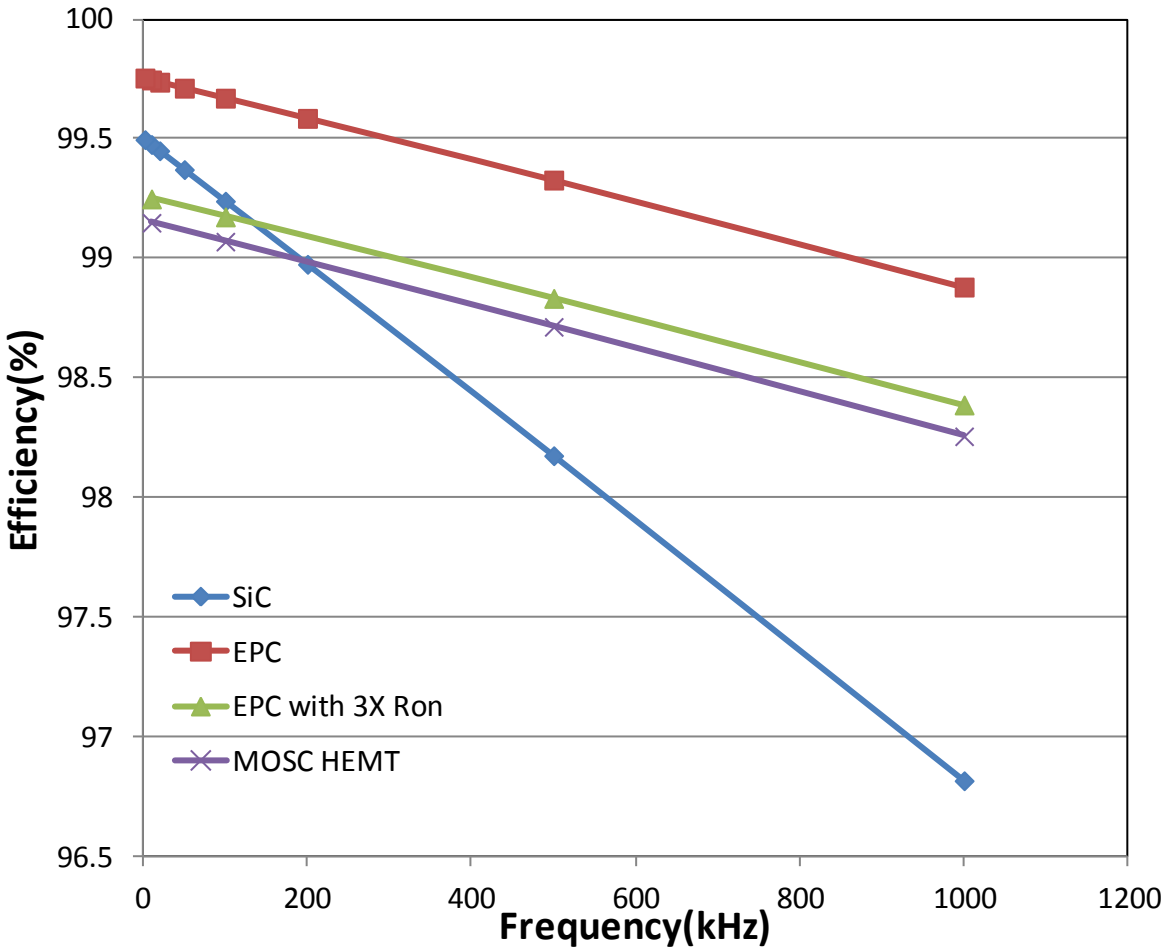
Efficiency Comparison



- Most of the losses coming from transistor.
- Diode and gate drive losses negligible.

Rensselaer

Efficiency


100
99.5
99
98.5
98
97.5
97
96.5
Efficiency(%)
0
200
400
600
800
1000
1200
Frequency(kHz)
SiC
EPC
EPC with 3X Ron
MOSC HEMT