High current high frequency Si MOSFET technology for power conversion

Steven Sapp, Jon Gladish, Art Black, Ashok Challa, Gary Dolny

PwrSOC 2012

Solutions for Your Success™

Outline

- High current trench MOSFET performance merits
- The evolution of higher operating frequency trench power switches
- Comparative study of trench and competing high current alternatives
- Power-loop issues and comparisons for high frequency operation
- State-of-the-art power switch devices and packages for 1+ MHz high current applications
- Conclusion

The message:

For POL power conversion, silicon trench switches in conjunction with improved package techniques will continue to advance the high power density* performance edge resulting in dominant package integrated systems.

* *Power density is used loosely to indicate both reduced power loss in the MOSFET switches and area reduction resulting from filter inductor and capacitor size reduction resulting from co-packaging and increased operating frequency.*

Si Trench FET a candidate for Power SiP/SoC?

- Characterization comparisons indicate that Trench MOSFET devices are improving and capable of operating at higher frequency with significantly higher current density compared to lateral devices.
- Higher operating frequency is needed to enable better system in-package (SiP) or system-on-chip (SoC) power converters.
- High current and frequency operating conditions require switching devices with better R*Q merit.
- Lower power loop parasitic L and R enable Si trench switches to perform closer to the levels expected based on their R*Q merit.
- Switching losses increase with frequency making conduction loss less prominent - but not less! At least not unless resistance in the overall power loop decreases too.

Definitions:

SG-Trench: shielded-gate trench with or without charge-balance.

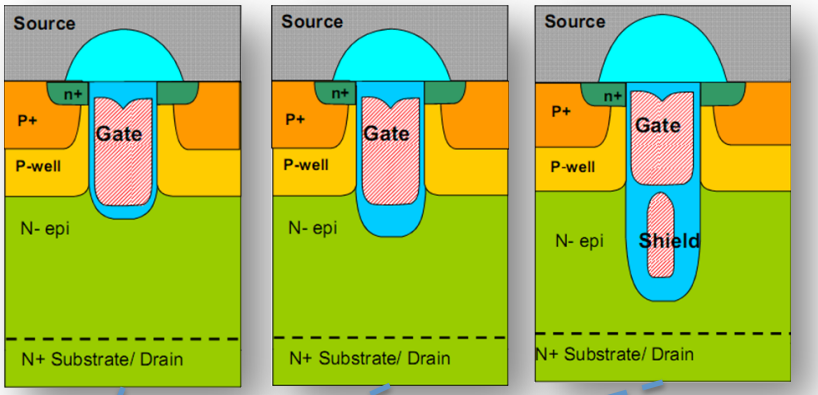
V-LDMOS: LDMOS device with source or drain connected through the substrate.

BV-R_{DS} fundamental trade-off

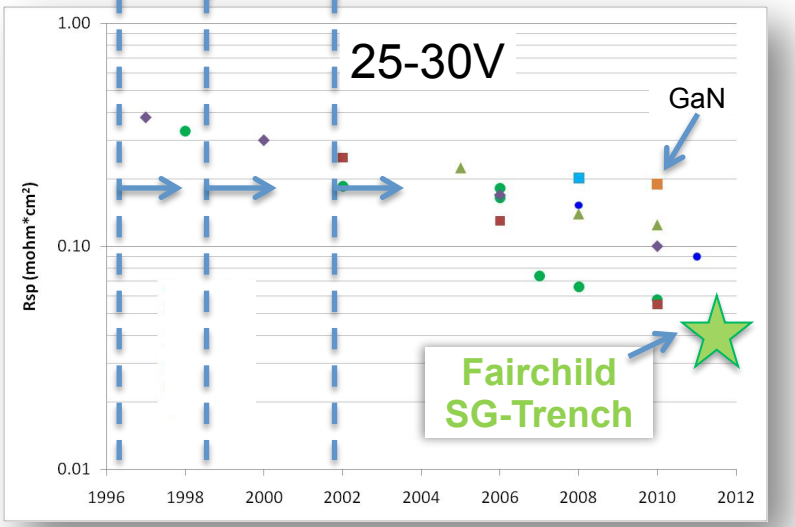
- Conduction loss due to on-resistance increases as the power switch voltage rating increases.
- Charge balanced Si, and wide band gap materials enable reduced conduction loss.
- V-LDMOS has not demonstrated competitive R_{SP}. Better quoted R_{SP} do not include metal contribution.
- GaN R_{SP} not currently competitive with Si below 150V but it provides lower Q at the same BV and R_{DS}. The gap between material capability and current performance suggests improvement possibilities.

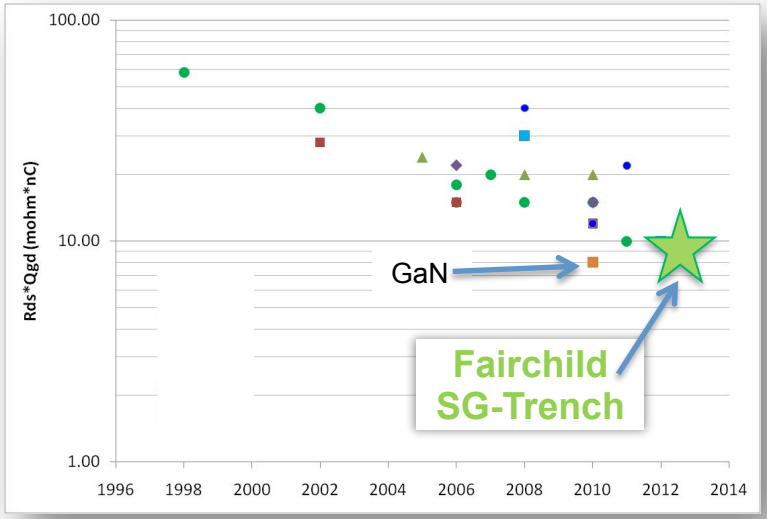
FAIRCHILD SEMICONDUCTOR®

Trench technology evolution



- The focus on reducing switching losses has driven Si trench MOSFET devices to better R_{SP} and $R*Q_{GD}$ FOM.
- Today's discrete low voltage GaN has poorer R_{SP} compared to silicon trench but better $R*Q_{GD}$ FOM.
- SG-Trench will continue to improve to enable higher performance SiP.

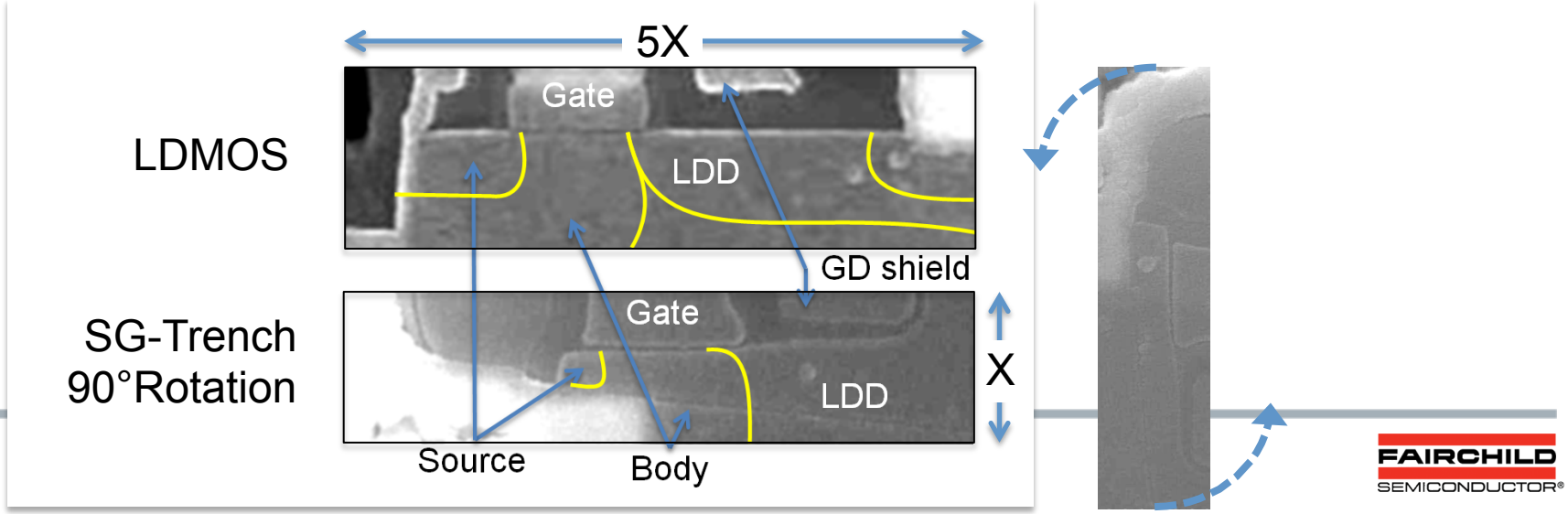




FAIRCHILD SEMICONDUCTOR®

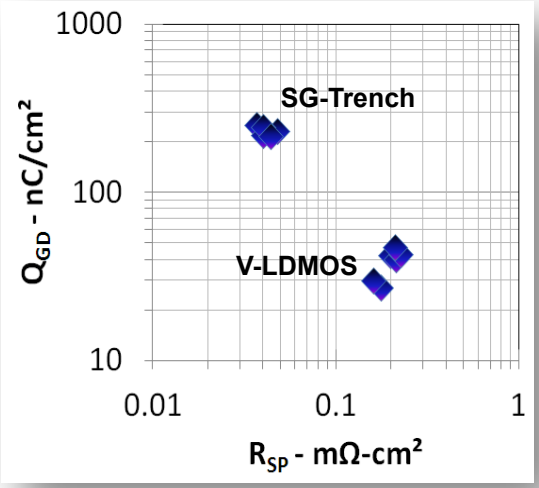
SG-Trench optimization influences

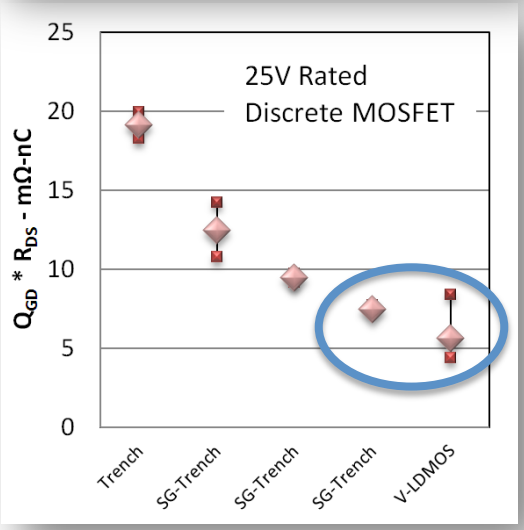
- SG-Trench and LDMOS share similar device architecture but trench consumes only 20% of the silicon surface area.
- Critical overlap dimensions for switching figure-of-merit (FOM) are controlled by different processes.
- SG-Trench MOSFET has demonstrated continuously improving switching FOM. Improvements are not driven so much by photo capability but instead by other process tools that continue to evolve and improve.
- LDMOS electric field control relies on RESURF while SG-Trench employs capacitive effect charge balance for reduced drift resistance.
- Silicon area consumed by the LDMOS degrades power density.



FAIRCHILD SEMICONDUCTOR®

Switching FOM – the road to high frequency



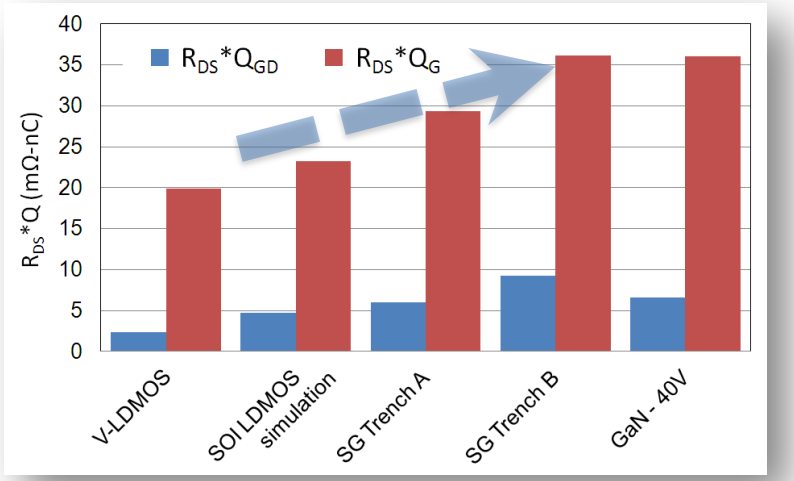


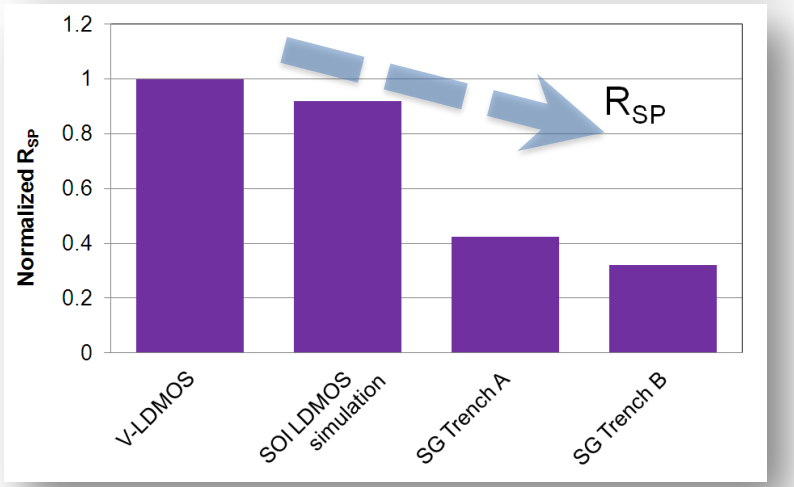
- SG-Trench compared to V-LDMOS shows how differently these devices are optimized.
- The switching merit figure Q_{GD}*R_{DS} shows that SG-Trench and V-LDMOS are similar despite the device design differences.
- While a lateral MOSFET has somewhat better switching FOM, the R_{SP} penalty degrades power density.
- Toward to goal of improving SiP solutions, SG-Trench devices can yield comparable performance to V-LDMOS.

FAIRCHILD SEMICONDUCTOR®

Switching - conduction FOM trade-off

- A comparison of device characteristics indicates a clear trade-off of switching and conduction loss features. As switching FOM improves, conduction FOM degrades.
- SG-Trench has improving switching FOM while maintaining much better R_{SP}.
- V-LDMOS technology shows better switching FOM but the power density is much lower compared to SG-Trench technology.

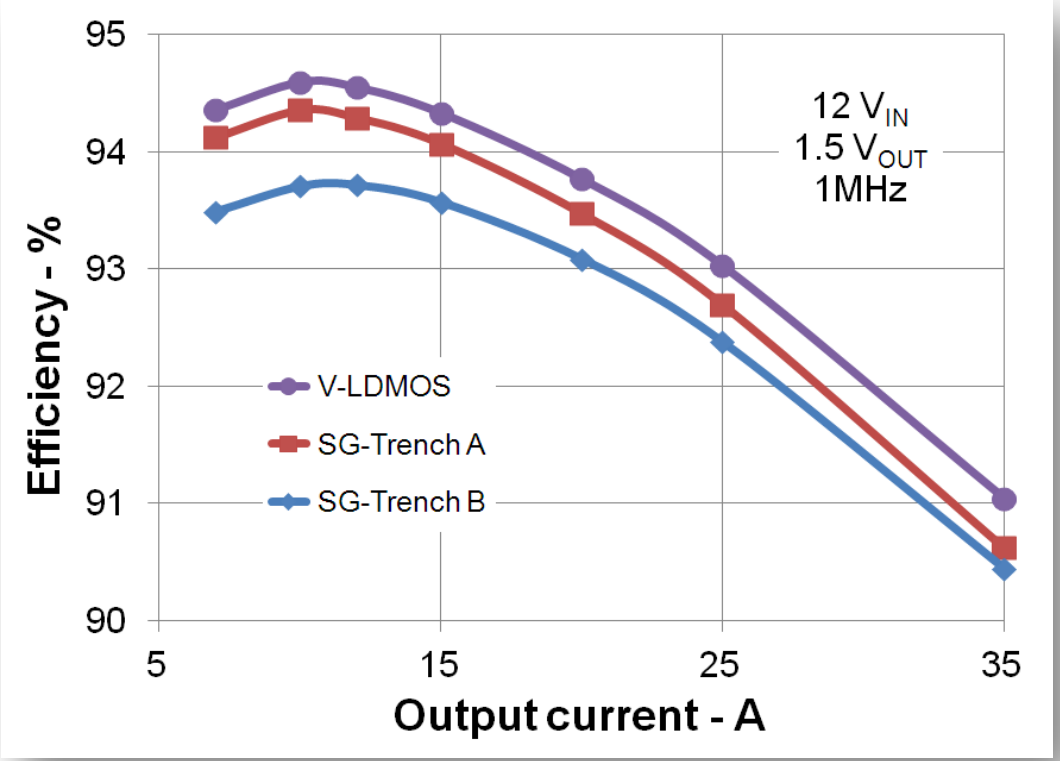




FAIRCHILD SEMICONDUCTOR®

Simulated efficiency

- A comparison of simulated efficiency using switches with features described on the previous slide shows that performance ranks in same order as switching FOM.
- SG-Trench with improved switching FOM gives competitive efficiency and higher power density.
- The V-LDMOS requires 3x the power switch die size and may not fit in a comparable package.

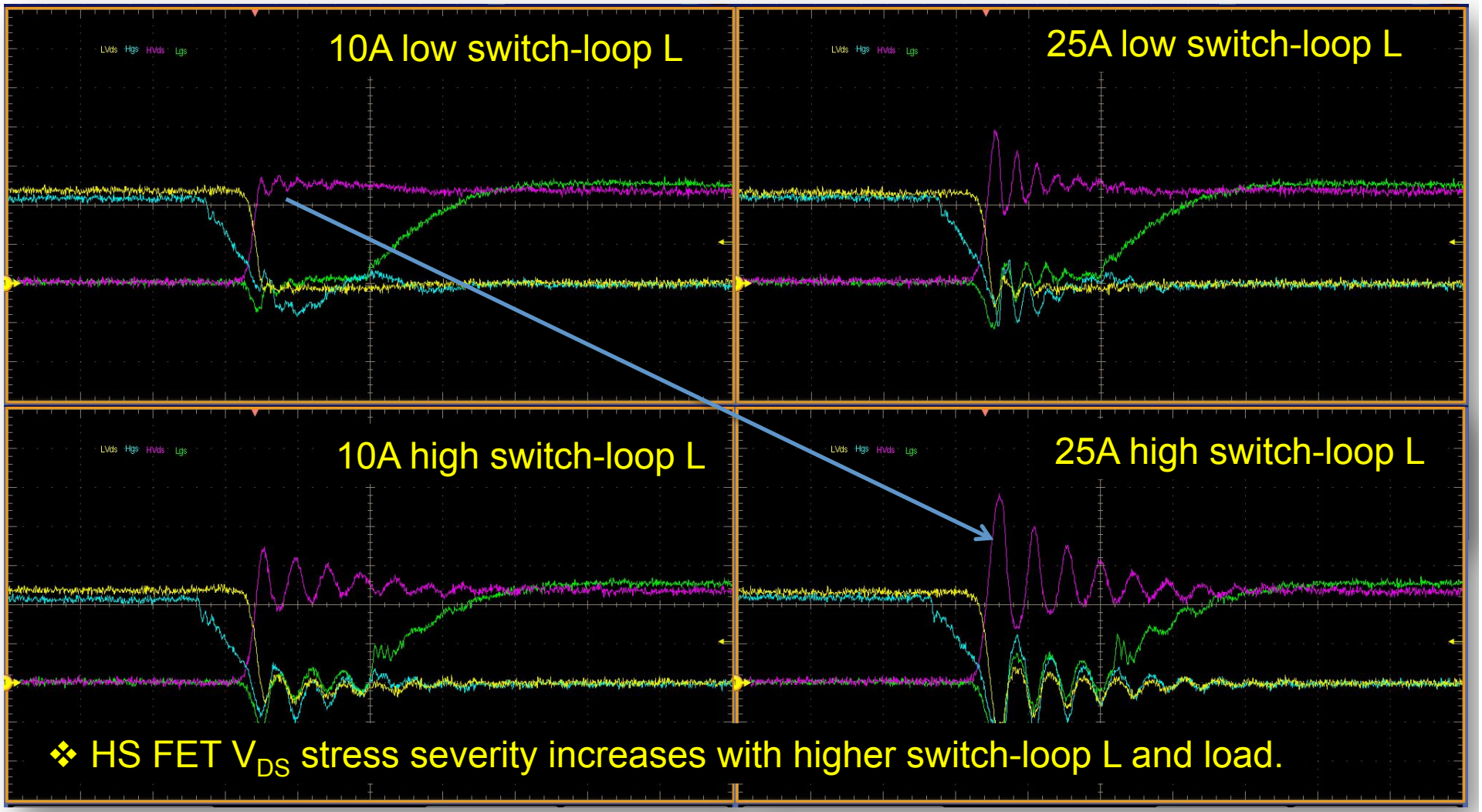


FAIRCHILD SEMICONDUCTOR®

Faster switching issues

- Voltage overshoot increases with faster switching. Power loop inductance from package interconnects and board traces interact with the switching transitions to cause voltage spikes - L di/dt.
- Small format co-packaged power switches will reduce switch loop parasitic inductance, both within the package and in the external HF switch loop.
- The primary benefit of reduced parasitic inductance is reduced HS switch V_{DS} peak over-shoot at full load.
- Fast switching trench MOSFETs may even be too fast for low inductance packages. Faster switching induces a higher voltage across the LS GS and GD capacitive divider leading to shoot-through loss.
- With better FOM (Si or GaN), HS V_{DS} stress increases and switch-node overshoot and ringing may lead to EMI.
- Power supply integration in a package or chip can enable lower parasitic inductance and enable the use of faster power switches.

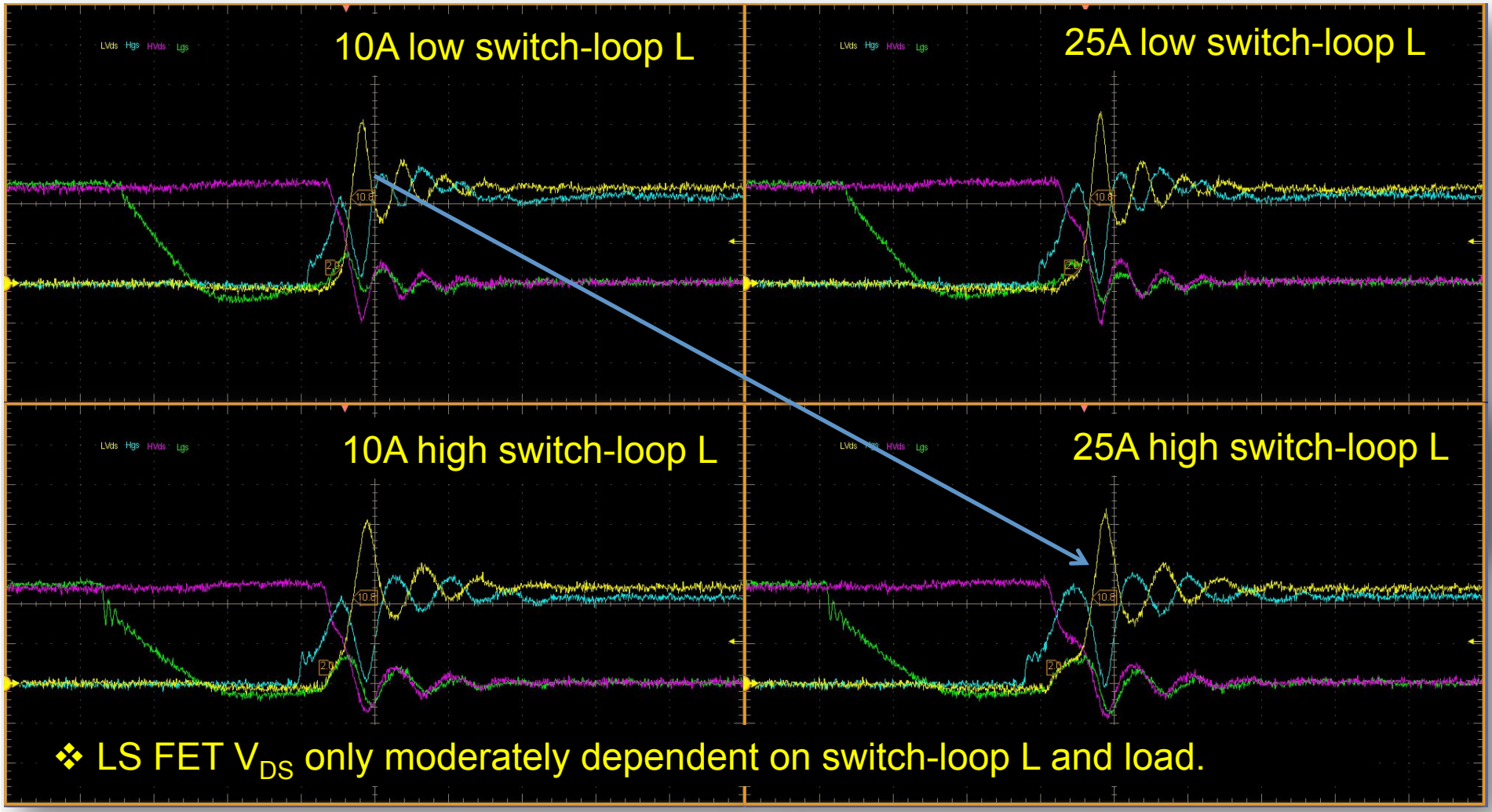
Switch-loop inductance impact on HS V_{DS}



❖ HS FET V_{DS} stress severity increases with higher switch-loop L and load.

FAIRCHILD SEMICONDUCTOR®

Switch-loop inductance impact on LS V_{DS}

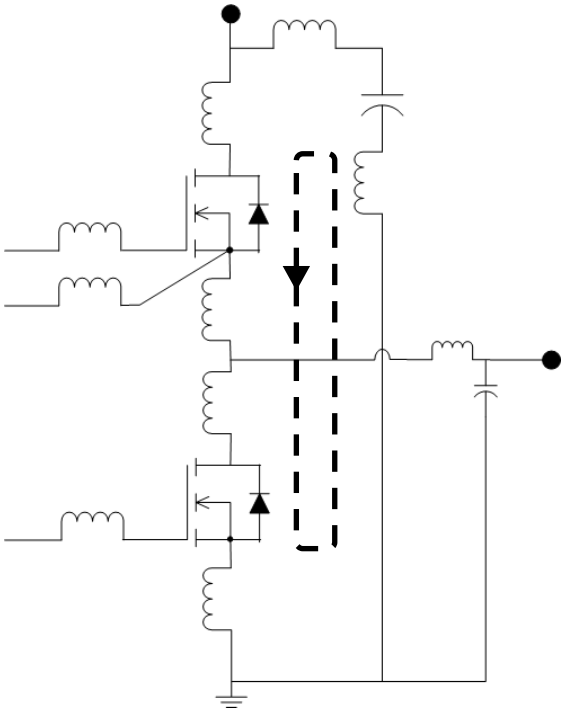


❖ LS FET V_{DS} only moderately dependent on switch-loop L and load.

FAIRCHILD SEMICONDUCTOR®

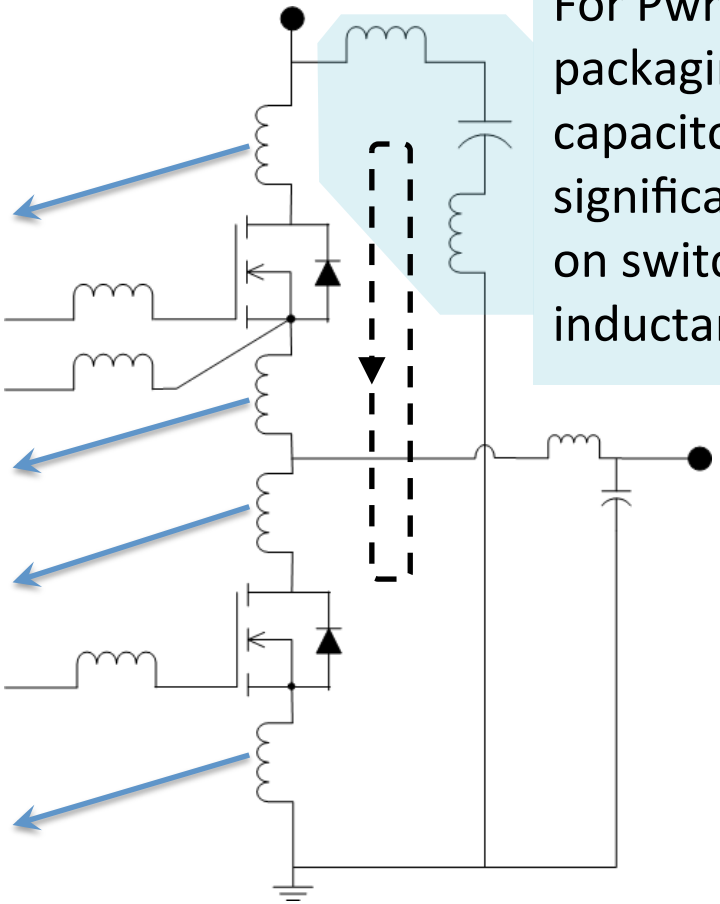
Package Inductance Improvement for PwrSiP

- For high frequency the package needs lower switch loop inductance and resistance to reduce switching and conduction loss.
- A copper clip from LS drain to HS source provides low impedance.
- Integration of other system components can reduce their series impedance.
- DrMOS integrates power switches with the gate driver to reduce drive loop impedance (HS source Kelvin reference).
- Lower loop impedance possible once integrated in a package or on a chip.



PWB, Package, and Interconnect

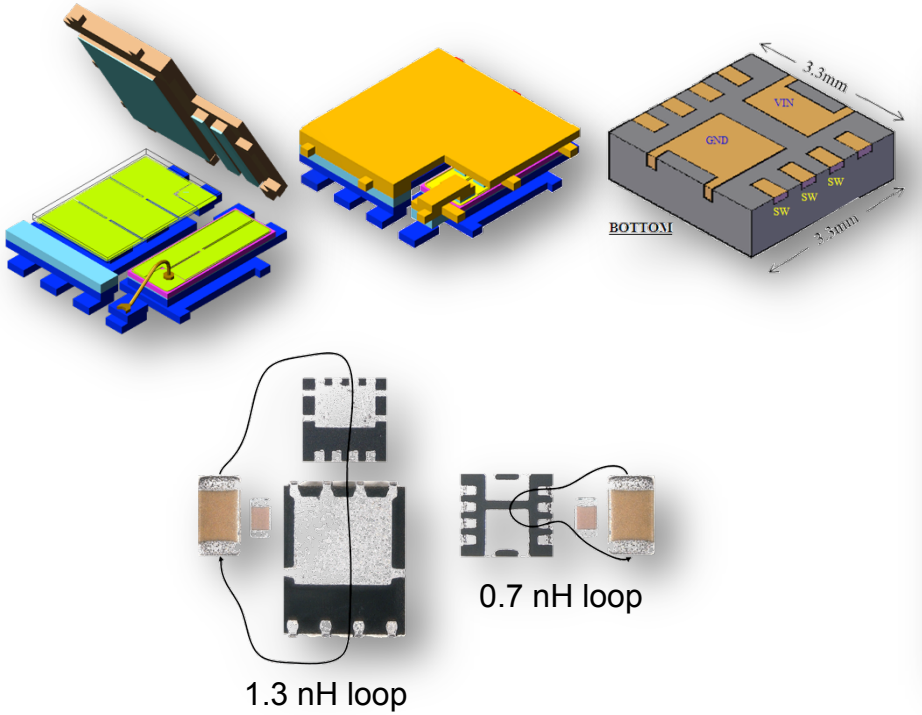
Discrete[1]	Power Stage[2]	DrMOS
0.003nH	0.009nH	0.009nH
5-20nH	5-20nH	1.2 & 1.2nH
0.8nH	0.15nH	0.15nH
0.003nH	0.003nH	0.003nH
5-20nH	5-20nH	1.2nH
0.8nH	0.07nH	0.07nH

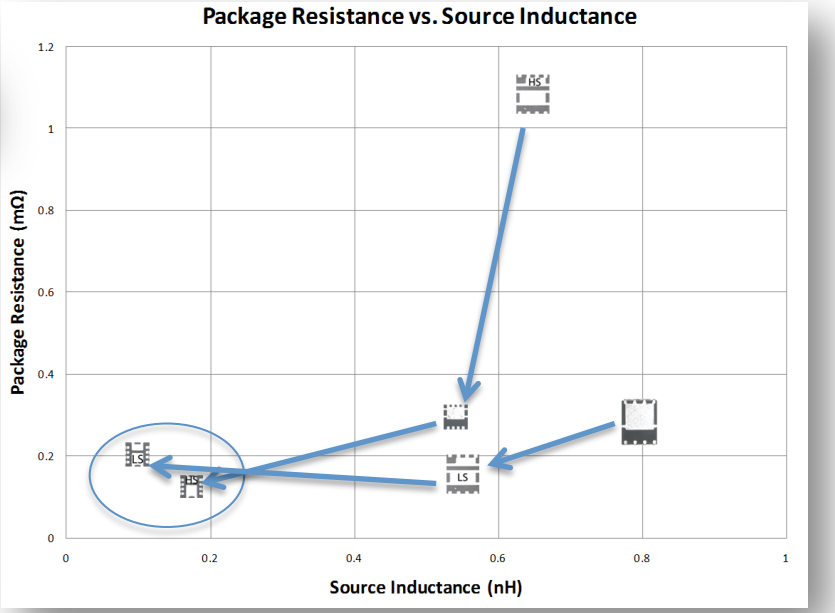


For PwrSiP co-packaging of input capacitor will have significant impact on switch loop inductance.

[1] Common connection and gate drive loop impedance depends on circuit board layout.
[2] Gate drive loop impedance depends on circuit board layout.

Power Stage: co-packaged HS and LS FETs



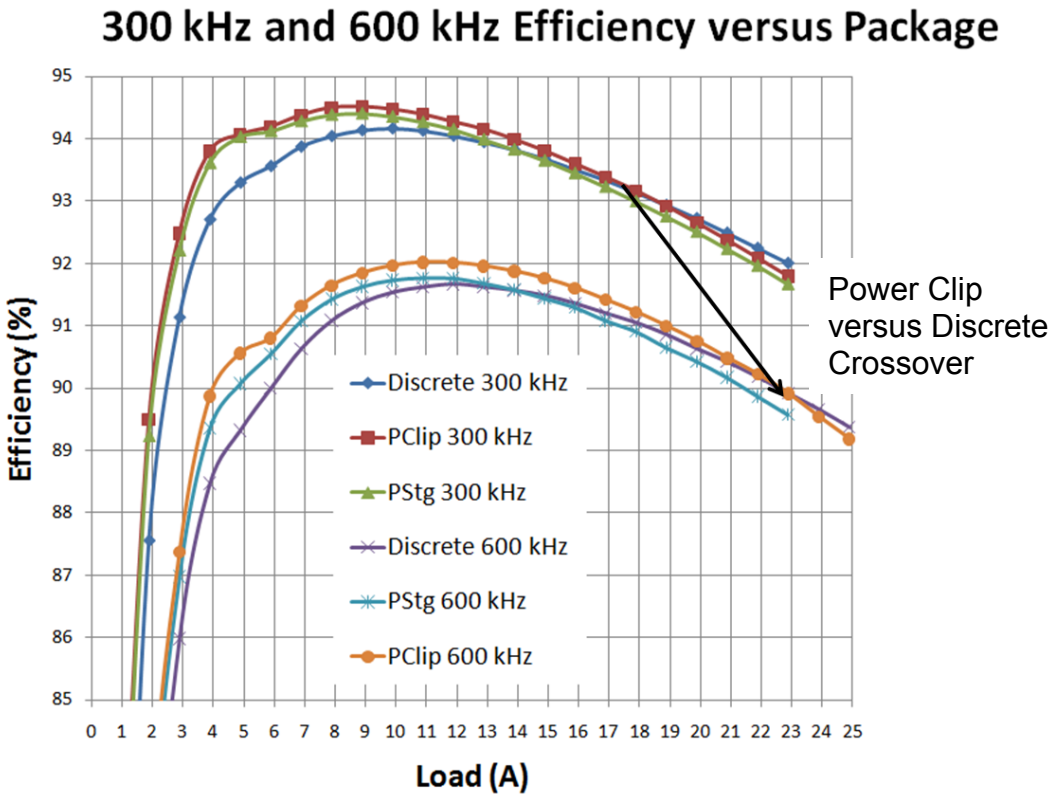


- Dual discrete packages are optimized for improved thermal performance and low package parasitic.
- Flip chip LS trench MOSFET results in a large portion of the exposed copper being connected to ground for low thermal resistance.
- A common clip connecting HS source to LS drain and switch-node results in very low parasitic resistance and inductance.
- Smaller package size leads to 2x reduction in switch loop inductance.

FAIRCHILD SEMICONDUCTOR®

Power Stage performance data

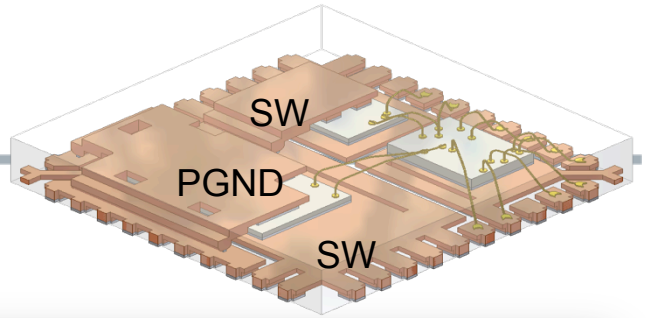
	Large Footprint		Med Footprint		Small Footprint	
						
	Pwr 33 HS	**Pwr 56 LS**	**Pwr Stage HS**	**Pwr Stage LS**	**Pwr Clip HS**	**Pwr Clip LS**
VDS [V]	25	25	25	25	25	25
VGS [V]	12	12	12	12	12	12
R_{DSON} Typ.@4.5V_G [mΩ]	4.3	1.6	4.4	1.8	5.4	1.4
R_{DSON} Max.@4.5V_G [mΩ]	5.7	2.1	5.7	2.2	7.3	2.1
Q_G Typ. @4.5Vg [nC]	12	32	12	27	9	30
Q_{GS} Typ. @4.5Vg [nC]	3.0	8.2	3.3	8.2	2.6	9.3
Q_{GD} Typ. @4.5Vg [nC]	3.3	9.6	2.7	7.6	2.3	7.7
C_{OSS} Typ. [nC]	441	1270	448	946	332	1126

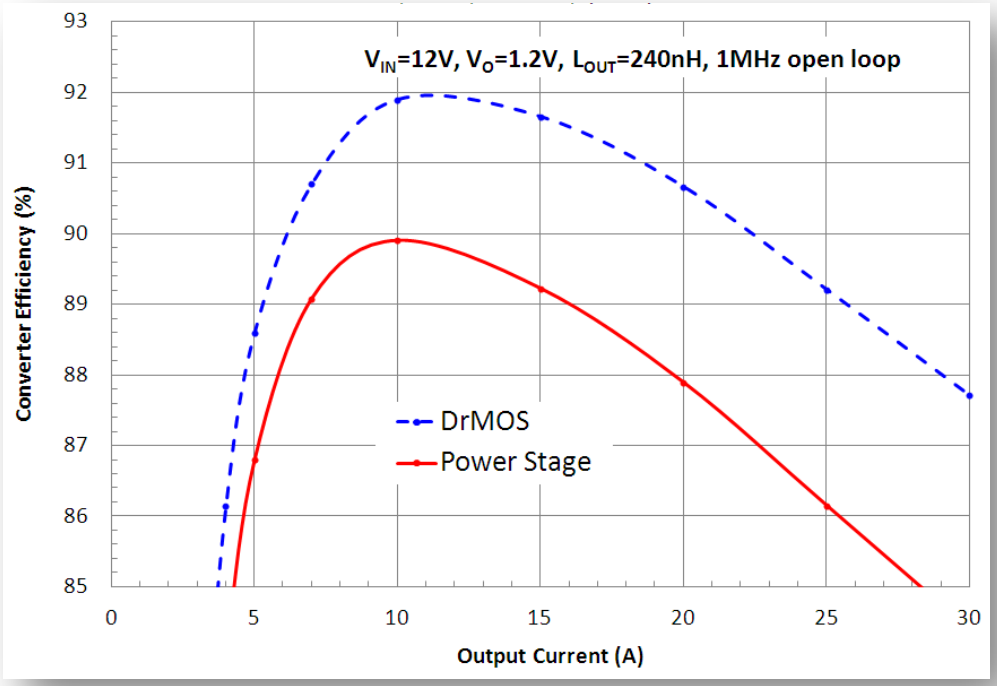


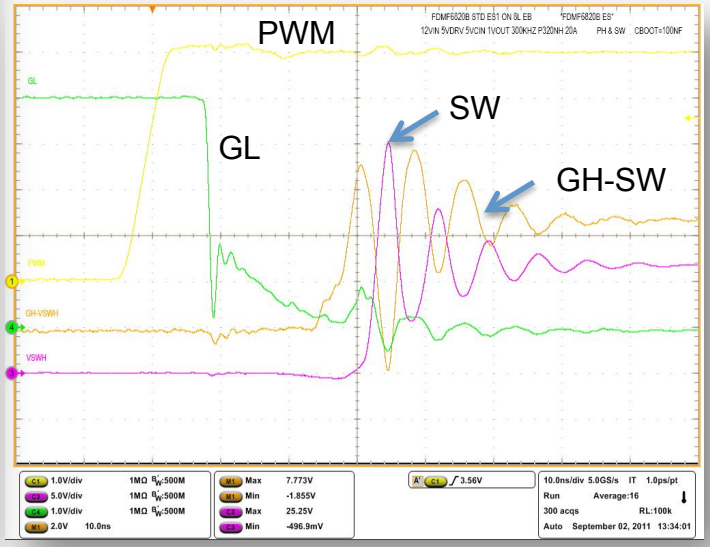
- With improved FOM silicon and improved package design, able to significantly shrink package while still maintaining low $R_{DS(ON)}$.
- Equivalent silicon in smaller package has better efficiency. Improvement is most dramatic at higher frequency.

FAIRCHILD SEMICONDUCTOR®

DrMOS Performance data







- Integrating the driver IC and Power MOSFETs into a common package greatly reduces V_{IN}-to-P_{GND} loop inductance and resistance as well as gate drive loop.
- The resulting predictable low inductance environment provides for extremely fast edge rates on SW-node and minimized dead time requirement.
- Even with a relatively low inductance package, ring voltages can still exceed 2x of V_{IN}.
- After driver and power switch integration, system level passive co-packaging, and ultimately integration on a chip can further improve the performance.

FAIRCHILD SEMICONDUCTOR®

Conclusions

- Trench Si switch technology continues to improve resulting in the most practical high current converter solutions for POL power conversion.
- Discrete solutions like Power Stage and DrMOS with high performance trench MOSFET switches are pushing power density and operating frequency higher.
- Package integrated converters utilizing high performance trench MOSFETs offer the promise of an even higher density power supply solution.