

High-frequency LDMOS in 0.18um BCD Technology for Power Supply-On-Chip

IL-Yong Park, Dongbu HiTek
Ashraf Lotfi, Enpirion

Introduction

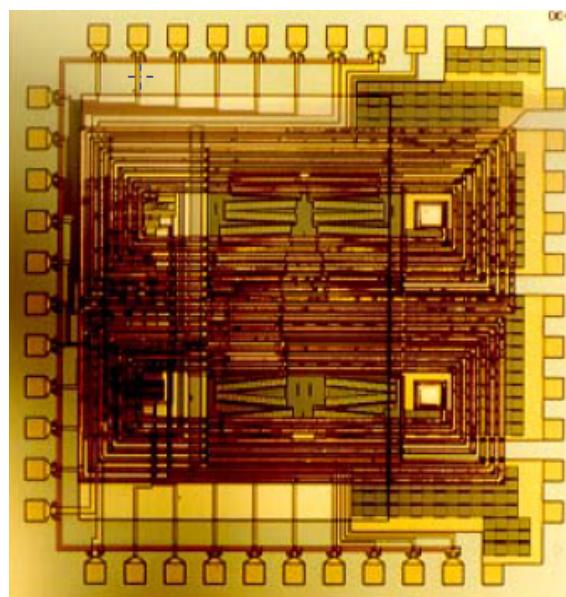
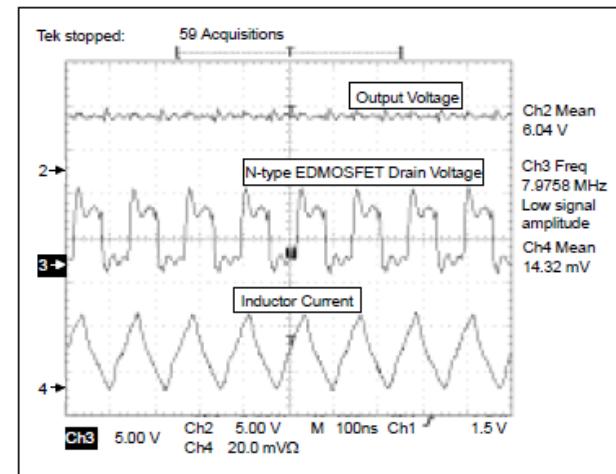
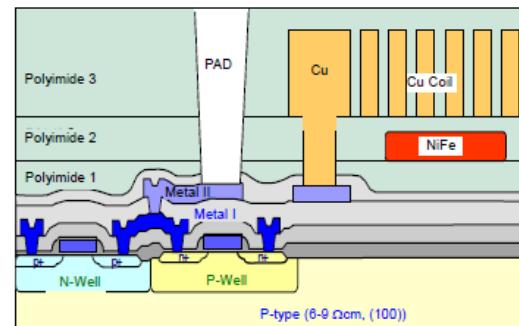
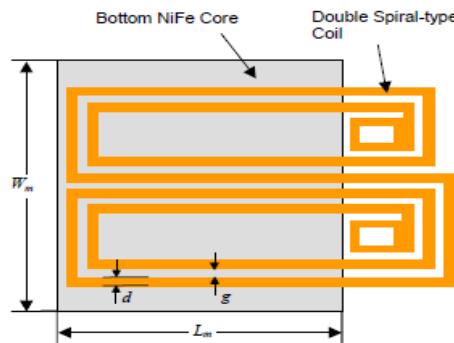
- DC/DC converter market requires high efficiency and high current driving capability
- Power SOC (Supply-On-Chip) requires
 - high efficiency and fast switching DC/DC converter
 - integrated passives (inductor)
- Fast switching DC/DC converter allows to reduce inductor size and increase the power density per unit volume

Introduction

- High frequency LDMOS achieves
 - low parasitic capacitance
 - fast switching speed realizing low switching power dissipation
 - DC power dissipation might higher than conventional low Rsp LDMOS
- Dongbu HiTek developed high frequency LDMOS with thin gate oxide, short gate length, high breakdown voltage in 0.18um Analog CMOS/BCD technology

Introduction

Monolithic DC/DC Converter (2002, ETRI)



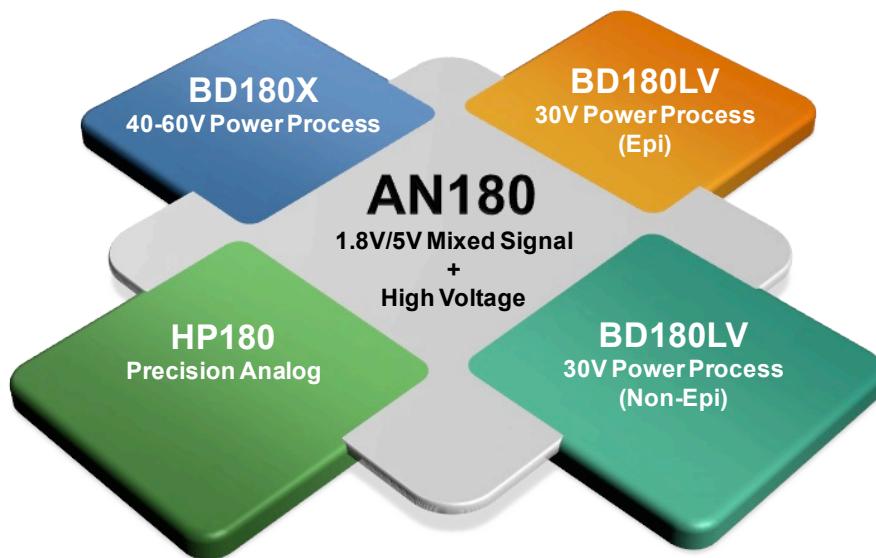
0.8um CMOS + DE(Drain-Extended)CMOS Process

Waveforms of FET switching voltage and thin-film inductor current when $V_i=3.5$ V, $V_o=6.0$ V, and the operating frequency was 8 MHz.

Micro inductor: 0.5 ~ 0.6 uH
Magnetic Material; NiFe (2.5um)

Power Efficiency: 72%

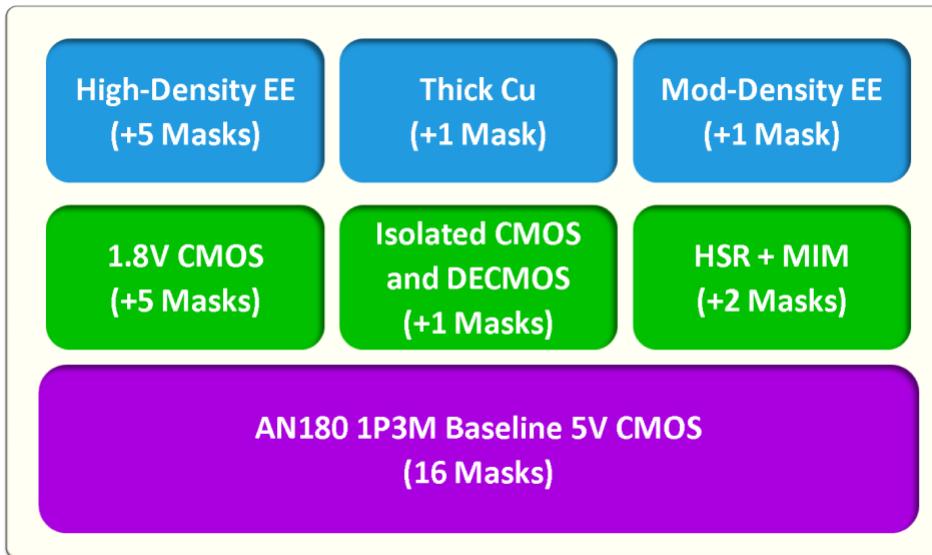
AN180 Process



<0.18um modular technology platform for power management application>

- Process Modularity
 - To save development time for the process and optimize the mask layer
 - Use 1 process platform and provide several process options
 - Process modularity is the Key feature
- * Currently BD180LV (non-epi) version merged into AN180

AN180 Process



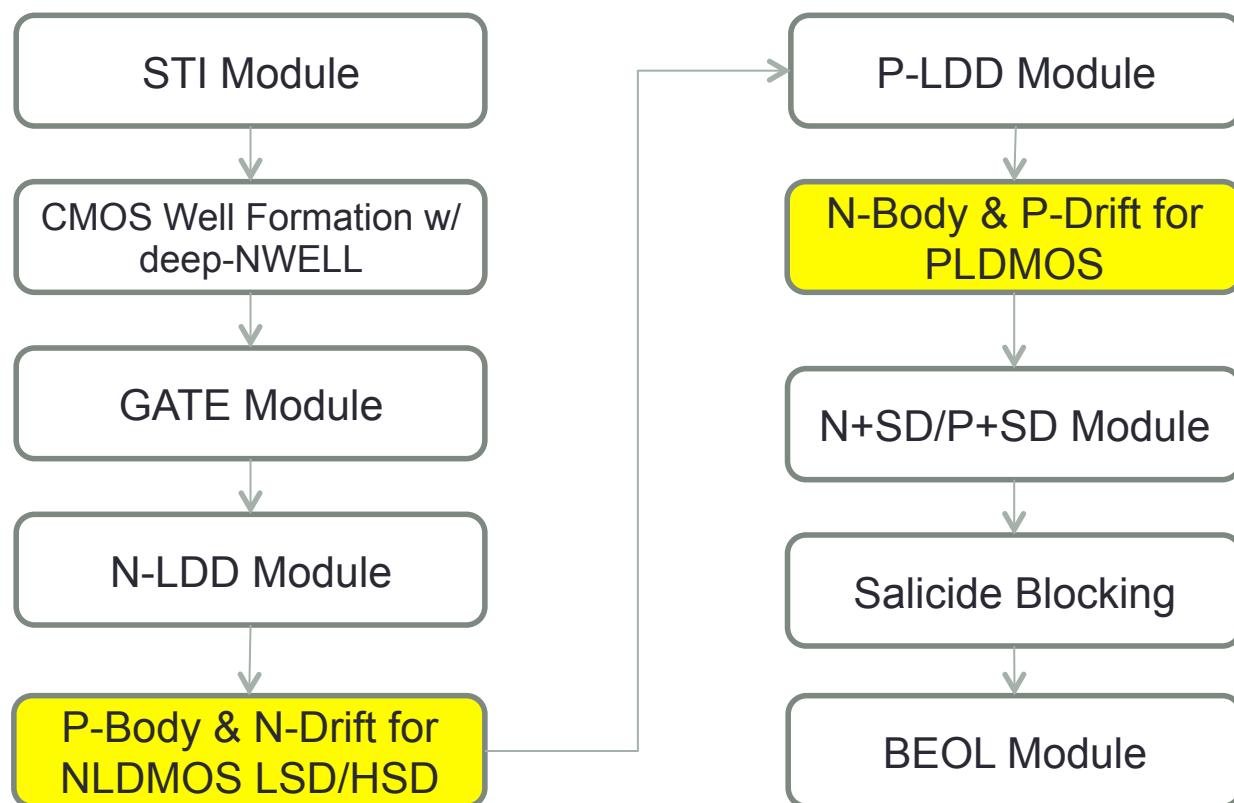
Process modularity of 0.18um 30V
AN180 process

- Process Modularity
 - 5V CMOS baseline
 - HVCmos and iso CMOS
 - 1.8V CMOS option
 - HSR, MIM option
 - Thick Cu option
 - Mod-density EEPROM
 - High-density EEPROM
 - **High Frequency LDMOS
(additional implants)**

Process Features

- 4 additional implant masks for HF-LDMOS;
 - 2 mask for NLDMOS
 - 2 mask for PLDMOS
 - No additional thermal budget → fully compatible with existing AN180 process
- For fast switching
 - 30Å thin gate oxide for V_{gs} power scaling
 - 0.26µm channel length
 - Drift implant after gate formation for small gate-to-drain overlap capacitance
- High driving current capability
 - Short channel length even at high drain voltage without punch-through
 - Optimized halo implant at source side

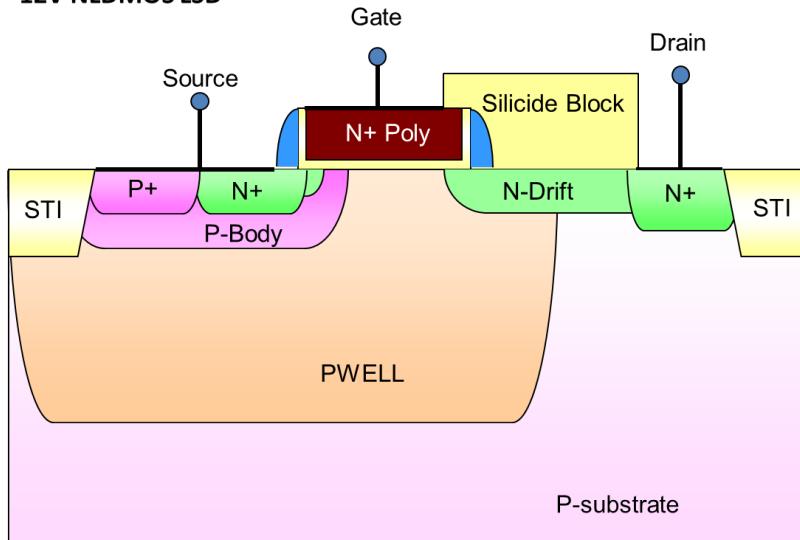
Process Flow



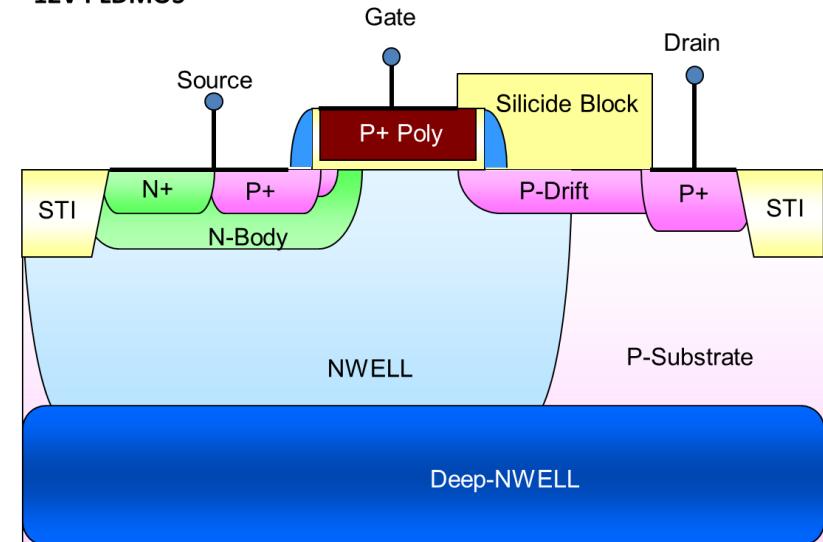
Additional implants for HF-LDMOS module

Device Structure

12V NLDMOS LSD



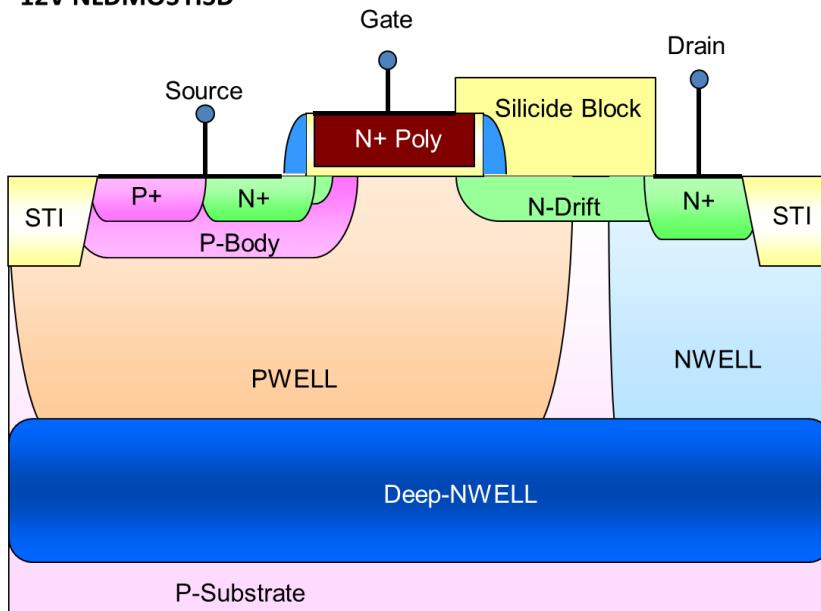
12V PLDMOS



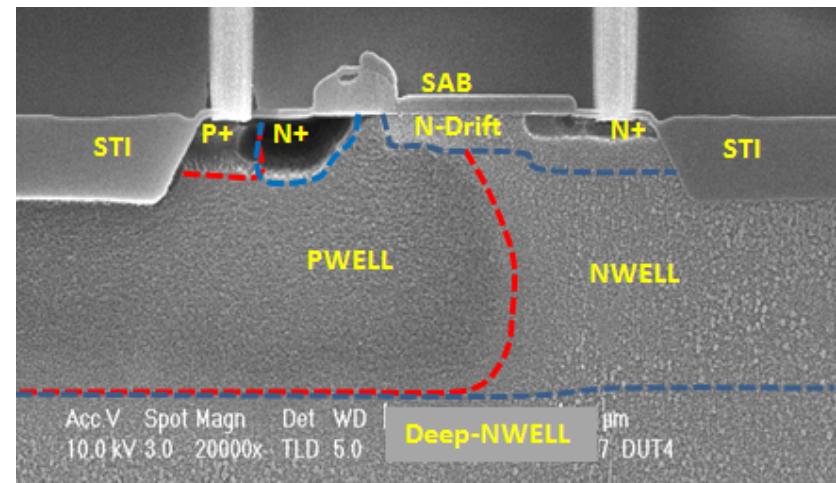
- Dedicated Implant Layers are used
 - 2 layers for P-Body and N-Drift of NLDMOS
 - 2 layers for N-Body and P-Drift of PLDMOS
- PWELL/NWELL extension
 - For the RESURF action, WELL is extended to the middle of drift region

Device Structure

12V NLD MOS HSD



<VSEM photograph of 12V NLD MOS>

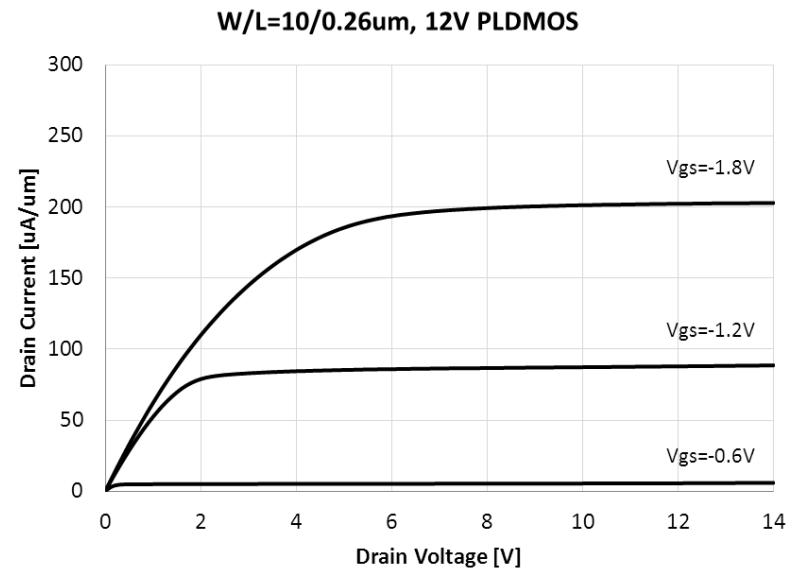
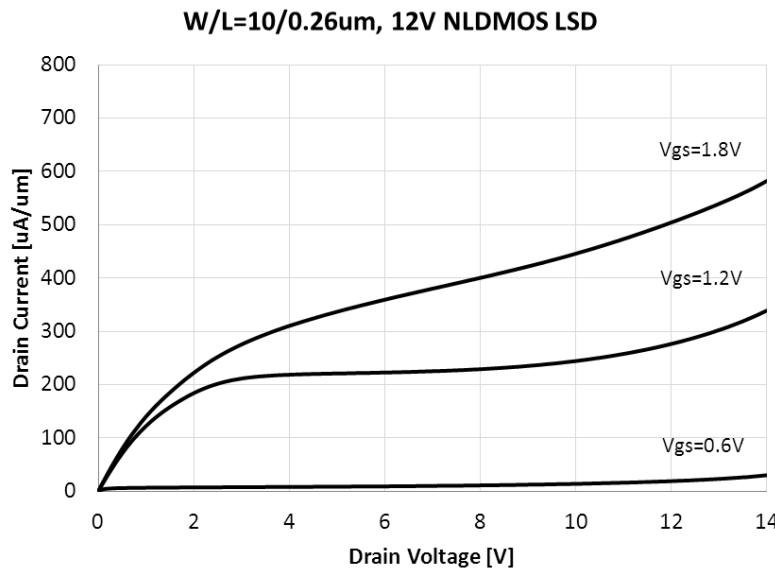


- Single-sided high tilt implant
 - To prevent punch-through breakdown even at high voltage of 20V
 - Source region width is limited by shadowing effect
- Optimized 2-step drift implant
 - At surface region of N-Drift for better HCI immunity

Summary of Electrical Performance

Parameters		Values		
		12V nLD LSD	12V nLD HSD	12V pLD
L_{CH}	μm	0.26	0.26	0.26
V_T	V	0.45	0.45	0.40
$I_{D,SAT}$	$\mu\text{A}/\mu\text{m}$	500	500	200
BV_{DSS}	V	20	20	20
R_{SP}	$\text{m}\Omega \cdot \text{mm}^2$	14	15	38
I_{OFF}	$\text{pA}/\mu\text{m}$	3	3	3
C_{ISS}	$\text{fF}/\mu\text{m}$	1.98	-	2.07
C_{OSS}	$\text{fF}/\mu\text{m}$	0.46	-	0.45
$F_{T,MAX}$	GHz	37.2	36.5	12.9
F_{MAX}	GHz	66.9	50	38.4

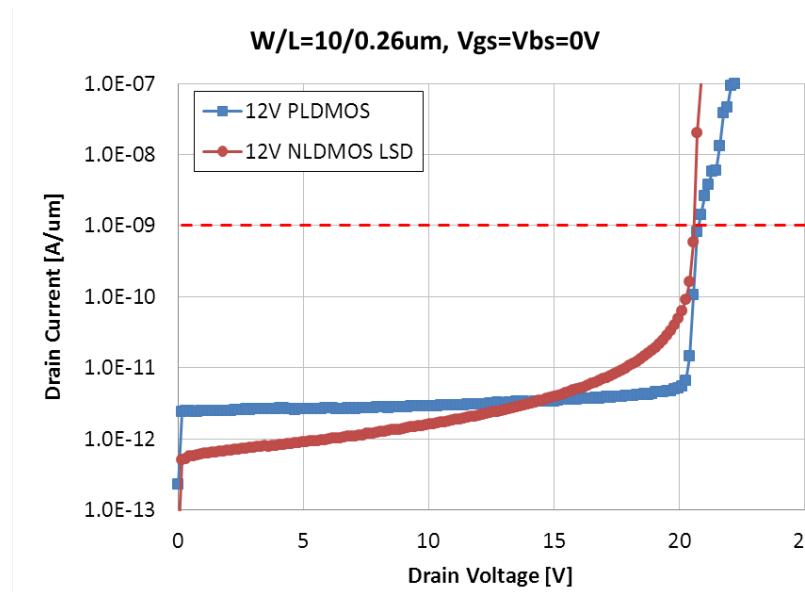
12V HF-LDMOS I-V Characteristics



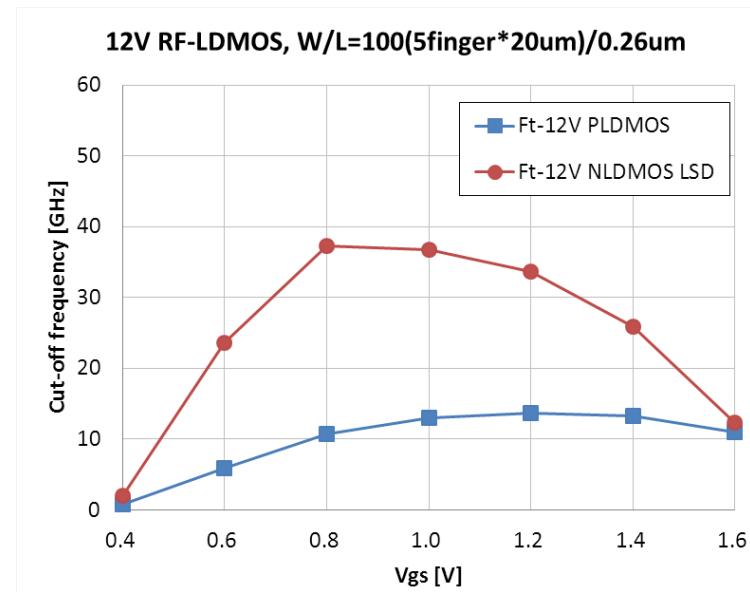
<DC output characteristics at V_{gs}=0.6V, 1.2V and 1.8V>

- Stable I-V characteristics up to 14V of V_{ds} at 1.8V of V_{gs}
 - On-state BV: 18.5V, Off-state BV: 20V
- Current capability
 - NLD MOS $I_{d,sat} = 500[\mu\text{A}/\text{um}]$ at $V_{gs}=1.8\text{V}$ and $V_{ds}=12\text{V}$
 - PLDMOS $I_{d,sat} = 200[\mu\text{A}/\text{um}]$ at $V_{gs}=-1.8\text{V}$ and $V_{ds}=-12\text{V}$

12V HF-LDMOS – BV_{dss} & F_t



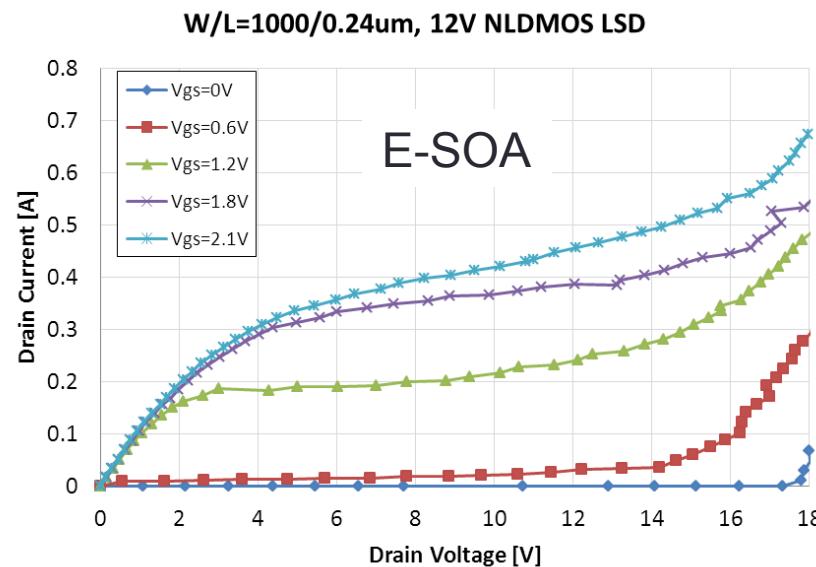
<Off-state breakdown characteristics>



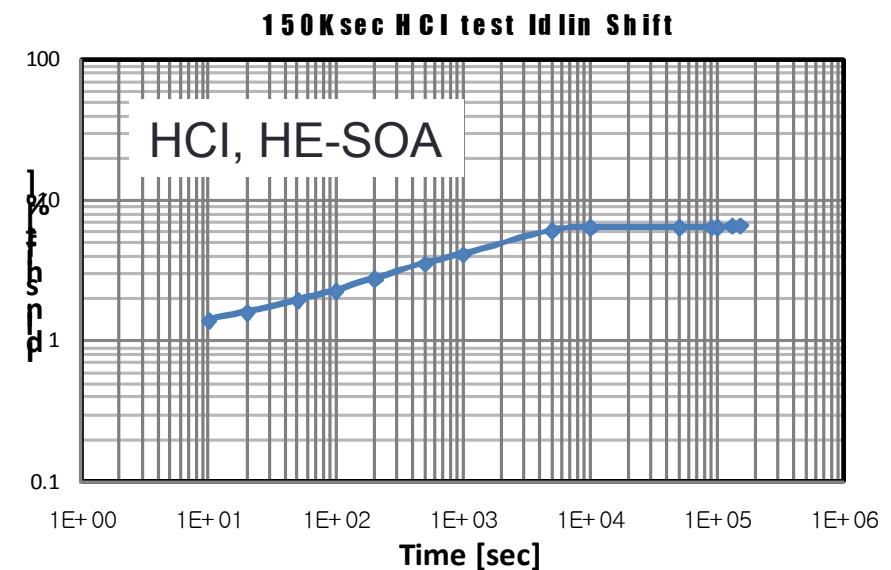
<Measured F_t vs V_{gs} at V_{dS}=6V>

- Over 20V off-state breakdown voltage with low leakage
 - 4A, 6A, 9A, 15A in production, 20A and 40V product in develop.
- F_t and F_{max} characteristics according to V_{gs} at V_{dS}=6V
 - F_{t,max}/F_{max} = 37.2GHz/66.9GHz for 12V RF NLD MOS LSD
 - F_{t,max}/F_{max} = 12.9GHz/38.4GHz for 12V RF PLDMOS

12V HF-LDMOS – Reliability (HCI)



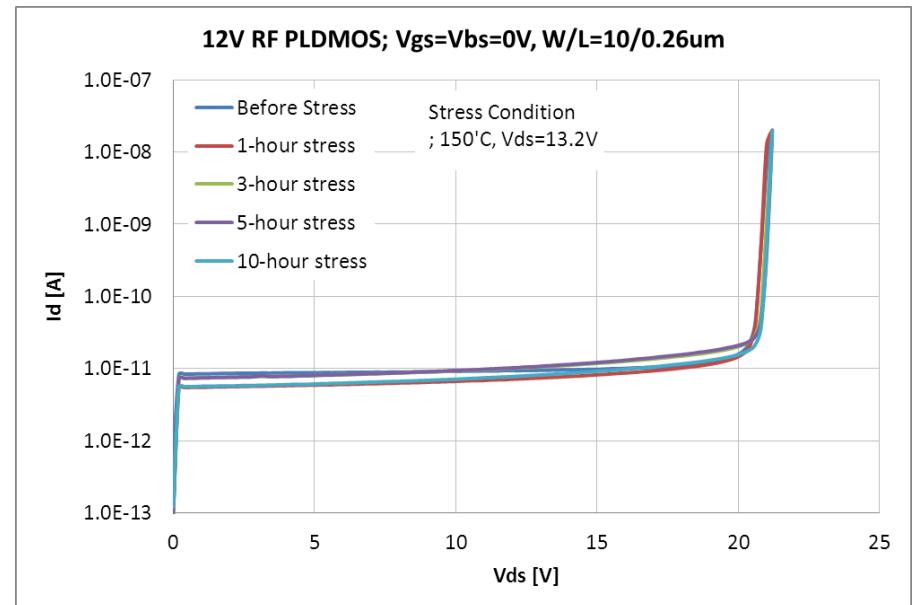
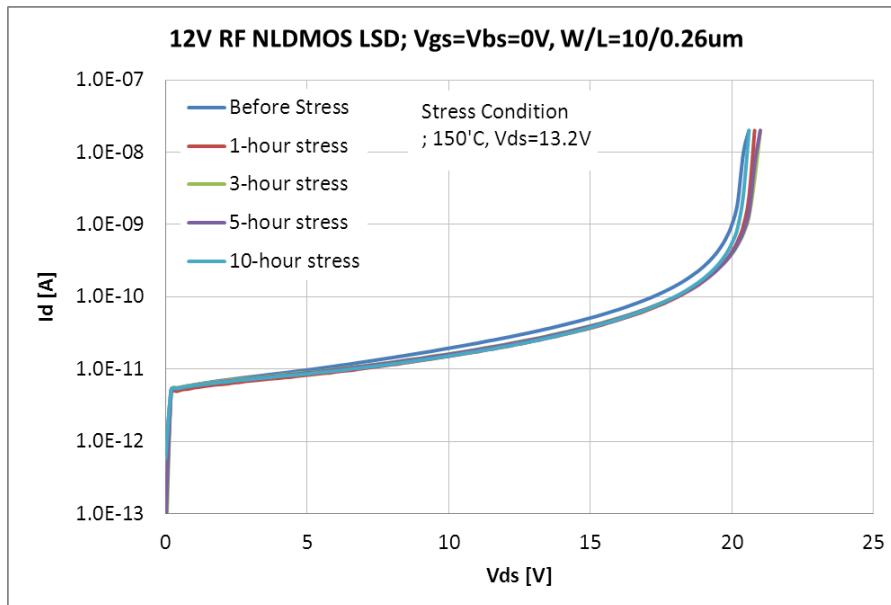
<TLP I-V characteristics; pulse width=100ns>



<Long-term HCI test at Vds=12V, Vgs=1.8V>

- Wide electrical SOA enough for operation up to 15V of Vds
- Long-term HCI results;
 - Idlin drift 6.7% after 150Ksec stress at Vds=12V and Vgs=1.8V

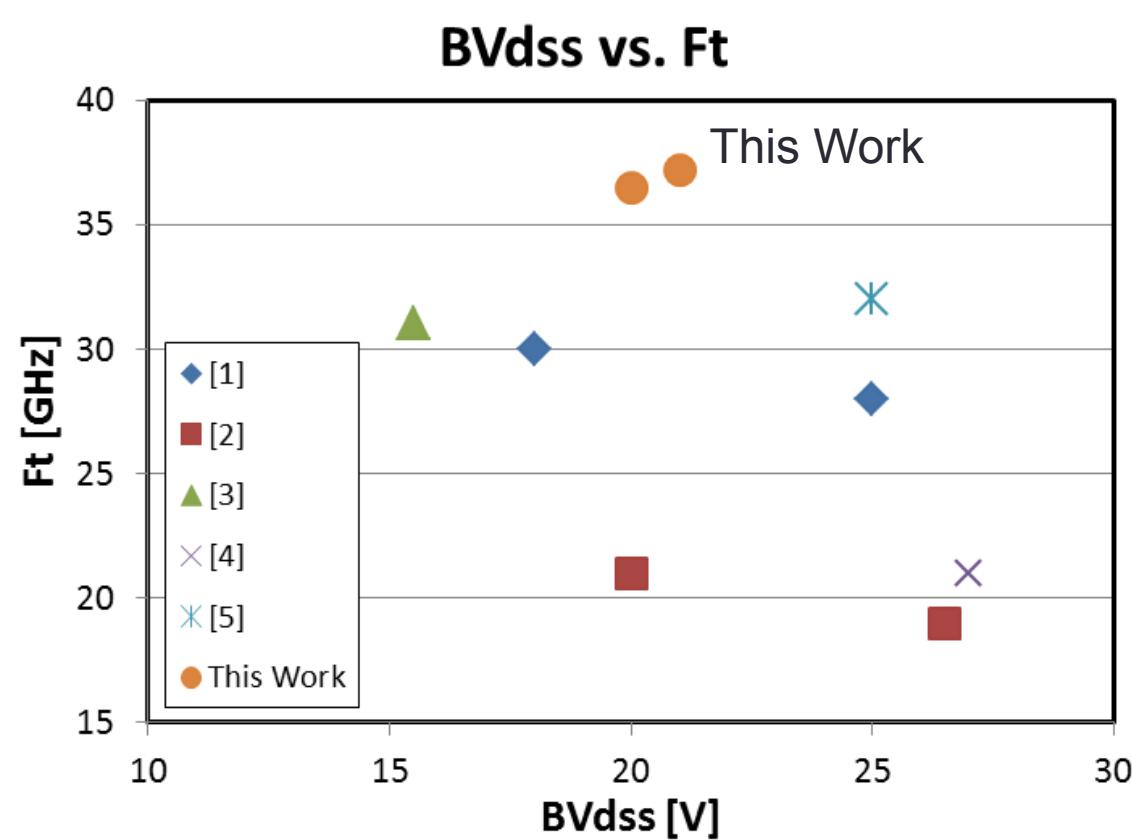
12V HF-LDMOS – Reliability (HTRB)



<BV_{dss} curve with stress time; stress condition 150'C, V_{ds}=13.2V>

- Negligible BV & Off-leakage shift with stress time during Hot Temperature Reverse Biasing stress test
- Customer: product level HTOL (up to 1500 hrs) qualified

BV vs. Ft comparison



[1] Z. Lee et al., IEEE BCTM, pp.1-4, 2006

[2] K. E. Ehwal et al., IEDM Tech. Dig., pp. 895-898, 2001

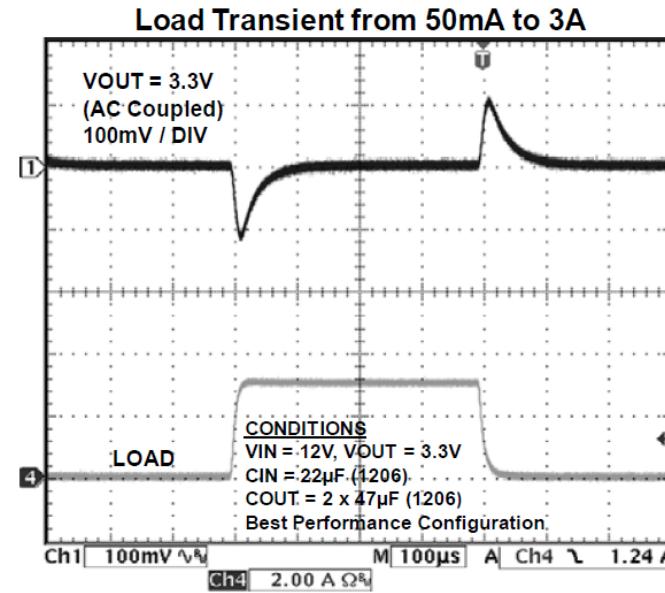
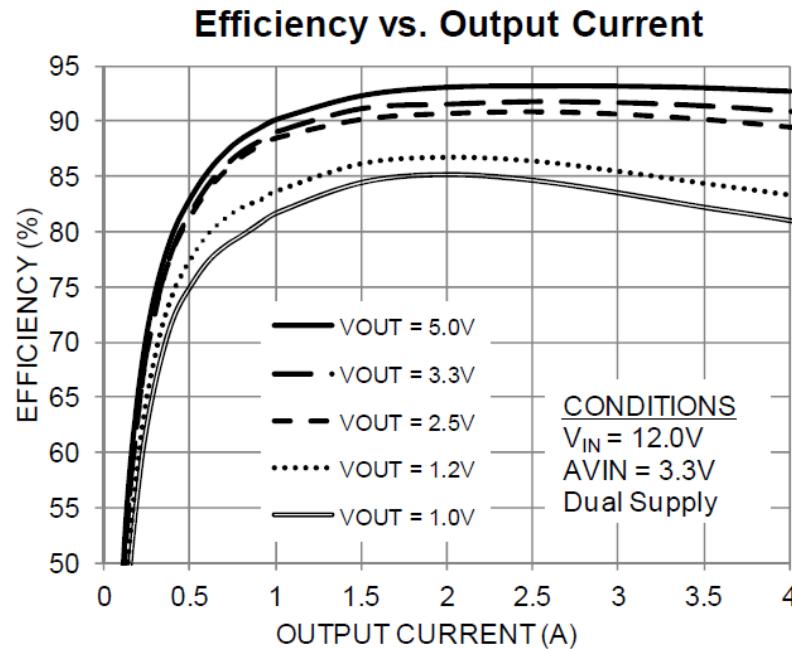
[3] D. Muller et al., IEEE T-ED, Vol. 54, No. 4, pp. 861-867, 2007

[4] N. R. Mohapatra et al., IEEE ISPSD, pp.1-4, 2006

[5] Andreas Mai and Holger Rucker, Solid-St. Electron., pp. 45-50, 2011

Application – ENPIRION DC/DC Converter

- Enpirion unveils the [EN2340QI](#) 4 Amp, [EN2360QI](#) 6 Amp, [EN2390QI](#) 9 Amp, and [EN23F0QI](#) 15 Amp devices further broaden Enpirion's extensive PowerSoC (power-system-on-chip) portfolio by using **AN180 12V High Frequency LDMOS** and **integrated inductor**
- [EN2340QI](#) Measurement data (refer to datasheet)



Summary

- 12V HF-N/PLDMOS transistors with 1.8V V_{gs} have been developed and integrated on **Dongbu HiTek 0.18μm Analog CMOS (AN180)**/BCD(BD180LV) process
- Each of 2 additional implants are used to make NLDMOS and PLDMOS without adding thermal budget
- Short channel length(0.26um) and small gate-to-drain overlap capacitance are used to achieve high F_t, which can reduce the inductor size of the DC/DC converter system
- BV_{dss}*F_t figure-of-merit
 - 744GHz*V for 12V RF NLDMOS
 - 258GHz*V for 12V RF PLDMOS

Summary (Cont.)

- Enpirion developed DC-DC converter using 12V HF-LDMOS process and integrated controller, power MOSFET, and integrated inductor into one chip realizing Power System-On-Chip (PowerSoC)
- The Enpirion shows high efficiency, highest density and reliability without compromising the performance



Thank You!

IL-Yong Park, Dongbu HiTek, ipark@dsemiusa.com

Ashraf Lotfi, Enpirion, lotfi@enpirion.com