Power SOC 2012

Waiting for PSOC….

Applications of PSIP/PSOC Products

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Overview

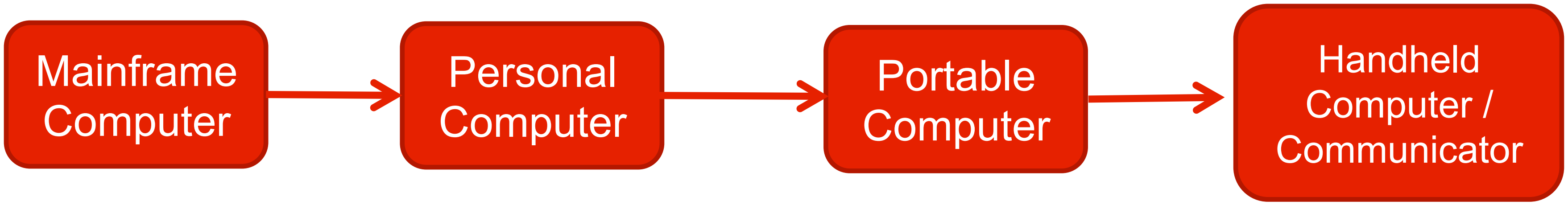
1. Introduction
2. Trends and Dislocations
3. Product Trend Setters
4. Inductor Integration Options
5. Why not?........PSOC Technical Challenges
6. New Power Circuit Needs
7. Why PSOC?.....Product Needs
8. Implementation Hurdles
9. Conclusion

1. Introduction

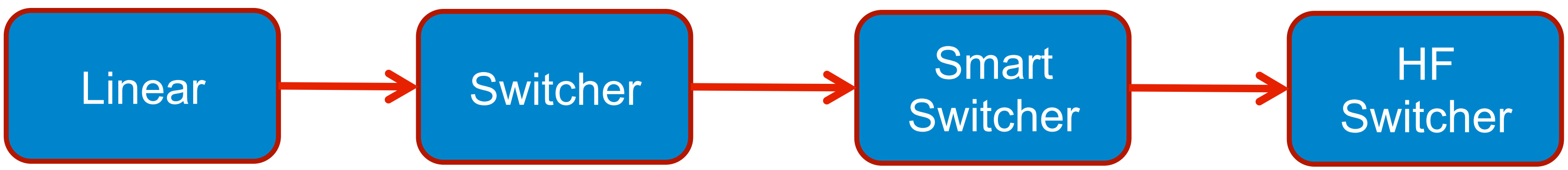
- The trend to smaller size, higher efficiency, and faster response is universal across electronic equipment
- In the past decade, the progress of Moore’s law has been threatened by limitations of power density
- Thus far, the SOC and its Power Regulators have remained as separate entities.
- This is about to change…………………..

2. Trends

1. Equipment

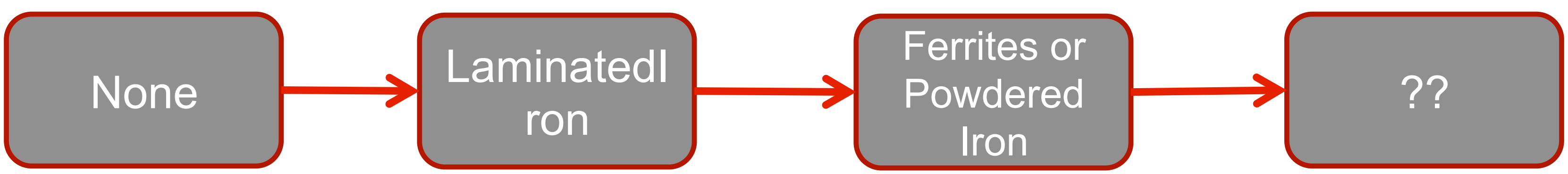


2. Power Solutions

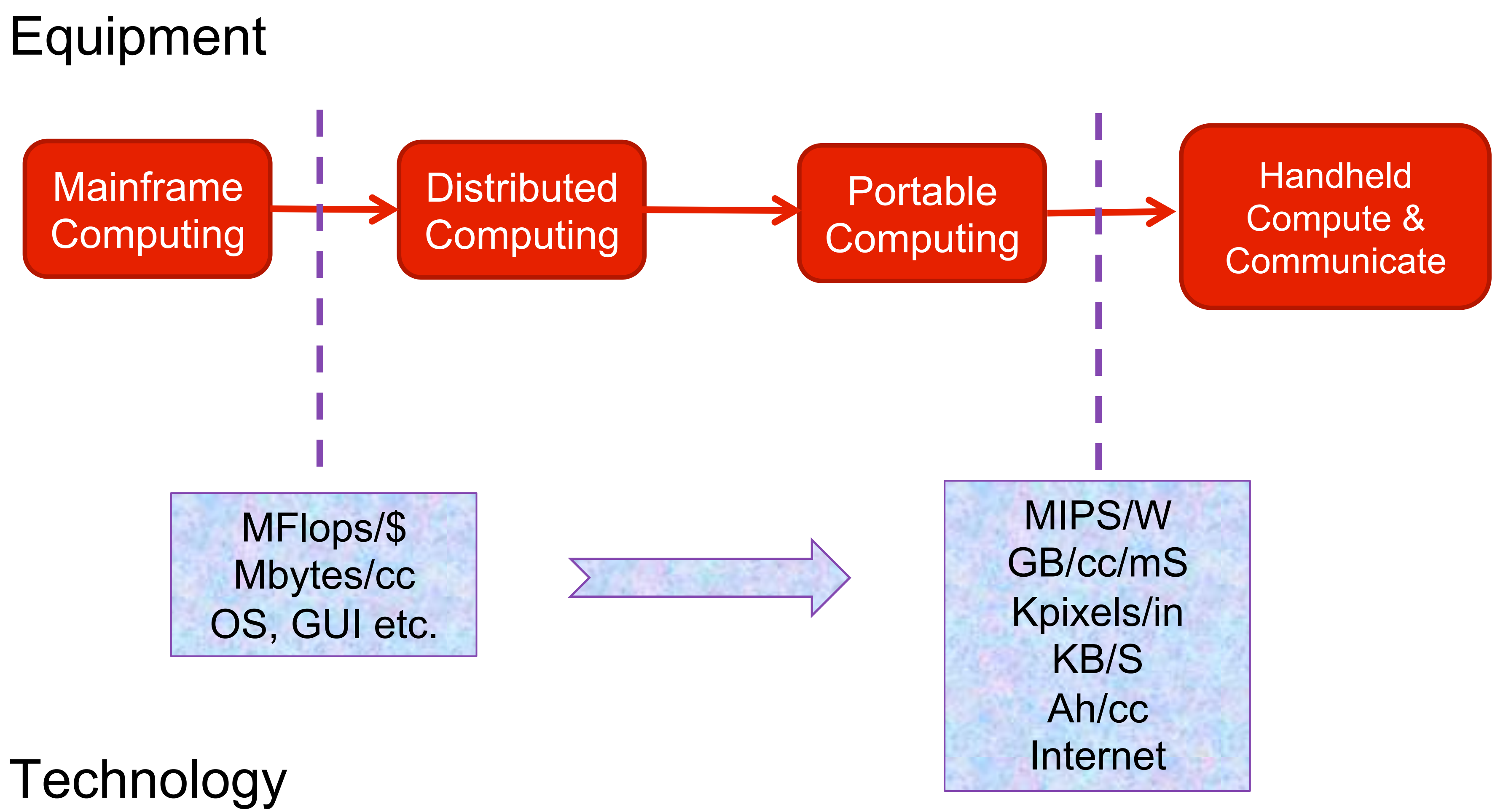


[Not nearly as dramatic]

3. Magnetic Components

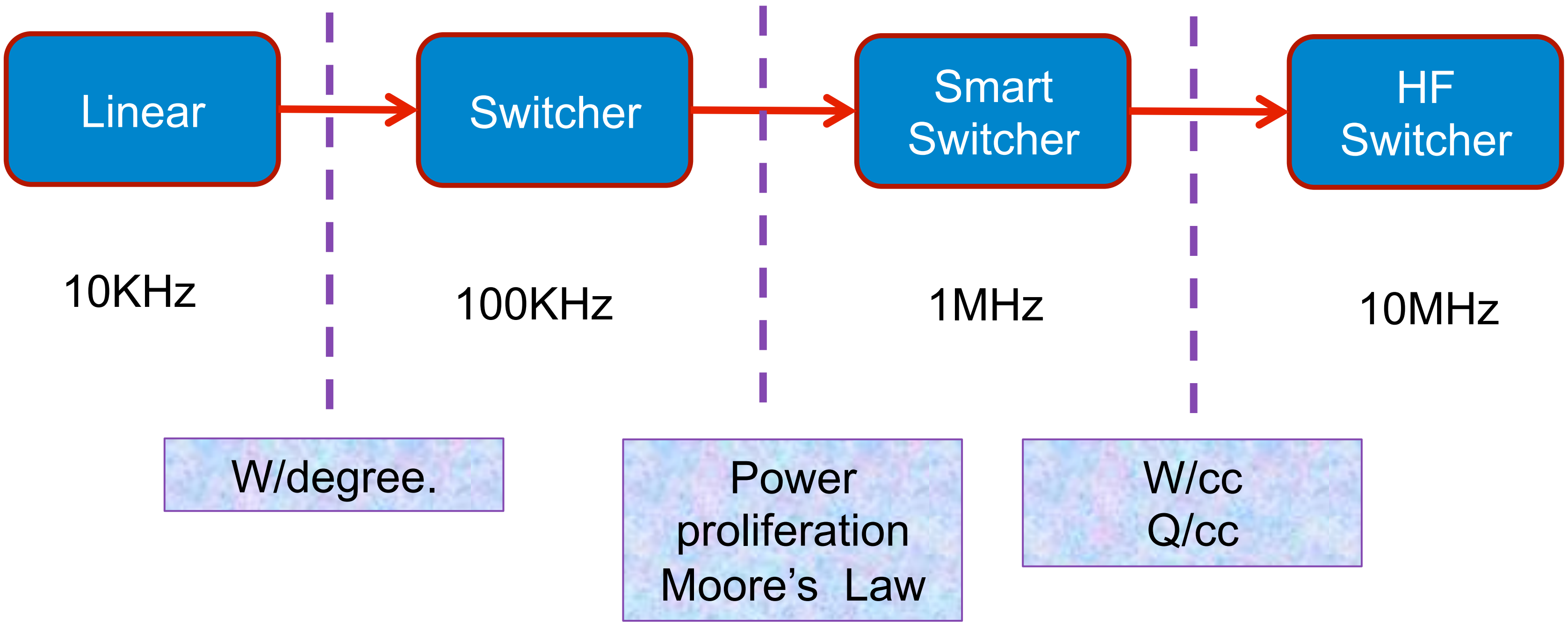


2. Dislocations



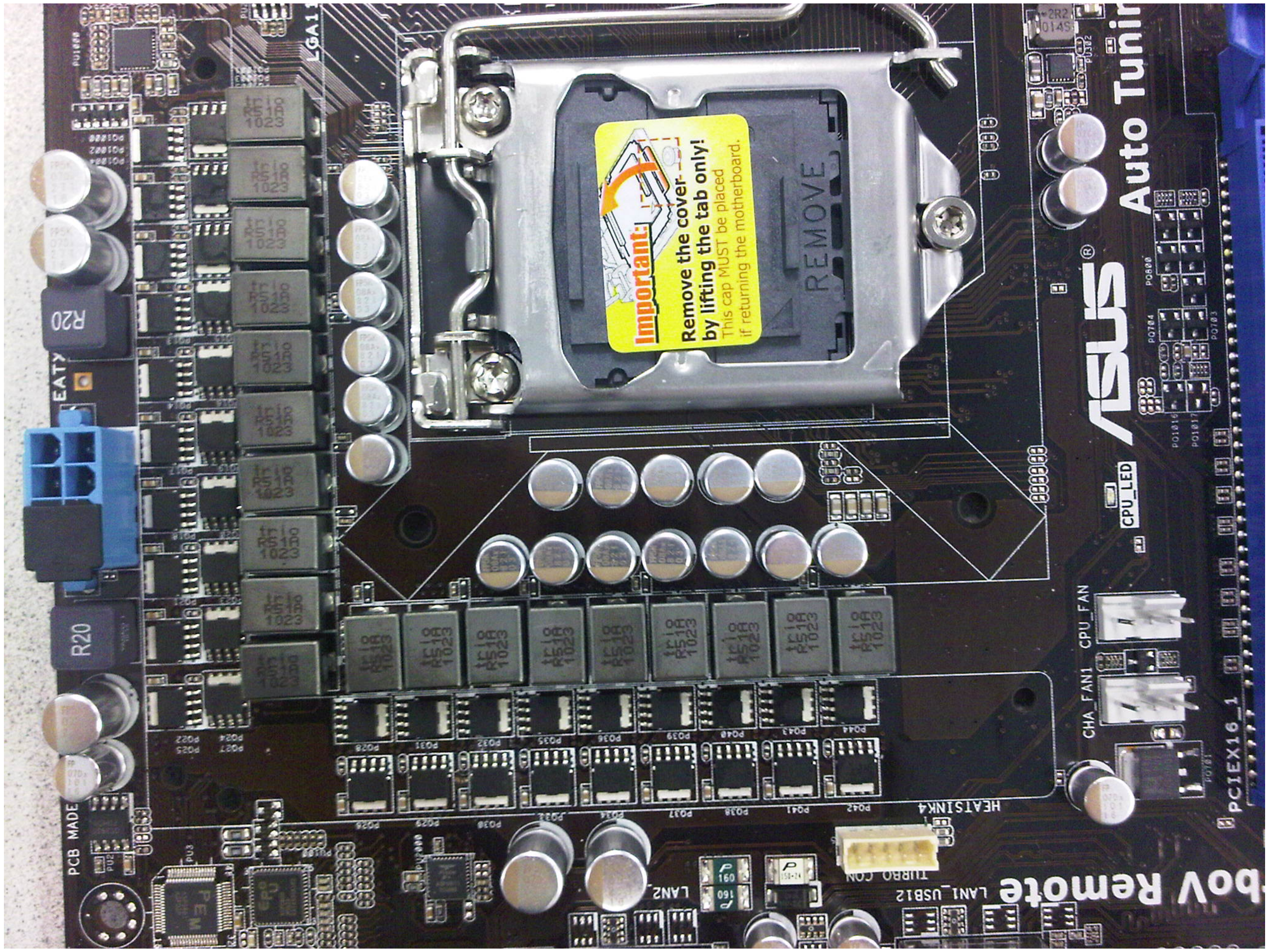
2. Dislocations

Power solutions



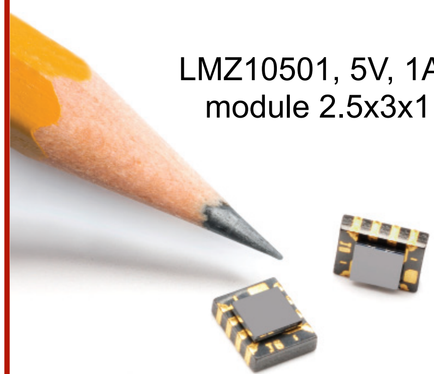
Technology

So What is the Problem?

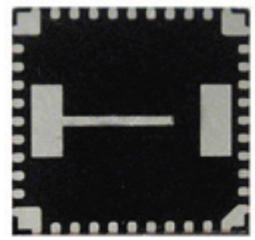


Power Regulation

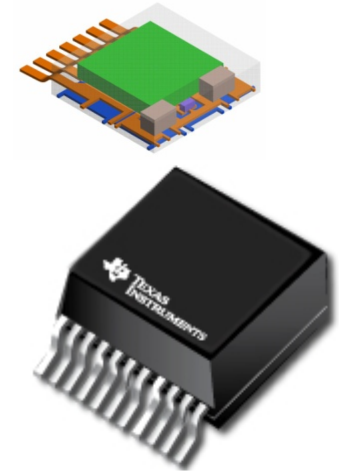
3. Product Trend-Setters



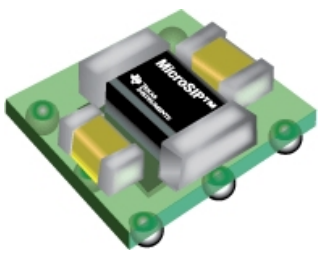
LMZ10501, 5V, 1A power module 2.5x3x1.4mm



TPS84A20, 17V, 10A power module 10x10x4.3mm

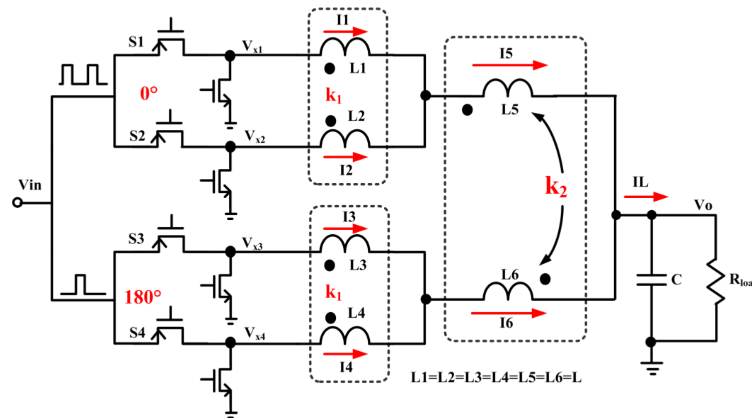


LMZ3610, 36V, 10A power module 15x15x6mm



TPS82671, 4.8V, 0.6A microsip 2.3x2.9x1mm

SC220, 5V, 0.6A power regulator 3.9x4.9x1.8mm

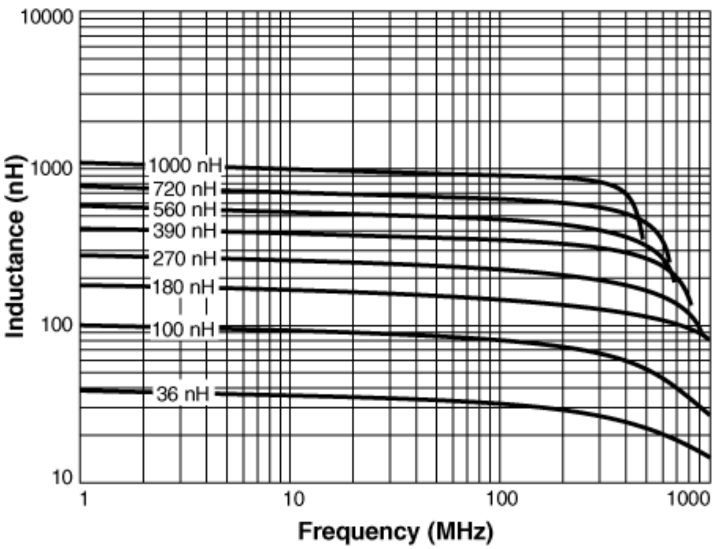


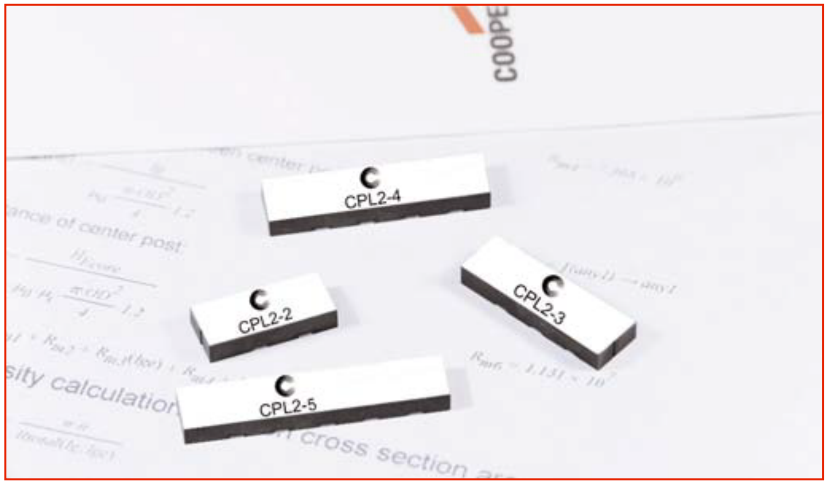
A 100 MHz Two-Phase Four Segment DC-DC Converter with Light Load Efficiency Enhancement *

3. Component Trend-Setters: Inductors

Coilcraft PFML Series

CWS Planar Power Inductor 20A

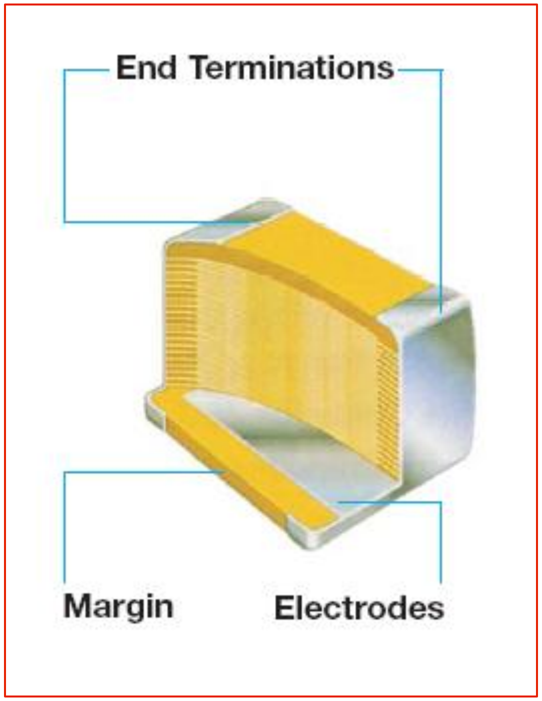




Cooper Coupled Inductors

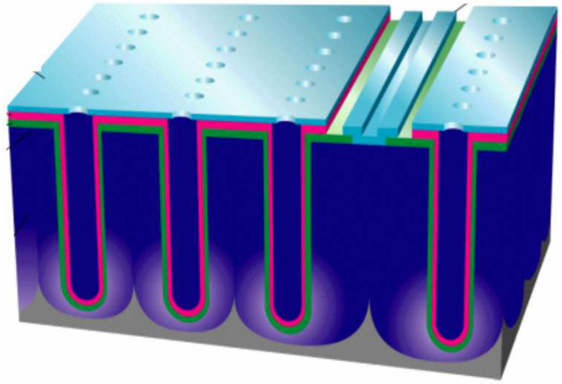
3. Component Trend-Setters: Caps

- Will the ubiquitous MLCC be superseded by integrated structures?

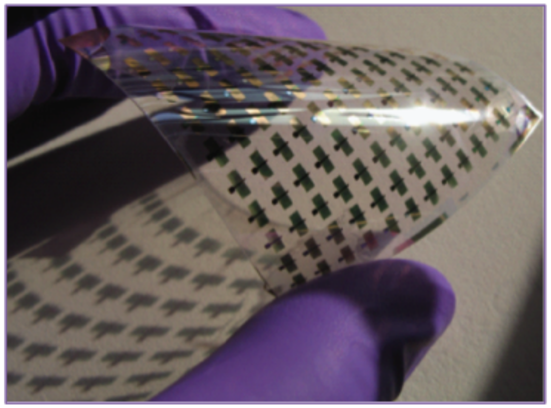


MLC Chip Capacitor

OR



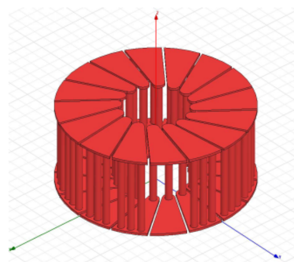
IPIiA Silicon Trench Caps



Printed Metacapacitors

4. Integration Options for Inductors

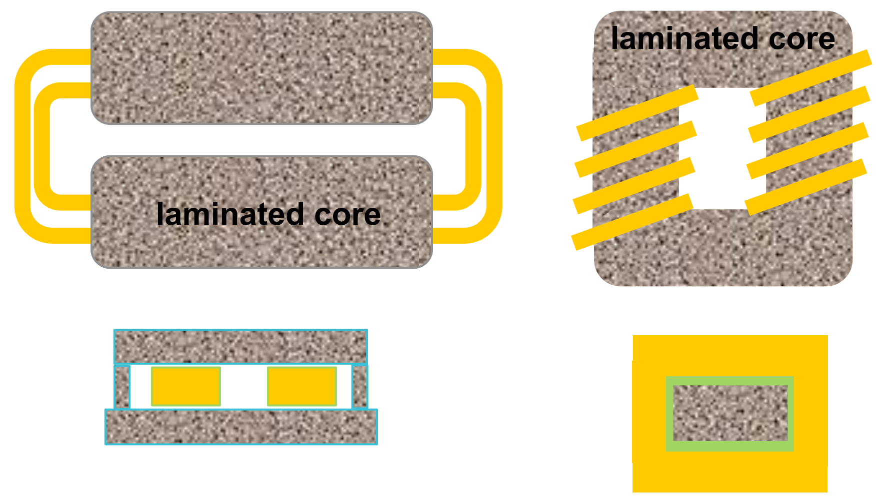
1. Aircore



150nH 8 x 3mm

- Large size limits designs to vhf
- EMI can be a concern

2. Laminated ferric core



<u>Planar/ Racetrack</u>

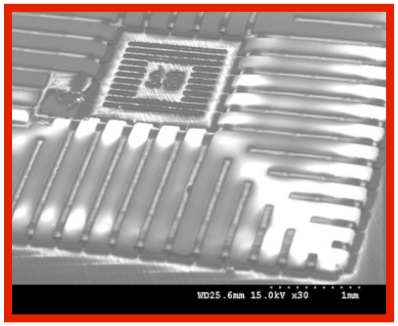
+ Lower dcr
+ Higher power density
− Costly magnetic fab

<u>Toroid (solenoid)</u>

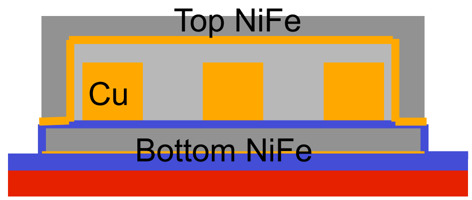
+ Simpler fab
+ Additional Cu layer for interconnect
− Anisotropy challenge

Practical Implementation

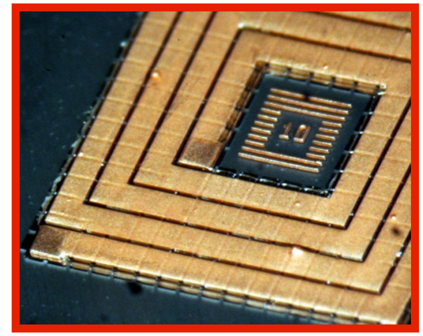
- Real fabrication teaches many lessons………



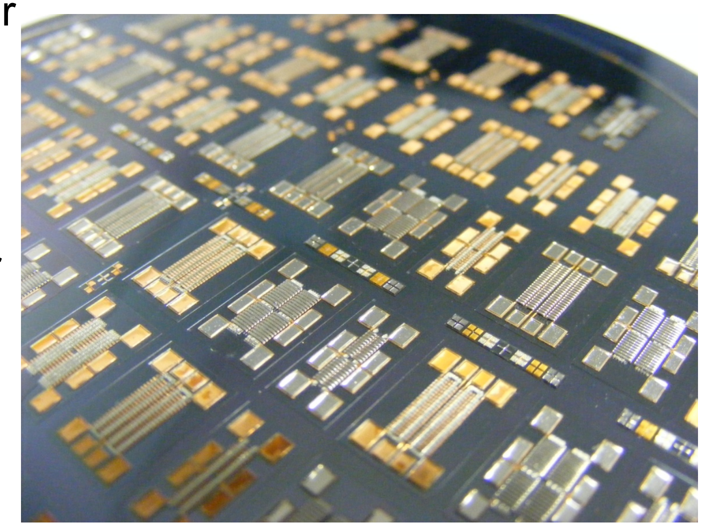
Laminated inductor on test switcher



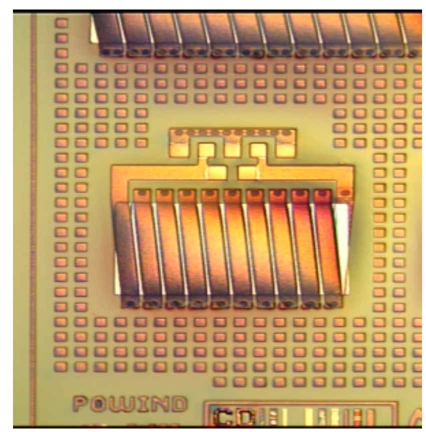
Bottom/Top NiFe Inductor Cross Section



Inductor after bottom NiFe and Cu plating



Bar Inductors on a wafer



[Courtesy of Georgia Tech]

5. Why Not?............Device Challenges

1. Integrated circuit die size may not match required inductor area
2. Yield and stress issues when depositing thick films on fine-geometry silicon
3. Copper losses…
   – larger inductance require multiple turns, higher dcr
   – Larger currents require thicker copper
4. Eddy current losses need to be controlled by fine lamination fabrication, can be slow and costly
5. Hysteresis losses,- control requires anisotropic alignment
6. Core material and deposition system
7. Reliable insulation between turns and conductive core
8. Cost
9. Etc.

6. Circuit Needs

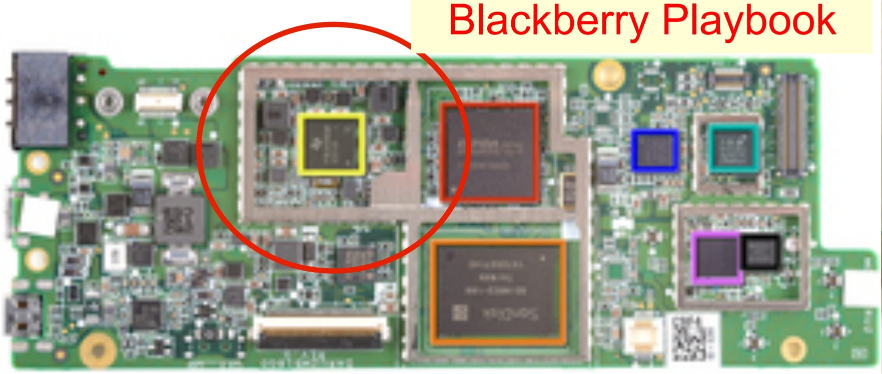
In order to facilitate efficient PSOC applications, new architectures will be required for power applications:

1. Use of higher switching frequencies:
   from 1 – 5MHz today to > 20MHz
2. Use of finer pitch geometries: from 0.18 to 0.35u today to 45 –90nm
3. Two-stage regulation back in vogue
4. SIMO (Single I/P Multi O/P) topologies
5. Mixed use of switched cap and switched inductor
6. Soft switched topologies
7. Use of in-circuit inductors / transformers
8. Etc.

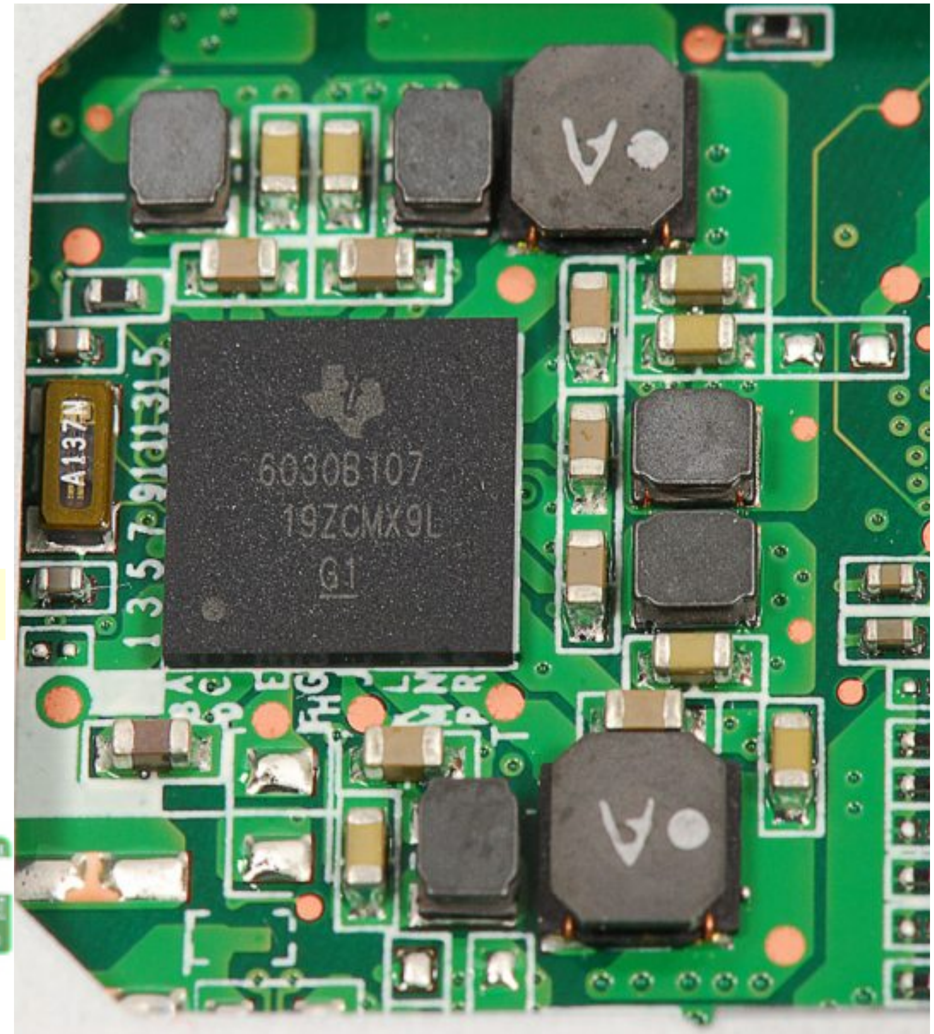
But, successful implementation will provide a dramatic increase in power density and response times

7. Why PSOC? – Product Needs

- Portable devices require multiple switching regs, each with external L's & C's
- e.g. TWL6030:
  - 7 X 6MHz switchers
  - 1 charger
  - 11 LDO's



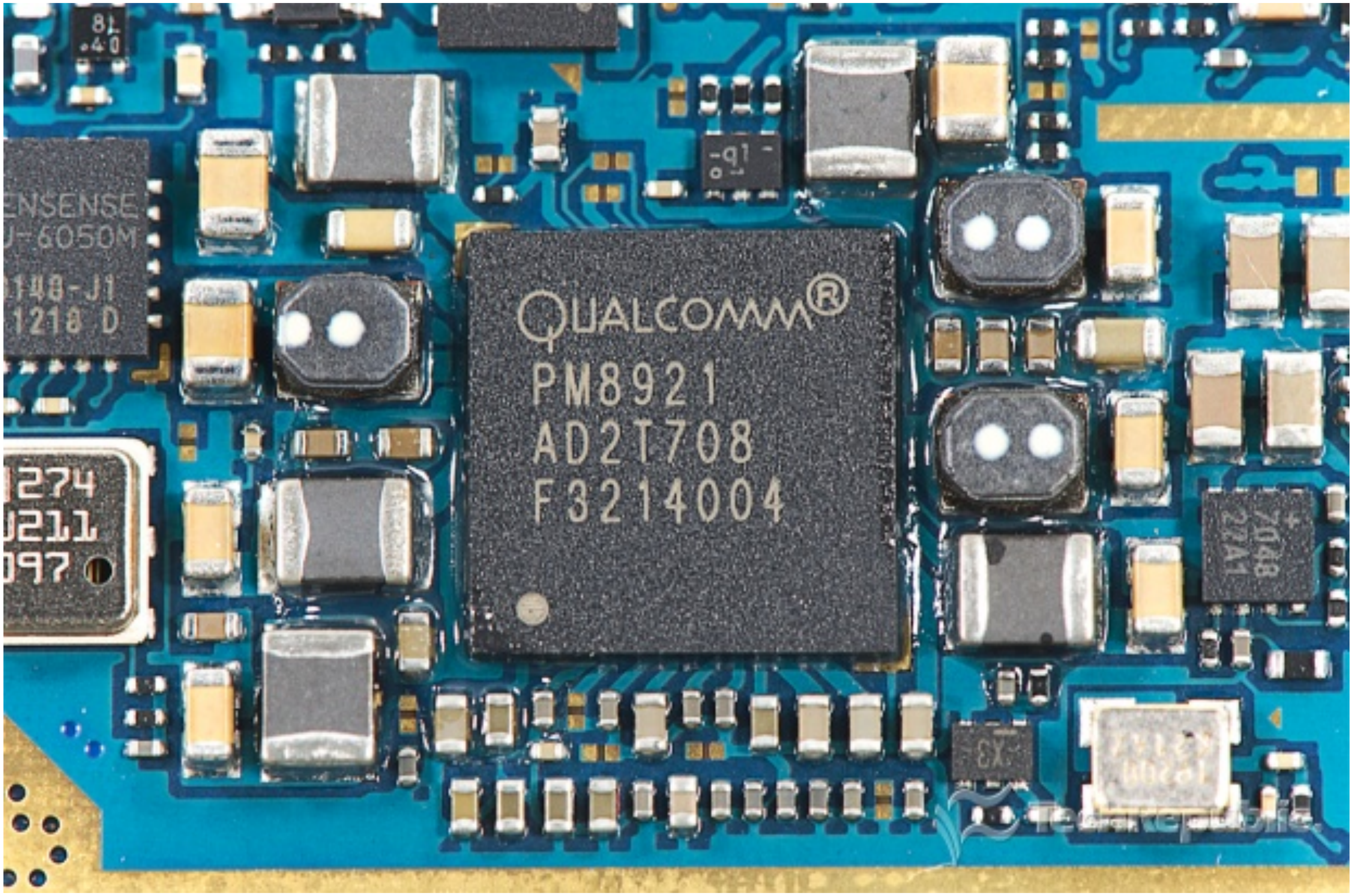
Blackberry Playbook



Kindle Fire PMIC

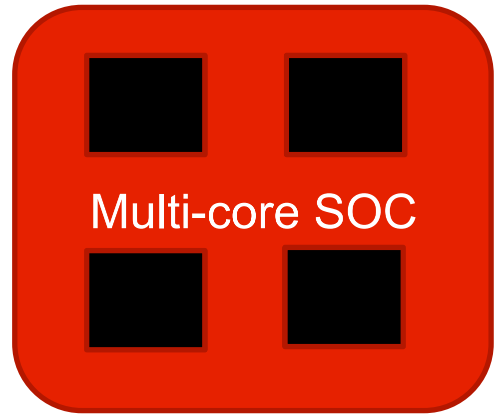
– Integration of 5X 1A inductors would reduce power board area by 30%

Example 2: Galaxy S III PMU

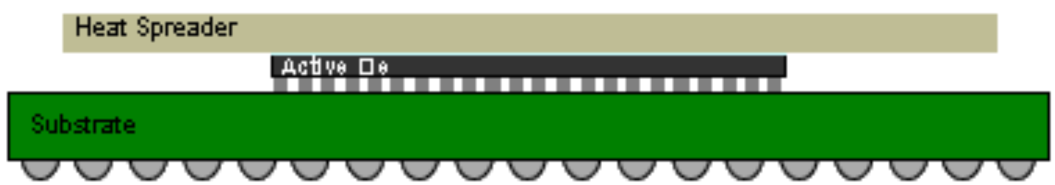


7. Example 3: Multicore DSP

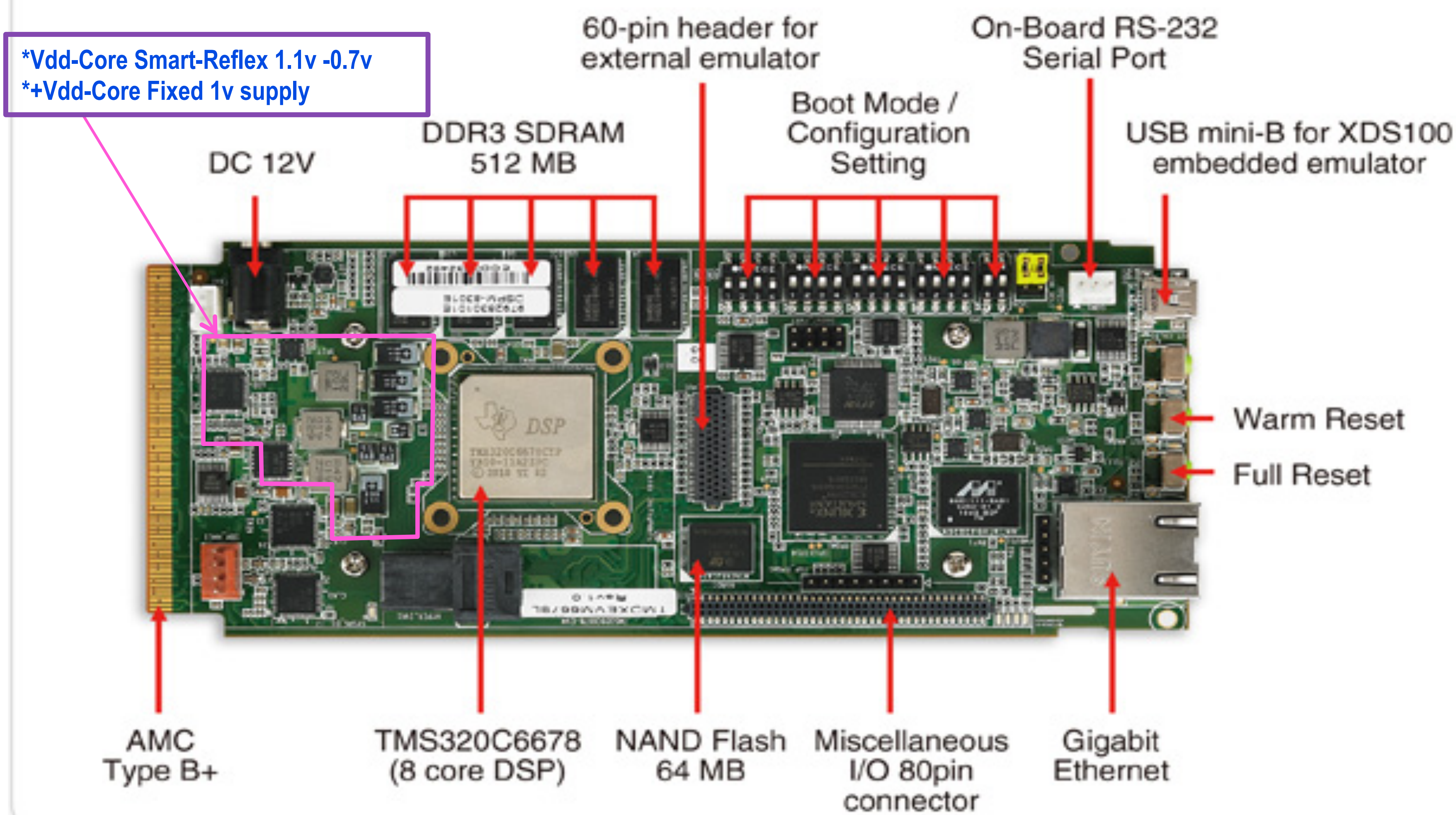
Multi-Core SOC



- Typically supplied by single or multiple board-level power regulators
- Growth of multi-core SOC leading to greater power demands
- Up to 5% copper loss between regulator and processor
- No load line, can add 5% more
- Slow power loop response prevents dynamic voltage positioning
- Strong case for in-package dynamic multi-rail regulator



TMS320C6678: 8- Core DSP



Implementation Hurdles

1. Identifying the application that will support product introduction at immature cost levels
2. Achieving Quality Factor > 20 at rated current and frequencies
3. Practical, high frequency & high efficiency power regulators
4. Acceptable levels of magnetic noise & susceptibility
5. Cost-effective, reliable, volume manufacturing process

None of these seem insurmountable

8. Conclusion

- Low voltage SOC's are increasingly constrained by large, slow, external power solutions.
- The need for more dynamic control, and proliferation of internal power domains is creating a product dislocation
- Over a decade of research into on-chip power solutions has addressed many of the technical challenges: relatively high energy density caps and inductors have been demonstrated
- We can expect to see increasing numbers of PowerSOC solutions appear, initially in low volume, niche applications.

Thank you!